SN65HVD1050A-Q1 EMC-Optimized High-Speed Can Transceiver

1 Features

- Qualified for Automotive Applications
- Improved Drop-In Replacement for TJA1050
- Meets or Exceeds the Requirements of ISO 11898-2
- GIFT/ICT Compliant
- ESD Protection up to ±12 kV (Human-Body Model) on Bus Pins
- High Electromagnetic Compliance (EMC)
- Bus-Fault Protection of –27 V to 40 V
- Dominant Time-Out Function
- Thermal Shutdown Protection
- Power Up and Power Down Glitch-Free Bus Inputs and Outputs
  - High Input Impedance With Low V_{CC}
  - Monotonic Outputs During Power Cycling

2 Applications

- GMW3122 Dual-Wire CAN Physical Layer
- SAE J2284 High-Speed CAN for Automotive Applications
- SAE J1939 Standard Data Bus Interfaces
- ISO 11783 Standard Data Bus Interfaces
- NMEA 2000 Standard Data Bus Interfaces

3 Description

The SN65HVD1050A-Q1 meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a Controller Area Network (CAN). The device is qualified for use in automotive applications.

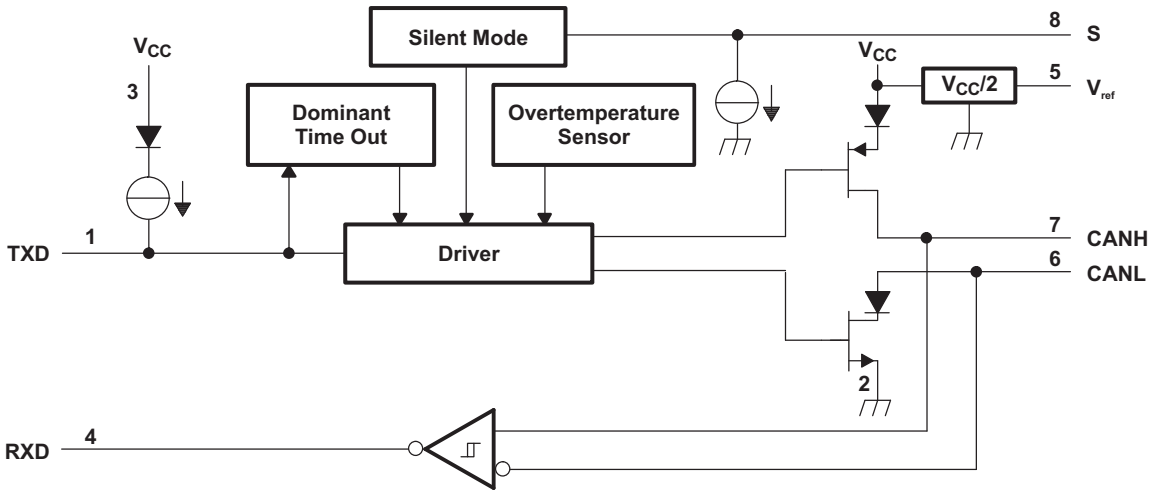
As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD1050A-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Function Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2011) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table, see POA at the end of the data sheet ... 1
- Deleted obsolete SN65HVD1050AL device from the data sheet ... 1

5 Description (continued)

Designed for operation is especially harsh environments, the SN65HVD1050A-Q1 features cross-wire, overvoltage, and loss of ground protection from –27 V to 40 V, overtemperature protection, a –12-V to 12-V common-mode range, and withstands voltage transients according to ISO 7637.

Pin 8 provides for two different modes of operation: high-speed or silent mode. The high-speed mode of operation is selected by connecting S (pin 8) to ground.

If a high logic level is applied to the S pin of the SN65HVD1050A-Q1, the device enters a listen-only silent mode during which the driver is switched off while the receiver remains fully functional.

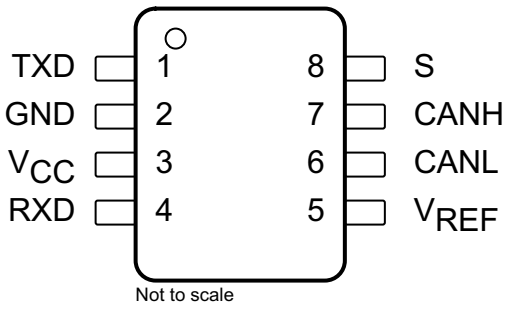
In silent mode, all bus activity is passed by the receiver output to the local protocol controller. When data transmission is required the local protocol controller must transition the device to high speed mode by placing a logic low on the S pin to resume full operation.

A dominant time-out circuit in the SN65HVD1050A-Q1 prevents the driver from blocking network communication with a hardware or software failure. The time-out circuit is triggered by a falling edge on TXD (pin 1). If no rising edge is seen before the time-out constant of the circuit expires, the driver is disabled. The circuit is then reset by the next rising edge on TXD.

V_{REF} (pin 5) is available as a V_{CC} / 2 voltage reference.

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CANH	7	I/O	HIGH-level CAN bus line
CANL	6	I/O	LOW-level CAN bus line
GND	2	GND	Ground connection
RXD	4	O	CAN receiver data output (low in dominant bus state, high in recessive bus state)
V_{REF}	5	O	Common-mode stabilization output for split termination
S	8	I	Silent mode select pin (active-high)
TXD	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
V_{CC}	3	Supply	Transceiver 5-V supply voltage input

7 Specifications

7.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.3	6	V
	Voltage at any bus terminal (CANH, CANL, V_{ref})		–27	40	V
I_O	Receiver output current			20	mA
V_I	Voltage input, ISO 7637 transient pulse(3) (CANH, CANL)		–150	100	V
V_I	Voltage input (TXD, S)		–0.3	6	V
T_J	Junction temperature		–40	150	°C
P_D	Average power dissipation	V_{CC} = 5 V, T_J = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, CL at RXD = 15 pF	112		mW
		V_{CC} = 5.5 V, T_J = 130°C, R_L = 45 Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, CL at RXD = 15 pF		170	
	Thermal shutdown temperature		190		°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with ISO 7637 test pulses 1, 2, 3a, 3b per IBEE system level test (Pulse 1 = –100 V, Pulse 2 = 100 V, Pulse 3a = –150 V, Pulse 3b = 100 V). If dc may be coupled with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal. This device has been tested with dc bus shorts to 40 V with leading common-mode chokes. If common-mode chokes are used in the system and the bus lines may be shorted to dc, ensure that the choke type and value in combination with the node termination and shorting voltage either will not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	All pins except 6 and 7	±4000	V
			Pins 6 and 7(3)	±12000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(4)(5)		±1500	
		Machine model(6)		±200	

(1) All typical values at 25°C.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Test method based upon JEDEC Standard 22 Test Method A114E, CANH and CANL bus pins stressed with respect to each other and GND.
(4) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(5) Tested in accordance JEDEC Standard 22, Test Method C101C.
(6) Tested in accordance JEDEC Standard 22, Test Method A115A.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–12	12	V
V_{IH}	High-level input voltage	TXD, S	2	5.25	V
V_{IL}	Low-level input voltage	TXD, S	0	0.8	V
V_{ID}	Differential input voltage		–6	6	V
I_{OH}	High-level output current	Driver	–70		mA
		Receiver	–2		
I_{OL}	Low-level output current	Driver		70	mA
		Receiver		2	
T_A	Operating free-air temperature	See *Thermal Information*.	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]			SN65HVD1050A-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	Low-K thermal resistance[3]	211	°C/W
		High-K thermal resistance[3]	131	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		79	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		53	°C/W
ψ_{JT}	Junction-to-top characterization parameter		8	°C/W
ψ_{JB}	Junction-to-board characterization parameter		49.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		79	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction temperature (T_J) is calculated using the following $T_J = T_A + (P_D \times R_{\theta JA})$.
(3) Tested in accordance with the Low-K (EIA/JESD51-3) or High-K (EIA/JESD51-7) thermal metric definitions for leaded surface-mount packages.

7.5 Electrical Characteristics: Supply Current

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)[1]

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	5-V supply current	Silent mode	S at V_{CC}, V_I= V_{CC}		6	10	mA
		Dominant	V_I = 0 V, 60-Ω load, S at 0 V		50	70	
		Recessive	V_I = V_{CC}, No load, S at 0 V		6	10	

(1) All typical values are at 25°C with a 5-V supply.

7.6 Electrical Characteristics: Driver

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)[1]

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(D)}$	Bus output voltage (dominant)	CANH	V_I = 0 V, S at 0 V, R_L = 60 Ω, See Figure 3 and Figure 4	2.9	3.4	4.5	V
		CANL		0.8		1.5	
$V_{O(R)}$	Bus output voltage (recessive)		V_I = 3 V, S at 0 V, R_L = 60 Ω, See Figure 3 and Figure 4	2	2.3	3	V
$V_{OD(D)}$	Differential output voltage (dominant)		V_I = 0 V, R_L = 60 Ω, S at 0 V, See Figure 3, Figure 4, and Figure 5	1.5		3	V
			V_I = 0 V, R_L = 45 Ω, S at 0 V, See Figure 3, Figure 4, and Figure 5	1.4		3	V
$V_{OD(R)}$	Differential output voltage (recessive)		V_I = 3 V, S at 0 V, See Figure 3 and Figure 4	–0.012		0.012	V
			V_I = 3 V, S at 0 V, No Load	–0.5		0.05	
$V_{OC(ss)}$	Steady state common-mode output voltage		S at 0 V, Figure 10	2	2.3	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage				30		mV
I_{IH}	High-level input current, TXD input		V_I at V_{CC}	–2		2	µA
I_{IL}	Low-level input current, TXD input		V_I at 0 V	–50		–10	
$I_{O(off)}$	Power-off TXD output current		V_{CC} at 0 V, TXD at 5 V			1	
$I_{OS(ss)}$	Short-circuit steady-state output current		V_{CANH} = –12 V, CANL open, See Figure 13	–105	–72		mA
			V_{CANH} = 12 V, CANL open, See Figure 13		0.36	1	
			V_{CANL} = –12 V, CANH open, See Figure 13	–1	–0.5		
			V_{CANL} = 12 V, CANH open, See Figure 13		71	105	
C_O	Output capacitance		See receiver input capacitance.				

(1) All typical values are at 25°C with a 5-V supply.

7.7 Electrical Characteristics: Receiver

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	S at 0 V, See Table 1		800	900	mV
V_{IT-}	Negative-going input threshold voltage	S at 0 V, See Table 1	500	650		mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)		100	125		mV
V_{OH}	High-level output voltage	I_O = –2 mA, See Figure 8	4	4.6		V
V_{OL}	Low-level output voltage	I_O = 2 mA, See Figure 8		0.2	0.4	V
$I_{I(off)}$	Power-off bus input current	CANH or CANL = 5 V, Other pin at 0 V, V_{CC} at 0 V, TXD at 0 V		165	250	µA
$I_{O(off)}$	Power-off RXD leakage current	V_{CC} at 0 V, RXD at 5 V			20	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD at 3 V, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C_{ID}	Differential input capacitance	TXD at 3 V, V_I = 0.4 sin (4E6πt)		6		pF
R_{ID}	Differential input resistance	TXD at 3 V, S at 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	TXD at 3 V, S at 0 V	15	30	40	kΩ
$R_{I(m)}$	Input resistance matching $[1 – (R_{IN\ (CANH)} / R_{IN\ (CANL)})] \times 100\%$	$V_{(CANH)} = V_{(CANL)}$	–3%	0%	3%	

(1) All typical values are at 25°C with a 5-V supply.

7.8 Switching Characteristics: Device

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	S at 0 V, See Figure 11	90	230	ns
$t_{d(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	S at 0 V, See Figure 11	90	230	ns

7.9 Switching Characteristics: Driver

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)(1)

			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	S at 0 V, See Figure 6	25	65	120	ns
t_{PHL}	Propagation delay time, high-to-low level output	S at 0 V, See Figure 6	25	45	120	ns
t_r	Differential output signal rise time	S at 0 V, See Figure 6		25		ns
t_f	Differential output signal fall time	S at 0 V, See Figure 6		50		ns
t_{en}	Enable time from silent mode to dominant	See Figure 9			1	µs
$t_{(dom)}$	Dominant time out(2)	↓V_I, See Figure 12	300	450	700	µs

(1) All typical values are at 25°C with a 5-V supply.
(2) The TXD dominant time out (t(dom)) will disable the driver of the transceiver once the TXD has been dominant longer than $t_{(dom)}$which will release the bus lines to recessive preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults locking the bus dominant it will limit the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case where five successive dominant bits are followed immediately by an error frame. This along with the $t_{(dom)}$ minimum will limit the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ $t_{(dom)}$ = = 11 bits / 300 µs = 37 kbps.

7.10 Switching Characteristics: Receiver

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S at 0 V or V_{CC}, See Figure 8	60	100	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		45	70	130	ns
t_r	Output signal rise time			8		ns
t_f	Output signal fall time			8		ns

(1) All typical values are at 25°C with a 5-V supply.

7.11 S Pin Characteristics

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High level input current	S at 2 V	20	40	70	µA
I_{IL}	Low level input current	S at 0.8 V	5	20	30	µA

(1) All typical values are at 25°C with a 5-V supply.

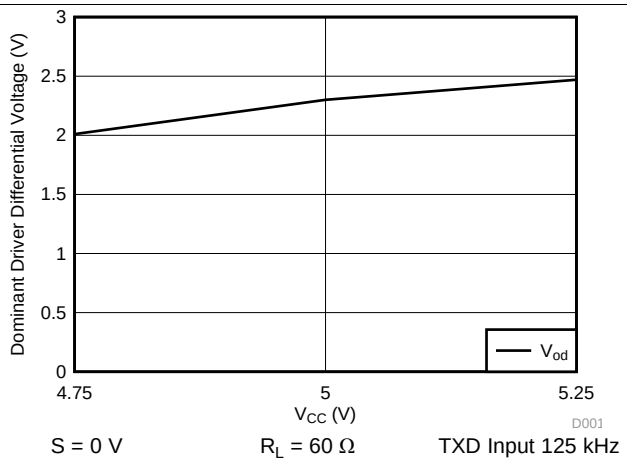
7.12 V_{REF} Pin Characteristics

over recommended operating conditions, T_A = –40 to 125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Reference output voltage	–50 µA < I_O < 50 µA	0.4 V_{CC}	0.5 V_{CC}	0.6 V_{CC}	V

(1) All typical values are at 25°C with a 5-V supply.

7.13 Typical Characteristics



S = 0 V R_L = 60 Ω TXD Input 125 kHz

Figure 1. Driver Differential Voltage vs Supply Voltage

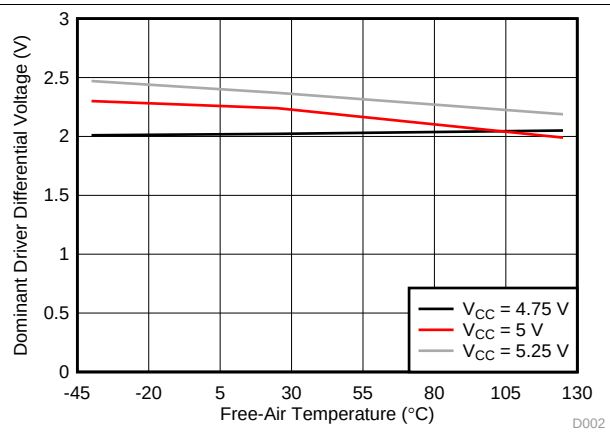


Figure 2. Dominant Driver Differential Voltage vs Free-Air Temperature

8 Parameter Measurement Information

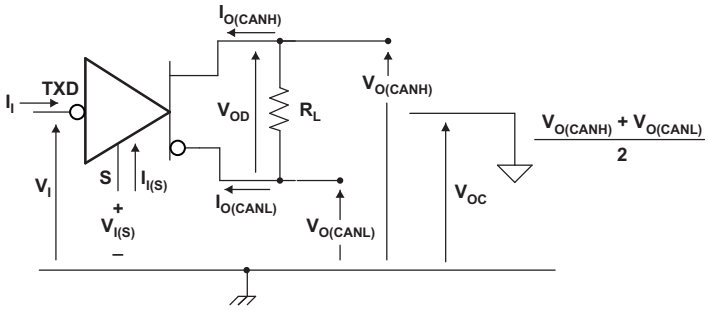


Figure 3. Driver Voltage, Current, and Test Definition

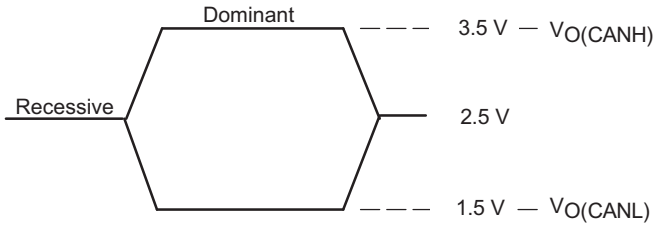


Figure 4. Bus Logic State Voltage Definitions

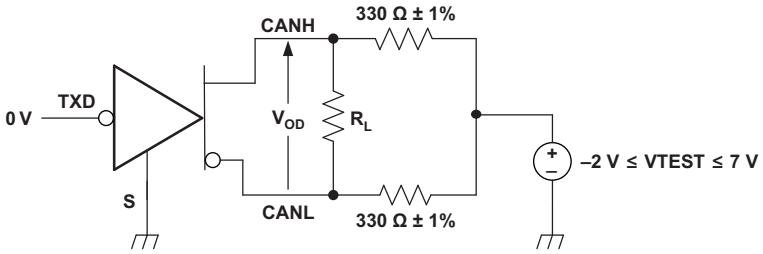


Figure 5. Driver V_{OD} Test Circuit

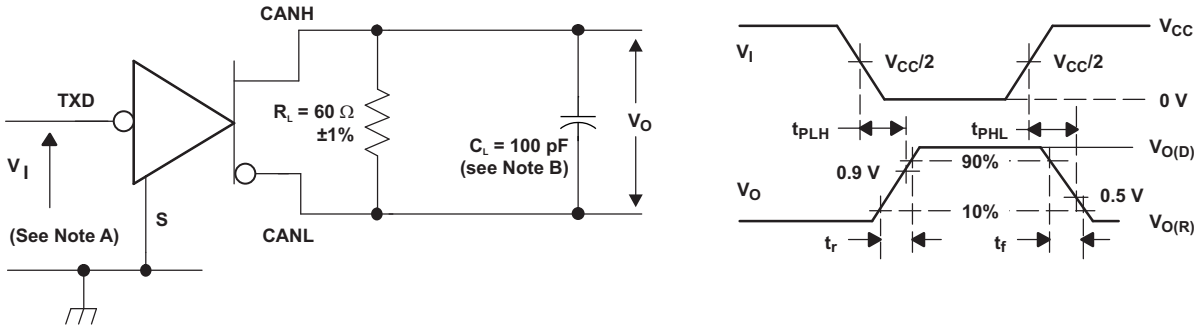


Figure 6. Driver Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

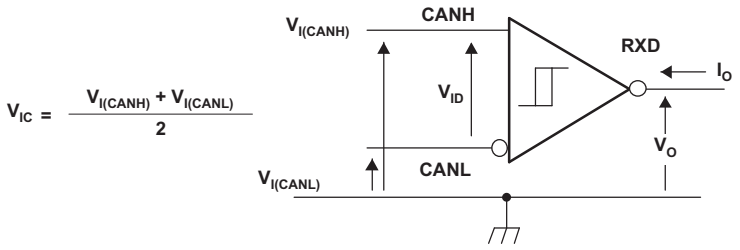
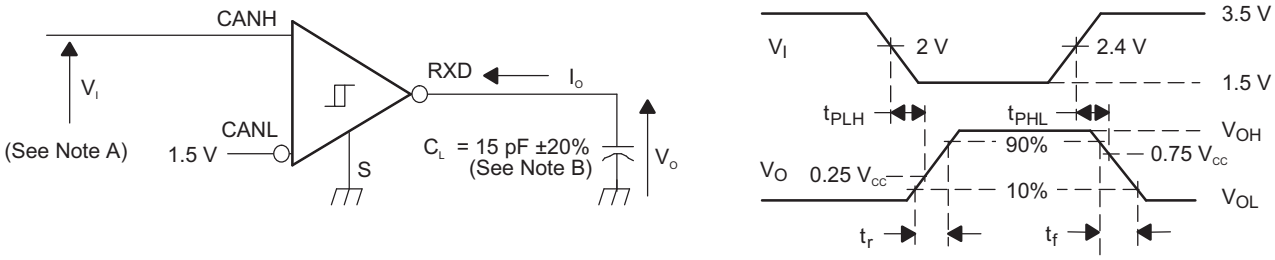


Figure 7. Receiver Voltage and Current Definitions



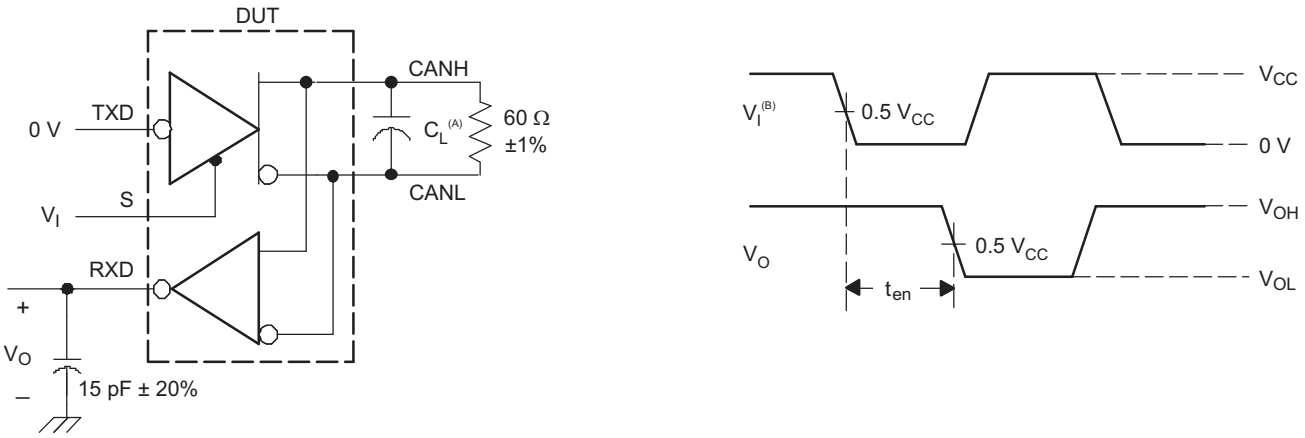
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 8. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

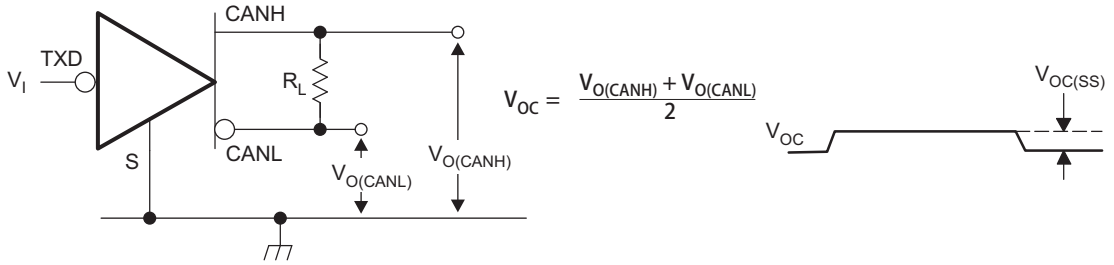
INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

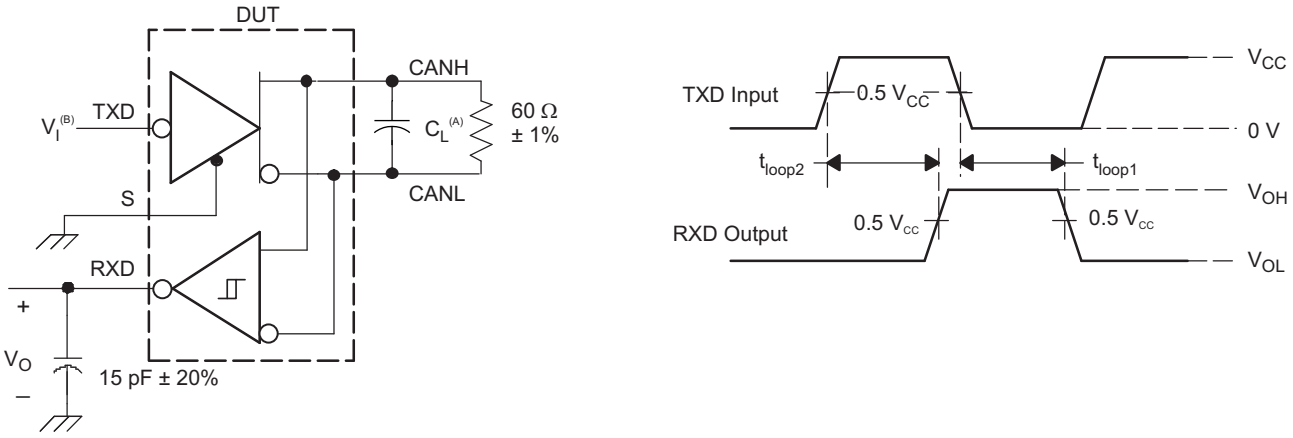
B. All V_I input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. t_{en} Test Circuit and Waveforms



NOTE: All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

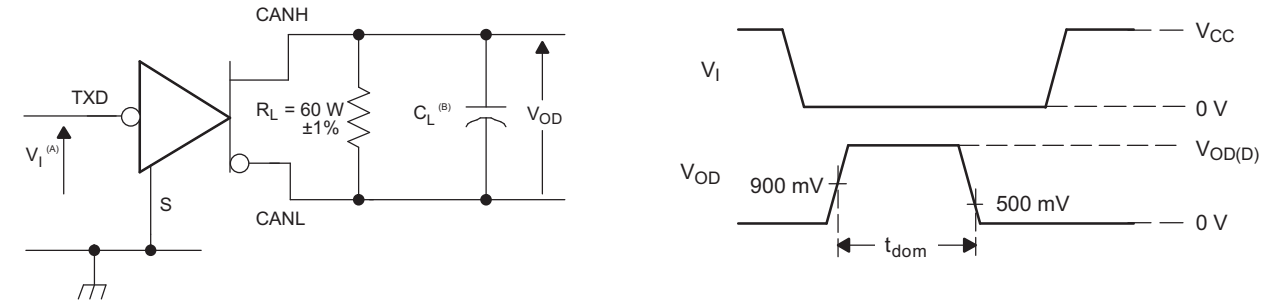
Figure 10. Common-Mode Output Voltage Test and Waveforms



A. C_L = 100 pF and includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 11. $t_{(LOOP)}$ Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{CC} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

B. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

Figure 12. Dominant Time-Out Test Circuit and Waveforms

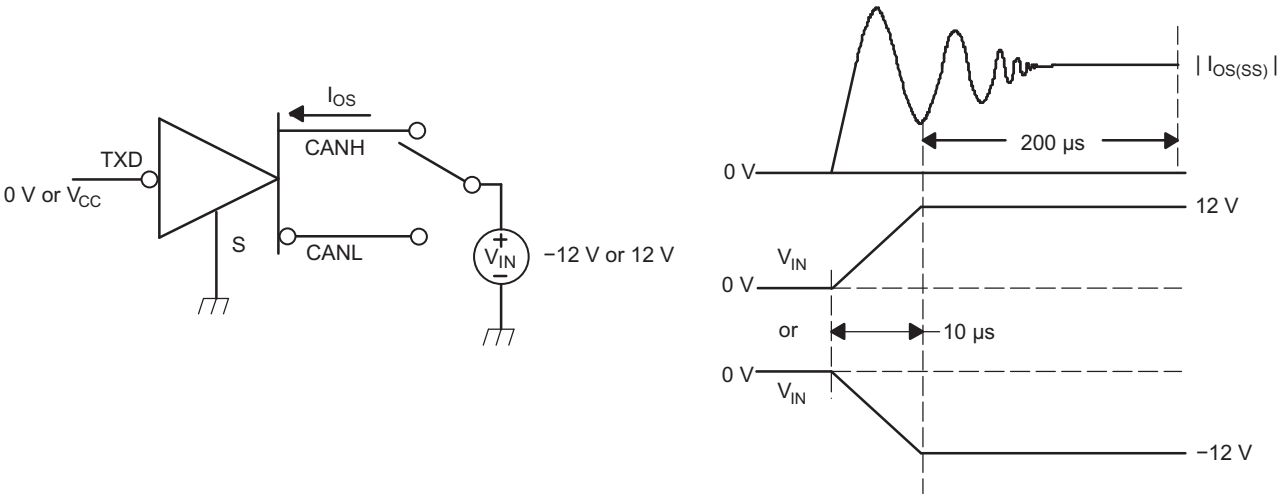


Figure 13. Driver Short-Circuit Current Test and Waveforms

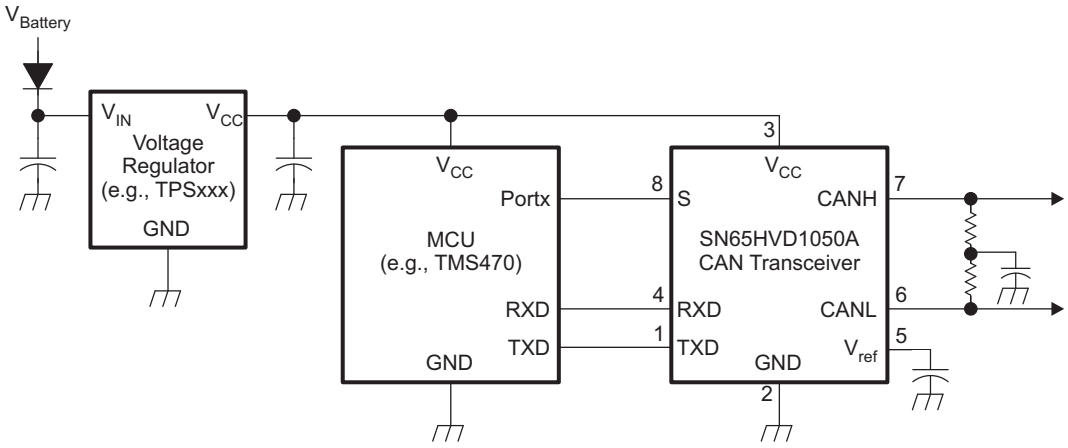


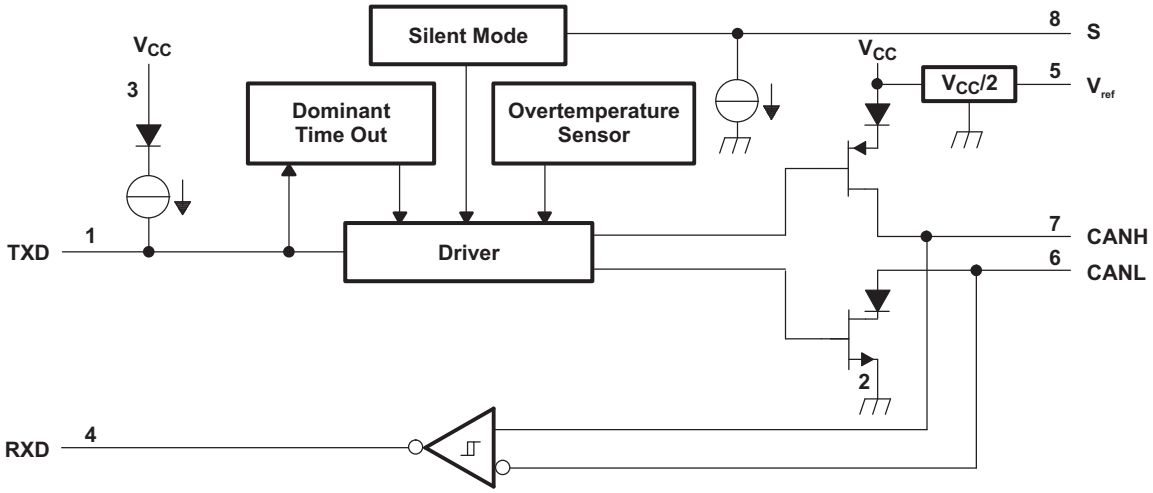
Figure 14. Typical Application

9 Detailed Description

9.1 Overview

The SN65HVD1050A-Q1 CAN transceiver is compatible with the ISO 11898-2 high-speed controller area network (CAN) physical layer standard. The device is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 TXD Dominant State Time-Out

During normal mode operation (the only mode where the CAN driver is active), the TXD dominant time-out circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period, t_{DST}. The dominant time-out circuit is triggered by a falling edge on TXD. If no rising edge occurs before the time-out constant of the circuit expires (t_{DST}), the CAN bus driver is disabled, thus freeing the bus for communication between other network nodes. The CAN driver is reactivated when a recessive signal occurs on the TXD pin, thus clearing the dominant-state time-out. The CAN bus pins are biased to recessive level during a TXD dominant-state time-out, and SPLIT (V_{REF}) remains on.

NOTE

The maximum dominant TXD time allowed by the TXD dominant state time-out limits the minimum possible data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(dom)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:

Minimum Bit Rate = 11 / $t_{(dom)}$

9.3.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal-shutdown threshold, the device turns off the CAN driver circuits. The SPLIT (V_{REF}) pin remains biased. This condition is cleared when the temperature drops below the thermal-shutdown temperature of the device.

9.3.3 Undervoltage Lockout and Unpowered Device

The device has undervoltage detection and lockout on the V_{CC} supply. If an undervoltage condition is detected on V_{CC}, the device protects the bus.

Feature Description (continued)

The TXD pin is pulled up to V_{CC} to force a recessive input level if the pin floats. The S pin is pulled up to GND to force the device into normal mode if the pin floats.

The bus pins [CANH, CANL, and SPLIT (V_{REF})] all have low leakage currents when the device is unpowered.

9.4 Device Functional Modes

9.4.1 Operating Modes

The device has two main operating modes: normal mode and silent mode. Operating mode selection is made through the S input pin.

Table 2. Operating Modes

S PIN	MODE	DRIVER	RECEIVER	RXD PIN
LOW	Normal	Enabled (On)	Enabled (On)	Mirrors CAN bus
HIGH	Silent	Disabled (Off)	Enabled (On)	Mirrors CAN bus

9.4.1.1 Normal Mode

This is the normal operating mode of the device. Normal mode is selected by setting S low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state, the bus pins are biased to 0.5 × V_{CC}. In dominant state, the bus pins (CANH and CANL) are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

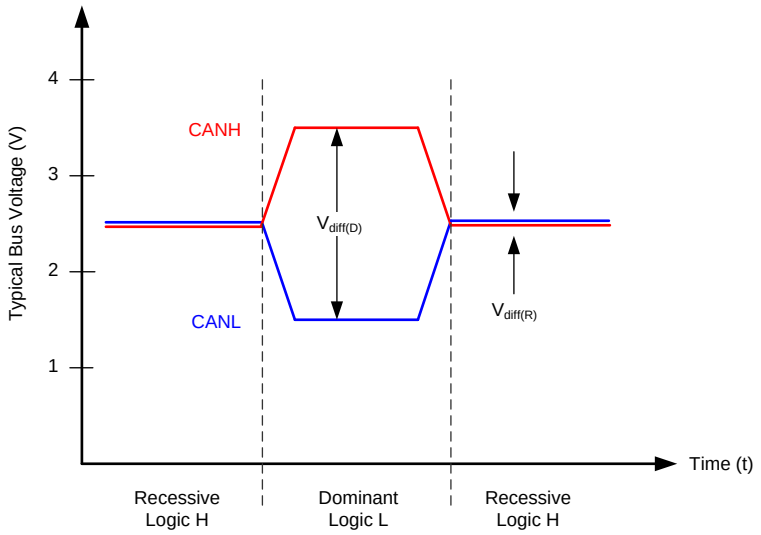


Figure 15. Bus Logic-State Voltage Definitions

The SPLIT (V_{REF}) pin is biased to 0.5 × V_{CC} for bus common mode bus voltage bias stabilization in split termination network applications.

9.4.1.2 Silent Mode

Silent mode disables the driver (transmitter) of the device; however, the receiver still operates and translates the differential signal from CANH and CANL to the digital output on RXD. It is selected by setting S high. The bus pins (CANH and CANL) are biased to 0.5 × V_{CC}. The SPLIT (V_{REF}) pin is biased to 0.5 × V_{CC}.

Table 3 and Table 4 lists the functional modes of the SN65HVD1050A-Q1.

Table 3. Driver(1)

INPUTS		OUTPUTS		BUS STATE
TXD	S	CANH	CANL	
L	L or Open	H	L	Dominant
H	X	Z	Z	Recessive
Open	X	Z	Z	Recessive
X	H	Z	Z	Recessive

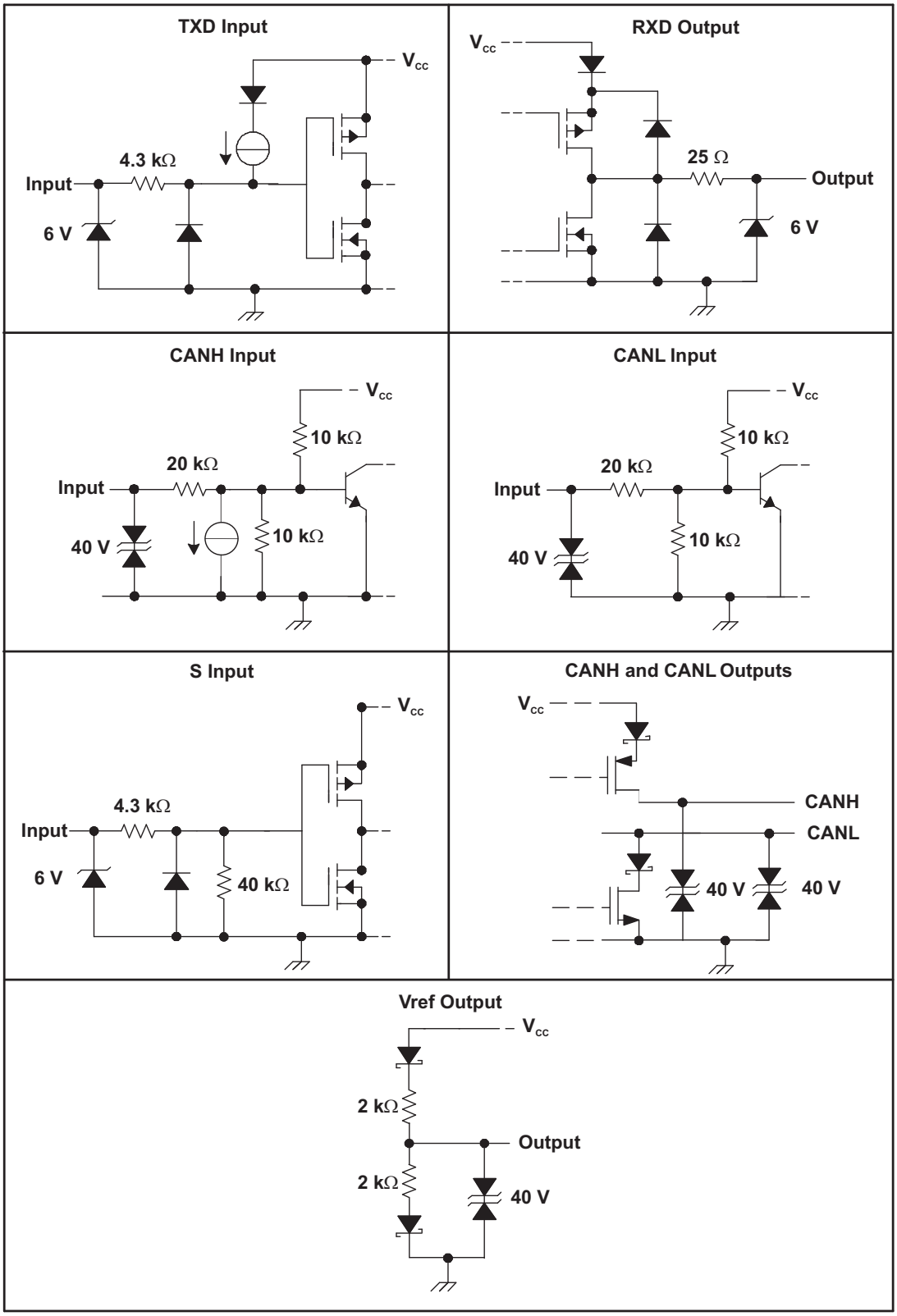
(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance

Table 4. Receiver(1)

DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9$ V	L	Dominant
0.5 V < V_{ID} < 0.9 V	?	?
$V_{ID} \leq 0.5$ V	H	Recessive
Open	H	Recessive

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance

9.4.2 Equivalent Input and Output Schematic Diagrams



10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Using the Device With 3.3-V Microcontrollers

The input level threshold for the digital input pins of this device is 3.3-V compatible; however, a few application considerations must be taken when using this device with 3.3-V microcontrollers. The TXD input pin has an internal pullup source to V_{CC}. Some microcontroller vendors recommend using an open-drain configuration on their I/O pins in this case, even though the pullup limits the current. As such, care must be taken at the application level that TXD has sufficient pullup to meet system timing requirements for CAN. The internal pullup on TXD especially may not be sufficient to overcome the parasitic capacitances and allow for adequate CAN timing; thus, an additional external pullup may be required. Care must also be taken with the RXD pin of the microcontroller, as the RXD output of this device drives the full V_{CC} range (5 V). If the microcontroller RXD input pin is not 5-V tolerant, this must be addressed at the application level. Other options include using a CAN transceiver from Texas Instruments with I/O level adapting or a 3.3-V CAN transceiver.

10.1.2 Using SPLIT (V_{REF}) With Split Termination

The SPLIT (V_{REF}) pin voltage output provides 0.5 × V_{CC} in normal mode. This pin is specified for both the SPLIT sink/source current condition and the V_{REF} sink/source current condition. The circuit may be used by the application to stabilize the common-mode voltage of the bus by connecting it to the center tap of split termination for the CAN network (see Figure 16). The SPLIT (V_{REF}) pin provides a stabilizing recessive voltage drive to offset leakage currents of unpowered transceivers or other bias imbalances that might bring the network common-mode voltage away from 0.5 × V_{CC}. Using this feature in a CAN network improves the electromagnetic-emissions behavior of the network by eliminating fluctuations in the bus common-mode voltage levels at the start of message transmissions.

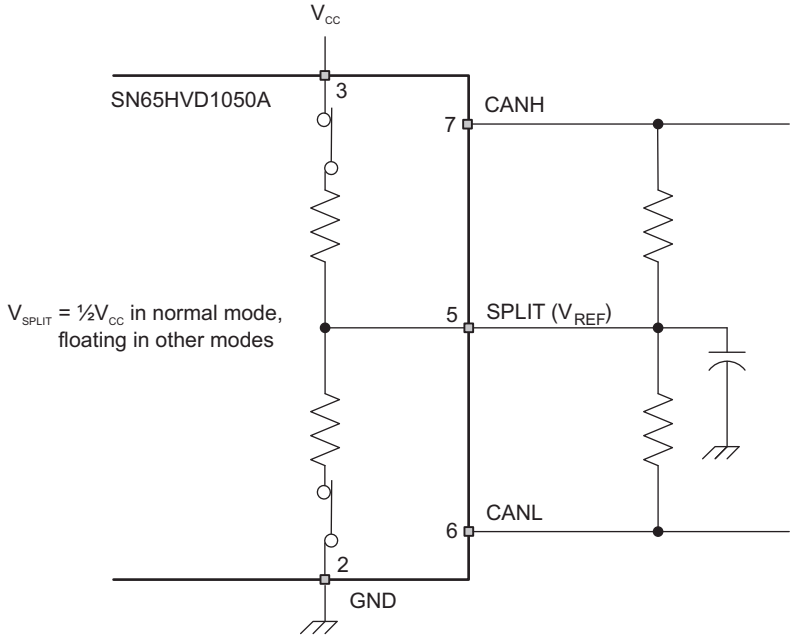


Figure 16. SPLIT Pin Stabilization Circuitry and Application

10.2 Typical Application

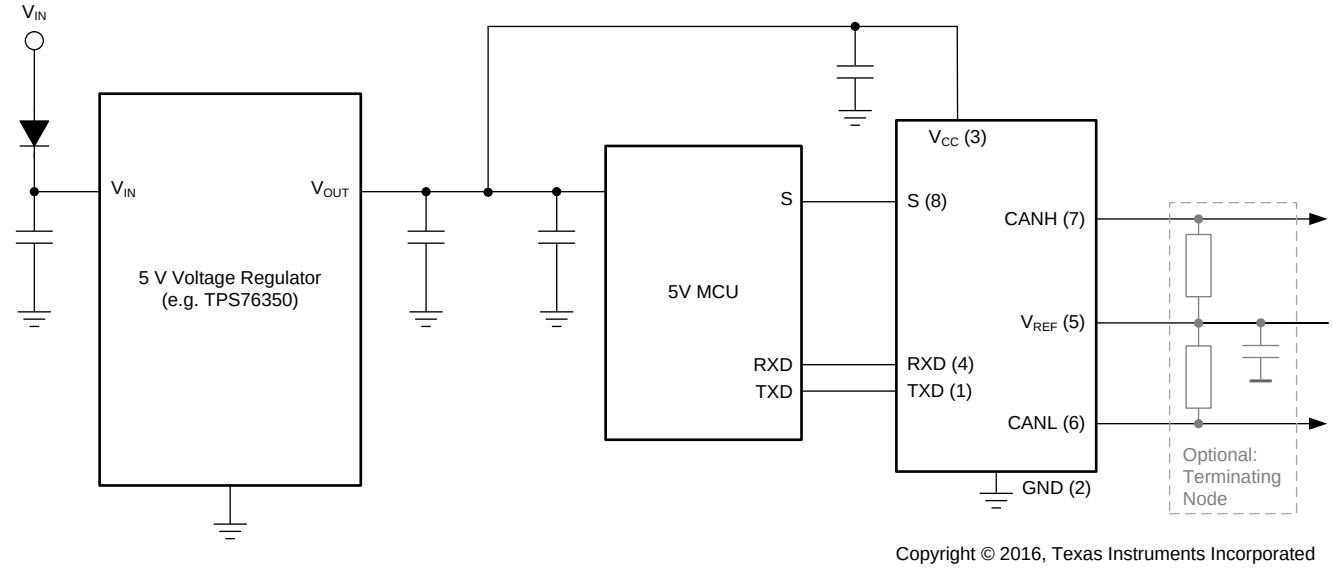


Figure 17. Typical Application Using Split Termination for Stabilization

10.2.1 Design Requirements

10.2.1.1 Bus Loading, Length, and Number of Nodes

The ISO 11898 Standard specifies up to 1-Mbps data rate, a maximum bus length of 40 meters, a maximum drop-line (stub) length of 0.3 meters, and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet, and NMEA200 (see Figure 18).

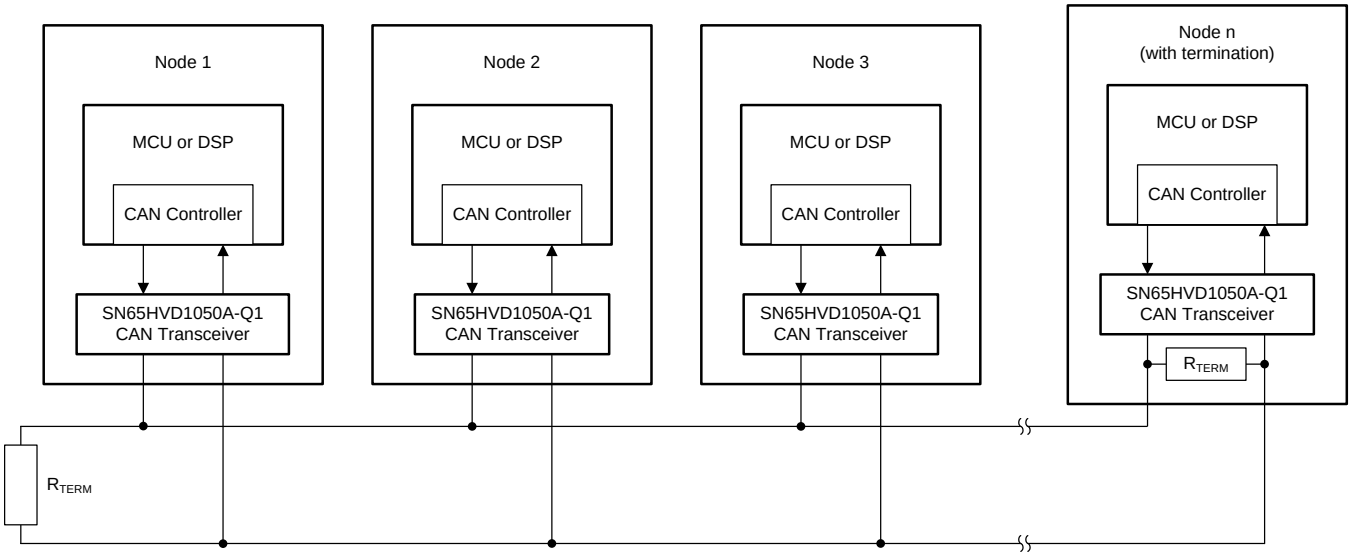


Figure 18. Typical CAN Bus

Typical Application (continued)

A high number of nodes requires a transceiver with high input impedance and wide common-mode range, such as the SN65HVD1050A-Q1 CAN transceiver. ISO 11898-2 specifies that the driver differential output with a 60-Ω load (two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVD1050A-Q1 device is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output voltage minimum of 1.2 V across a common-mode range of –2 V to 7 V through a 330-Ω coupling network. This network represents the bus loading of 90 SN65HVD1050A-Q1 transceivers based on their minimum differential input resistance of 30 kΩ. Therefore, the SN65HVD1050A-Q1 supports up to 90 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets, and signal integrity; thus the practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1-km with changes in the termination resistance, cabling, less than 64 nodes, and a significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

10.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so it is not removed from the bus.

Termination is typically a 120-Ω resistor at each end of the bus. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used (see Figure 19 and *Using SPLIT (V_{REF}) With Split Termination*).

Care must be taken when determining the power ratings of the termination resistors. A typical worst case fault condition is when the system power supply and ground are shorted across the termination resistance, which results in much higher current through the termination resistance than the current limit of the CAN transceiver.

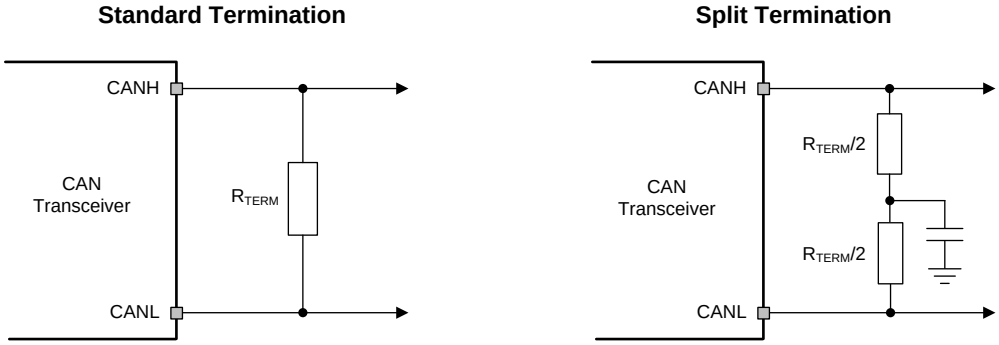


Figure 19. CAN Termination Scheme

10.2.1.3 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (the TXD pin) to the differential outputs (the CANH and CANL pins), plus the delay from the receiver inputs (the CANH and CANL) to its output (the RXD pin). A typical loop delay for the SN65HVD1050A-Q1 transceiver is displayed in Figure 21 and Figure 22.

Typical Application (continued)

10.2.2 Detailed Design Procedure

10.2.2.1 ESD Protection

A typical application that employs a CAN-bus network may require some form of ESD, burst, and surge protection to shield the CAN transceiver against unwanted transients, which could cause potential damage to the transceiver. To help shield the SN65HVD1050A-Q1 transceiver against these high energy transients, transient voltage suppressors can be implemented on the CAN differential bus terminals. These devices help to absorb the impact of an ESD, burst, or surge strike.

10.2.2.2 Transient Voltage Suppresser (TVS) Diodes

Transient voltage suppressors are the preferred protection components for a CAN bus due to their low capacitance, which allows for design into every node of a multi-node network without requiring a reduction in data rate (see Figure 20). With response times of a few picoseconds and power ratings of up to several kilowatts, TVS diodes present the most effective protection against ESD, burst, and surge transients.

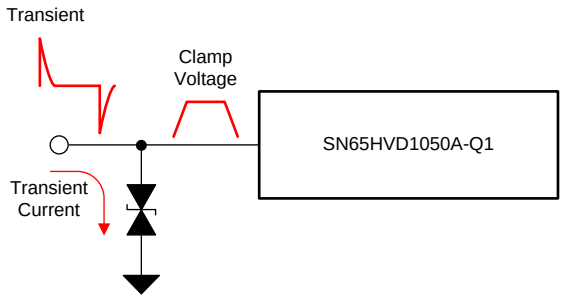


Figure 20. Transient

10.2.3 Application Curves

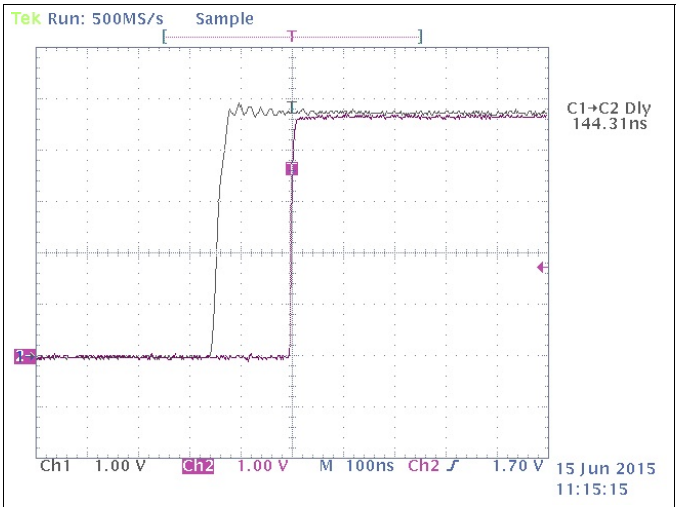


Figure 21. tLoop Delay Waveform Dominant to Recessive

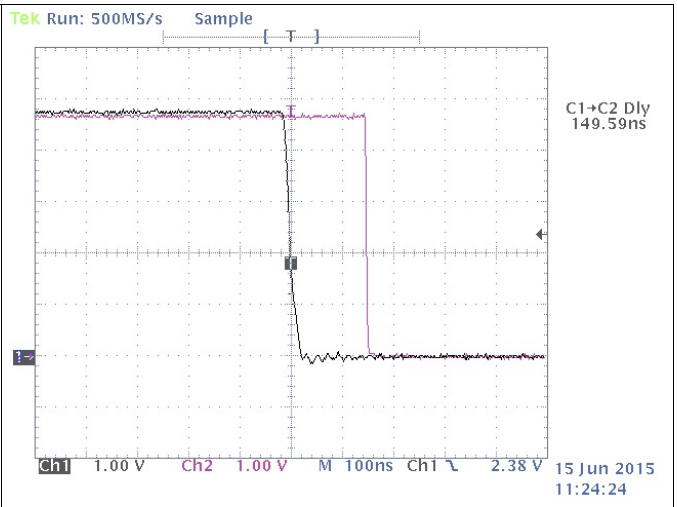


Figure 22. tLoop Delay Waveform Recessive to Dominant

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor located as close as possible to the V_{CC} supply pins. One option is the TPS76350 device, which is a linear voltage regulator that is suitable for the 5-V supply rail.

12 Layout

12.1 Layout Guidelines

In order for the PCB design to be successful, start with a design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. On-chip IEC ESD protection is good for laboratory and portable equipment, but it is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

Use V_{CC} and ground planes to provide low inductance.

NOTE

High-frequency current follows the path of least impedance and not the path of least resistance.

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. An example placement of the transient voltage suppressor (TVS) device indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 23.

The bus transient protection and filtering components must be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.

Bus termination: Figure 23 shows split termination, which is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground through capacitor C6. Split termination provides common-mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure that the terminating node is not removed from the bus because this causes signal integrity issues if the bus is not properly terminated on both ends. Bypass and bulk capacitors must be placed as close as possible to the supply pins of transceiver, examples include C2 and C3 (V_{CC}).

Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit the current of digital lines, serial resistors may be used. Examples are R1, R2, R3, and R4.

To filter noise on the digital I/O lines, a capacitor may be used close to the input side of the I/O as shown by C1 and C4.

Because the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-kΩ to 10-kΩ pullup or pulldown resistor must be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open-drain host processor is used to drive the TXD pin of the device, an external pullup resistor between 1 kΩ and 10 kΩ must be used to drive the recessive input state of the device.

Pin 5: SPLIT must be connected to the center point of a split termination scheme to help stabilize the common-mode voltage to V_{CC} / 2. If SPLIT is unused, it must be left floating.

Pin 8: Is shown assuming the mode pin, STB, is used. If the device is only to be used in normal mode, R3 is not needed, and the pads of C4 could be used for the pulldown resistor to GND

12.2 Layout Example

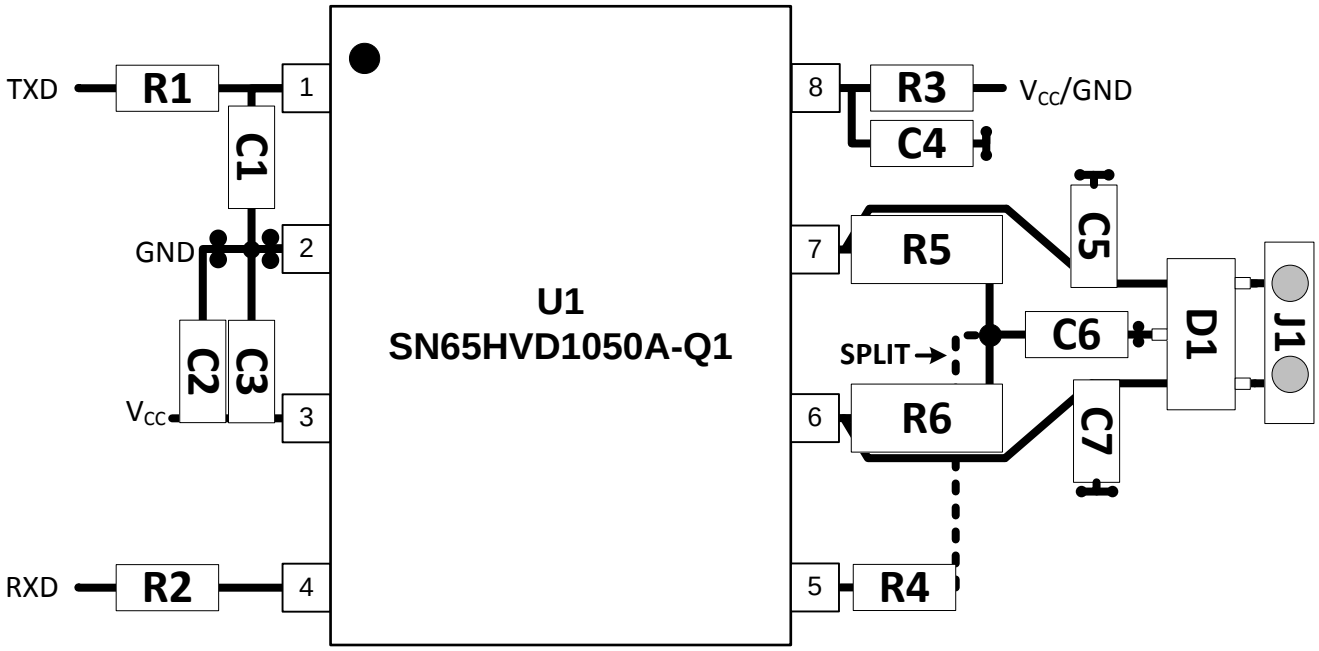


Figure 23. SN65HVD1050A-Q1 Layout Example

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me*to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1050AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1050AQ
SN65HVD1050AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1050AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

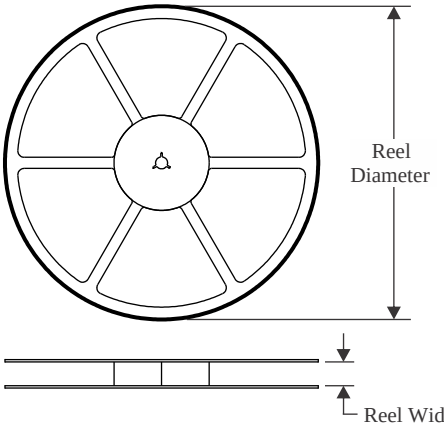
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

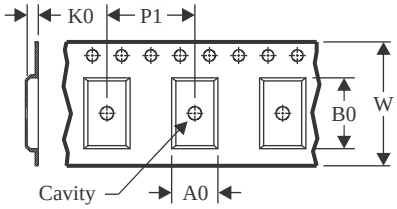
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

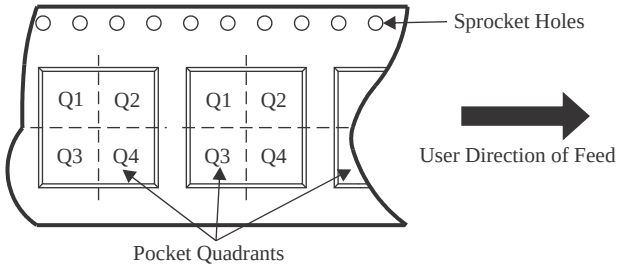


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

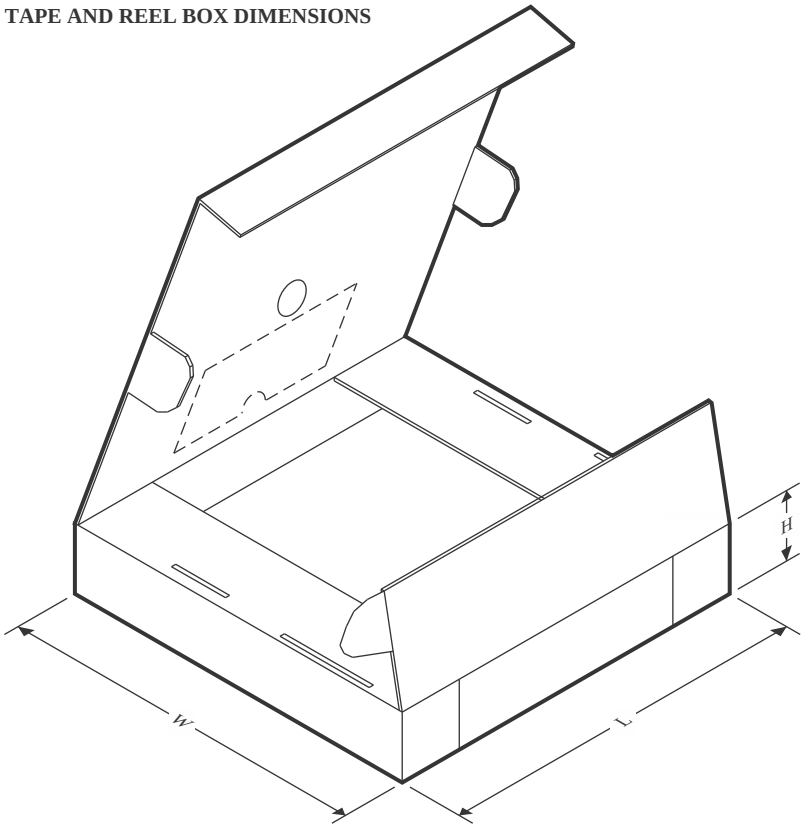
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

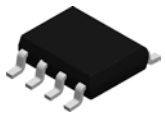
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1050AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD1050AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1050AQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
SN65HVD1050AQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

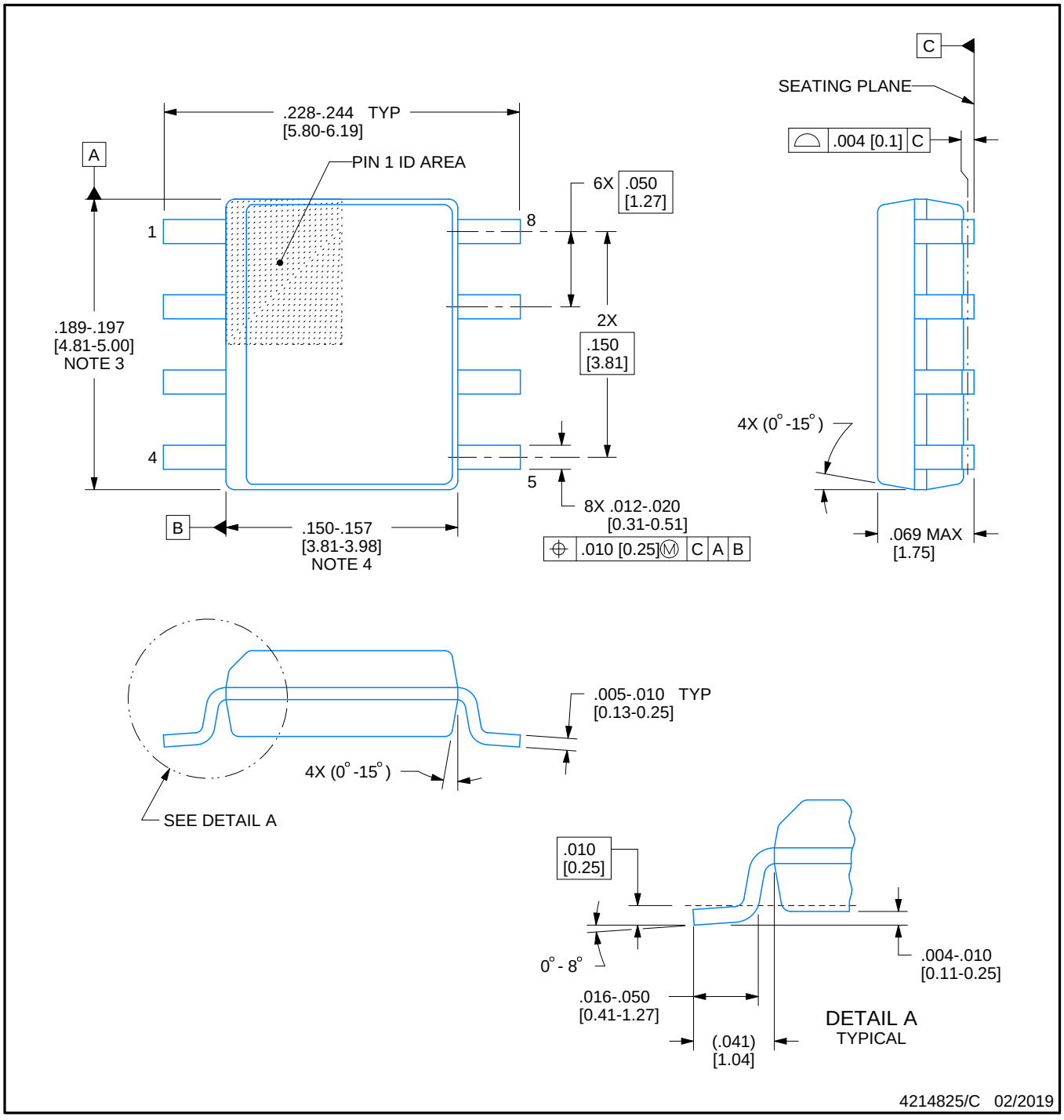


PACKAGE OUTLINE

D0008A

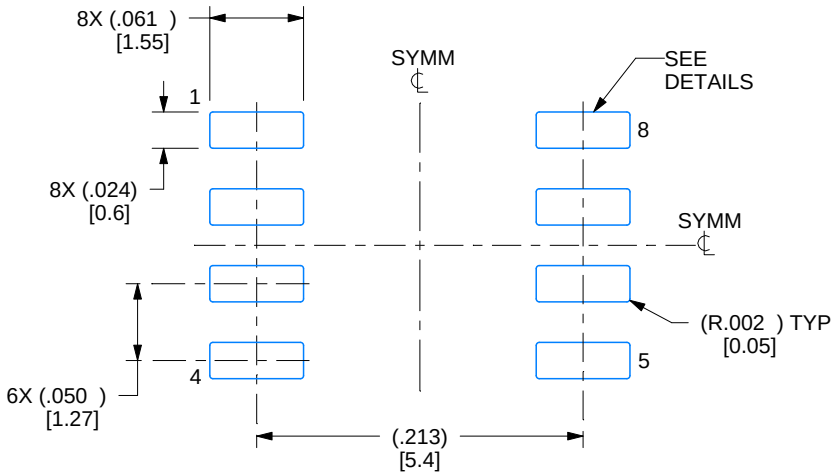
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

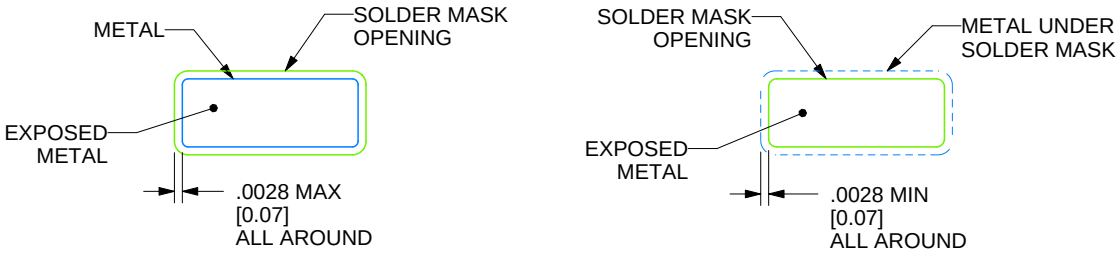


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

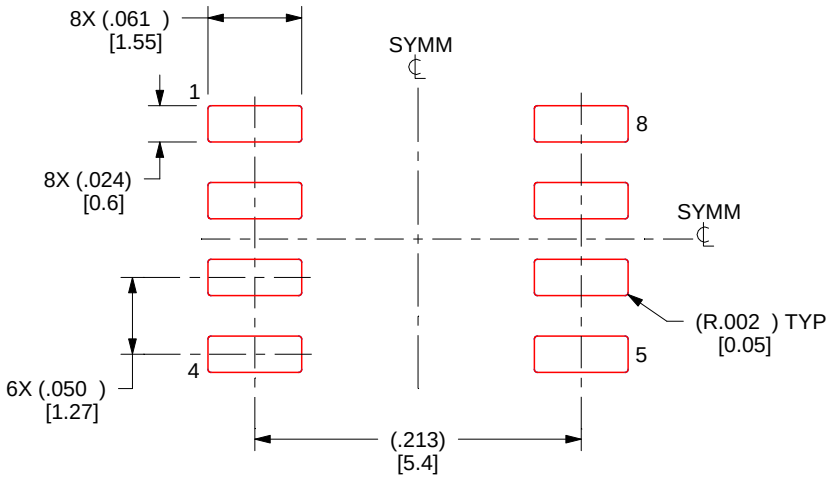
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025