ControlNet™ TRANSCEIVER

Check for Samples: SN65HVD61

FEATURES

- **Compatible With the ControlNet Standard**
- **I/O Operates From 2.5-V to 5-V Supply**
- **Receiver thresholds within –120mV to 120mV**
- **Receiver hysteresis >50mV**
- **Low Power Standby Mode**
- **Thermal Shutdown Protection**
- **Power-Up/Down Glitch-free Bus Inputs and Outputs**
- **Short-Circuit Protection on Outputs**
- **RoHS Compliant**
- **ControlNet Vendor ID 806**

DESCRIPTION

The SN65HVD61 is designed to meet the requirements for the driver and receiver circuitry of the ControlNet coaxial-based physical layer.

These devices are single-channel circuits with one transceiver for single node operation or distributed stand-alone applications.

The pull-or-pull transmitter circuit is designed to sink current from a center-tapped transformer, providing galvanic isolation from the shared bus.

These devices incorporate a differential receiver (RX) with the 120 mV sensitivity needed by ControlNet industrial applications.

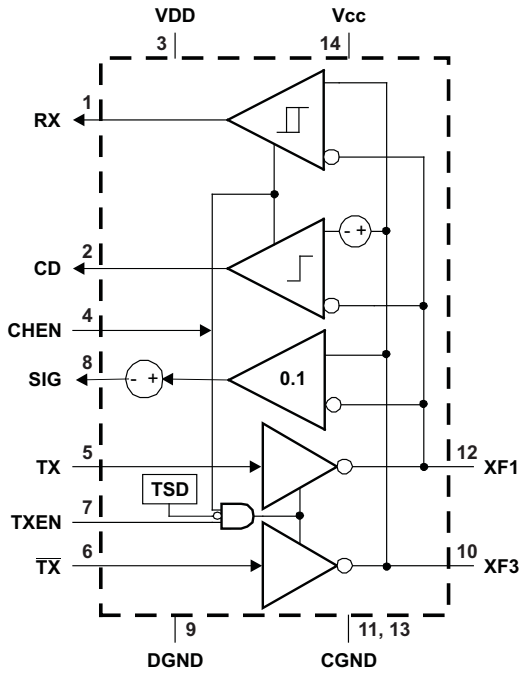
A secondary receiver (CD) detects the presence of a valid positive differential signal.

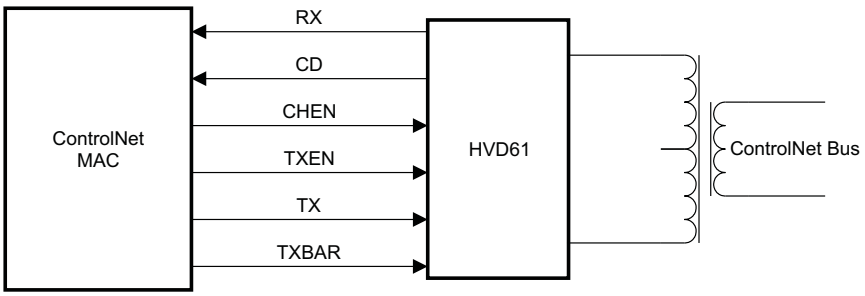
The third signal receiver function (SIG) provides a scaled analog output which is proportional to the differential voltage between XF1 and XF3. This output can be used for diagnostic purposes.

APPLICATIONS

- **Industrial Networks**
- **Programmable Controllers**
- **Industrial Drives**

FUNCTIONAL DIAGRAM





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ControlNet is a trademark of ODVA.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PACKAGE(1)	MARKED AS
SN65HVD61	D	65HVD61
	DR(2)	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) R suffix indicates tape and reel

ABSOLUTE MAXIMUM RATINGS(1)

				VALUE	UNIT
V_{CC}	Supply voltage(2) (3)			–0.3 to 6	V
V_{DD}	Supply voltage(4)			–0.3 to 6	V
	Logic input voltage range (TX, TXBAR , TXEN, CHEN)			–0.5 to 6	V
	Bus terminal voltage range (XF1, XF3)			–22 to +22	V
	Logic input current, (TX, TXBAR , TXEN, CHEN)			–20 to 20	mA
	Bus terminal current (XF1, XF3)			Internally limited	
	Receiver output current (RX, CD)			±15	mA
	Electrostatic discharge	Human Body Model(4)	Bus pins (XF1, XF3)	16	kV
			All other pins	4	kV
		Charged Device Model (5)	All pins	1500	V
		Machine Model (6)		200	V
T_J	Junction temperature (see (7) below regarding thermal shutdown)			170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) DGND and CGND should be connected to a common ground plane external to the device. All voltage values, except differential I/O bus voltages, are with respect to the ground plane
(3) V_{CC} and V_{DD} lower limits are DC conditions, see application information regarding start-up transients.
(4) Tested in accordance JEDEC Standard 22, Test Method A114-A.
(5) Tested in accordance JEDEC Standard 22, Test Method C101.
(6) Tested in accordance JEDEC Standard 22, Test Method A115-A.
(7) If the internal junction temperature exceeds 170°C, a thermal shutdown function will disable the transmitter.

DISSIPATION RATINGS

CIRCUIT BOARD MODEL(1)	$T_A \le 25°C$	DERATING FACTOR(2) ABOVE $T_A = 25°C$	$T_A = 65°C$	$T_A = 100°C$
Low-K	625 mW	5 mW/°C	425 mW	250 mW
High-K	1180 mW	9.5 mW/°C	800 mW	475 mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages. For additional information about JEDEC thermal models, see Texas Instruments Application Note *Thermal Characteristics of Logic and Linear Packages using JEDEC PCB Designs* (SZZA017).
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage (1)		4.5	5	5.5	V
V_{DD}	Input/Output supply voltage (2)		2.375		5.5	V
V_{IH}	High-level logic input voltage	TX, TXBAR, TXEN, CHEN	0.7×VDD		VDD	V
V_{IL}	Low-level logic input voltage		0		0.3×VDD	
	Bus pin common-mode voltage	(VXF1 + VXF3) / 2	4.5		5.5	V
	Voltage at any bus terminal (XF1, XF3)		–10		15	V
	Transmitter peak output current (XF1, XF3)			130	150	mA
I_{OH}	High-level logic output current	RX, CD	–8			mA
I_{OL}	Low-level logic output current				8	
	Output current	SIG	–1		1	mA
T_A	Operating free-air temperature	4.75 V ≤ V_{CC} ≤ 5.25 V	–40		100	°C
		4.5 V ≤ V_{CC} ≤ 5.5 V	–30		100	
T_J	Junction temperature				150	
	Signaling rate			10		Mbps
	Relative humidity (non-condensing)				95%	

(1) A power-shutdown feature keeps the device disabled when the voltage at V_{CC} is below 2.1 V.
(2) The I/O ring voltage for this device (V_{DD}) should be the same as the power supply voltage for the controller with which it interfaces. In the case where the voltages are different, designers must consider the logic threshold compatibility between devices.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
BUS PINS (XF1, XF3)							
$V_{OL(TX)}$	Transmitter output low voltage	Connect to V_{CC} through 37.5 Ω, ±1% resistor			0.9	1.2	V
$V_{OH(TX)}$	Transmitter output high voltage			V_{CC}–0.05	V_{CC}		
$V_{O(OFF)}$	Transmitter off noise level, |XF3-XF1|	R_L = 37.5 Ω, 0 to 20 MHz BW, TX and TXBAR inputs idle, CHEN and TXEN inputs LO				5	mV
$V_{SW(PP)}$	Receiver-to-bus reflection, peak-to-peak	R1=R2=50 Ω, C1=C2=15pF, See Figure 3				200	mV
V_{TH+}	Positive-going differential input threshold voltage	4.5V < Vcm < 5.5V			35	120	mV
V_{TH-}	Negative-going differential input threshold voltage	4.5V < Vcm < 5.5V		–120	–35		mV
V_{hys}	Hysteresis voltage (V_{TH+} – V_{TH-})	4.5V < Vcm < 5.5V, RX output		50	70		mV
V_{CD}	Carrier detect threshold voltage, (XF3–XF1)	4.5V < Vcm < 5.5V		23	175	255	mV
I_I	Bus terminal input leakage current	V_I = 10V, TXEN at 0V, Other input at –10V to 10V				1.2	mA
		V_I = –10V, TXEN at 0V Other input at –10V to 10V		–1.7			
$I_{I(off)}$	Bus terminal input leakage current	V_{CC} < 2V, V_I = -10V to 10V Other input at –10 V to 10 V		–1.7		1.2	mA
I_{OS}	Short-circuit output current	0 < V_O < V_{CC}		–400		400	mA
R_{IN}	Bus terminal input resistance	V_I = –10V to 10V, Other input at CGND, DC		12			kΩ
C_{IN}	Differential input capacitance (XF1-to-XF3)	10 MHz AC test frequency, 1V_{PP} amplitude using HP4194A or equivalent impedance analyzer, V_{CC} = 0V			7	11	pF
LOGIC INPUTS (TX, TXBAR, TXEN,CHEN)							
I_I	Logic input current	TX, TXBAR, TXEN, CHEN		–100		100	µA
$I_{I(off)}$	Logic input power-off current	V_{DD} at 0 V, TX,TXBAR, TXEN, CHEN			–100	100	µA
LOGIC OUTPUTS (RX, CD)							
V_{OH}	Logic output voltage, high level	C_L = 15 pF		0.8×V_{DD}			V
		I_O = –4 mA, V_{DD} > 3V		2.4			
V_{OL}	Logic output voltage, low level	C_L = 15 pF				0.2×V_{DD}	V
		I_O = 4 mA				0.4	
I_{OZ}	Logic output high-impedance-state current	RX, CD, 0 < V_O < V_{DD}		–20		20	µA
$I_{O(off)}$	Logic output power-off current	V_{DD} at 0 V, 0 < V_O < 5.5V		–1		1	mA
SIGNAL STRENGTH PIN (SIG)							
$V_{SIG(0)}$	SIG output voltage with zero differential input voltage	R_L = 5 kΩ		1.125	1.25	1.375	V
GAIN	SIG gain $\Delta V_O/\Delta V_{ID}$	V_{ID} switching at 10 Mbps, V_O measured with 20 MHz bandwidth, See Figure 10	4.75V ≤ V_{CC} ≤ 5.25V			120	mV/V
			4.5V ≤ V_{CC} ≤ 5.5V			140	
POWER SUPPLY PINS (V_{CC}, CGND, VDD, DGND)							
I_{CC}	Analog supply current (dynamic)	CHEN and TXEN at logic high, No load			36	65	mA
	Analog supply current, chip disabled	CHEN at logic low			1.8	3	
	Analog supply current, Lowest power conditions	CHEN at DGND, TX and TXBAR at V_{DD}			0.8	2	
I_{DD}	I/O supply current, I/O, dynamic	CHEN at logic high, no load				5	mA
	I/O supply current, I/O, chip disabled	CHEN at logic low				105	µA

(1) All typical values are at 25°C and with a 5 V supply. For typical values with a 3.3V supply, refer to the TYPICAL CHARACTERISTICS curves.

SWITCHING CHARACTERISTICS

over operating recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TRANSMITTER							
t_r	Output rise time (10%-to-90%) differential	R_L = 37.5 Ω, C_L = 15 pF, CHEN and TXEN at logic high, See Figure 1 (1)			20	30	ns
t_f	Output fall time (90%-to-10%) differential				20	30	
t_{PLH}	Propagation delay time, low-to-high-level differential output				22	50	
t_{PHL}	Propagation delay time, high-to-low-level differential output				24	50	
$t_{sk(p)}$	Pulse skew, differential (XF3-XF1) $\lvert t_{PLH} - t_{PHL} \rvert$				2	5	
$t_{OUT\ SKEW}$	Output delay skew, $t_{pON} - t_{pOFF}$, single-ended outputs	R_L = 37.5 Ω, C_L = 15 pF, CHEN and TXEN at logic high, See Figure 2		0	7	12	ns
t_{ON}-t_{OFF}	Symmetry, turn-on-time-to-turn-off-time, 10%/90%, each single-ended output			0	9	12	
t_{PZL}	Propagation delay time, disabled-to-low-level output	R_L = 37.5 Ω, C_L = 15 pF, See Figure 4	TXEN changing, CHEN at VDD			250	ns
t_{PLZ}	Propagation delay time, low-level-to-disabled-output					400	
t_{PZL}	Propagation delay time, disabled-to-low-level output		CHEN changing, TXEN at VDD			400	
t_{PLZ}	Propagation delay time, low-level-to-disabled-output					400	
SR	Output differential slew rate	See Figure 1	0°C < T < 85°C			1	V/ns
	Transmit jitter, differential	10 Mbps Manchester-code			2.5		ns
RECEIVERS (RX and CD)							
t_r	Output rise time (10%-to-90%)	V_{ID} = ±2.5V, R_L = 1 kΩ, C_L = 15 pF, See Figure 5			2	20	ns
t_f	Output fall time (90%-to-10%)				2	20	
t_{PLH}	Propagation delay time, low-to-high-level output				25	40	
t_{PHL}	Propagation delay time, high-to-low-level output				25	40	
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$		RX		0.2	4.5	
			CD			7	
t_{PZL}	Propagation delay time,high-impedance-to-low-level output	V_{ID} = –2.5V, R_L = 1kΩ, C_L = 15 pF, See Figure 6				1000	ns
t_{PLZ}	Propagation delay time,low-level-to-high-impedance output					55	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	V_{ID} = 2.5V, R_L = 1kΩ, C_L = 15 pF, See Figure 7				1000	ns
t_{PHZ}	Propagation delay time, high-level-to-high- impedance output					55	
	Receive jitter	10 Mbps Manchester-code			0.5		

(1) 30 ns maximum represents the worst-case allowable rise/fall time when connected to a transformer-coupler network.

PARAMETER MEASUREMENT INFORMATION

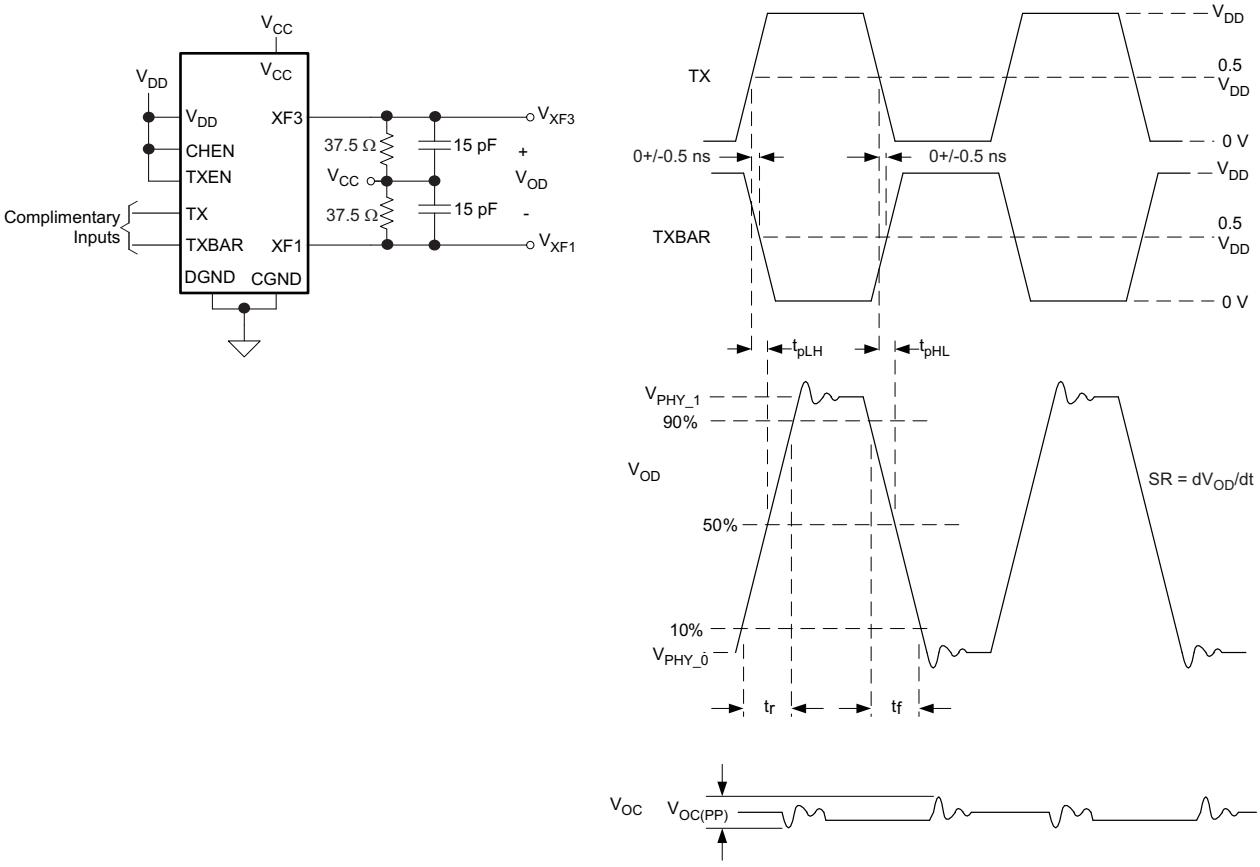


Figure 1. Transmitter Differential Switching Characteristics

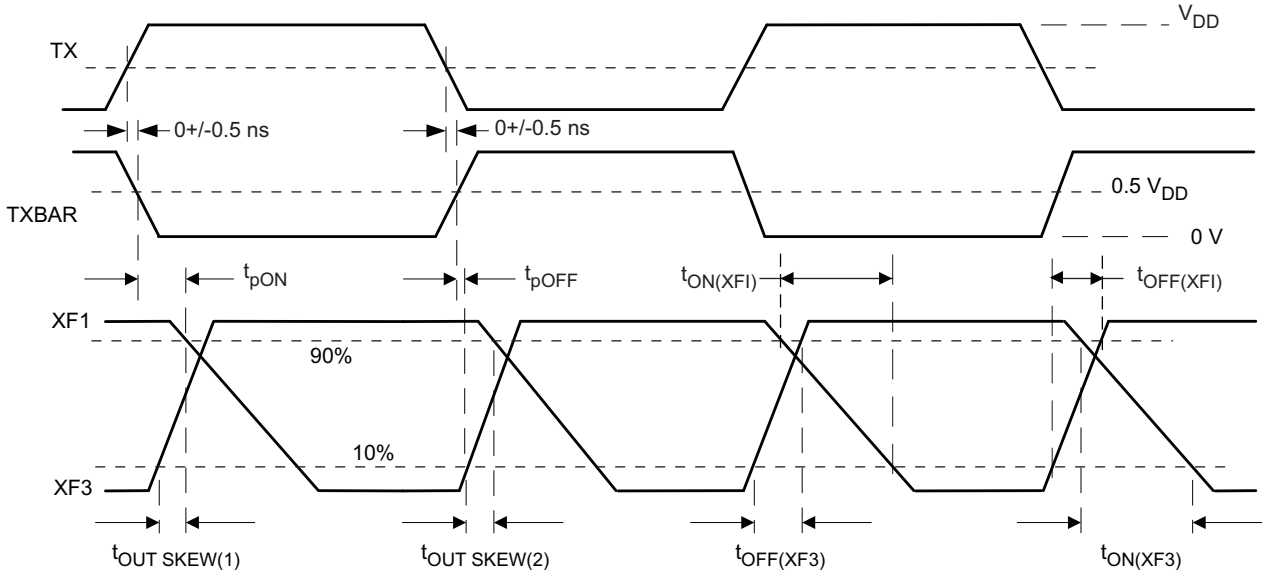


Figure 2. Transmitter Single-Ended Switching Characteristics

PARAMETER MEASUREMENT INFORMATION (continued)

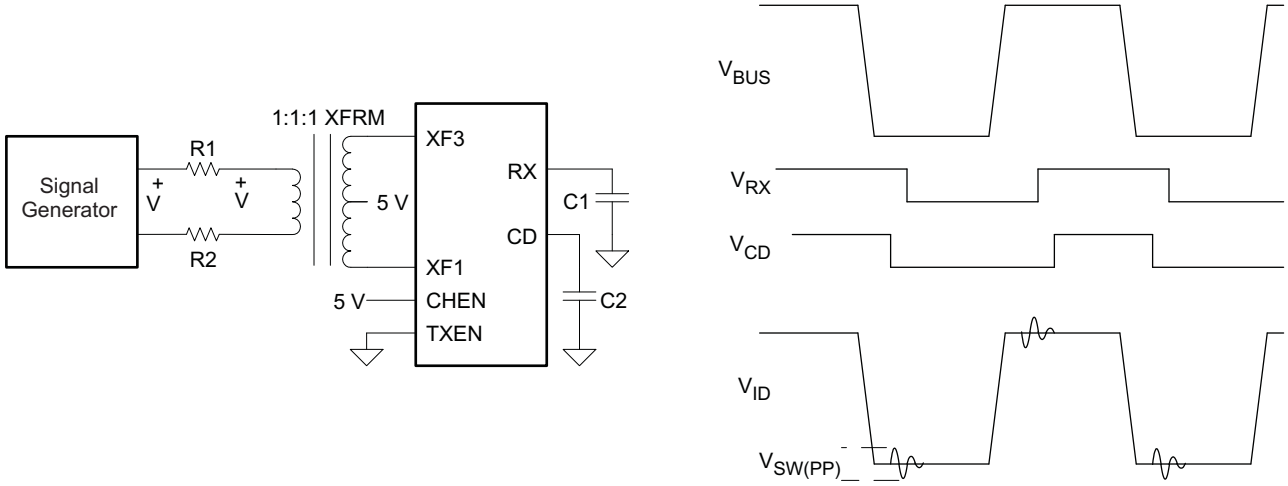


Figure 3. Receiver-to-Bus Reflection Measurement

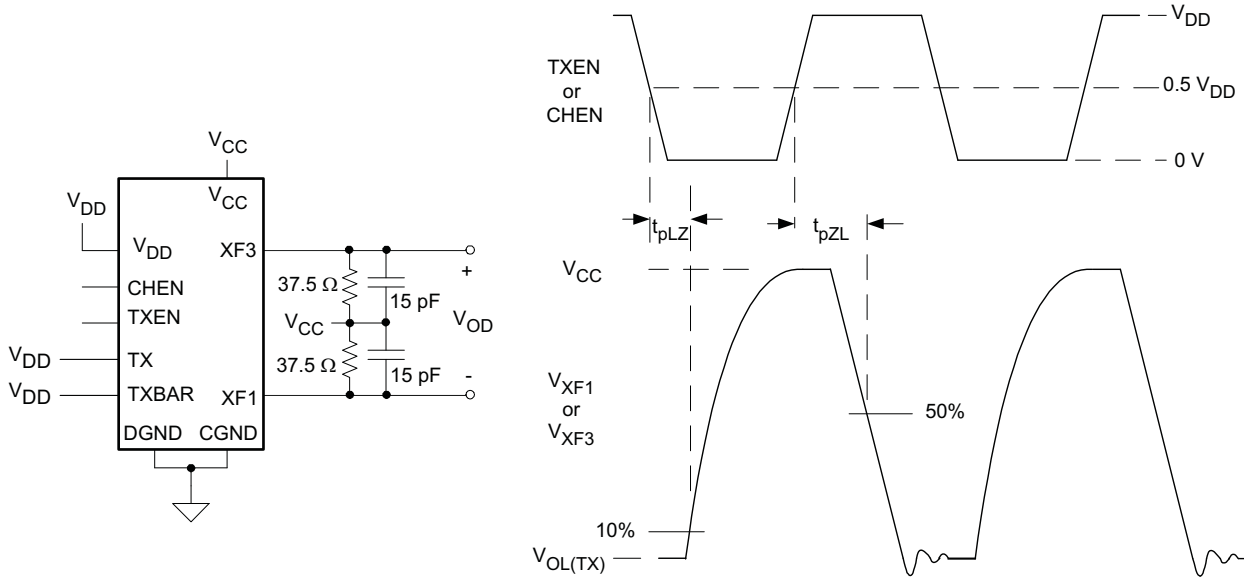


Figure 4. Transmitter Enable/Disable Test Circuits and Characteristics

PARAMETER MEASUREMENT INFORMATION (continued)

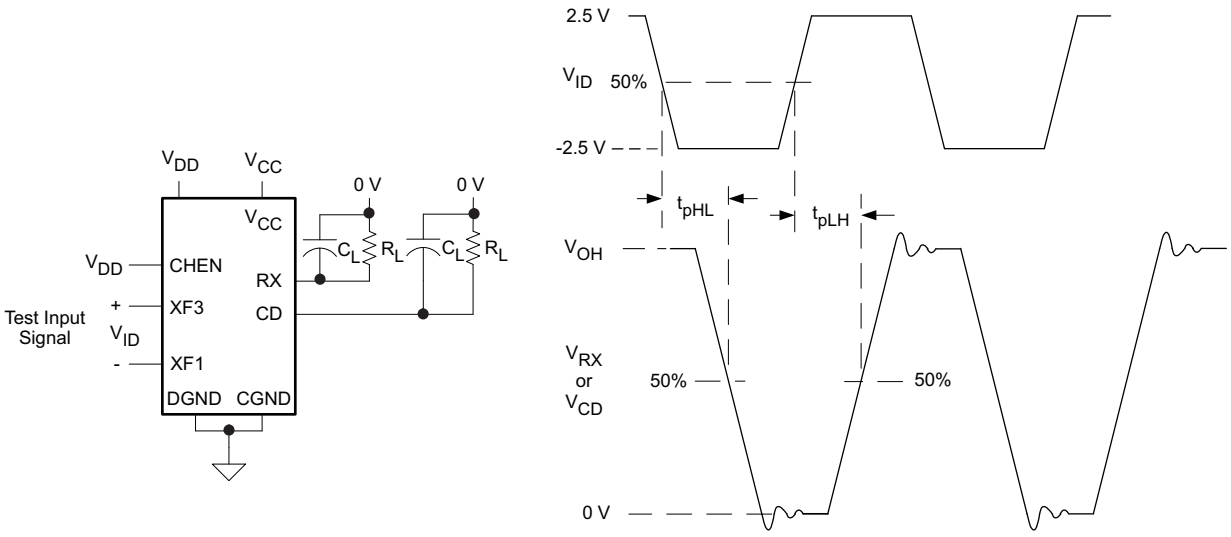


Figure 5. Test Circuit and Signal Waveforms, Receiver and Carrier Detect

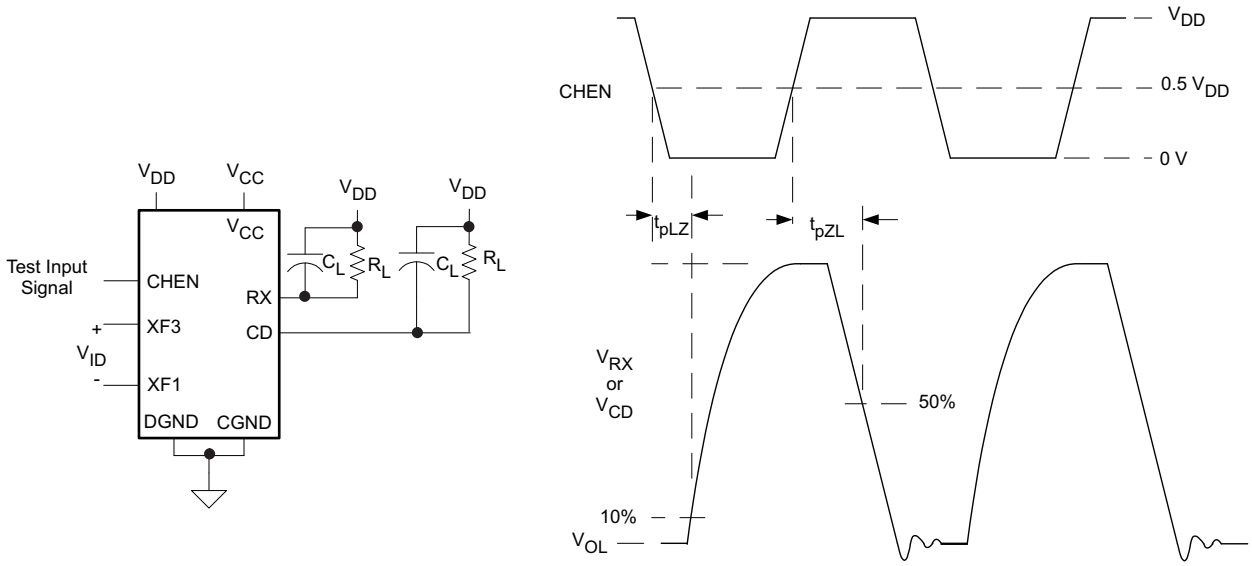


Figure 6. Test Circuit and Signal Waveforms, Receiver Enable and Disable With Low Bus Input

PARAMETER MEASUREMENT INFORMATION (continued)

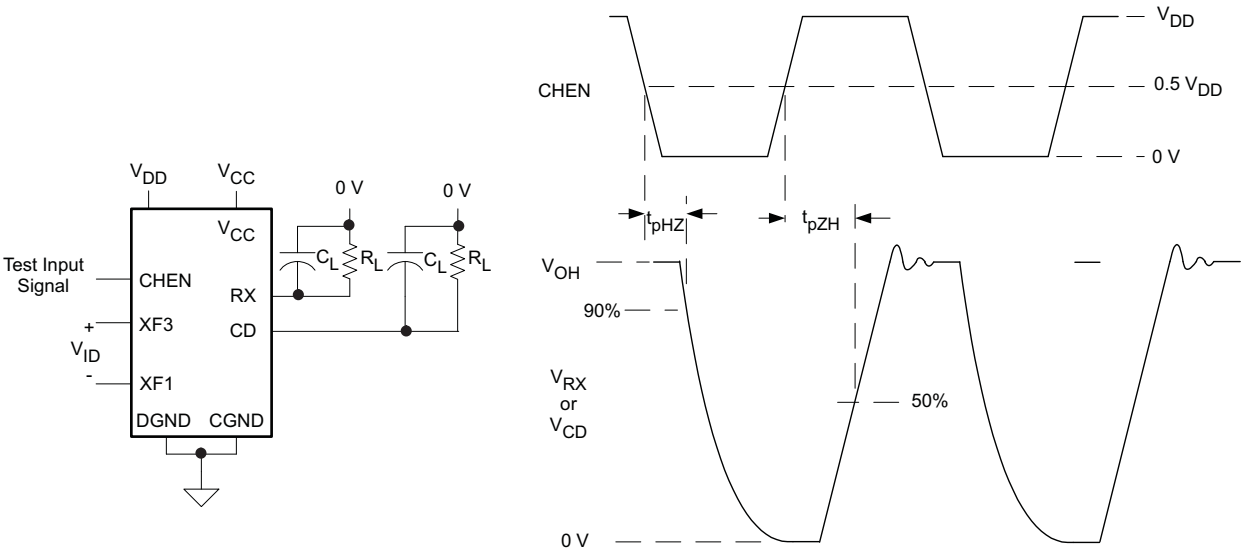


Figure 7. Test Circuit and Signal Waveforms, Receiver Enable and Disable With High Bus Input

Table 1. FUNCTION TABLES

TRANSMITTER					
INPUTS				OUTPUTS	
CHEN	TXEN	TX	TXBAR	XF1	XF3
L or OPEN	X	X	X	Z	Z
H	L or OPEN	X	X	Z	Z
	H	L or OPEN	L or OPEN	Z	Z
		L or OPEN	H	Z	L
		H	L or OPEN	L	Z
	H(1)	H(1)	H(1)	L(1)	L(1)

(1) This combination is not supported and should be avoided in ControlNet applications

RECEIVER			
INPUTS			OUTPUT
CHEN	XF1, XF3	CONDITION	RX
L or OPEN	X	Chip disabled	Z
H	$(V_{XF3} - V_{XF1}) < V_{TH-}$	Negative signal	L
	$V_{TH-} < (V_{XF3} - V_{XF1}) < V_{TH+}$	No signal	?
	$V_{TH+} < (V_{XF3} - V_{XF1})$	Positive signal	H

CARRIER DETECT			
INPUTS			OUTPUT
CHEN	XF1, XF3	CONDITION	CD
L or OPEN	X	Chip disabled	Z
	$(V_{XF3} - V_{XF1}) < V_{CD}$	Carrier not detected	L
	$V_{CD} < (V_{XF3} - V_{XF1})$	Carrier detected	H

TYPICAL CHARACTERISTICS

CD VOLTAGE vs INPUT VOLTAGE

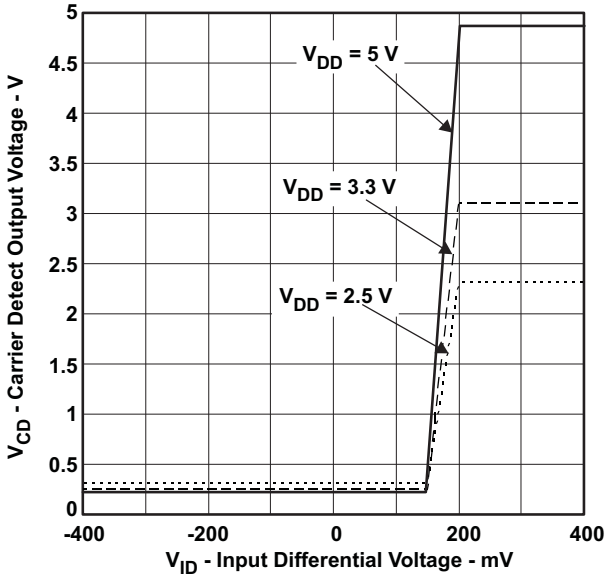


Figure 8.

RX VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

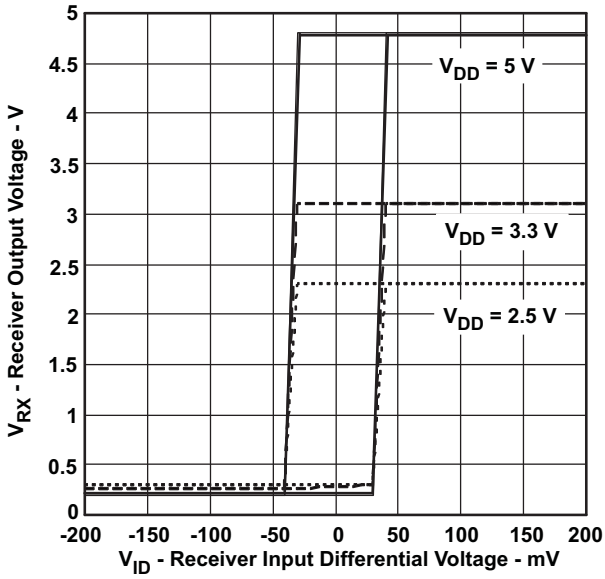


Figure 9.

SIG VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

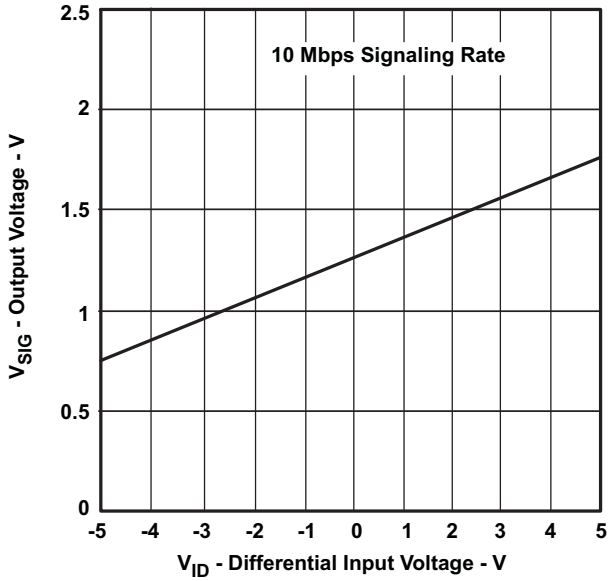


Figure 10.

APPLICATION INFORMATION

THERMAL SHUTDOWN

In most cases, the device's internal junction temperature will not reach the thermal shutdown temperature if operated within the recommended operating conditions. However, during fault conditions, such as driver short-circuit, the junction temperature may reach the thermal shutdown limit. This also depends on the thermal characteristics of the device mounting, the circuit board, and environmental factors. After the device reaches the thermal shutdown temperature, the driver outputs will be disabled, and the device will cool down. If the short-circuit is still present when the drivers are re-enabled, this *thermal shutdown cycle* will repeat until the short-circuit fault is removed.

For long-term reliability, the package power dissipation must not exceed the values in the data sheet POWER DISSIPATION RATINGS for extended periods.

POWER-UP TRANSIENTS

The absolute maximum ratings for Vcc and Vdd specify the limits for these supplies. During initial power-on, these supply voltages may instantaneously drop below the given lower limit. Designers should consider that diodes in the circuitry will begin to turn on if the voltage becomes too negative, and that damage may occur if these diodes dissipate significant power internal to the device. The actual threshold for possible damage is a function of both undervoltage magnitude and undervoltage transient duration. Further, the allowable undervoltage transient conditions depend on factors such as device junction temperature and power supply source impedance.

THERMAL CHARACTERISTICS OF IC PACKAGES

Junction-to-Ambient Thermal Resistance (θ_{JA}) is defined as the difference in junction temperature to ambient temperature divided by the operating power. θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives best case in-use condition and consists of 2 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

Junction-to-case thermal resistance (θ_{JC}) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

Junction-to-board thermal resistance (θ_{JB}) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system.

	JEDEC High-K Model	JEDEC Low-K Model
θ_{JA}	105.7°C/W	199.5°C/W
θ_{JB}	52.3	52.3
θ_{JC}	56.32°C/W	56.32°C/W

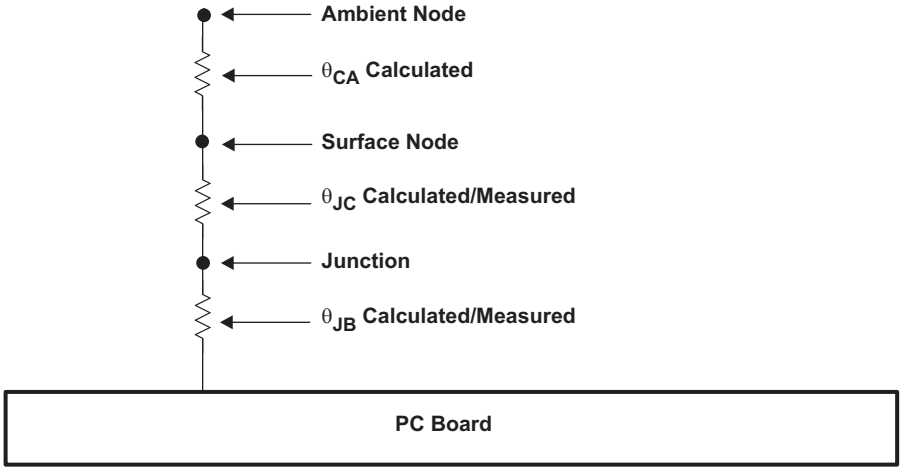


Figure 11. Thermal Resistance

Additional information about thermal metrics for integrated circuits is available in the Texas Instruments Application Note *IC Package Thermal Metrics* (SPRA953).

ControlNet APPLICATION

In a typical ControlNet application, several nodes will be connected to a common bus, as shown in Figure 12. At any time, only one node should actively drive the bus; all active nodes continually receive the bus state. The node which is actively driving the bus will sink current through either the XF1 or XF3 terminal, causing the voltage on the bus to be either differential high or differential low.

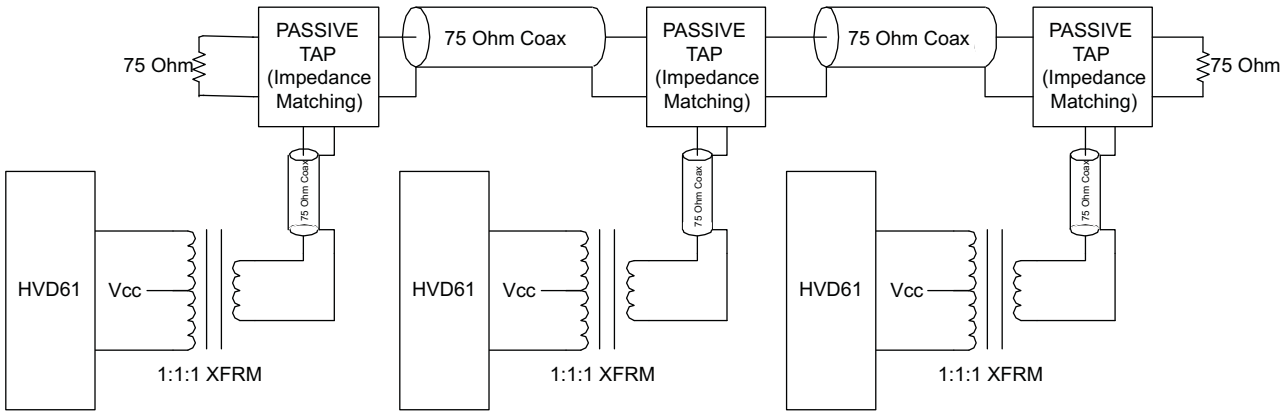


Figure 12. Typical ControlNet Application

SYSTEM-LEVEL EMC PROTECTION

The ControlNet network is intended to operate reliably in harsh industrial environments. At a system level, the network is tested according to several international electromagnetic compatibility (EMC) standards. The requirements are summarized in the Table 2 and Figure 13.

Table 2. EMC Standard Requirements

EMC STANDARD	DESCRIPTION OF TEST METHOD	LEVEL
IEC 61000-4-2	Electro Static Discharge (ESD) Immunity	6 kV Contact 8 kV Air-Gap
IEC 61000-4-3	Radiated Radio Frequency (RF) Immunity	10V/m at 80 MHz to 2.7GHz
IEC 61000-4-4	Fast Transients / Burst Immunity	1 kV
IEC 61000-4-5	Surge Immunity	1 kV
IEC 61000-4-6	Conducted Radio Frequency (RF) Immunity	10V at 150 kHz to 80 MHz 1kHz AM 80% modulation

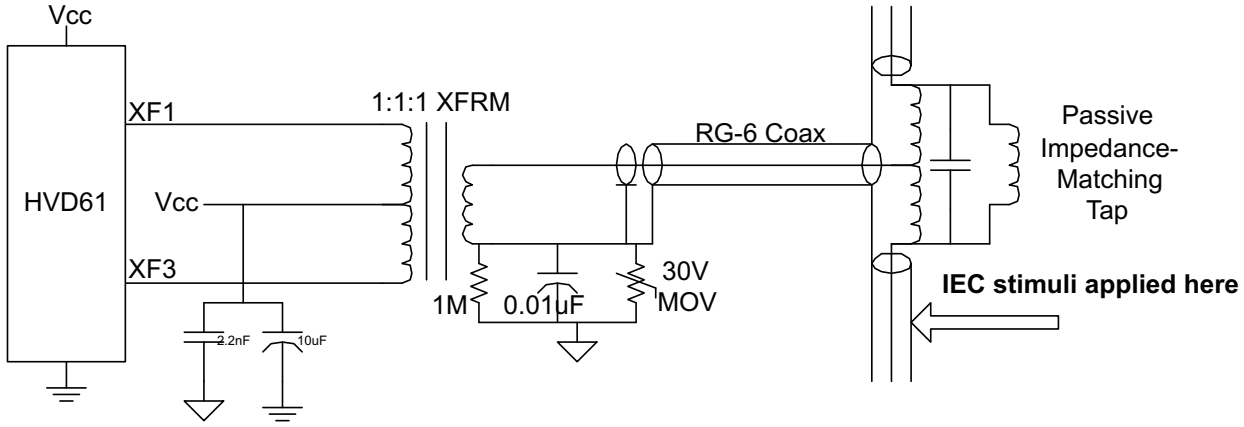


Figure 13. Simplified Test Set-Up for EMC Standards

DRIVER FUNCTIONS

The ControlNet standard requires the transmitter to generate a signal with nominal amplitude of 8.2Vpp into a 37.5 Ω load. This applies to the double-terminated coax bus as shown in Figure 12. Rise and fall times should not exceed 30 nsec, and the signal slew rate should not exceed 1 V/nsec. Transmit signal distortion (ringing, droop, overshoot) should not exceed 10% of the peak-to-peak amplitude.

RECEIVER FUNCTIONS

The function of the primary receiver (RX) and the carrier detect (CD) depends on the signals XF1 and XF3. The purpose of RX is to indicate the status of the two ControlNet bus lines, based on the signals XF1 and XF3. If the voltage at XF3 is greater than the voltage at XF1, then the bus state is positive, and RX should output a HIGH voltage. This corresponds to a Phy_1 symbol. If the voltage at XF3 is less than the voltage at XF1, then the bus state is negative, and RX should output a LOW voltage. This corresponds to a Phy_0 symbol. See Figure 14. Note that the allowable variation in V_{TH-}, V_{TH+}, and V_{CD} is specified in the ELECTRICAL CHARACTERISTICS table.

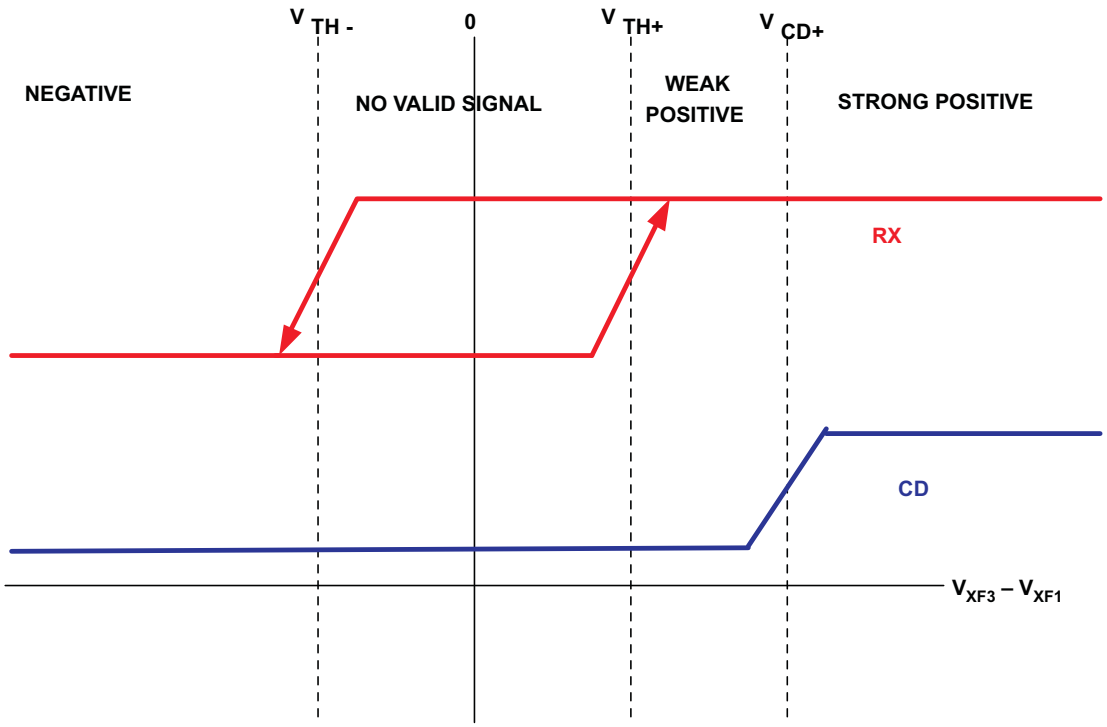


Figure 14. RX and CD Functions

SIGNAL STRENGTH OUTPUT

Vsig should be sampled at the beginning of a transmission in the preamble portion of the ControlNet Frame. This portion is the same for all nodes with the exception of the amplitude. Sampling Vsig in the preamble will provide the most consistent measurement. Further oversampling coupled with multiple frame sampling may provide further cable diagnostics such as identifying reflections due to cable breaks. By sampling multiple times in the preamble of a packet the distance to the break or short may be calculated.

REVISION HISTORY

NOTE: Page numbers of current version may differ from previous versions.

Changes from Revision C (May 2007) to Revision D **Page**

- Changed ControlNet is a trademark of ControlNet International, Ltd to ControlNet is a trademark of ODVA 1
- Changed Vcc MIN from "4.75V" to "4.5V" and changed Vcc MAX from "5.25V" to "5.5V" in the ROC table 3
- Changed V_{DD} spec. MAX voltage from "5.25V" to "5.5V" in the ROC table 3
- Changed Bus pin common-mode voltage MIN spec. from "4.75V to "4.5V" and MAX spec. from "5.25V to "5.5V" in the ROC table 3
- Added second T_A spec and condiitions in the ROC table 3
- Changed V_{TH+} spec. Test Conditions from "4.75V < Vcm < 5.25V" to "4.5V < Vcm < 5.5V" 4
- Changed V_{TH-} spec. Test Conditions from "4.75V < Vcm < 5.25V" to "4.5V < Vcm < 5.5V" 4
- Changed V_{hys} spec. Test Conditions from "4.75V < Vcm < 5.25V" to "4.5V < Vcm < 5.5V" 4
- Changed V_{CD} spec. Test Conditions from "4.75V < Vcm < 5.25V" to "4.5V < Vcm < 5.5V" 4
- Changed $I_{O(off)}$ spec. Test Conditions maximum voltage from "5.25V" to "5.5V" 4
- Added second GAIN spec with conditions of 4.5V ≤ V_{CC} ≤ 5.5V in the ELEC CHARA TABLE, and added 140 mV/V to the MAX column 4
- Changed I_{DD} (chip disabled) spec MAX from "10" to "105" µA 4
- Added "0°C < T < 85°C" to Test Conditions for SR spec. 5
- Deleted minimum spec value (1 ns) for Receivers (RX and CD) "Output rise time, t_r and Output fall time, t_f" 5
- Changed RECEIVERS (RX and CD) t_{PLH} spec and t_{PHL} spec MAX value from "35" tp "40" ns. 5
- Changed $t_{sk(p)}$ spec MAX value from "3.5" to 4.5" for RX test condition 5
- Changed RECEIVER t_{PLZ} spec and t_{PHZ} spec MAX value from "40" to "55" ns. 5

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD61D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 100	65HVD61
SN65HVD61DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 100	65HVD61
SN65HVD61DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 100	65HVD61

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

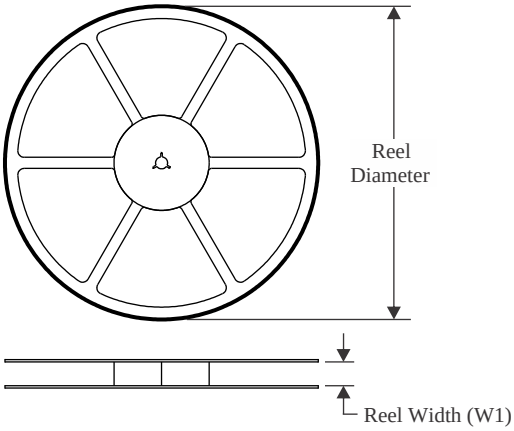
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

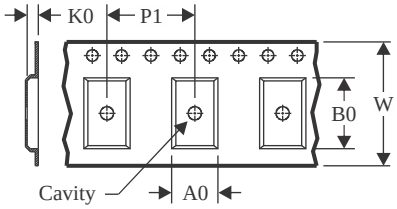
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

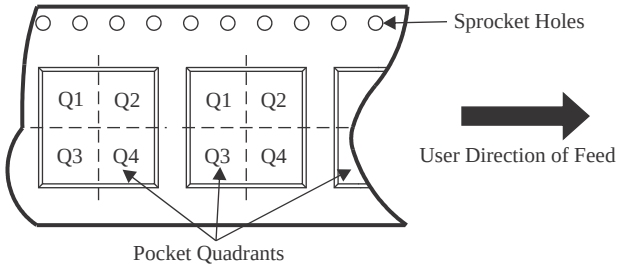


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

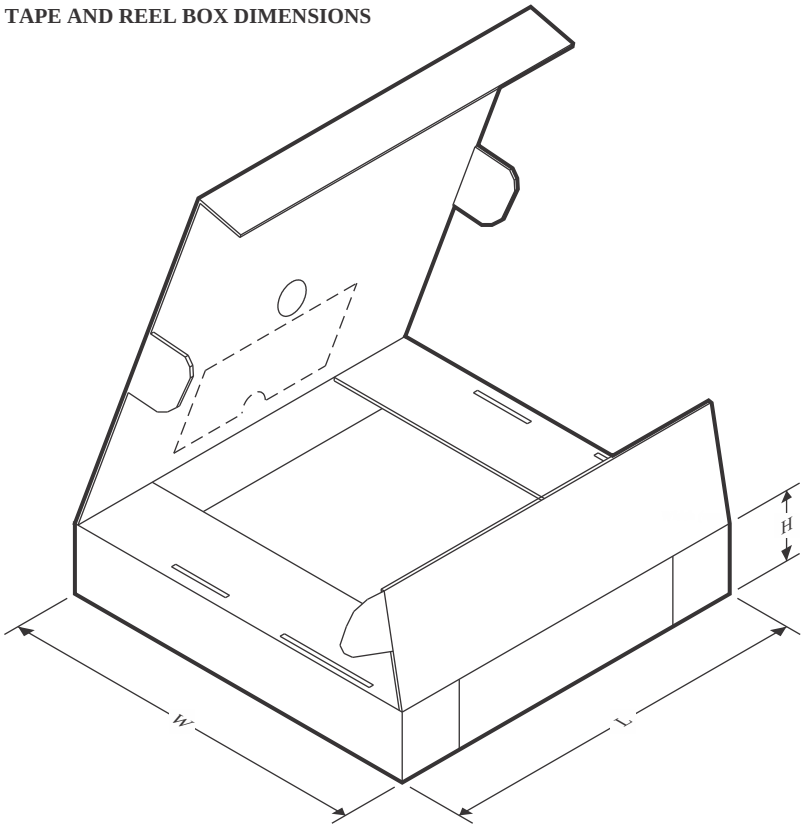
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

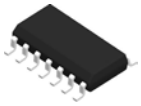
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD61DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD61DR	SOIC	D	14	2500	353.0	353.0	32.0

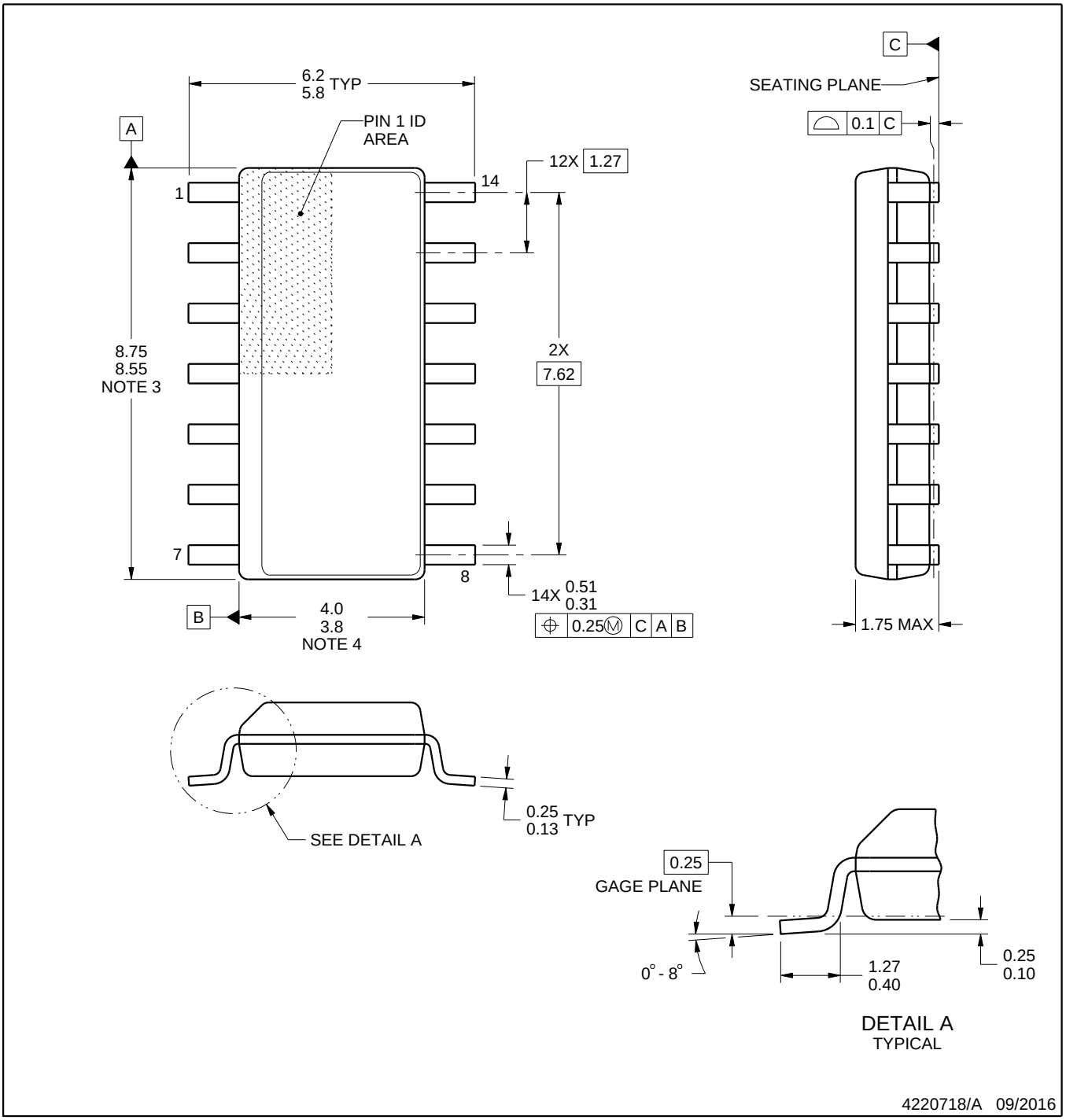


PACKAGE OUTLINE

D0014A

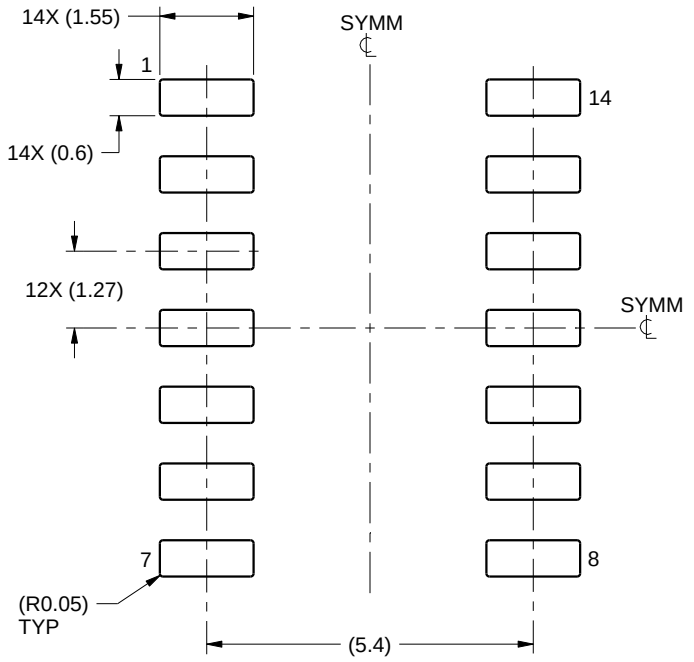
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

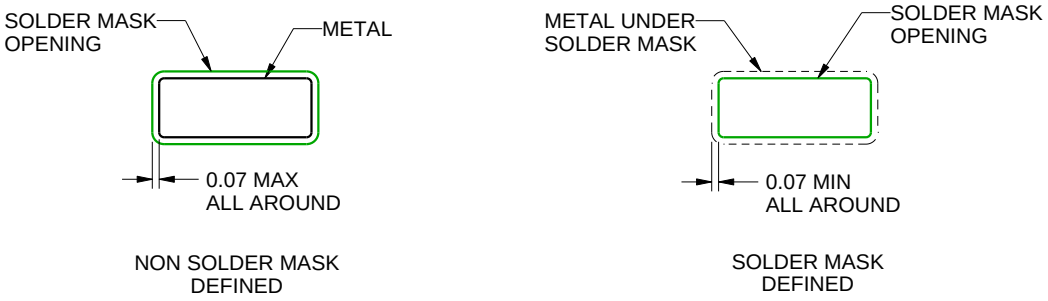


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

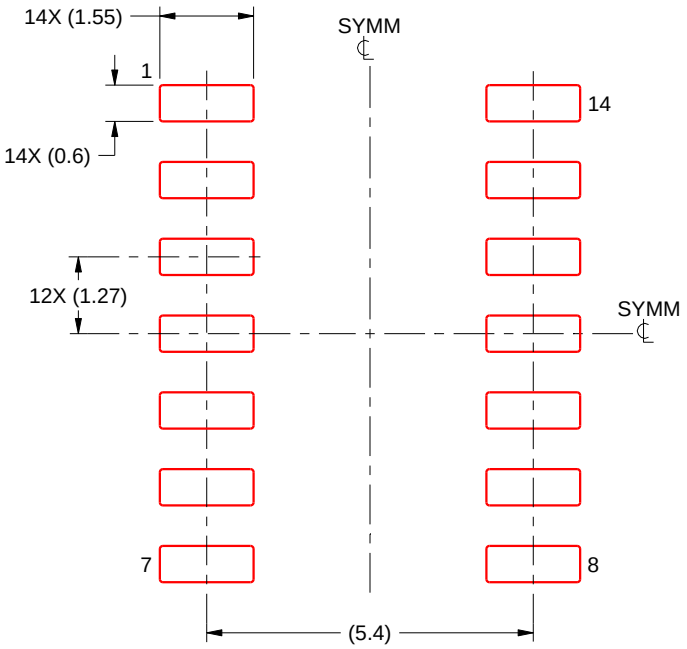
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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