

3.3-V Dual Differential LVPECL/LVDS Buffer to LVTTTL Translator

FEATURES

- Dual 3.3-V Differential LVPECL/LVDS to LVTTTL Buffer Translator
- 24-mA LVTTTL Outputs
- Operating Range
 - PECL $V_{CC} = 3\text{ V to }3.6\text{ V}$ With $GND = 0\text{ V}$
- Support for Clock Frequencies to $>180\text{ MHz}$
- 2-ns Typical Propagation Delay
- Internal Input Pullup and Pulldown Resistors
- Built-in Temperature Compensation
- Drop-In Compatible to MC100LVELT23

APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion for Clock or Data

DESCRIPTION

The SN65LVELT23 is a low-power dual LVPECL/LVDS to LVTTTL translator device. The device includes circuitry to maintain inputs at $V_{CC}/2$ when left open. The SN65LVELT23 is housed in an industry-standard SOIC-8 package and is also available in a TSSOP-8 option.

PINOUT ASSIGNMENT

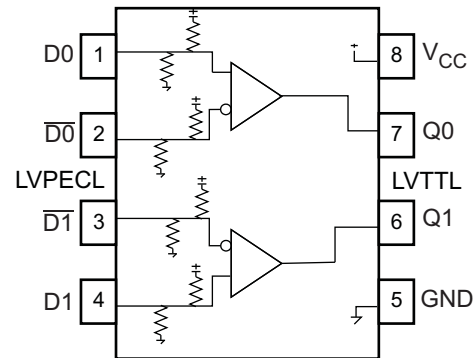


Table 1. PIN DESCRIPTION

PIN	FUNCTION
$D_0, \overline{D}_0, D_1, \overline{D}_1$	PECL inputs
Q_0, Q_1	TTL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION⁽¹⁾

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65LVELT23D	LVEL23	SOIC	NiPdAu
SN65LVELT23DGK	SIMI	MSOP	NiPdAu

(1) Devices with lead (Pb)-bearing terminals not initially available; contact [TI sales representative](#) for further information.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITION	VALUE	UNIT
Absolute supply voltage, V_{CC}		3.8	V
Absolute input voltage, V_I	$GND = 0$ and $V_I \leq V_{CC}$	0 to 3.8	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		-40 to 85	°C
Storage temperature range		-65 to 150	°C

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT-BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT, NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
MSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC	79	°C/W
		MSOP	120	
θ_{JC}	Junction-to-case thermal resistance	SOIC	98	°C/W
		MSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Moisture sensitivity level	Level 1
Flammability rating (oxygen index: 28 to 34)	UL 94 V-0 at 0.125 in. (3.18 mm)
ESD human-body model	2 kV
ESD charged-device model	1.5 kV
Internal pulldown resistor	50 k Ω
Internal pullup resistor	50 k Ω
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

LVTTTL OUTPUT DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3\text{ V}$; $GND = 0\text{ V}$)⁽²⁾

PARAMETER	CONDITION	–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS} Output short-circuit current		–120		–30	–120		–30	–120		–30	mA
V_{OH} Output high voltage ⁽³⁾	$I_{OH} = -3.0\text{ mA}$	2.4			2.4			2.4			V
V_{OL} Output low voltage	$I_{OL} = 24\text{ mA}$			0.5			0.5			0.5	V

- (1) Device meets the specifications after thermal equilibrium has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) All values vary 1:1 with V_{CC} ; V_{CC} can vary $\pm 0.3\text{ V}$
- (3) LVTTTL output $R_L = 500\ \Omega$ to GND

LVPECL INPUT DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3\text{ V}$; $GND = 0.0\text{ V}$)⁽²⁾

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CCH} Power-supply current (outputs set to high)		10	21	25	10	21	25	10	21	25	mA
I_{CCL} Power-supply current (outputs set to low)		15	21	27	15	21	27	15	21	27	mA
V_{IH} Input high voltage ⁽³⁾		2135		2420	2135		2420	2135		2420	mV
V_{IL} Input low voltage ⁽³⁾		1490		1825	1490		1825	1490		1825	mV
V_{IHCMR} Input high-voltage common-mode range (differential) ⁽⁴⁾		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH} Input high current				150			150			150	μA
I_{IL} Input low current		–150			–150			–150			μA

- (1) Device meets the specifications after thermal equilibrium has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input and output parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.3\text{ V}$.
- (3) LVTTTL output $R_L = 500\ \Omega$ to GND
- (4) V_{IHCMR} minimum varies 1:1 with GND, V_{IHCMR} maximum varies 1:1 with V_{CC} .

AC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3\text{ V}$; $GND = 0.0\text{ V}$)⁽²⁾ (3)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX} Maximum switching frequency ⁽⁴⁾		180	300		180	300		180	300		MHz
t_{PLH}/t_{PHL} Propagation delay to output at 1.5 V		1.2	1.6	2.2	1.2	1.7	2.2	1.2	1.8	2.2	ns
t_{SK++} Output-to-output skew++			30	160		30	150		30	150	ps
t_{SK--} Output to output skew--			45	180		45	160		45	135	ps
t_{SKPP} Part- to-part skew ⁽⁵⁾			60	200		60	200		70	200	ps
t_{JITTER} Random clock jitter (RMS)			4	10		4	10		4	10	ps
V_{PP} Input voltage swing ⁽⁶⁾		200	800	1000	200	800	1000	200	800	1000	mV
t_r/t_f Output rise/fall times (0.8 V – 2 V)		330	585	900	330	600	900	330	630	900	ps

- (1) Device meets the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.3\text{ V}$.
- (3) TTL output $R_L = 500\ \Omega$ to GND and $C_L = 20\text{ pF}$ to GND; see [Figure 1](#).
- (4) f_{max} measured for $V_{OL} < 0.5\text{ V}$ and $V_{OH} > 2.4\text{ V}$. See [Figure 5](#).
- (5) Skews are measured between outputs under identical conditions.
- (6) 200-mV input assured full logic swing at the output.

Typical Output Loading Used for Device Evaluation

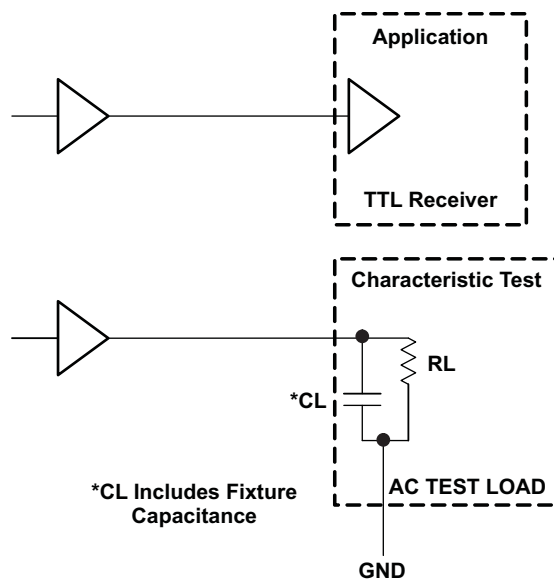


Figure 1. TTL Output Loading Used for Device Evaluation

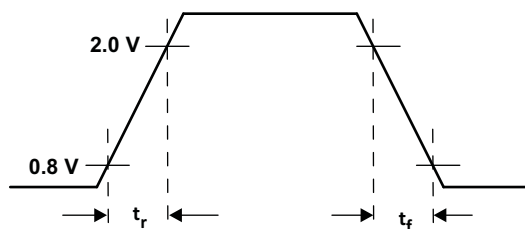


Figure 2. Output Rise and Fall Times

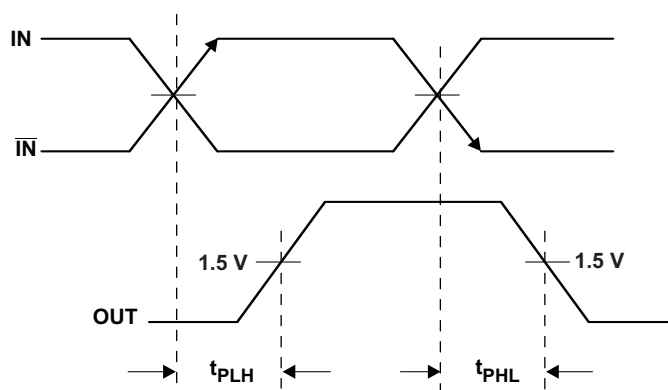


Figure 3. Output Propagation Delay

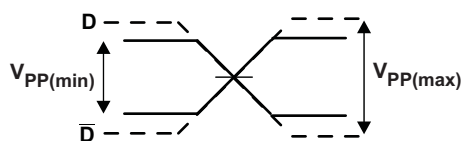


Figure 4. Input Voltage Swing

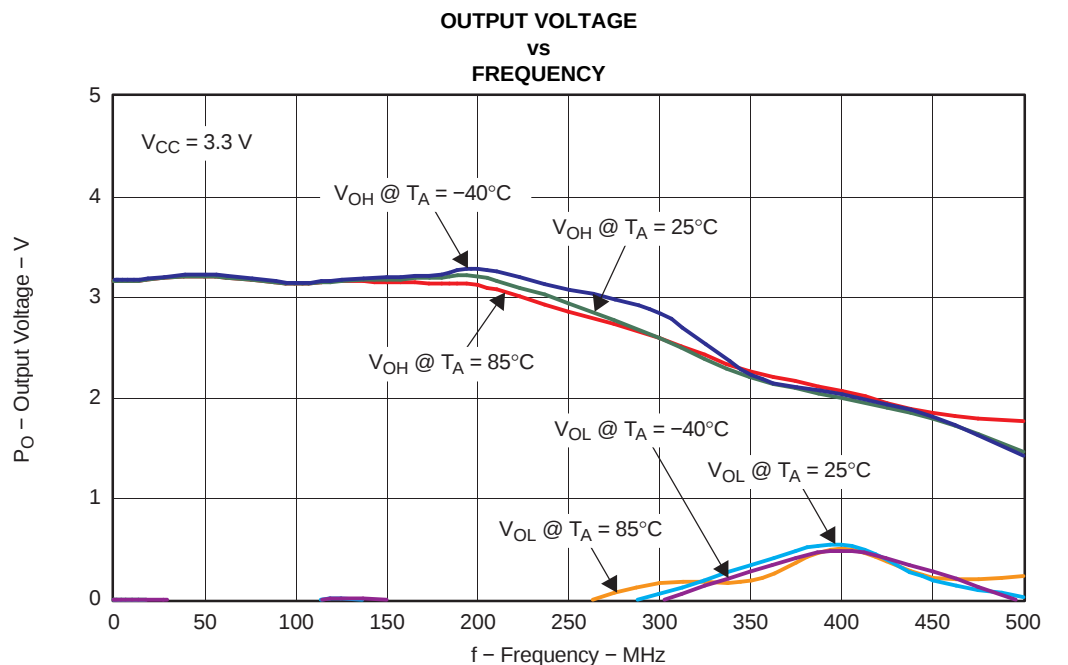


Figure 5.

G001

REVISION HISTORY

Changes from Revision Original (June 2009) to Revision A	Page
Changed MIN and MAX values for t_{PLH}/t_{PHL} in AC CHARACTERISTICS table.....	3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVELT23D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL23
SN65LVELT23D.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL23
SN65LVELT23DGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIMI
SN65LVELT23DGK.B	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIMI
SN65LVELT23DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-1-260C-UNLIM	-40 to 85	SIMI
SN65LVELT23DGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIMI
SN65LVELT23DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL23
SN65LVELT23DR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL23
SN65LVELT23DRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL23
SN65LVELT23DRG4.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL23

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVELT23DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVELT23DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVELT23DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65LVELT23DRG4	SOIC	D	8	2500	353.0	353.0	32.0

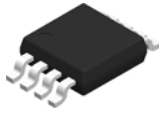
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LVELT23D	D	SOIC	8	75	506.6	8	3940	4.32
SN65LVELT23D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65LVELT23DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65LVELT23DGK.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

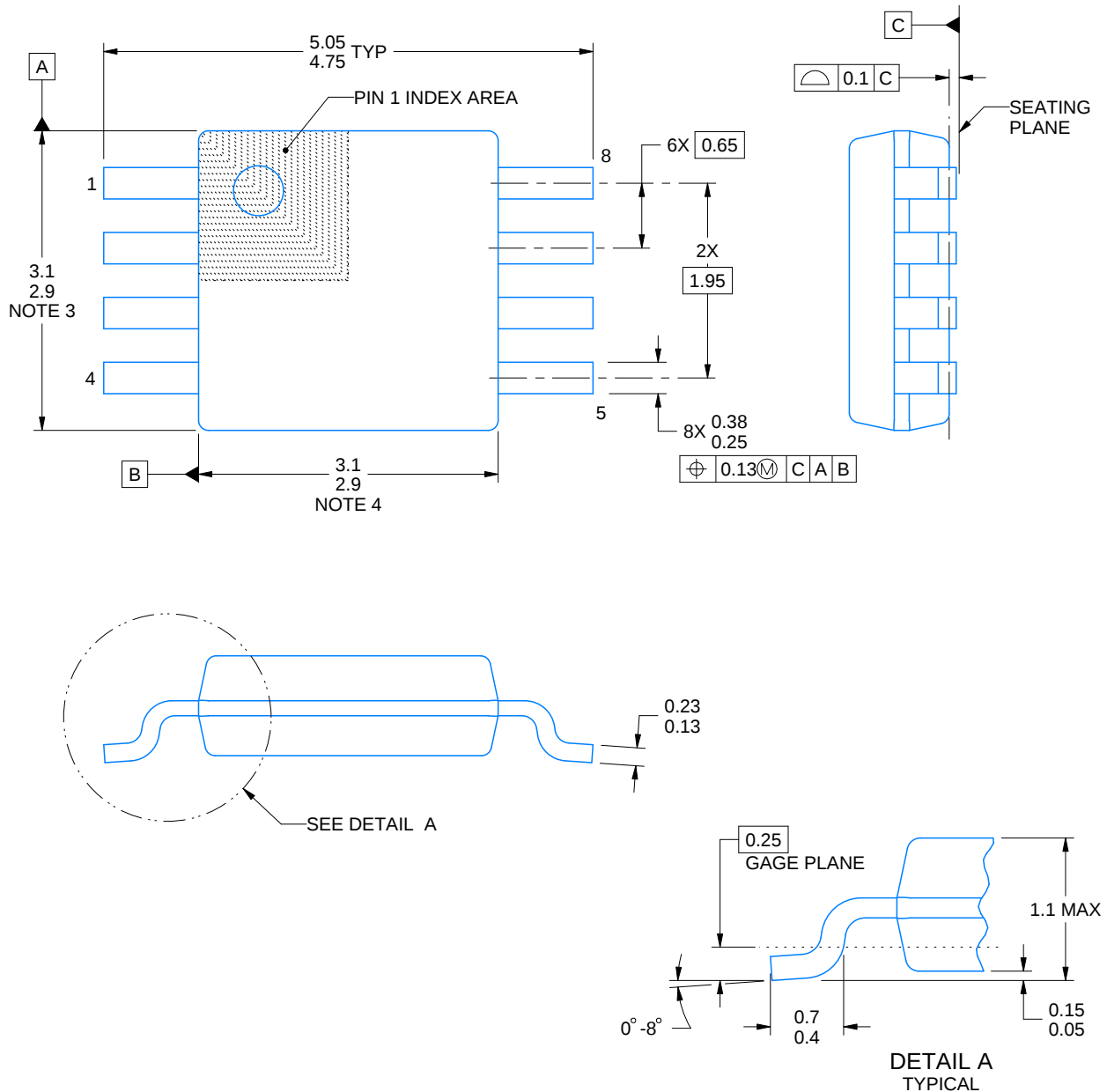
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

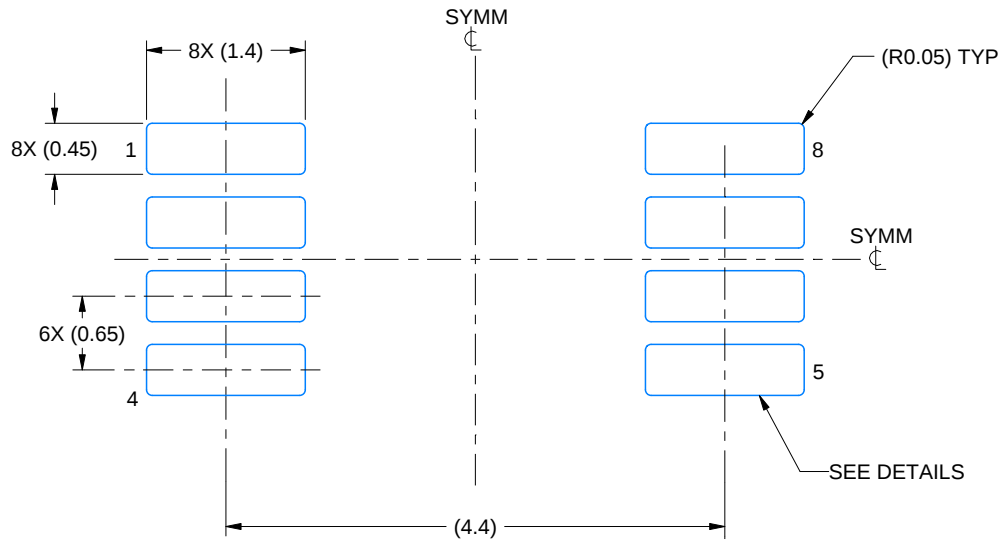
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

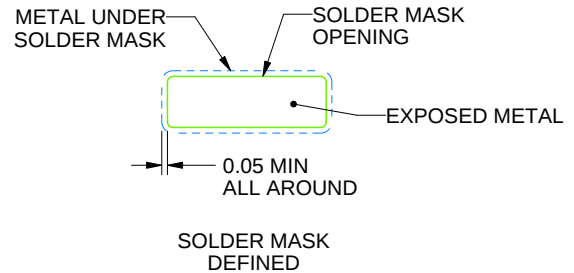
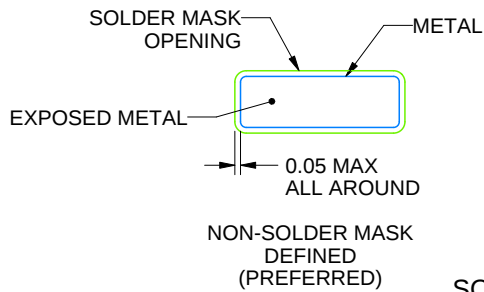
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

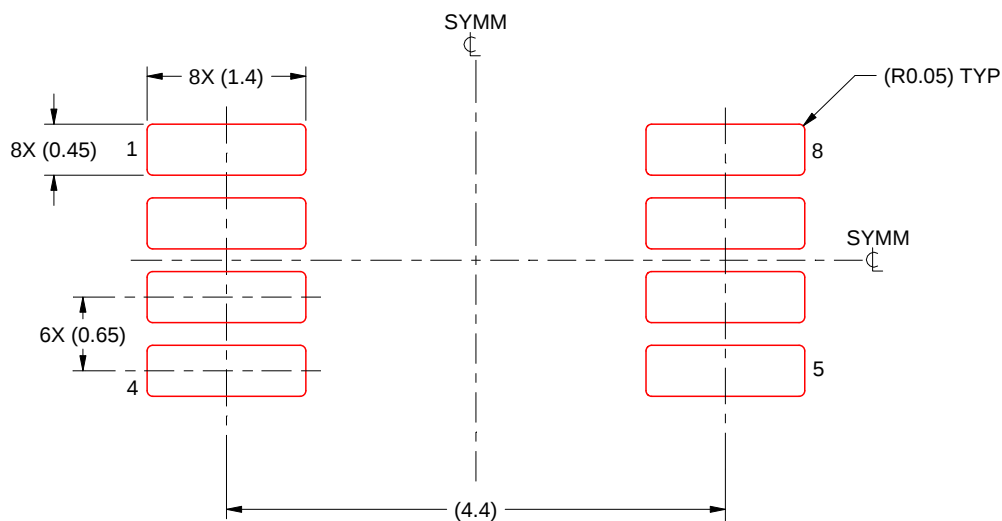
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

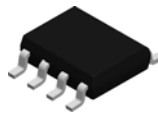


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

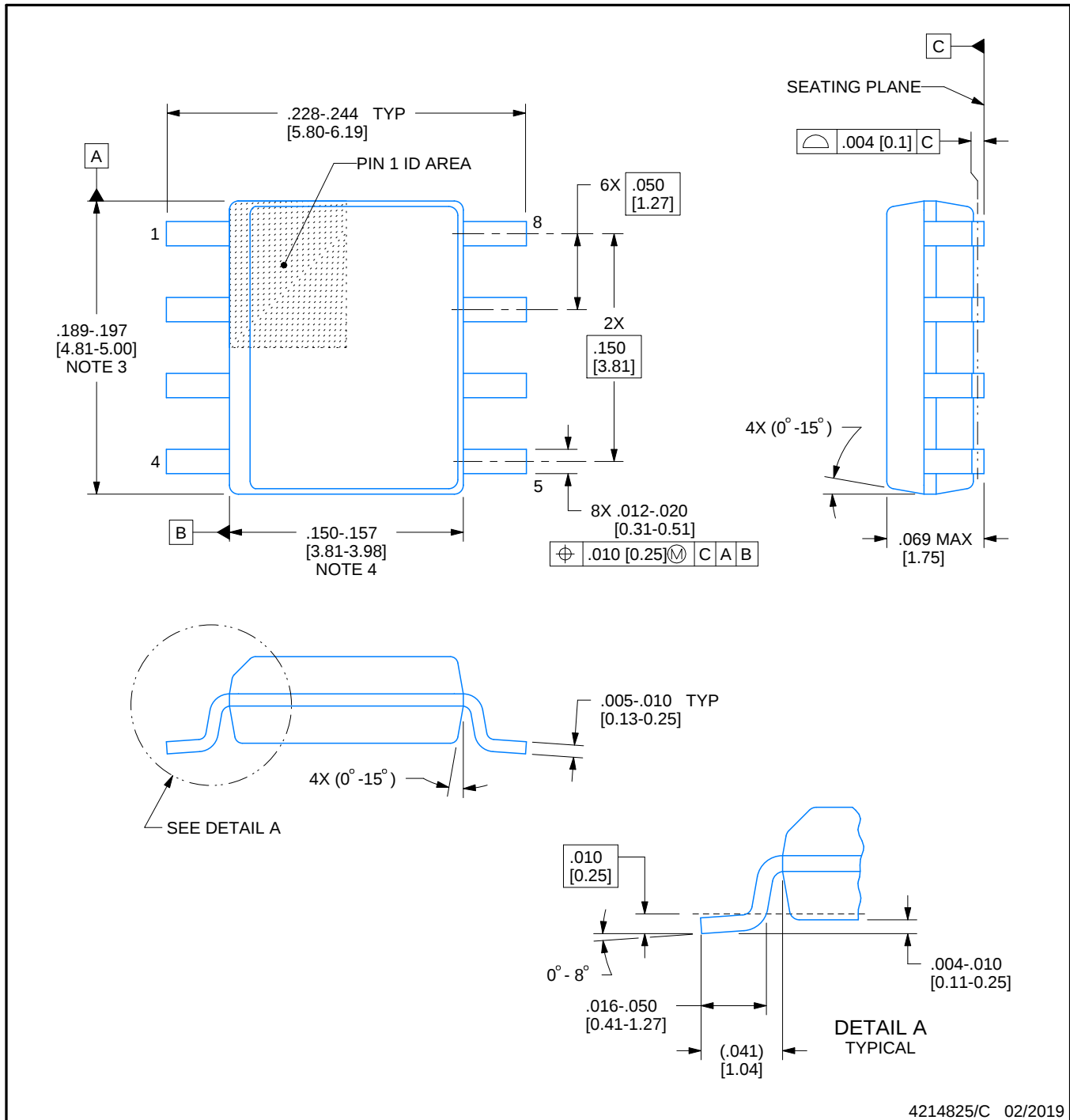


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

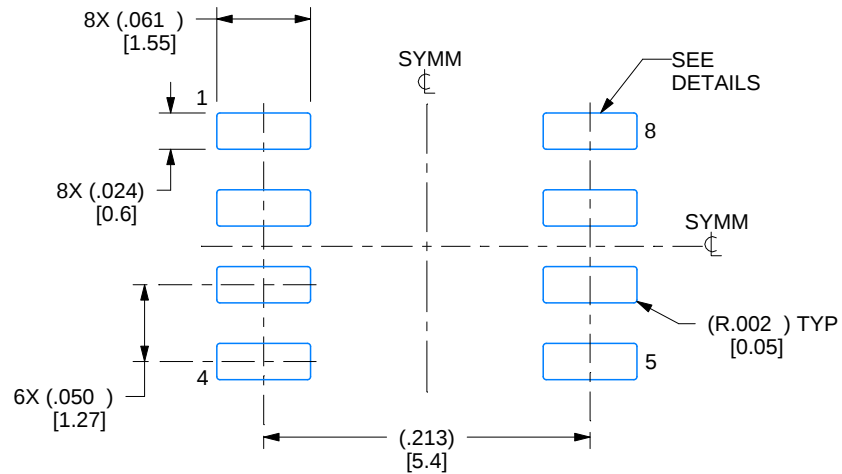
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

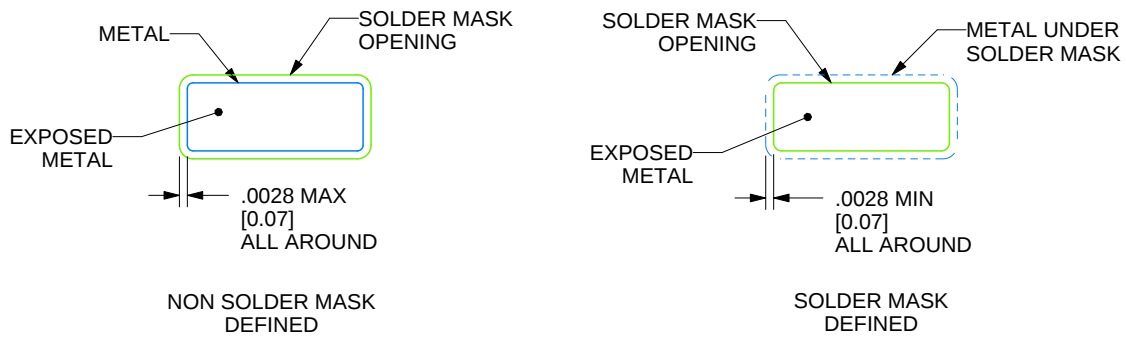
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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