

SN54ABT162827A, SN74ABT162827A 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS248F – JULY 1993 – REVISED JUNE 2004

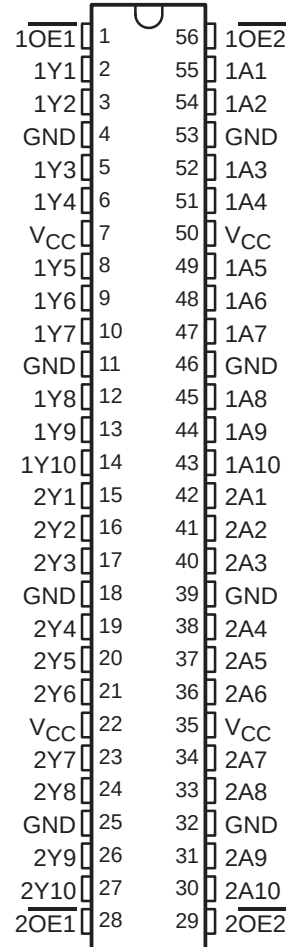
- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- I_{off} and Power-Up 3-State Support Hot Insertion
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

The 'ABT162827A devices are noninverting 20-bit buffers composed of two 10-bit buffers with separate output-enable signals. For either 10-bit buffer, the two output-enable ($1OE1$ and $1OE2$, or $2OE1$ and $2OE2$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

SN54ABT162827A . . . WD PACKAGE
SN74ABT162827A . . . DGG OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74ABT162827ADL	ABT162827A
		Tape and reel	SN74ABT162827ADLR	
	TSSOP – DGG	Tape and reel	SN74ABT162827ADGGR	ABT162827A
-55°C to 125°C	CFP – WD	Tube	SNJ54ABT162827AWD	SNJ54ABT162827AWD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54ABT162827A, SN74ABT162827A
20-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS248F – JULY 1993 – REVISED JUNE 2004

description/ordering information (continued)

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

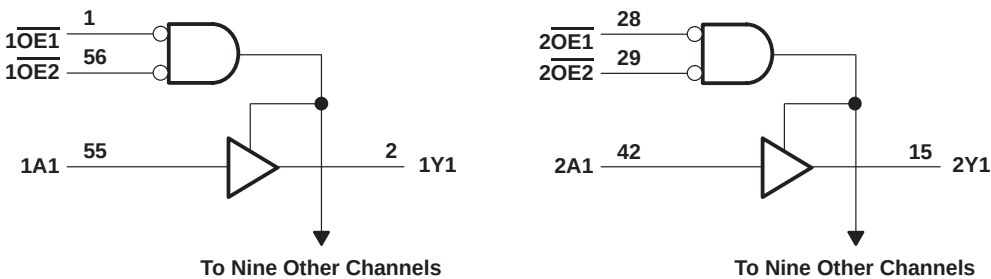
To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

(each 10-bit buffer)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ABT162827A, SN74ABT162827A
20-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS248F – JULY 1993 – REVISED JUNE 2004

recommended operating conditions (see Note 3)

		SN54ABT162827A		SN74ABT162827A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–3		–12	mA
I_{OL}	Low-level output current		8		12	mA
$\Delta t/\Delta V$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT162827A, SN74ABT162827A

20-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS248F – JULY 1993 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT162827A		SN74ABT162827A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2		-1.2		V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = -1 mA		3.35			3.35		3.35		V
		V _{CC} = 5 V, I _{OH} = -1 mA		3.85			3.85		3.85		
		V _{CC} = 4.5 V	I _{OH} = -3 mA	3.1			3.1		3.1		
			I _{OH} = -12 mA	2.6*					2.6		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 8 mA	0.4			0.8		0.65		V
			I _{OL} = 12 mA	0.8*					0.8		
V _{hys}				100							mV
I _I		V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
I _{OZPU}		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X		±50			±50		±50		μA
I _{OZPD}		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X		±50			±50		±50		μA
I _{OZH} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V		10			10		10		μA
I _{OZL} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V		-10			-10		-10		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V		-25	-75	-100	-25	-100	-25	-100	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	2			2		2		mA
			Outputs low	32			32		32		
			Outputs disabled	2			2		2		
ΔI _{CC} ¶	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled	1			1.5		1		mA
			Outputs disabled	0.05			1		0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5			1.5		1.5		
C _i		V _I = 2.5 V or 0.5 V		4							pF
C _O		V _O = 2.5 V or 0.5 V		7							pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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SN54ABT162827A, SN74ABT162827A
20-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS248F – JULY 1993 – REVISED JUNE 2004

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT162827A		SN74ABT162827A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.1	3.6	1	4.1	1	3.9	ns
t_{PHL}			1.1	2.8	4.2	1.1	5	1.1	4.7	
t_{PZH}	$\overline{\text{OE}}$	Y	1.5	3.4	6.3	1.5	7.2	1.5	6.9	ns
t_{PZL}			1.6	3.5	5.3	1.6	6.6	1.6	6.3	
t_{PHZ}	$\overline{\text{OE}}$	Y	2.1	4.1	6.5	2.1	6.8	2.1	6.6	ns
t_{PLZ}			1.5	3.5	5.9	1.5	7.3	1.5	6.3	

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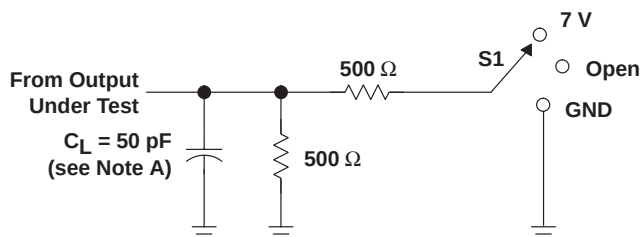
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20-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

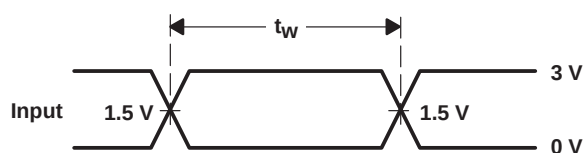
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PARAMETER MEASUREMENT INFORMATION

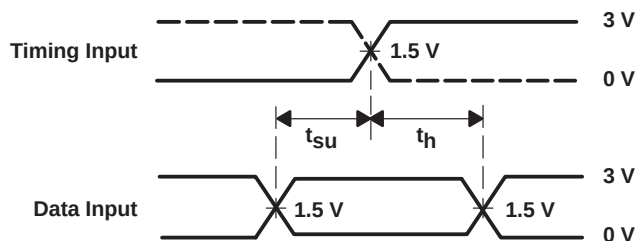


LOAD CIRCUIT

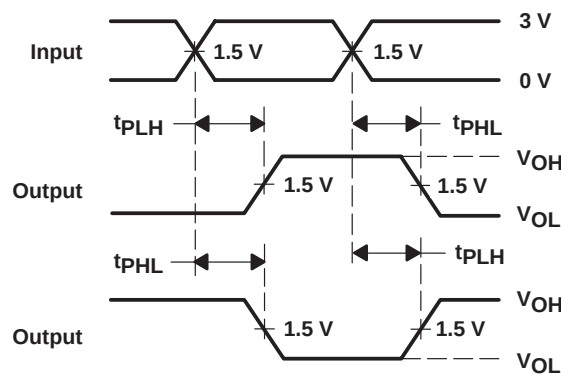
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



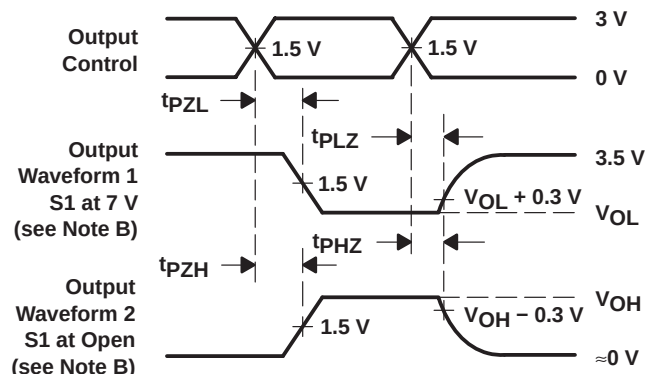
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT162827ADGGR	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A
SN74ABT162827ADGGR.B	Active	Production	TSSOP (DGG) 56	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A
SN74ABT162827ADL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A
SN74ABT162827ADL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A
SN74ABT162827ADLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A
SN74ABT162827ADLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

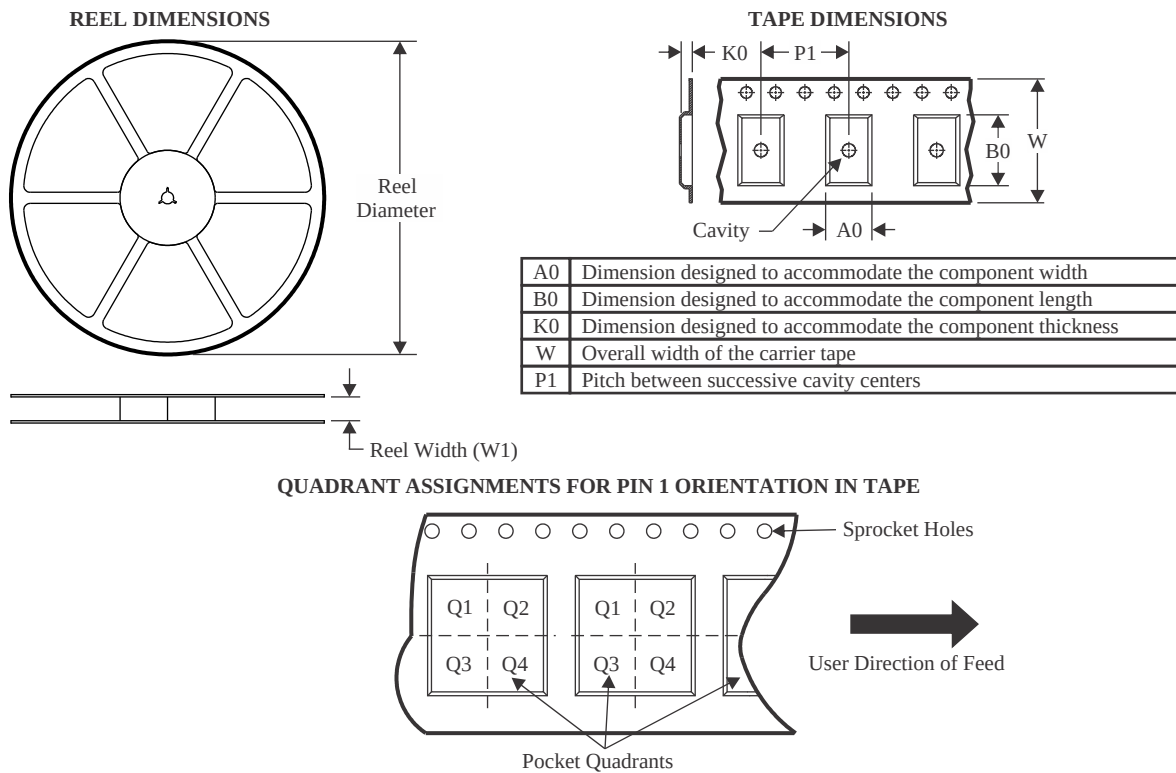
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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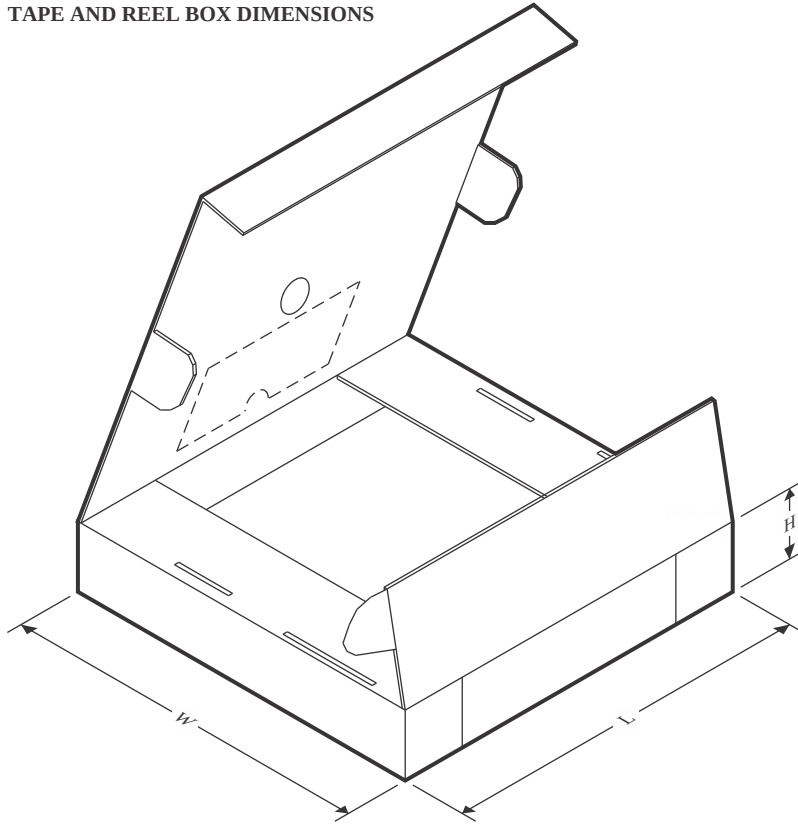
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162827ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT162827ADLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

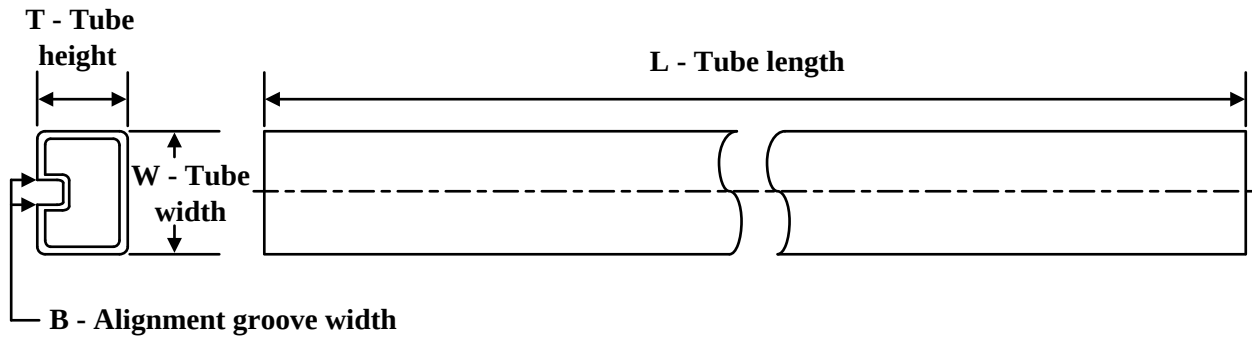
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162827ADGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT162827ADLR	SSOP	DL	56	1000	356.0	356.0	53.0

TUBE

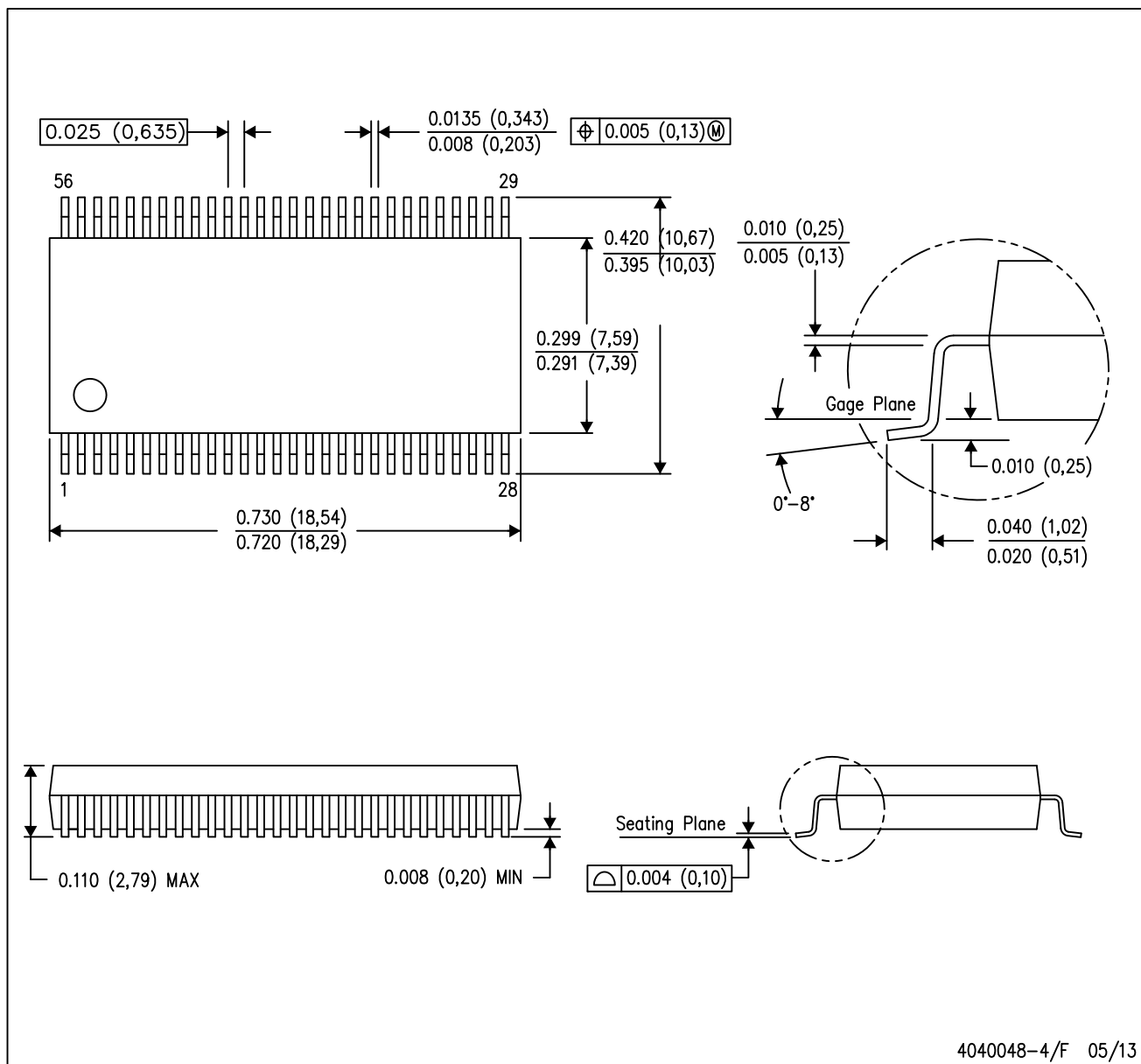


*All dimensions are nominal

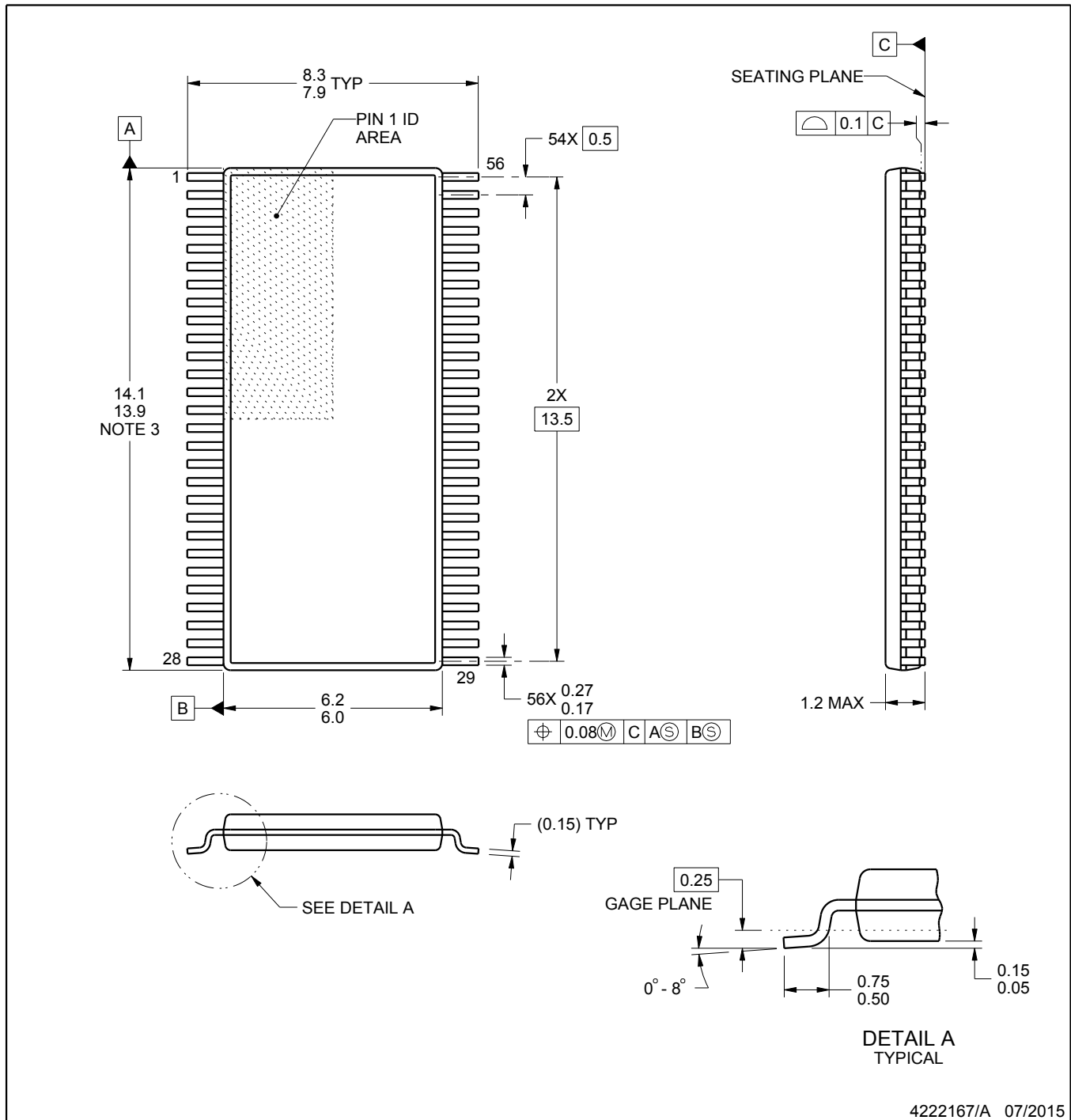
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT162827ADL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT162827ADL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118



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NOTES:

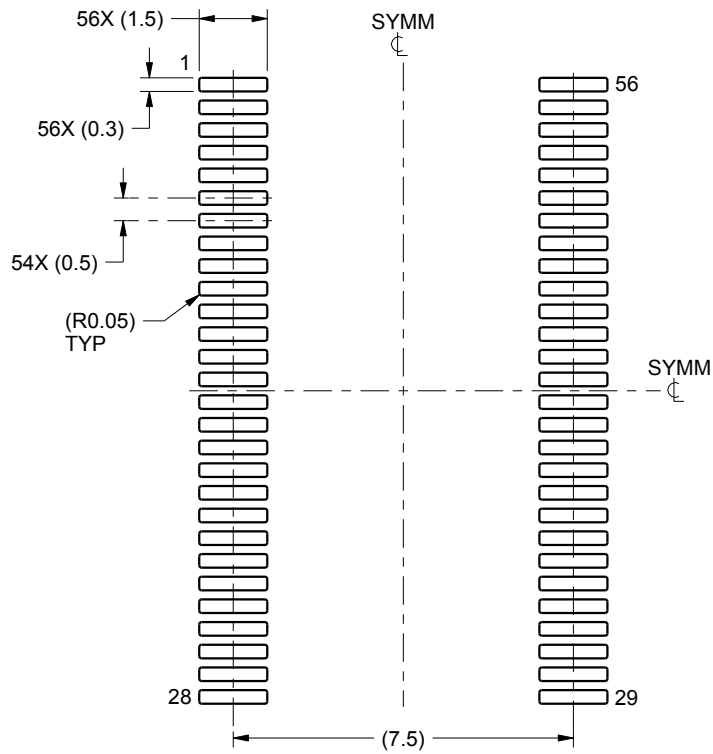
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

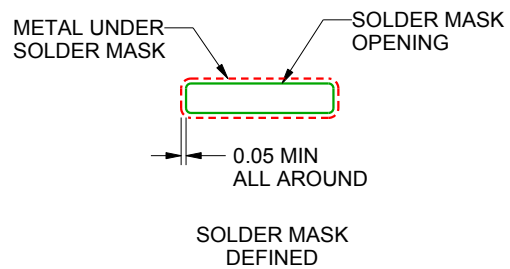
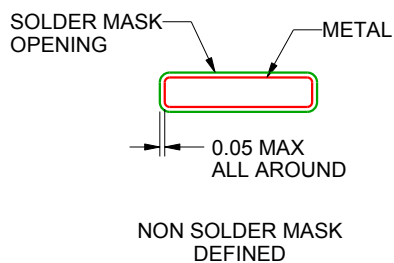
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

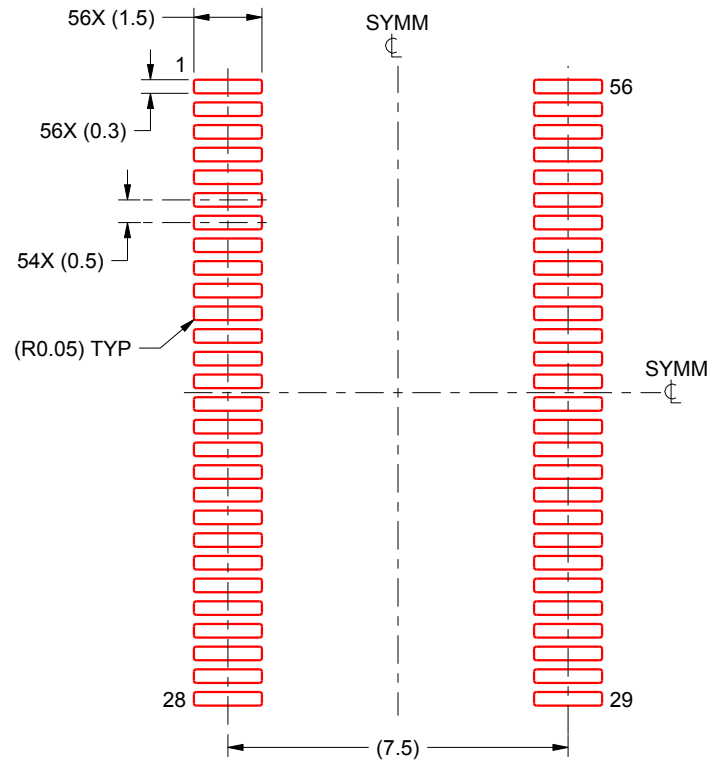
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025