SN74ABT16373A-EP
16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

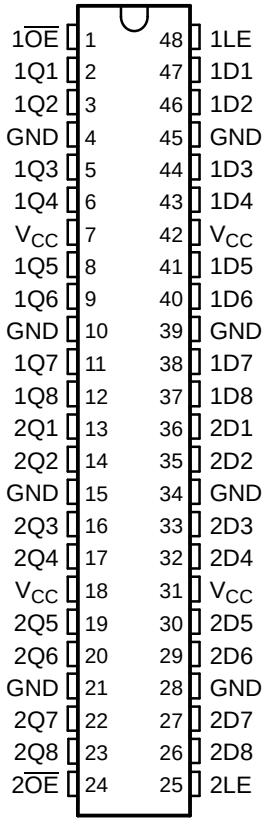
SCBS810 – MARCH 2006

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree** (1)
- **Member of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (–24-mA I_{OH}, 48-mA I_{OL})**
- **Plastic 300-mil Shrink Small-Outline (DL) Package**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold-compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74ABT16373A-EP is a 16-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The SN74ABT16373A-EP is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SSOP – DL	Tape and reel	CABT16373AMDLREP	ABT16373AMEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74ABT16373A-EP can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

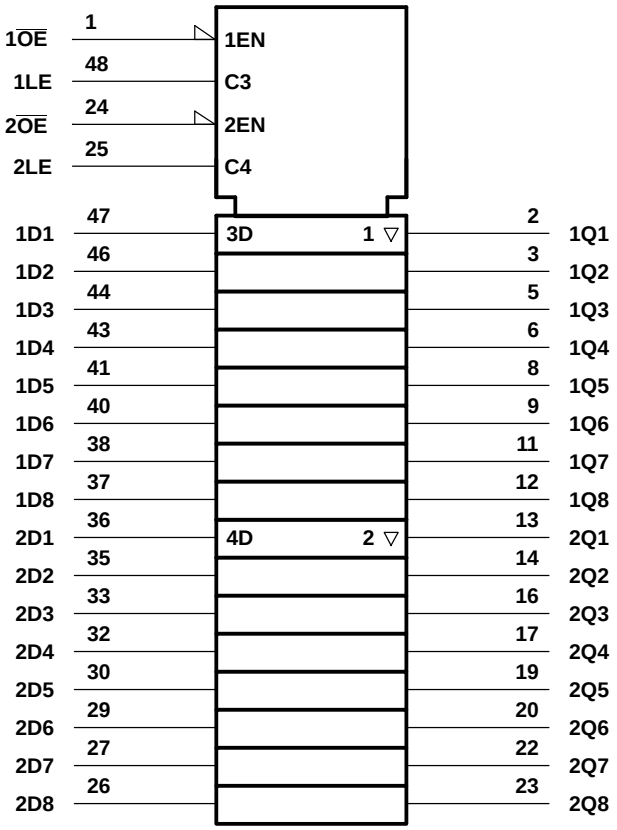
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16373A-EP is characterized for operation from –55°C to 125°C.

FUNCTION TABLE
(each 8-bit section)

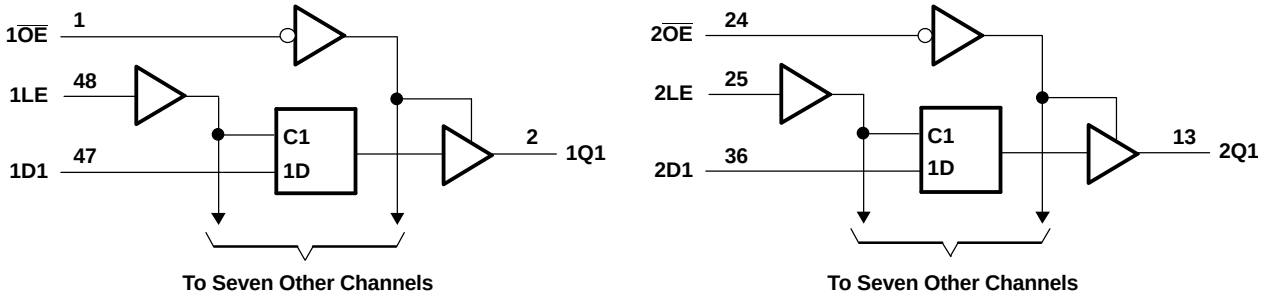
INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

LOGIC SYMBOL[(1)]



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high or power-off state		–0.5	5.5	V
I_O	Current into any output in the low state			96	mA
I_{IK}	Input clamp current	$V_I < 0$		–18	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(3)			94	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD 51.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		μs/V
T_A	Operating free-air temperature		–55	125	°C

(1) Unused inputs must be held high or low to prevent them from floating.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP(1)	MAX			
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		V
		V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		
		V_{CC} = 4.5 V,	I_{OH} = –24 mA		2			2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA				0.55		0.55	V
V_{hys}						100				mV
I_I		V_{CC} = 0 to 5.5 V,	V_I = V_{CC} or GND				±1		±1	µA
I_{OZPU}(2)		V_{CC} = 0 to 2.1 V,	V_O = 0.5 V to 2.7 V,	$\overline{OE}$ = X			±50		±50	µA
I_{OZPD}(2)		V_{CC} = 2.1 V to 0,	V_O = 0.5 V to 2.7 V,	$\overline{OE}$ = X			±50		±50	µA
I_{OZH}		V_{CC} = 2.1 V to 5.5 V,	V_O = 2.7 V,	$\overline{OE}$ ≥ 2 V			10		10	µA
I_{OZL}		V_{CC} = 2.1 V to 5.5 V,	V_O = 0.5 V,	$\overline{OE}$ ≥ 2 V			–10		–10	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100			µA
I_{CEX}	Outputs high	V_{CC} = 5.5 V,	V_O = 5.5 V				50		50	µA
I_O(3)		V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	mA
I_{CC}	Outputs high	V_{CC} = 5.5 V, I_O = 0,	V_I = V_{CC} or GND				2		2	mA
	Outputs low						85		85	
	Outputs disabled						2		2	
ΔI_{CC}(4)		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5	mA
C_i		V_I = 2.5 V or 0.5 V				3.5				pF
C_o		V_O = 2.5 V or 0.5 V				9.5				pF

(1) All typical values are at V_{CC} = 5 V.
(2) This parameter is characterized, but not production tested.
(3) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

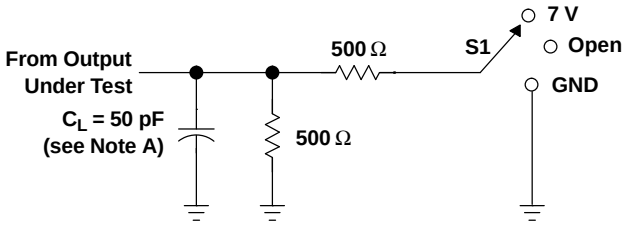
		V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t_w	Pulse duration, LE high	3.3		3.3		ns
t_{su}	Setup time, data before LE↓	1.5		2.4		ns
t_h	Hold time, data after LE↓	1		2.2		ns

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

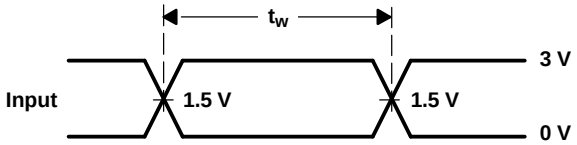
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.4	3.7	5.3	1.4	6.5	ns
t_{PHL}			2	4	5.4	2	6.5	
t_{PLH}	LE	Q	1.7	4.1	5.7	1.7	7	ns
t_{PHL}			2.3	4.3	5.6	2.3	6.3	
t_{PZH}	$\overline{OE}$	Q	1.1	3.4	5	1.1	6.4	ns
t_{PZL}			1.5	3.5	4.9	1.5	5.8	
t_{PHZ}	$\overline{OE}$	Q	2.4	5.1	7.1	2.4	8.3	ns
t_{PLZ}			1.6	4.4	6.3	1.6	8	

PARAMETER MEASUREMENT INFORMATION

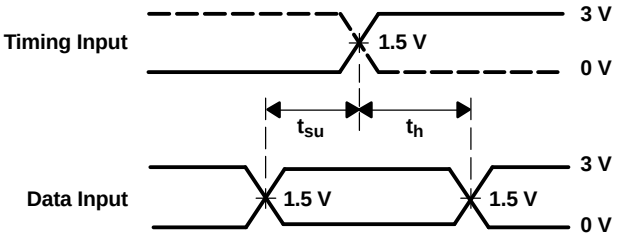


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

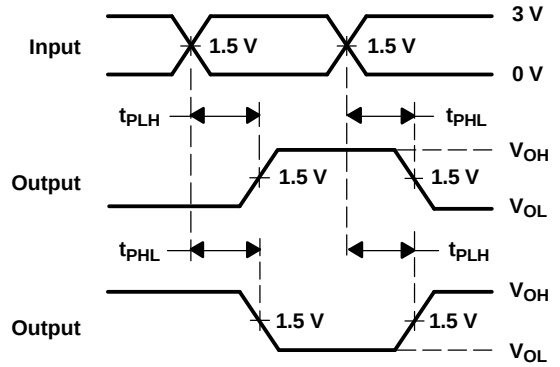
LOAD CIRCUIT



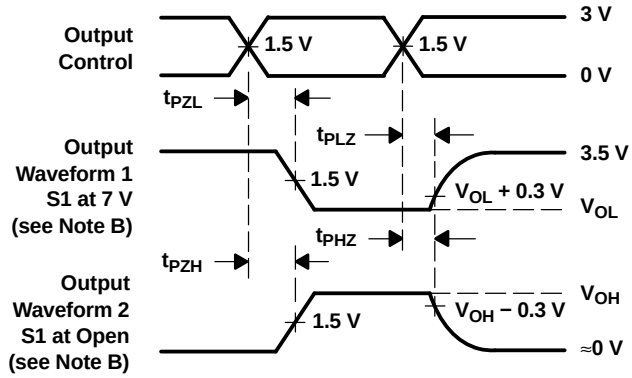
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

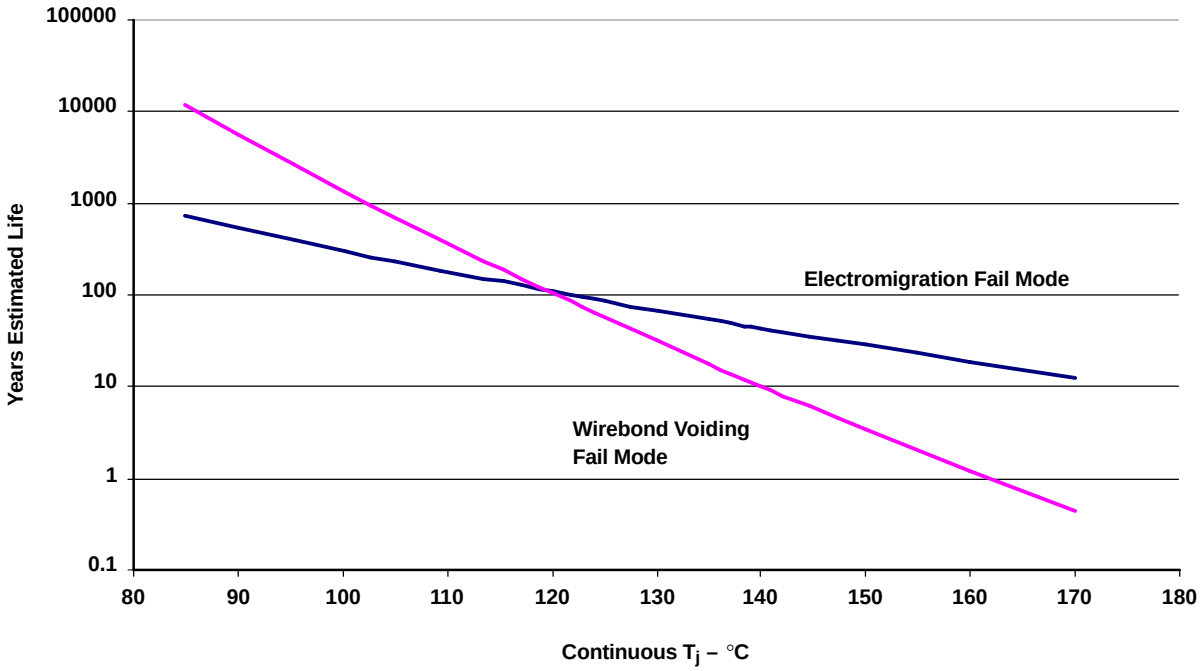


Figure 2. CABT16373AMDLREP Operating Life Derating Chart

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CABT16373AMDLREP	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ABT16373AMEP
V62/06628-01XE	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ABT16373AMEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74ABT16373A-EP :

- Catalog : SN74ABT16373A

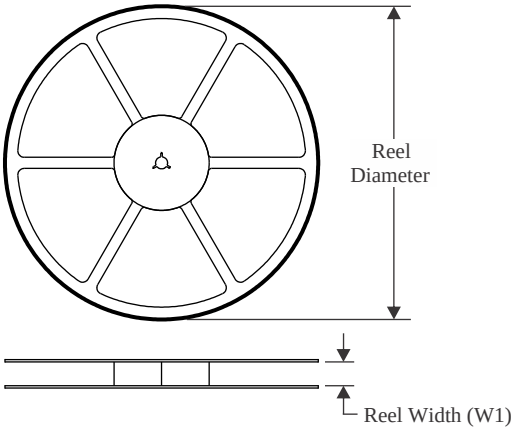
- Military : SN54ABT16373A

NOTE: Qualified Version Definitions:

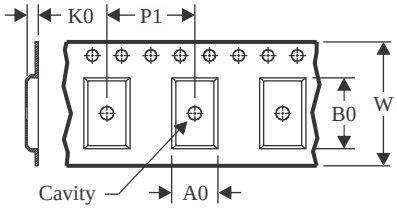
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

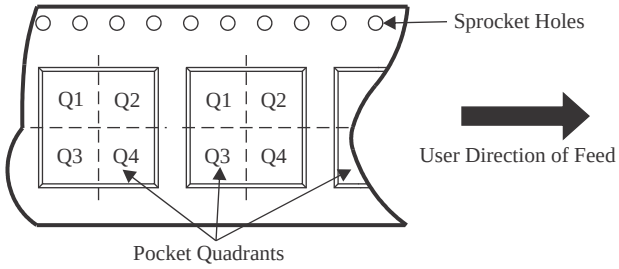


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

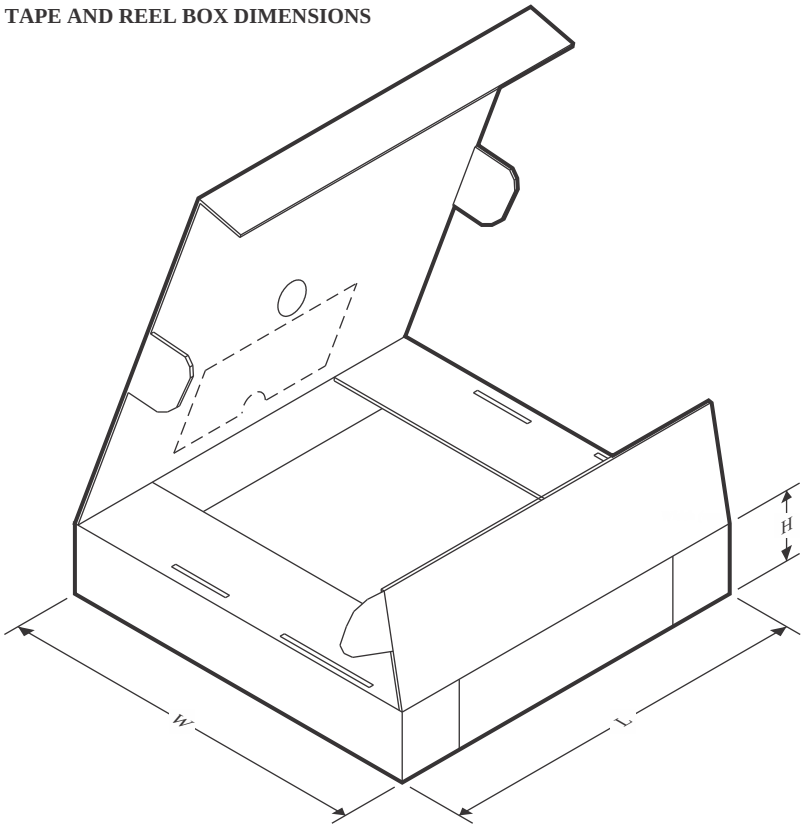
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CABT16373AMDLREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

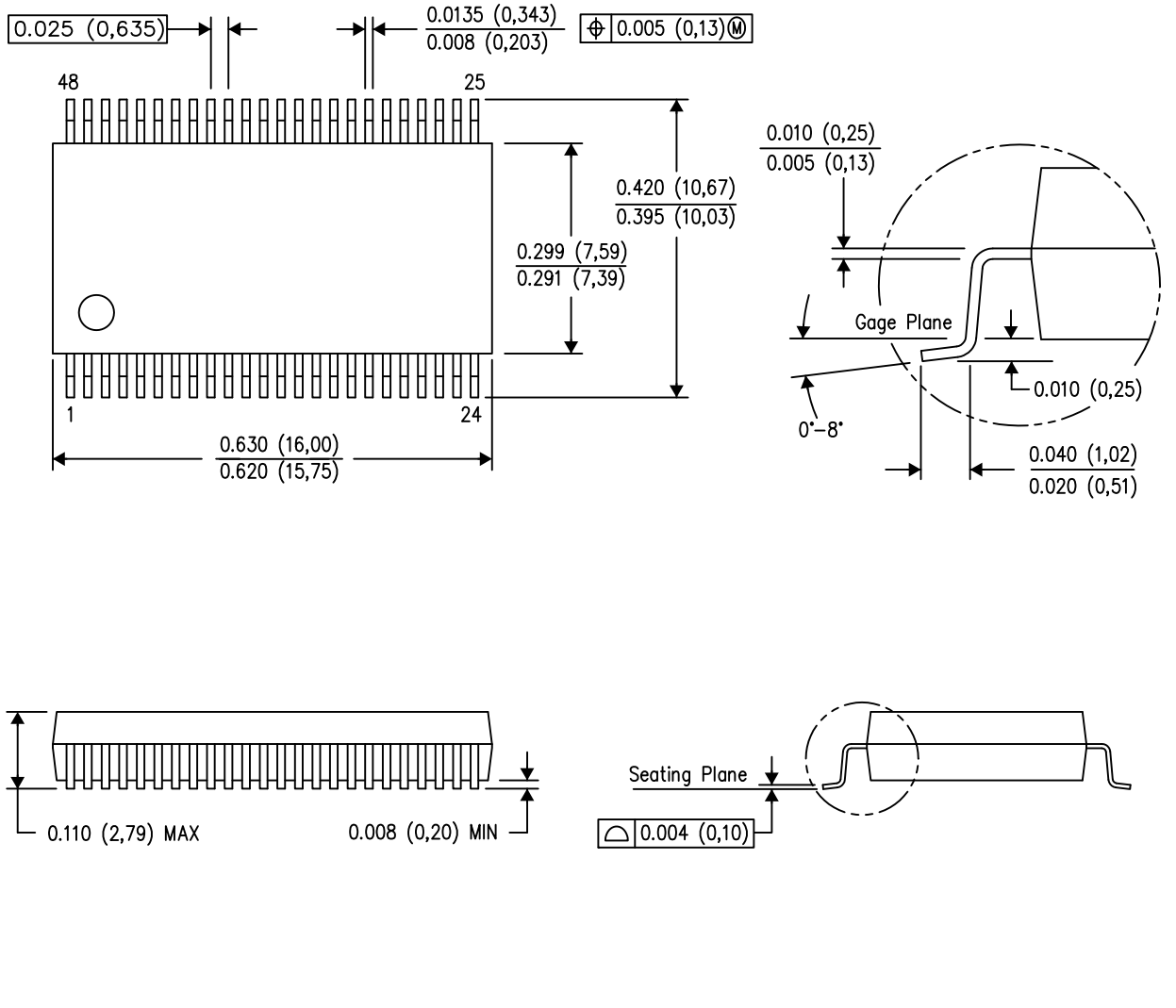
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CABT16373AMDLREP	SSOP	DL	48	1000	356.0	356.0	53.0

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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