

# SN54ABT16823, SN74ABT16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS217C – JUNE 1992 – REVISED JANUARY 1997

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

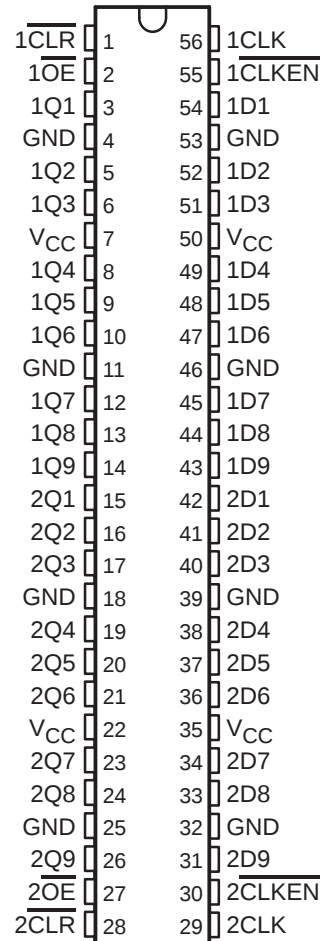
These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ( $\overline{\text{CLKEN}}$ ) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high disables the clock buffer, latching the outputs. Taking the clear ( $\overline{\text{CLR}}$ ) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ( $\overline{\text{OE}}$ ) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{\text{OE}}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54ABT16823 . . . WD PACKAGE  
SN74ABT16823 . . . DGG OR DL PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN54ABT16823, SN74ABT16823

## 18-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### description (continued)

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT16823 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABT16823 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

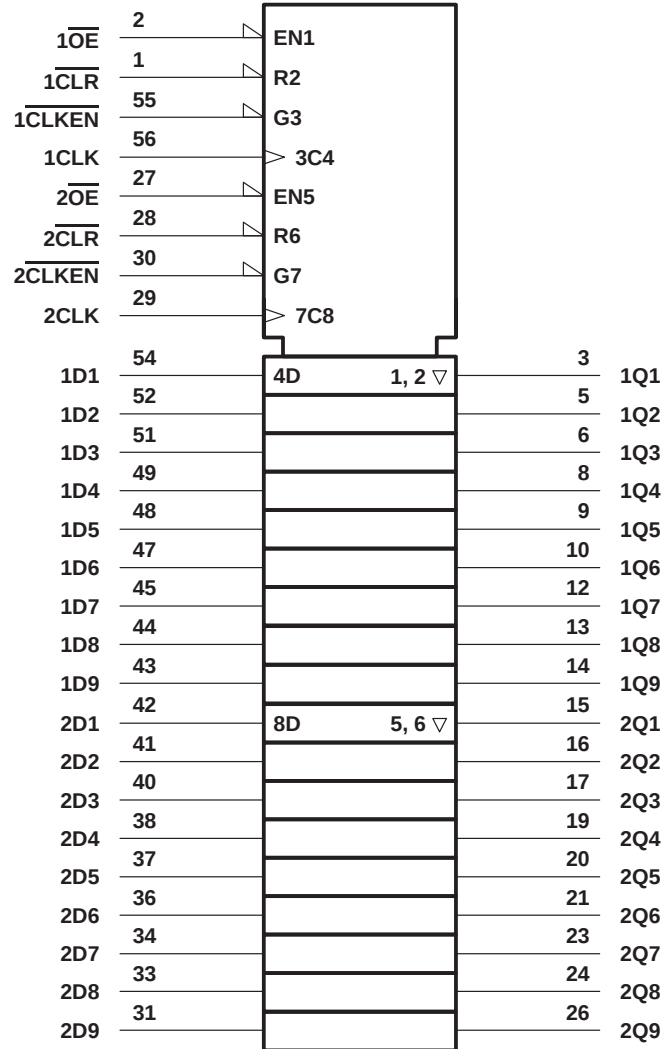
FUNCTION TABLE  
(each 9-bit flip-flop)

| INPUTS          |                  |                    |            |   | OUTPUT<br>Q |
|-----------------|------------------|--------------------|------------|---|-------------|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{CLKEN}$ | CLK        | D |             |
| L               | L                | X                  | X          | X | L           |
| L               | H                | L                  | $\uparrow$ | H | H           |
| L               | H                | L                  | $\uparrow$ | L | L           |
| L               | H                | L                  | L          | X | $Q_0$       |
| L               | H                | H                  | X          | X | $Q_0$       |
| H               | X                | X                  | X          | X | Z           |

SN54ABT16823, SN74ABT16823  
18-BIT BUS-INTERFACE FLIP-FLOPS  
WITH 3-STATE OUTPUTS

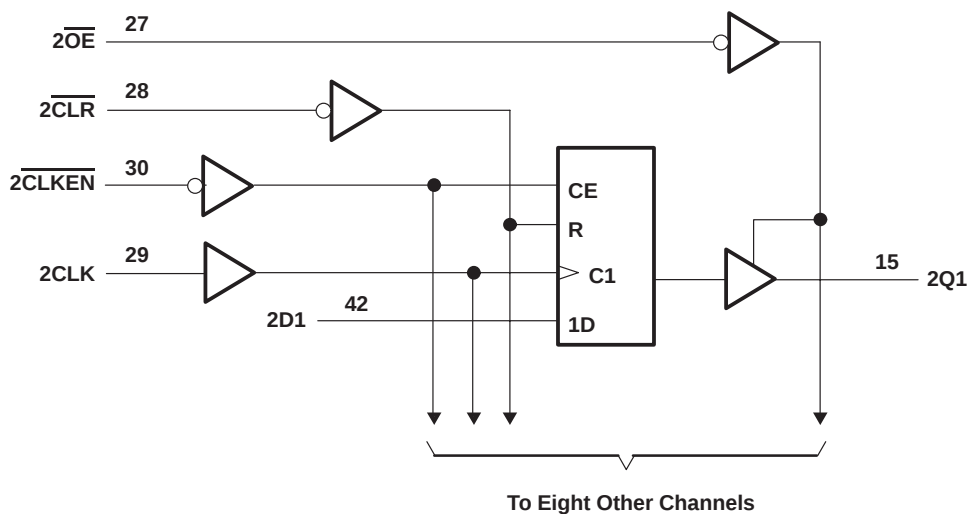
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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[illegible]

# SN54ABT16823, SN74ABT16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                           |                 |
|---------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                            | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT16823            | 96 mA           |
| SN74ABT16823                                                              | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package        | 81°C/W          |
| DL package                                                                | 74°C/W          |
| Storage temperature range, $T_{stg}$                                      | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

|                          |                                    | SN54ABT16823    |          | SN74ABT16823 |          | UNIT |
|--------------------------|------------------------------------|-----------------|----------|--------------|----------|------|
|                          |                                    | MIN             | MAX      | MIN          | MAX      |      |
| $V_{CC}$                 | Supply voltage                     | 4.5             | 5.5      | 4.5          | 5.5      | V    |
| $V_{IH}$                 | High-level input voltage           | 2               |          | 2            |          | V    |
| $V_{IL}$                 | Low-level input voltage            |                 | 0.8      |              | 0.8      | V    |
| $V_I$                    | Input voltage                      | 0               | $V_{CC}$ | 0            | $V_{CC}$ | V    |
| $I_{OH}$                 | High-level output current          |                 | –24      |              | –32      | mA   |
| $I_{OL}$                 | Low-level output current           |                 | 48       |              | 64       | mA   |
| $\Delta t/\Delta v$      | Input transition rise or fall rate | Outputs enabled |          |              | 10       | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate                 | 200             |          | 200          |          | μs/V |
| $T_A$                    | Operating free-air temperature     | –55             | 125      | –40          | 85       | °C   |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                     | TEST CONDITIONS                                                                        | T <sub>A</sub> = 25°C |                  |       | SN54ABT16823 |      | SN74ABT16823 |      | UNIT |
|-------------------------------|----------------------------------------------------------------------------------------|-----------------------|------------------|-------|--------------|------|--------------|------|------|
|                               |                                                                                        | MIN                   | TYP <sup>†</sup> | MAX   | MIN          | MAX  | MIN          | MAX  |      |
| V <sub>IK</sub>               | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA                                       |                       |                  | –1.2  |              | –1.2 |              | –1.2 | V    |
| V <sub>OH</sub>               | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA                                       |                       | 2.5              |       |              | 2.5  |              | 2.5  | V    |
|                               | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –3 mA                                         |                       | 3                |       |              | 3    |              | 3    |      |
|                               | V <sub>CC</sub> = 4.5 V                                                                |                       | 2                |       |              | 2    |              |      |      |
|                               |                                                                                        |                       | 2*               |       |              |      |              | 2    |      |
| V <sub>OL</sub>               | V <sub>CC</sub> = 4.5 V                                                                |                       |                  | 0.55  |              | 0.55 |              |      | V    |
|                               |                                                                                        |                       |                  | 0.55* |              |      |              | 0.55 |      |
| V <sub>hys</sub>              |                                                                                        |                       | 100              |       |              |      |              |      | mV   |
| I <sub>I</sub>                | V <sub>CC</sub> = 0 to 5.5 V,<br>V <sub>I</sub> = V <sub>CC</sub> or GND               |                       |                  | ±1    |              | ±1   |              | ±1   | μA   |
| I <sub>OZPU</sub>             | V <sub>CC</sub> = 0 to 2.1 V,<br>V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$  |                       |                  | ±50   |              | ±50  |              | ±50  | μA   |
| I <sub>OZPD</sub>             | V <sub>CC</sub> = 2.1 V to 0,<br>V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$  |                       |                  | ±50   |              | ±50  |              | ±50  | μA   |
| I <sub>OZH</sub>              | V <sub>CC</sub> = 2.1 V to 5.5 V,<br>V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V  |                       |                  | 10**  |              | 50   |              | 10   | μA   |
| I <sub>OZL</sub>              | V <sub>CC</sub> = 2.1 V to 5.5 V,<br>V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V  |                       |                  | –10** |              | –50  |              | –10  | μA   |
| I <sub>off</sub>              | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                          |                       |                  | ±100  |              |      |              | ±100 | μA   |
| I <sub>CEX</sub>              | Outputs high                                                                           |                       |                  | 50    |              | 50   |              | 50   | μA   |
| I <sub>O</sub> <sup>‡</sup>   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                        | –50                   | –100             | –200  | –50          | –200 | –50          | –200 | mA   |
| I <sub>CC</sub>               | Outputs high                                                                           |                       |                  | 0.5   |              | 0.5  |              | 0.5  | mA   |
|                               | Outputs low                                                                            |                       |                  | 80    |              | 80   |              | 80   |      |
|                               | Outputs disabled                                                                       |                       |                  | 0.5   |              | 0.5  |              | 0.5  |      |
| ΔI <sub>CC</sub> <sup>§</sup> | V <sub>CC</sub> = 5.5 V, One input at 3.4 V,<br>Other inputs at V <sub>CC</sub> or GND |                       |                  | 1.5   |              | 1.5  |              | 1.5  | mA   |
| C <sub>i</sub>                | V <sub>I</sub> = 2.5 V or 0.5 V                                                        |                       | 3.5              |       |              |      |              |      | pF   |
| C <sub>O</sub>                | V <sub>O</sub> = 2.5 V or 0.5 V                                                        |                       | 7.5              |       |              |      |              |      | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

\*\* These limits apply only to the SN74ABT16823.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

|                    |                                  |                                  | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     | SN54ABT16823 |     | SN74ABT16823 |     | UNIT |
|--------------------|----------------------------------|----------------------------------|-----------------------------------------------------|-----|--------------|-----|--------------|-----|------|
|                    |                                  |                                  | MIN                                                 | MAX | MIN          | MAX | MIN          | MAX |      |
| $f_{\text{clock}}$ | Clock frequency                  |                                  | 0                                                   | 150 | 0            | 150 | 0            | 150 | MHz  |
| $t_w$              | Pulse duration                   | $\overline{\text{CLR}}$ low      | 3.3                                                 |     | 3.3          |     | 3.3          |     | ns   |
|                    |                                  | CLK high or low                  | 3.3                                                 |     | 3.3          |     | 3.3          |     |      |
| $t_{\text{su}}$    | Setup time before CLK $\uparrow$ | $\overline{\text{CLR}}$ inactive | 1.6                                                 |     | 2            |     | 1.6          |     | ns   |
|                    |                                  | Data                             | 1.7                                                 |     | 1.7          |     | 1.7          |     |      |
|                    |                                  | CLKEN low                        | 2.8                                                 |     | 2.8          |     | 2.8          |     |      |
| $t_h$              | Hold time after CLK $\uparrow$   | Data                             | 1.2                                                 |     | 1.2          |     | 1.2          |     | ns   |
|                    |                                  | CLKEN low                        | 0.6                                                 |     | 0.6          |     | 0.6          |     |      |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)         | TO<br>(OUTPUT) | SN54ABT16823                                    |     |     |     |     | UNIT |
|------------------|-------------------------|----------------|-------------------------------------------------|-----|-----|-----|-----|------|
|                  |                         |                | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | MIN | MAX |      |
|                  |                         |                | MIN                                             | TYP | MAX |     |     |      |
| f <sub>max</sub> |                         |                | 150                                             |     |     | 150 |     | MHz  |
| t <sub>PLH</sub> | CLK                     | Q              | 1.6                                             | 3.9 | 5.5 | 1.6 | 7.7 | ns   |
| t <sub>PHL</sub> |                         |                | 2.1                                             | 3.9 | 5.4 | 2.1 | 6.4 |      |
| t <sub>PHL</sub> | $\overline{\text{CLR}}$ | Q              | 1.9                                             | 4.1 | 5.3 | 1.9 | 6.3 | ns   |
| t <sub>PZH</sub> | $\overline{\text{OE}}$  | Q              | 1                                               | 3.1 | 4.2 | 1   | 5.1 | ns   |
| t <sub>PZL</sub> |                         |                | 1.5                                             | 3.5 | 4.6 | 1.5 | 5.7 |      |
| t <sub>PHZ</sub> | $\overline{\text{OE}}$  | Q              | 2.2                                             | 4.3 | 6   | 2.2 | 6.8 | ns   |
| t <sub>PLZ</sub> |                         |                | 1.6                                             | 4.3 | 6.4 | 1.6 | 9.9 |      |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM<br>(INPUT)         | TO<br>(OUTPUT) | SN74ABT16823                                    |     |     |     |     | UNIT |
|------------------|-------------------------|----------------|-------------------------------------------------|-----|-----|-----|-----|------|
|                  |                         |                | V <sub>CC</sub> = 5 V,<br>T <sub>A</sub> = 25°C |     |     | MIN | MAX |      |
|                  |                         |                | MIN                                             | TYP | MAX |     |     |      |
| f <sub>max</sub> |                         |                | 150                                             |     |     | 150 |     | MHz  |
| t <sub>PLH</sub> | CLK                     | Q              | 1.6                                             | 3.9 | 5.5 | 1.6 | 6.8 | ns   |
| t <sub>PHL</sub> |                         |                | 2.1                                             | 3.9 | 5.4 | 2.1 | 6   |      |
| t <sub>PHL</sub> | $\overline{\text{CLR}}$ | Q              | 1.9                                             | 4.1 | 5.3 | 1.9 | 6.1 | ns   |
| t <sub>PZH</sub> | $\overline{\text{OE}}$  | Q              | 1                                               | 3.1 | 4.2 | 1   | 4.9 | ns   |
| t <sub>PZL</sub> |                         |                | 1.5                                             | 3.5 | 4.6 | 1.5 | 5.5 |      |
| t <sub>PHZ</sub> | $\overline{\text{OE}}$  | Q              | 2.2                                             | 4.3 | 5.6 | 2.2 | 6.1 | ns   |
| t <sub>PLZ</sub> |                         |                | 1.6                                             | 4.3 | 6.4 | 1.6 | 8.7 |      |

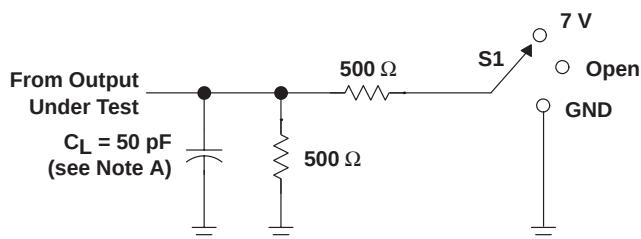
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## 18-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

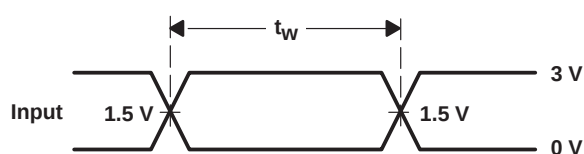
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#### PARAMETER MEASUREMENT INFORMATION

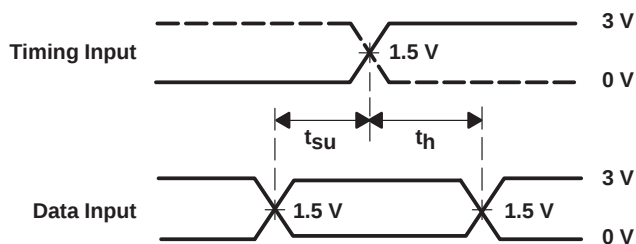


LOAD CIRCUIT

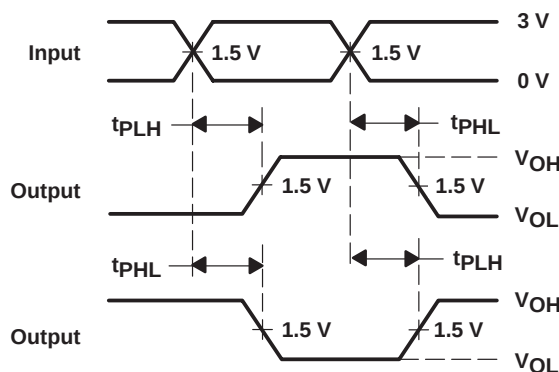
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



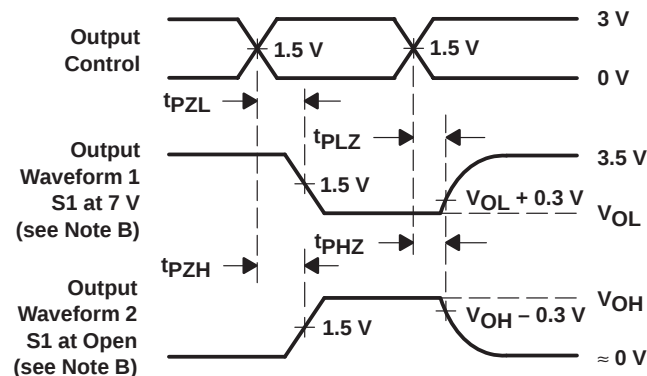
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74ABT16823DGGR</a> | Active        | Production           | TSSOP (DGG)   56 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT16823            |
| SN74ABT16823DGGR.B               | Active        | Production           | TSSOP (DGG)   56 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT16823            |
| SN74ABT16823DGGRG4               | Active        | Production           | TSSOP (DGG)   56 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT16823            |
| SN74ABT16823DGGRG4.B             | Active        | Production           | TSSOP (DGG)   56 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT16823            |
| <a href="#">SN74ABT16823DGVR</a> | Active        | Production           | TVSOP (DGV)   56 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AH823               |
| SN74ABT16823DGVR.B               | Active        | Production           | TVSOP (DGV)   56 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AH823               |
| <a href="#">SN74ABT16823DL</a>   | Active        | Production           | SSOP (DL)   56   | 20   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT16823            |
| SN74ABT16823DL.B                 | Active        | Production           | SSOP (DL)   56   | 20   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT16823            |
| <a href="#">SN74ABT16823DLR</a>  | Active        | Production           | SSOP (DL)   56   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT16823            |
| SN74ABT16823DLR.B                | Active        | Production           | SSOP (DL)   56   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT16823            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT16823DGGR   | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.9     | 14.7    | 1.4     | 12.0    | 24.0   | Q1            |
| SN74ABT16823DGGRG4 | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.9     | 14.7    | 1.4     | 12.0    | 24.0   | Q1            |
| SN74ABT16823DGVR   | TVSOP        | DGV             | 56   | 2000 | 330.0              | 24.4               | 6.8     | 11.7    | 1.6     | 12.0    | 24.0   | Q1            |
| SN74ABT16823DLR    | SSOP         | DL              | 56   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT16823DGGR   | TSSOP        | DGG             | 56   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ABT16823DGGRG4 | TSSOP        | DGG             | 56   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ABT16823DGVR   | TVSOP        | DGV             | 56   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ABT16823DLR    | SSOP         | DL              | 56   | 1000 | 356.0       | 356.0      | 53.0        |

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

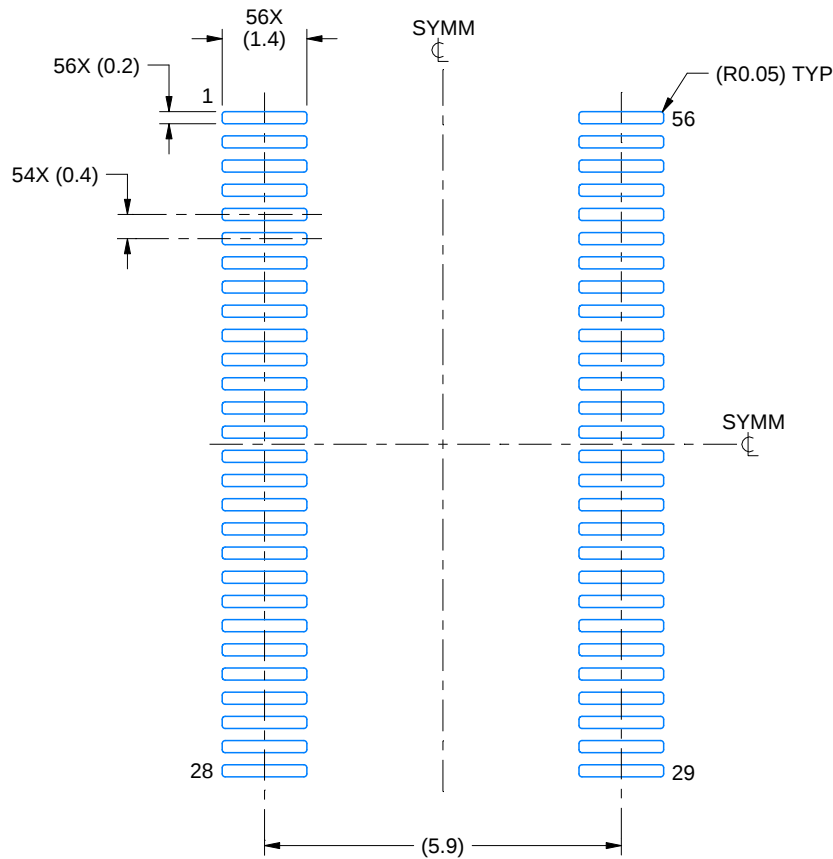


# EXAMPLE BOARD LAYOUT

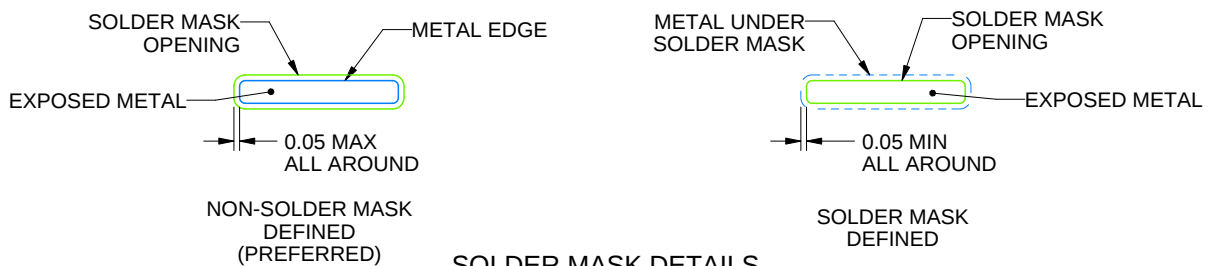
DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 8X



SOLDER MASK DETAILS

4220240/B 12/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

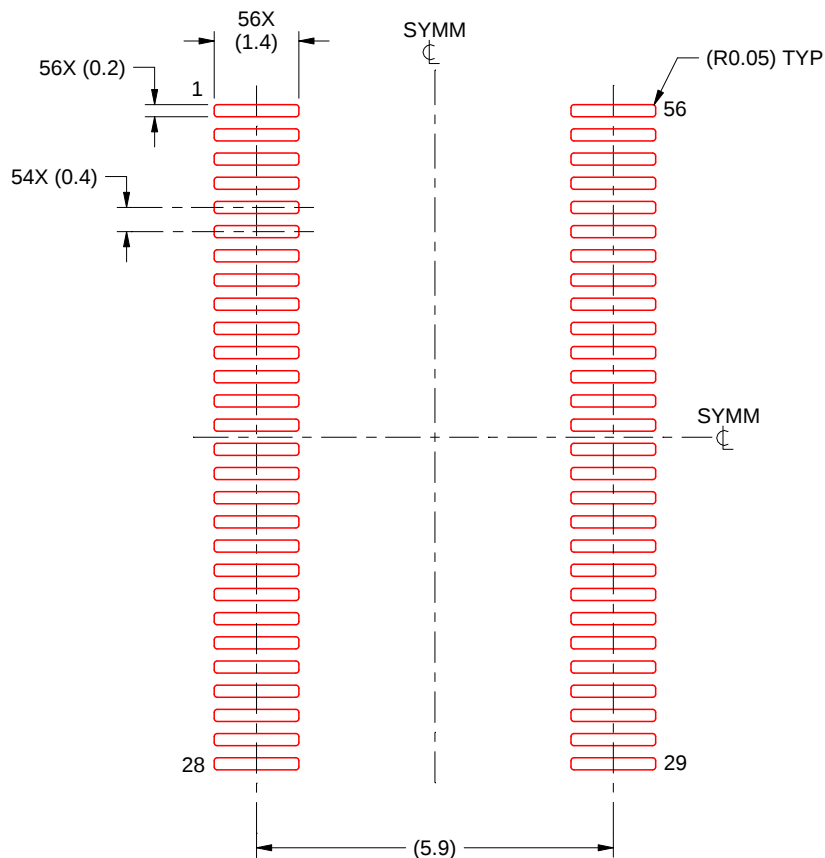
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 8X

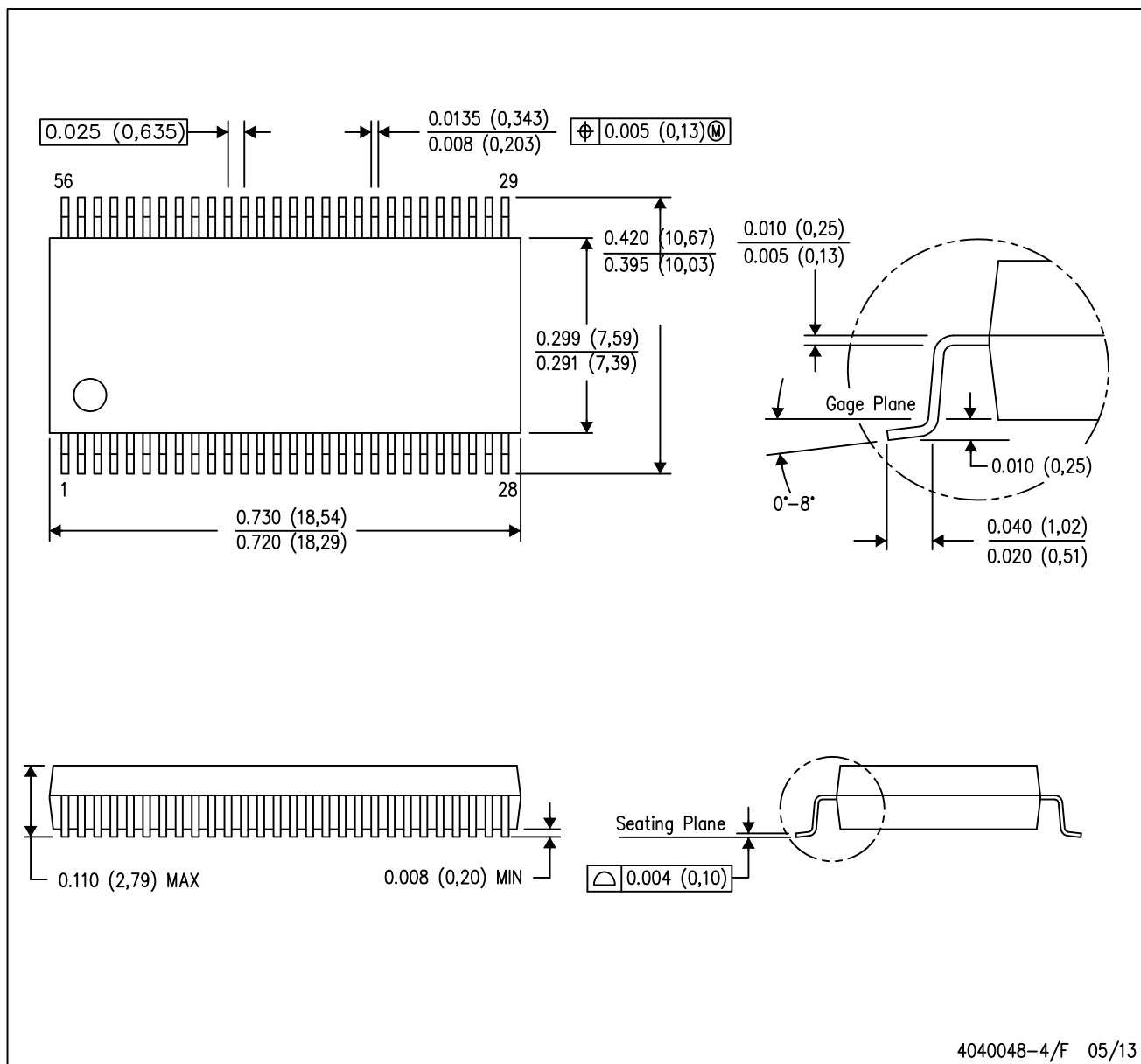
4220240/B 12/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed  $0.006$  (0,15).
  - Falls within JEDEC MO-118

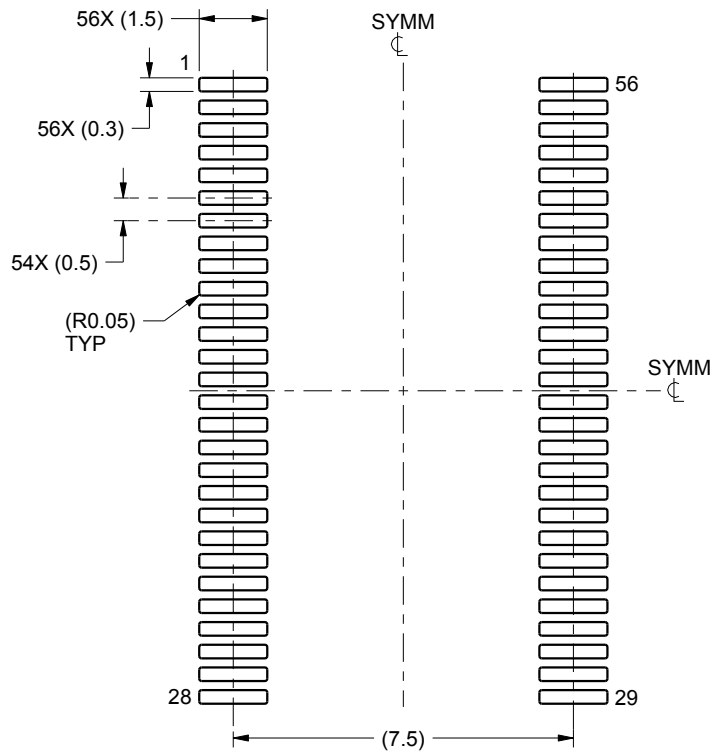


# EXAMPLE BOARD LAYOUT

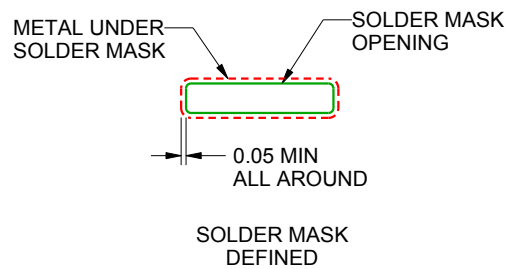
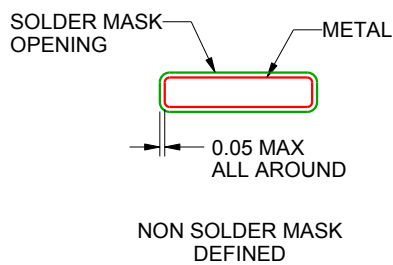
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

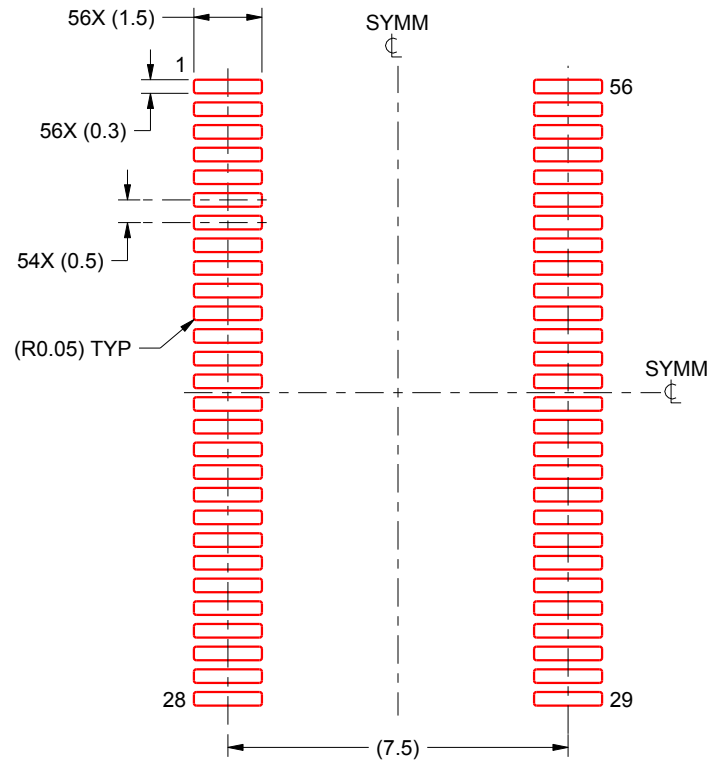
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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