

# SN54ABT16952, SN74ABT16952 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS082C – FEBRUARY 1991 – REVISED JANUARY 1997

- Members of the Texas Instruments **Widebus™** Family
- State-of-the-Art **EPIC-II<sup>B</sup>**™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

## description

The 'ABT16952 are 16-bit registered transceivers that contain two sets of D-type flip-flops for temporary storage of data flowing in either direction. The 'ABT16952 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable ( $\overline{OEAB}$  or  $\overline{OEBA}$ ) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16952 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16952 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

## SN54ABT16952 . . . WD PACKAGE SN74ABT16952 . . . DGG OR DL PACKAGE (TOP VIEW)

$\overline{1OEAB}$	1	56	$\overline{1OEBA}$
$\overline{1CLKAB}$	2	55	$\overline{1CLKBA}$
$\overline{1CLKENAB}$	3	54	$\overline{1CLKENBA}$
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
$V_{CC}$	7	50	$V_{CC}$
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
$V_{CC}$	22	35	$V_{CC}$
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
$\overline{2CLKENAB}$	26	31	$\overline{2CLKENBA}$
$\overline{2CLKAB}$	27	30	$\overline{2CLKBA}$
$\overline{2OEAB}$	28	29	$\overline{2OEBA}$



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# SN54ABT16952, SN74ABT16952

## 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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FUNCTION TABLE†

INPUTS				OUTPUT B
$\overline{\text{CLKENAB}}$	$\text{CLKAB}$	$\overline{\text{OEAB}}$	A	
H	X	L	X	$B_0^{\ddagger}$
X	L	L	X	$B_0^{\ddagger}$
L	$\uparrow$	L	L	L
L	$\uparrow$	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar, but uses  $\overline{\text{CLKENBA}}$ ,  $\text{CLKBA}$ , and  $\overline{\text{OEBA}}$ .

‡ Level of B before the indicated steady-state input conditions were established

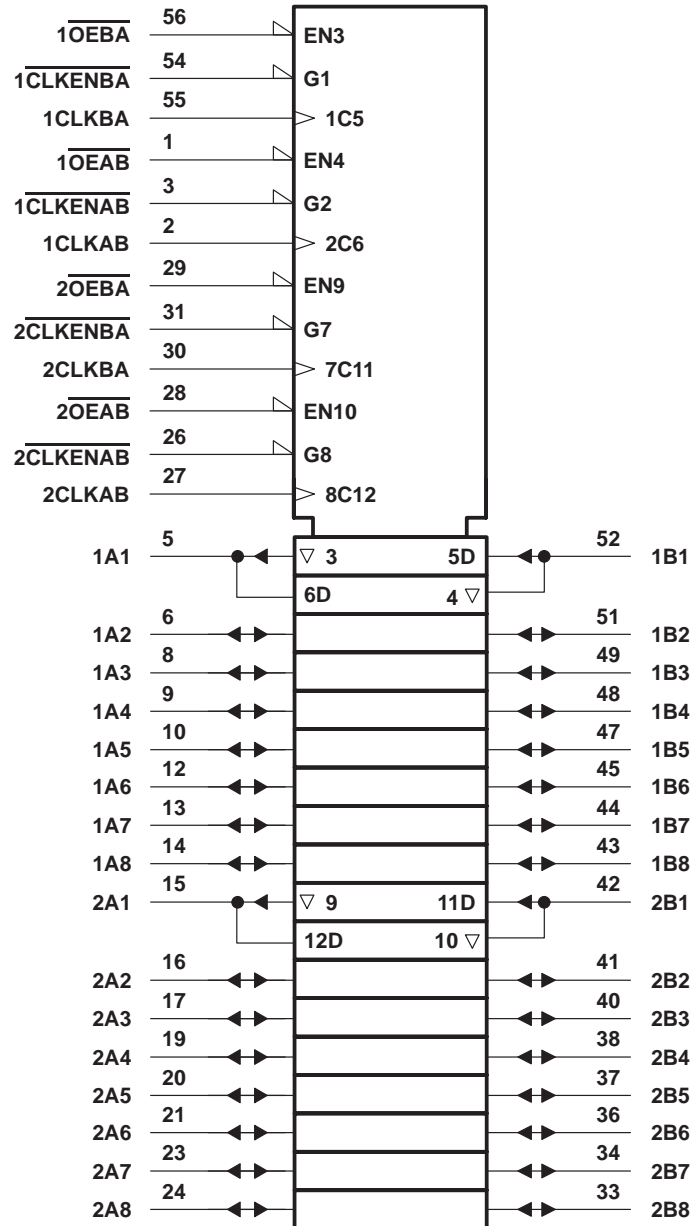


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SN54ABT16952, SN74ABT16952  
16-BIT REGISTERED TRANSCEIVERS  
WITH 3-STATE OUTPUTS

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

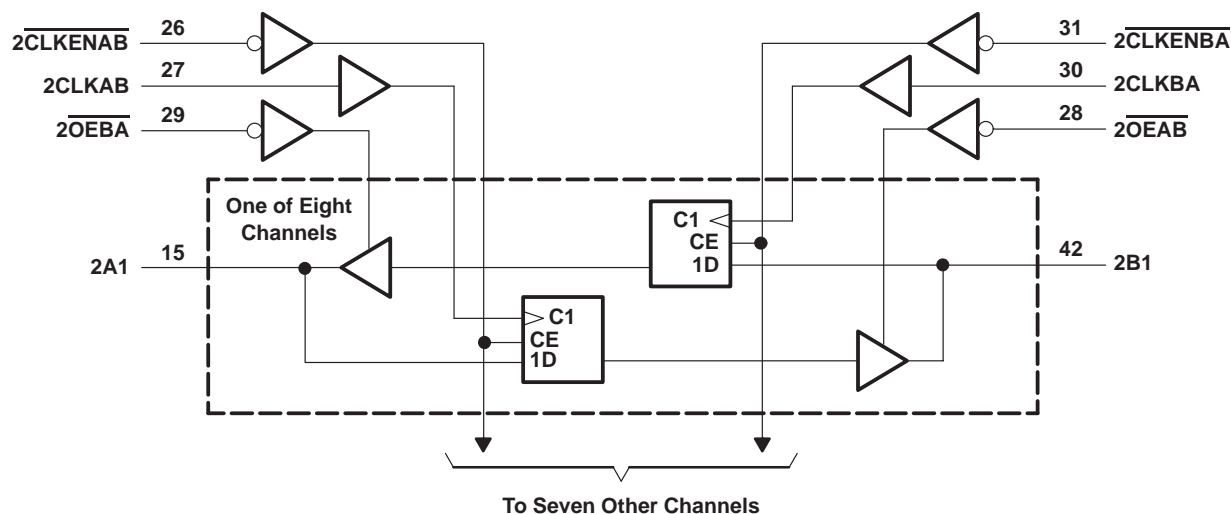
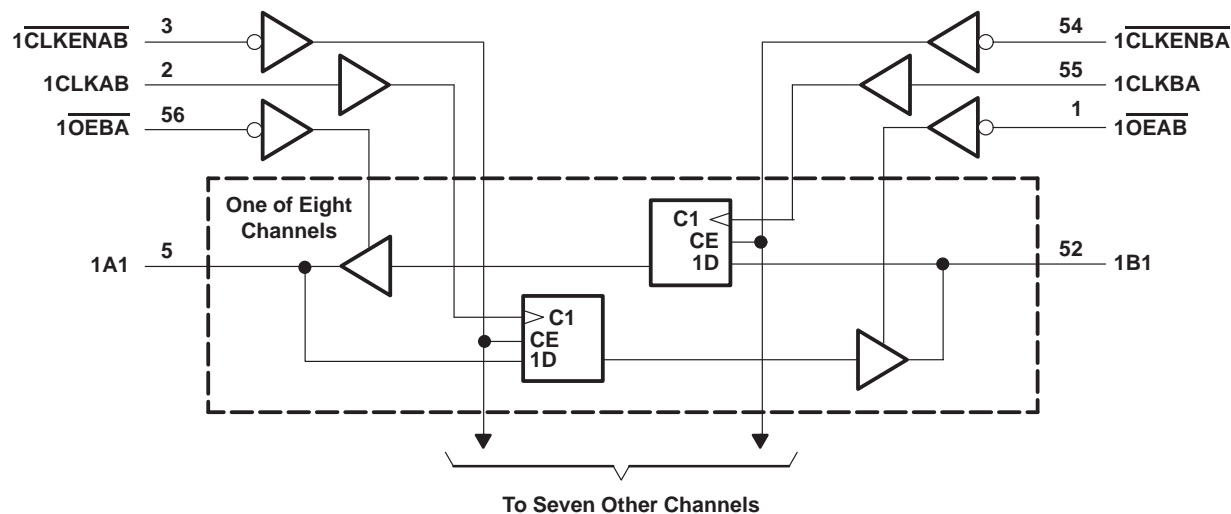
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## 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16952	96 mA
SN74ABT16952	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions (see Note 3)

		SN54ABT16952		SN74ABT16952		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled				ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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## 16-BIT REGISTERED TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT16952		SN74ABT16952		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA	2.5			2.5		2.5		V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA	3			3		3		
		V <sub>CC</sub> = 4.5 V	2			2				
									2	
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V			0.55	0.55				V
					0.55*				0.55	
V <sub>hys</sub>				100						mV
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1	±1		±1		μA
	A or B ports									
I <sub>OZH</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50		50		50	μA
I <sub>OZL</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50		-50		-50	μA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50		50		50	μA
I <sub>O</sub> §		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-200	-50	-200	-50	-200	mA
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			2	2		2		mA
ΔI <sub>CC</sub> ¶		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			0.5		0.5		0.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V			3					pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V			8.5					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			$V_{CC} = 5\text{ V}$ , $T_A = 25^{\circ}\text{C}$		SN54ABT16952		SN74ABT16952		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		0	150	0	150	0	150	MHz
$t_w^{\dagger}$	Pulse duration, CLKAB or CLKBA high or low		3.3		3.3		3.3		ns
$t_{\text{su}}$	Setup time, before CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B	3.5		3.5		3.5		ns
		$\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$	3		3		3		
$t_h$	Hold time, after CLKAB $\uparrow$ or CLKBA $\uparrow$	A or B	1		1		1		ns
		$\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$	1		1		1		

$^\dagger$  This parameter is warranted, but not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT16952		SN74ABT16952		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			150			150		150		MHz
$t_{\text{PLH}}$	CLK	A or B	1	2.6	3.9	1	4.4	1	4.3	ns
$t_{\text{PHL}}$			1	2.6	4.2	1	4.6	1	4.5	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	A or B	1	2.5	3.8	1	4.7	1	4.6	ns
$t_{\text{PZL}}$			1	2.8	5.1	1	6.1	1	6	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	A or B	1.7	3.4	4.7	1.7	6.1	1.7	5.5	ns
$t_{\text{PLZ}}$			1.3	3	3.9	1.3	4.8	1.3	4.2	

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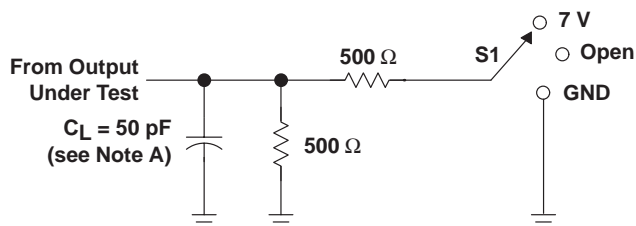


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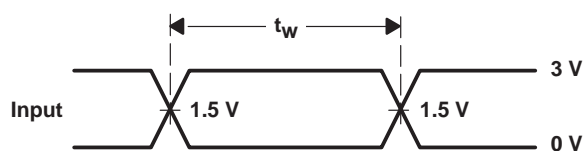
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## PARAMETER MEASUREMENT INFORMATION

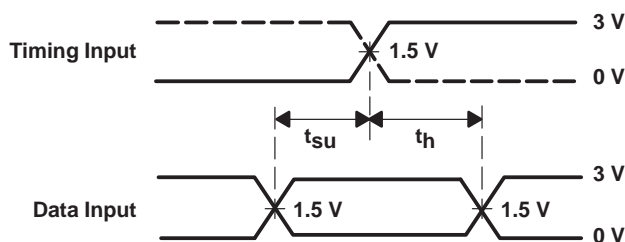


LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



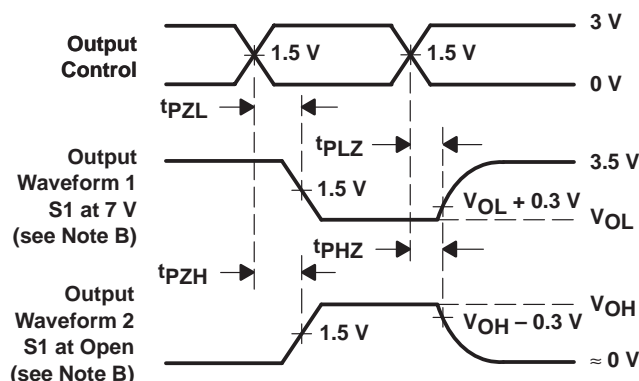
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74ABT16952DGGR</a>	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952
SN74ABT16952DGGR.B	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952
<a href="#">SN74ABT16952DL</a>	Active	Production	SSOP (DL)   56	20   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952
SN74ABT16952DL.B	Active	Production	SSOP (DL)   56	20   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952
<a href="#">SN74ABT16952DLR</a>	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952
SN74ABT16952DLR.B	Active	Production	SSOP (DL)   56	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16952

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16952DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ABT16952DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16952DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ABT16952DLR	SSOP	DL	56	1000	356.0	356.0	53.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16952DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABT16952DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

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