

# SN54ABT5403, SN74ABT5403 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS236B – JUNE 1992 – REVISED JANUARY 1997

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OLV}$  (Output Undershoot) < 0.5 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW) Package, Ceramic Chip Carriers (FK), and DIPs (JT)

## description

These 12-bit buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

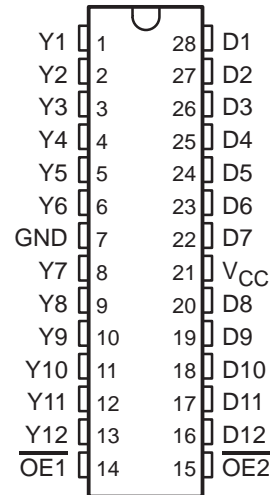
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all 12 outputs are in the high-impedance state. These devices provide inverted data.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

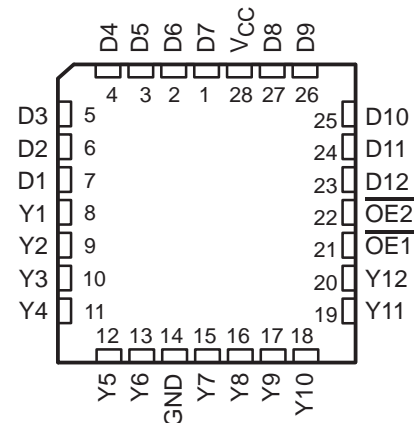
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT5403 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT5403 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT5403 . . . JT PACKAGE  
SN74ABT5403 . . . DW PACKAGE  
(TOP VIEW)



SN54ABT5403 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	D	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z



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**TEXAS  
INSTRUMENTS**

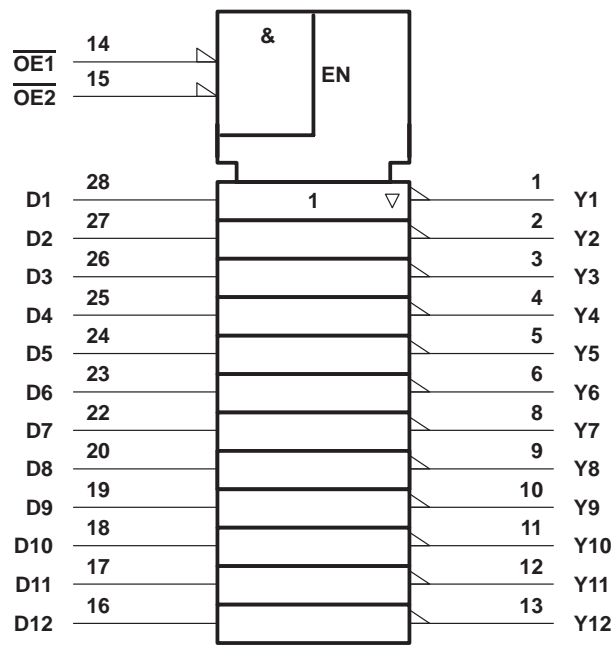
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 WITH 3-STATE OUTPUTS

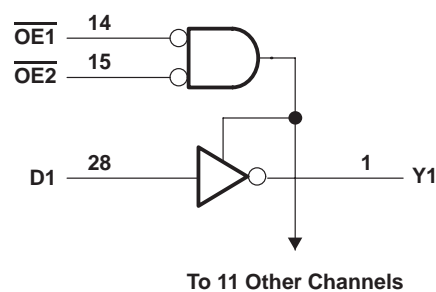
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for the DW and JT packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package	78°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

# SN54ABT5403, SN74ABT5403 12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

SCBS236B – JUNE 1992 – REVISED JANUARY 1997

## recommended operating conditions (see Note 3)

			SN54ABT5403		SN74ABT5403		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2		V
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current			–12		–12	mA
I <sub>OL</sub>	Low-level output current			12		12	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABT5403		SN74ABT5403		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA			–1.2		–1.2		–1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –1 mA	3.35	3.7		3.3		3.35		V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –1 mA	3.85	4.2		3.8		3.85		
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA				3		3.1		
		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –12 mA	2.6					2.6		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 8 mA				0.8		0.65		V
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 12 mA						0.8		
V <sub>hys</sub>				100						mV
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V			50		50		50	μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			–50		–50		–50	μA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V, Outputs high			50		50		50	μA
I <sub>O</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	–25	–45	–100	–25	–100	–25	–100	mA
I <sub>OS‡</sub>		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0	–50		–200	–50	–200	–50	–200	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND, Outputs high		5	50		50		50	μA
		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND, Outputs low		36	45		45		45	mA
		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND, Outputs disabled		1	50		50		50	μA
ΔI <sub>CC</sub> §	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND, Outputs enabled			1.5		1.5		1.5	mA
	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND, Outputs disabled			0.05		0.05		0.05	
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1.5		1.5		1.5	
C <sub>i</sub>		V <sub>I</sub> = 2.5 V or 0.5 V		3						pF
C <sub>o</sub>		V <sub>O</sub> = 2.5 V or 0.5 V		8						pF

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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# SN54ABT5403, SN74ABT5403

## 12-BIT LINE/MEMORY DRIVERS

### WITH 3-STATE OUTPUTS

SCBS236B – JUNE 1992 – REVISED JANUARY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

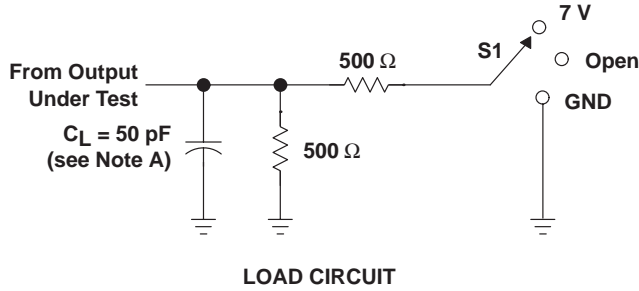
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT5403		SN74ABT5403		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	Y	2	4.5	6.1	2	7	2	6.9	ns
$t_{PHL}$			1.5	4.4	5.2	1.5	5.9	1.5	5.7	
$t_{PZH}$	$\overline{OE}$	Y	2.5	5.7	6.6	2.5	8.6	2.5	8.5	ns
$t_{PZL}$			2	4.4	5.5	2	6.9	2	6.8	
$t_{PHZ}$	$\overline{OE}$	Y	1.5	3.6	4.4	1.5	5.5	1.5	5.2	ns
$t_{PLZ}$			1.5	4.2	5.4	1.5	7.4	1.5	6.9	

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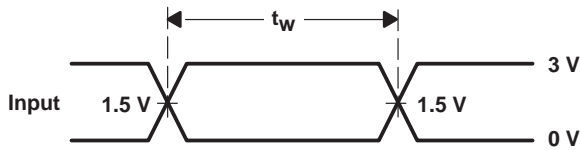


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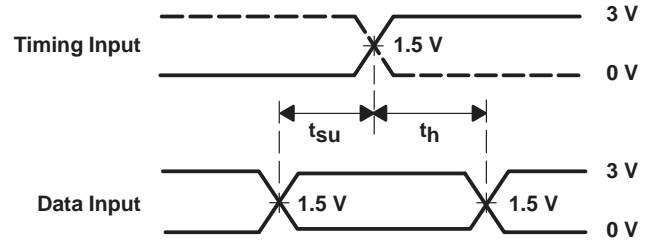
## PARAMETER MEASUREMENT INFORMATION



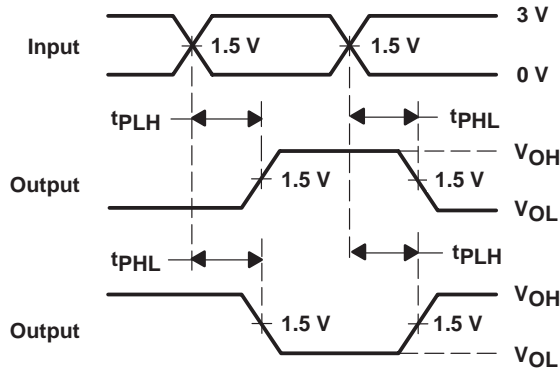
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



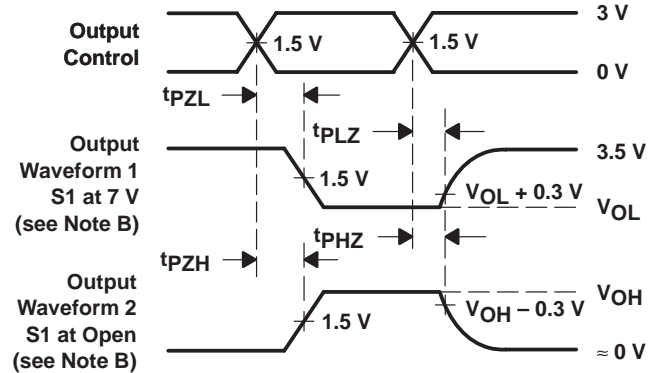
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74ABT5403DWR</a>	Active	Production	SOIC (DW)   28	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT5403
SN74ABT5403DWR.B	Active	Production	SOIC (DW)   28	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT5403

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT5403DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT5403DWR	SOIC	DW	28	1000	350.0	350.0	66.0



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