

SN74AC573 Octal D-type Transparent Latches with 3-State Outputs

1 Features

- Operation of 2V to 6V V_{CC}
- Inputs accept voltages to 6V
- Maximum t_{pd} of 9ns at 5V
- 3-State outputs drive bus lines directly

2 Applications

- Buffer registers
- Bidirectional bus drivers
- Working registers

3 Description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

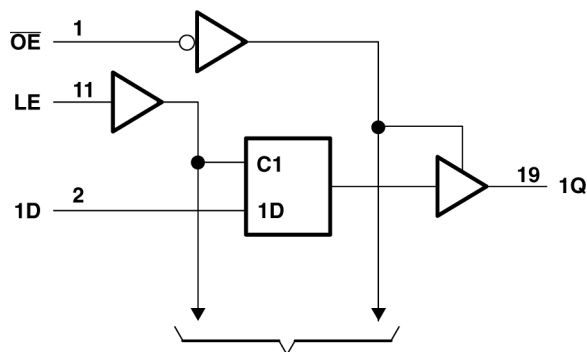
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74AC573	RKS (VQFN, 20)	4.5 mm × 2.5 mm	4.5mm × 2.5mm
	DB (SSOP, 20)	7.2 mm × 7.8 mm	7.2mm × 5.30mm
	DGV (TVSOP, 20)	5 mm × 6.4 mm	5mm × 4.4mm
	DW (SOIC, 20)	12.8 mm × 10.3 mm	12.80mm × 7.50mm
	NS (SOP, 20)	12.6 mm × 7.8 mm	12.6mm × 5.3mm
	N (PDIP, 20)	24.33 mm × 9.4 mm	24.33mm × 6.35mm
	PW (TSSOP, 20)	6.5 mm × 6.4 mm	6.50mm × 4.40mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) The body size (length × width) is a nominal value and does not include pins.



To Seven Other Channels

Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

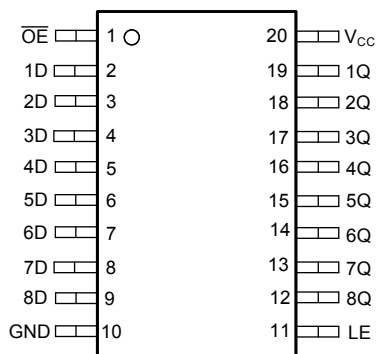


Figure 4-1. DB, DGV, DW, NS, N, or PW Packages, 20-Pin SSOP, TVSOP, SOIC, SOP, PDIP, or TSSOP (Top View)

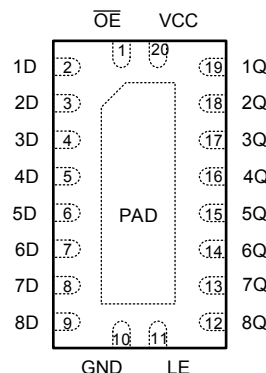


Figure 4-2. RKS Package, 20-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
OE	1	I	Output enable
1D	2	I	1D input
2D	3	I	2D input
3D	4	I	3D input
4D	5	I	4D input
5D	6	I	5D input
6D	7	I	6D input
7D	8	I	7D input
8D	9	I	8D input
GND	10	—	Ground
LE	11	I	Latch enable input
8Q	12	O	8Q output
7Q	13	O	7Q output
6Q	14	O	6Q output
5Q	15	O	5Q output
4Q	16	O	4Q output
3Q	17	O	3Q output
2Q	18	O	2Q output
1Q	19	O	1Q output
V _{CC}	20	—	Power pin
Thermal Pad ⁽²⁾		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) For RKS package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	+ 7	V
V_I ²	Input voltage range	-0.5	$V_{CC} + 0.5$	V
V_O ²	Output voltage range	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$(V_I < 0 \text{ or } V_I > V_{CC})$		± 20 mA
I_{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		± 20 mA
I_O	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		± 50 mA
	Continuous current through, V_{CC} or GND			± 200 mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	6	V
V_{IH}	High-level input voltage	$V_{CC} = 3 \text{ V}$	2.1	V
		$V_{CC} = 4.5 \text{ V}$	3.15	
		$V_{CC} = 5.5 \text{ V}$	3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 3 \text{ V}$	0.9	V
		$V_{CC} = 4.5 \text{ V}$	1.35	
		$V_{CC} = 5.5 \text{ V}$	1.65	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3 \text{ V}$	-12	mA
		$V_{CC} = 4.5 \text{ V}$	-24	
		$V_{CC} = 5.5 \text{ V}$	-24	
I_{OL}	Low-level output current	$V_{CC} = 3 \text{ V}$	12	mA
		$V_{CC} = 4.5 \text{ V}$	24	
		$V_{CC} = 5.5 \text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		8	ns/V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC	SN74AC573						UNIT
	DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RKS (VQFN)	
	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance ⁽¹⁾	101.2	70	69	60	126.2	68	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN74AC573		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = −50 μA		3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
	I _{OH} = −12 mA		3 V	2.58			2.48		
	I _{OH} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I _{OH} = −75 mA ⁽¹⁾		5.5 V				3.85		
V _{OL}	I _{OL} = 50 μA		3 V				0.1		V
			4.5 V				0.1		
			5.5 V				0.1		
	I _{OL} = 12 mA		3 V				0.36		
	I _{OL} = 24 mA		4.5 V				0.36		
			5.5 V				0.36		
	I _{OL} = 75 mA		5.5 V				1.65		
I _I	V _I = V _{CC} or GND		5.5 V				±0.1	±1	μA
I _{OZ}	V _O = V _{CC} or GND		5.5 V				±0.25	±2.5	μA
I _{CC}	V _I = V _{CC} or GND,	I _O = 0	5.5 V				4	40	μA
C _i	V _I = V _{CC} or GND		5 V	5					pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

5.5 Timing Requirements, $V_{CC} = 3.3\ \text{V} \pm 0.3\ \text{V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\ \text{V} \pm 0.3\ \text{V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		$T_A = 25^\circ\text{C}$		SN74AC573		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	6		7		ns
t_{su}	Setup time, data before LE $\downarrow$	3.5		4		ns
t_h	Hold time, data after LE $\downarrow$	2		2		ns

5.6 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		$T_A = 25^\circ\text{C}$		SN74AC573		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	4		5		ns
t_{su}	Setup time, data before LE $\downarrow$	3		3.5		ns
t_h	Hold time, data after LE $\downarrow$	2		2		ns

5.7 Switching Characteristics, $V_{CC} = 3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$		SN74AC573		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2.5	13	2	15	ns
t_{PHL}			2.5	12	2	14	
t_{PLH}	LE	Q	2.5	13	2	15	ns
t_{PHL}			2.5	12	2	14	
t_{PZH}	$\overline{OE}$	Q	2.5	11	2	12	ns
t_{PZL}			2.5	11	2	12.5	
t_{PHZ}	$\overline{OE}$	Q	2.5	12.5	2	13.5	ns
t_{PLZ}			2.5	9.5	2	10.5	

5.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

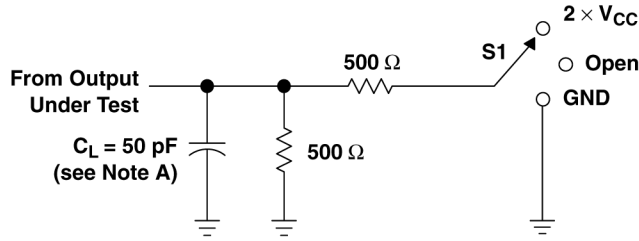
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$		SN74AC573		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2.5	10	2	11.5	ns
t_{PHL}			2.5	9.5	2	11	
t_{PLH}	LE	Q	2.5	9.5	2	11	ns
t_{PHL}			2.5	8.5	2	10	
t_{PZH}	$\overline{OE}$	Q	2.5	9	2	10	ns
t_{PZL}			2.5	8.5	2	9.5	
t_{PHZ}	$\overline{OE}$	Q	2.5	11	2	12	ns
t_{PLZ}			2.5	8	2	9	

5.9 Operating Characteristics

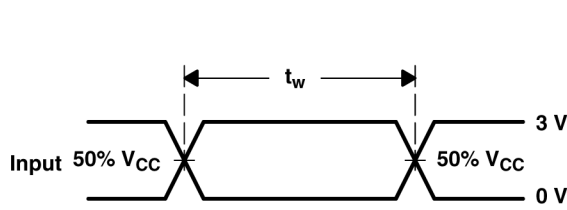
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$	$f = 1\text{ MHz}$	25	pF

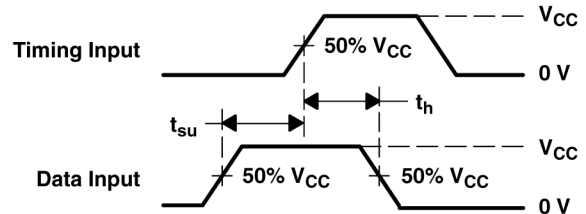
6 Parameter Measurement Information



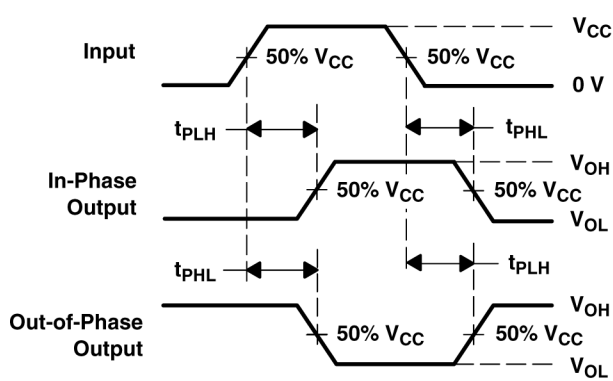
LOAD CIRCUIT



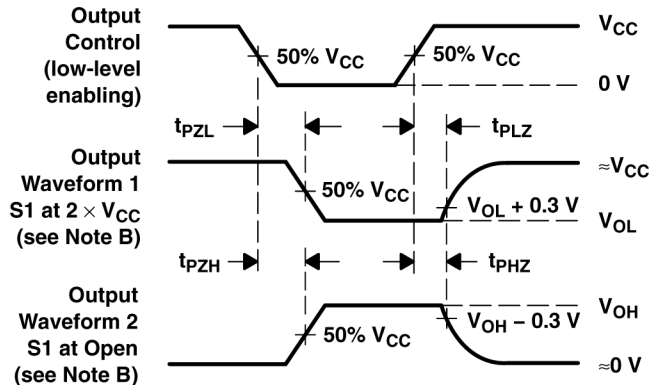
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

Table 6-1.

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	Open

7 Detailed Description

7.1 Overview

The eight latches are D-type transparent latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D Inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

7.2 Functional Block Diagram

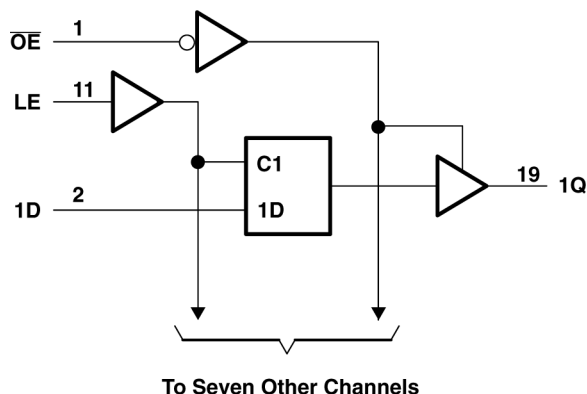


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

Table 7-1. Function Table (Each Latch)

INPUTS ⁽¹⁾			OUTPUT ⁽²⁾ Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

- (1) H = High voltage level, L = Low voltage level, X = High or low voltage level
 (2) H = Driving high, L = Driving low, Q₀ = Driving previous high or low state, Z = High impedance

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 5.2](#) table. The total current through Ground or V_{CC} must not exceed ± 70 mA as per [Section 5.1](#) table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1- μ F capacitor; if there are multiple V_{CC} pins, then TI recommends 0.01- μ F or 0.022- μ F capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- μ F and 1- μ F capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Layout Diagram](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

8.2.2 Layout Example

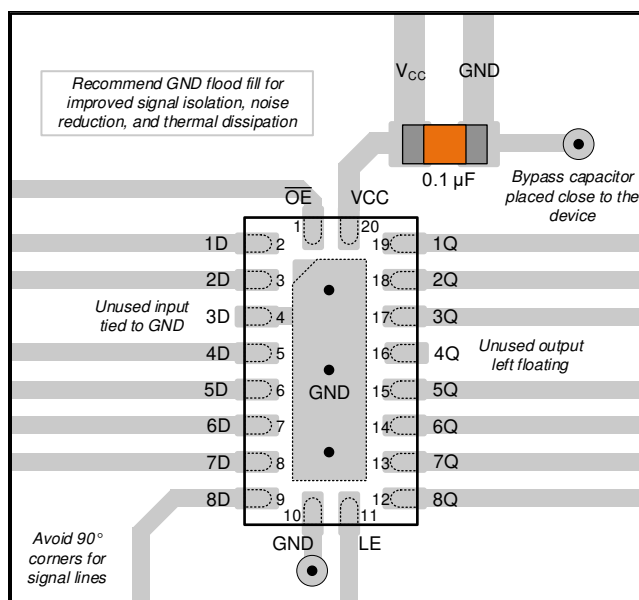


Figure 8-1. Layout example of the SN74AC573

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (November 2023) to Revision H (February 2024)	Page
• Added body size to <i>Package Information</i> table.....	1
• Updated RθJA values: DW = 58 to 101.2, PW = 83 to 126.2, all values in °C/W	5
• Added <i>Application and Implementation</i> section.....	9

Changes from Revision F (June 2023) to Revision G (November 2023)	Page
• Updated the <i>Package Information</i> table to include package lead size.....	1
• Added the <i>RKS</i> package information.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AC573DBR	NRND	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573DBR.A	NRND	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573DBRG4	NRND	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	AC573
SN74AC573DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573DWRG4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC573N
SN74AC573N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74AC573N
SN74AC573NSR	NRND	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573NSR.A	NRND	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573PW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	AC573
SN74AC573PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573PWRE4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC573
SN74AC573RKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC573
SN74AC573RKSR.A	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AC573

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AC573 :

- Automotive : [SN74AC573-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC573DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AC573NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AC573RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

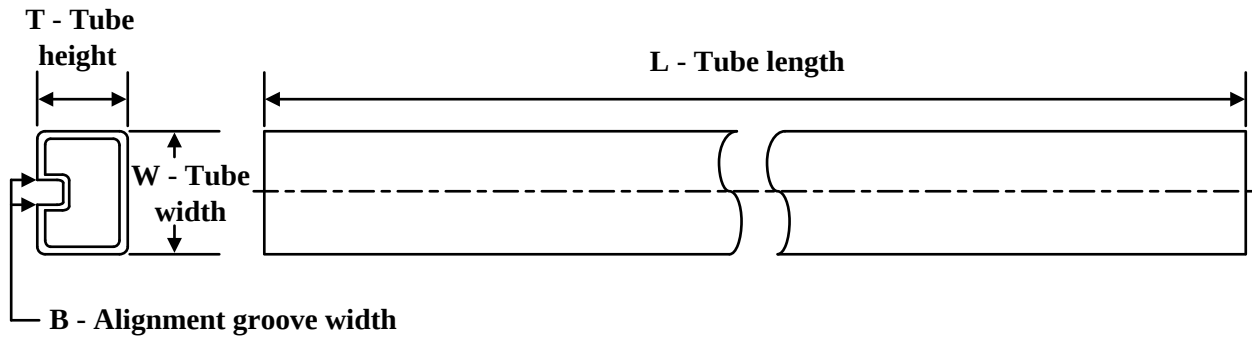
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC573DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AC573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AC573NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AC573PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AC573RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



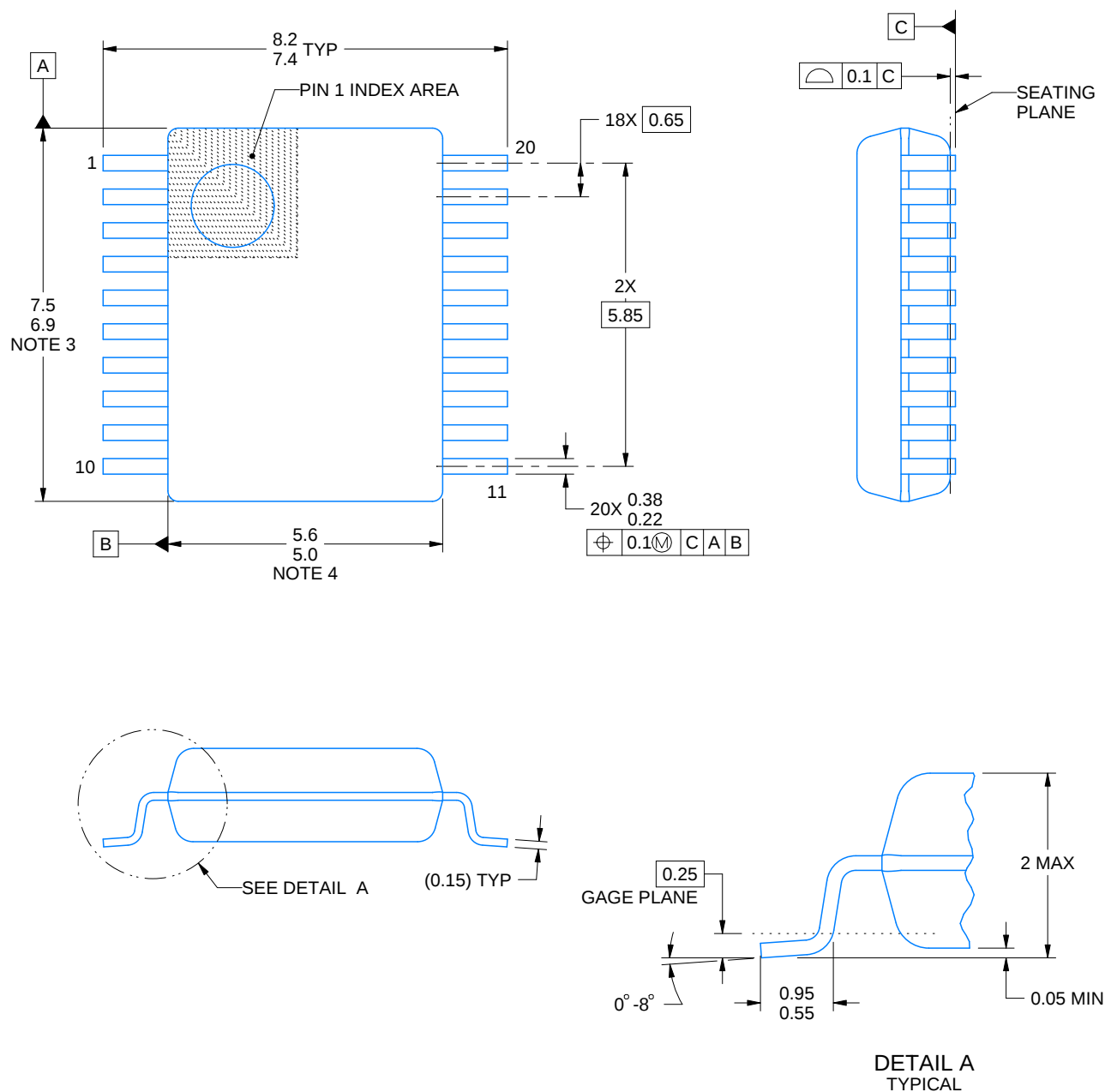
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AC573N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AC573N.A	N	PDIP	20	20	506	13.97	11230	4.32



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

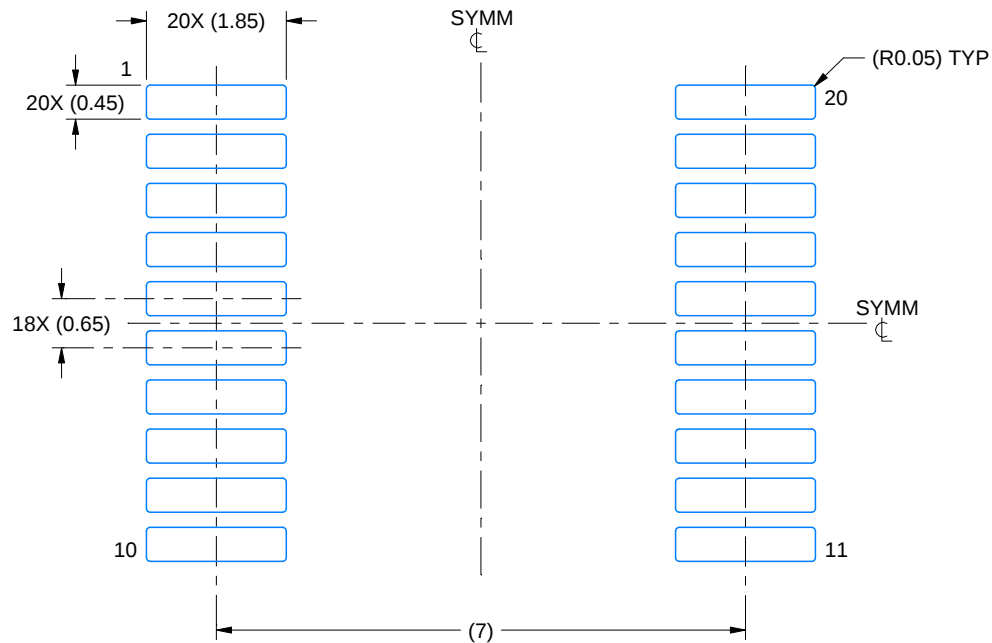
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

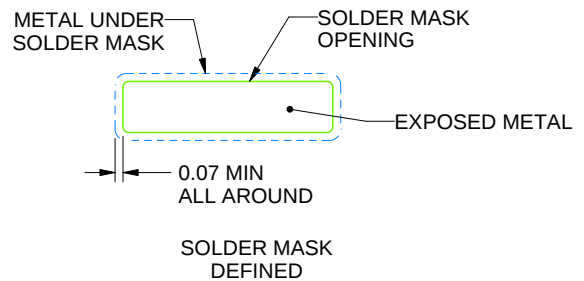
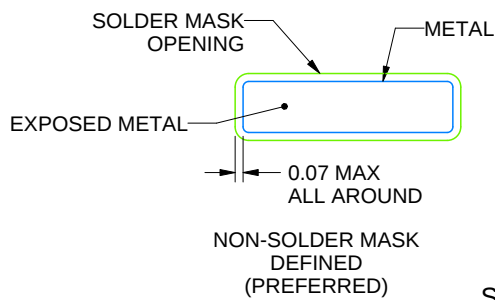
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

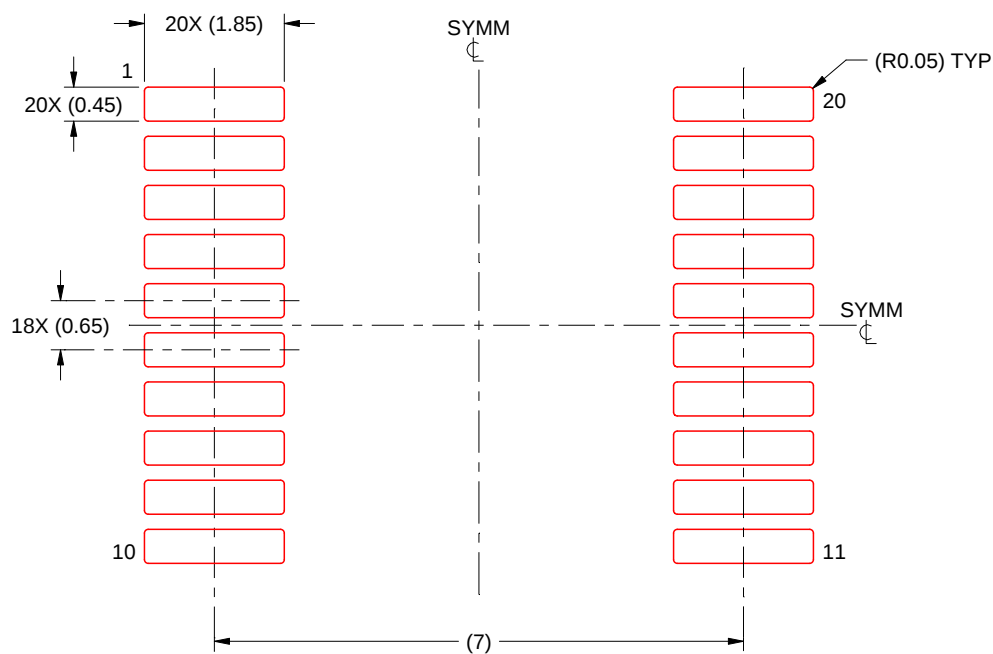
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

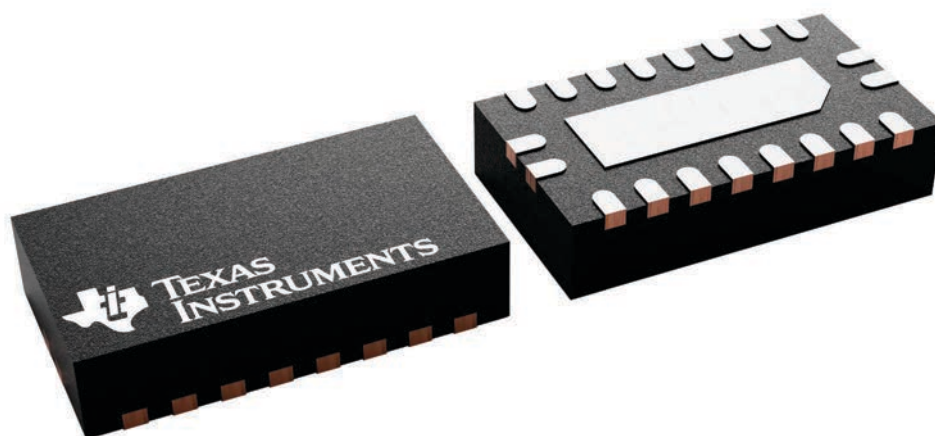
RKS 20

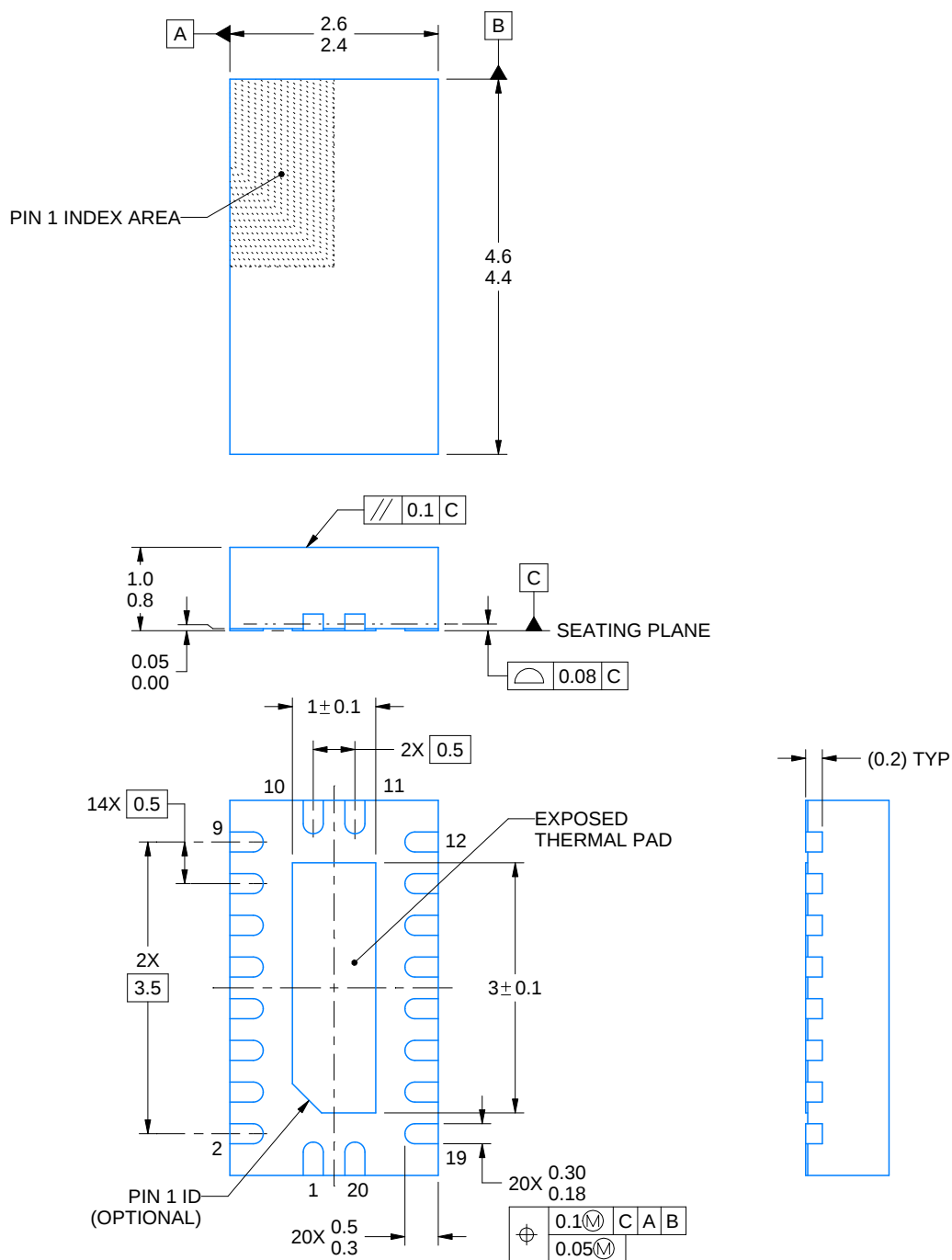
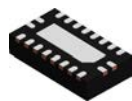
VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4222490/B 02/2021

NOTES:

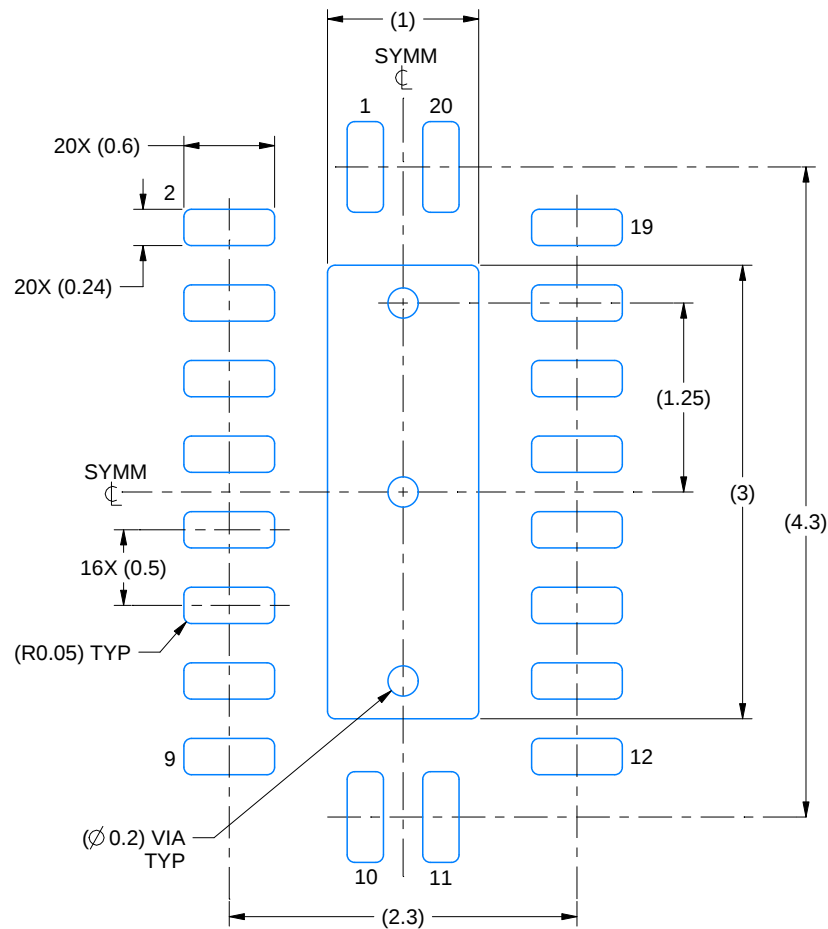
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

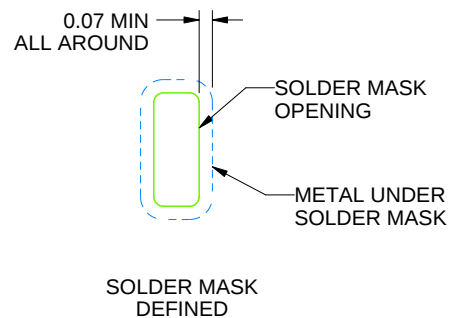
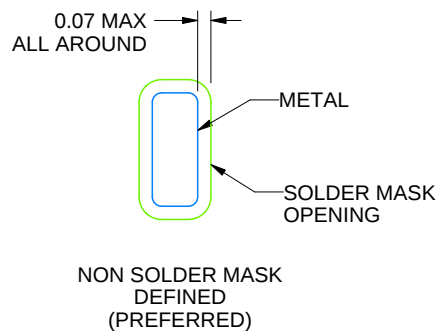
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

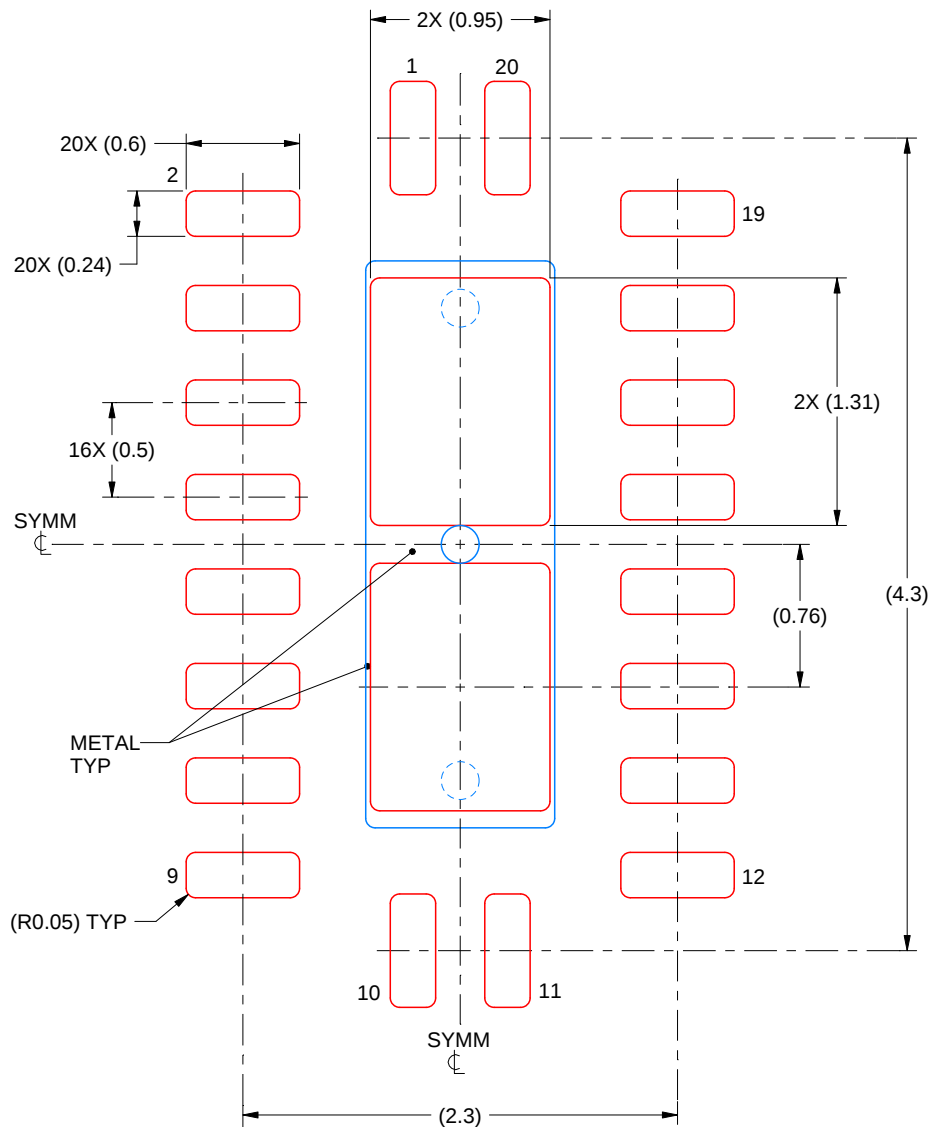
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

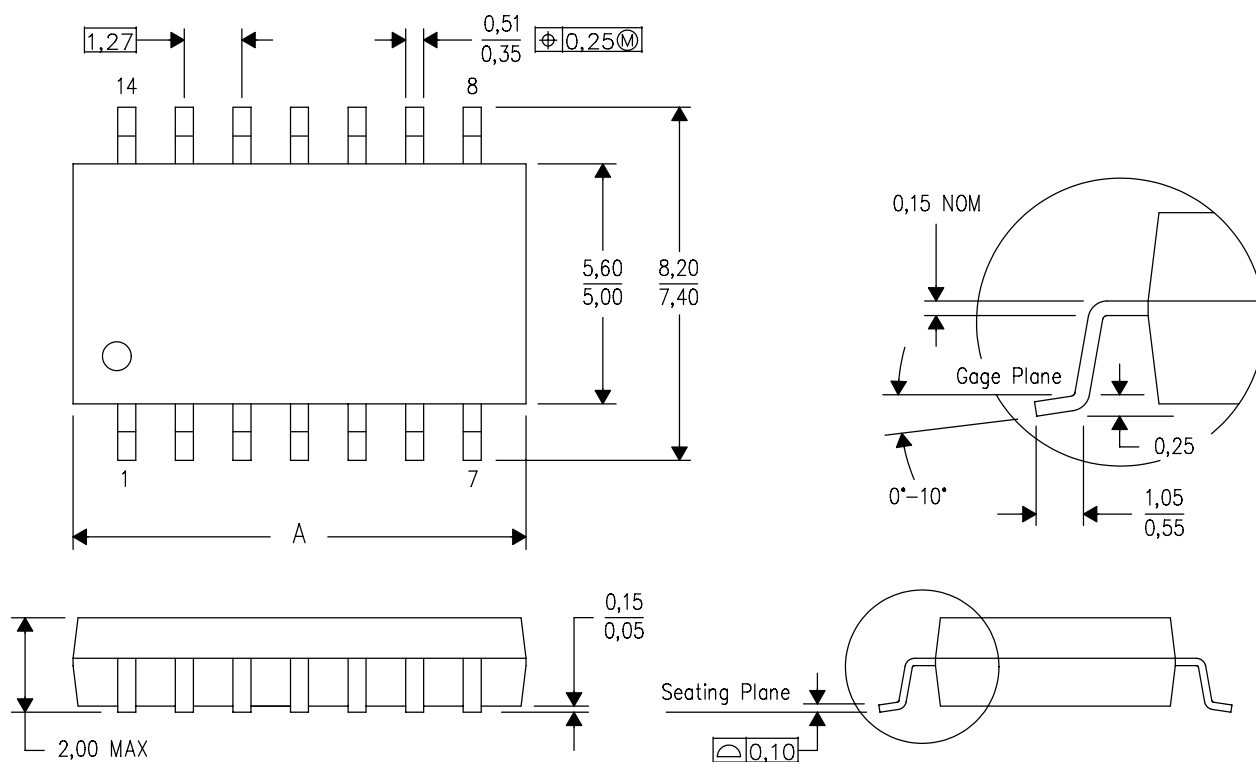
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

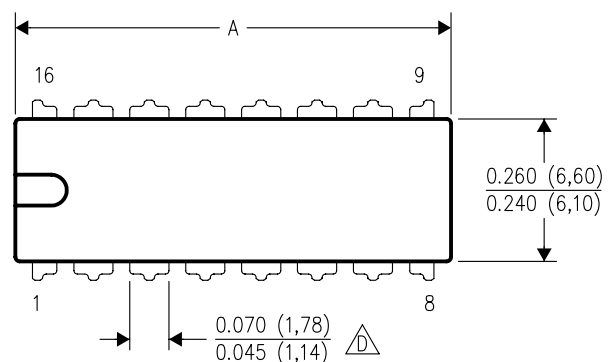
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

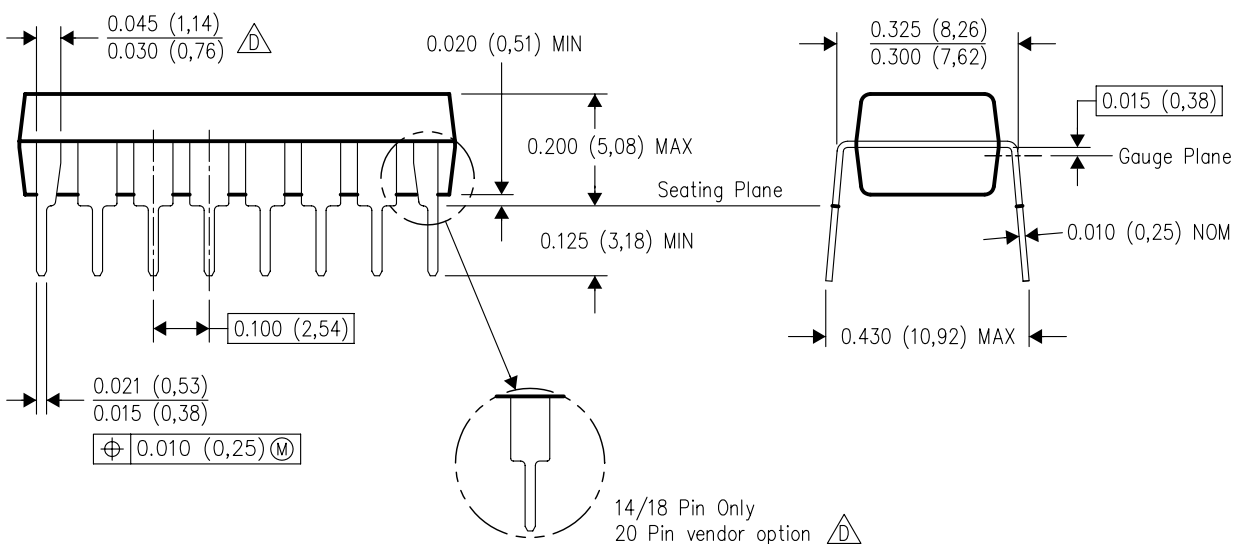
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

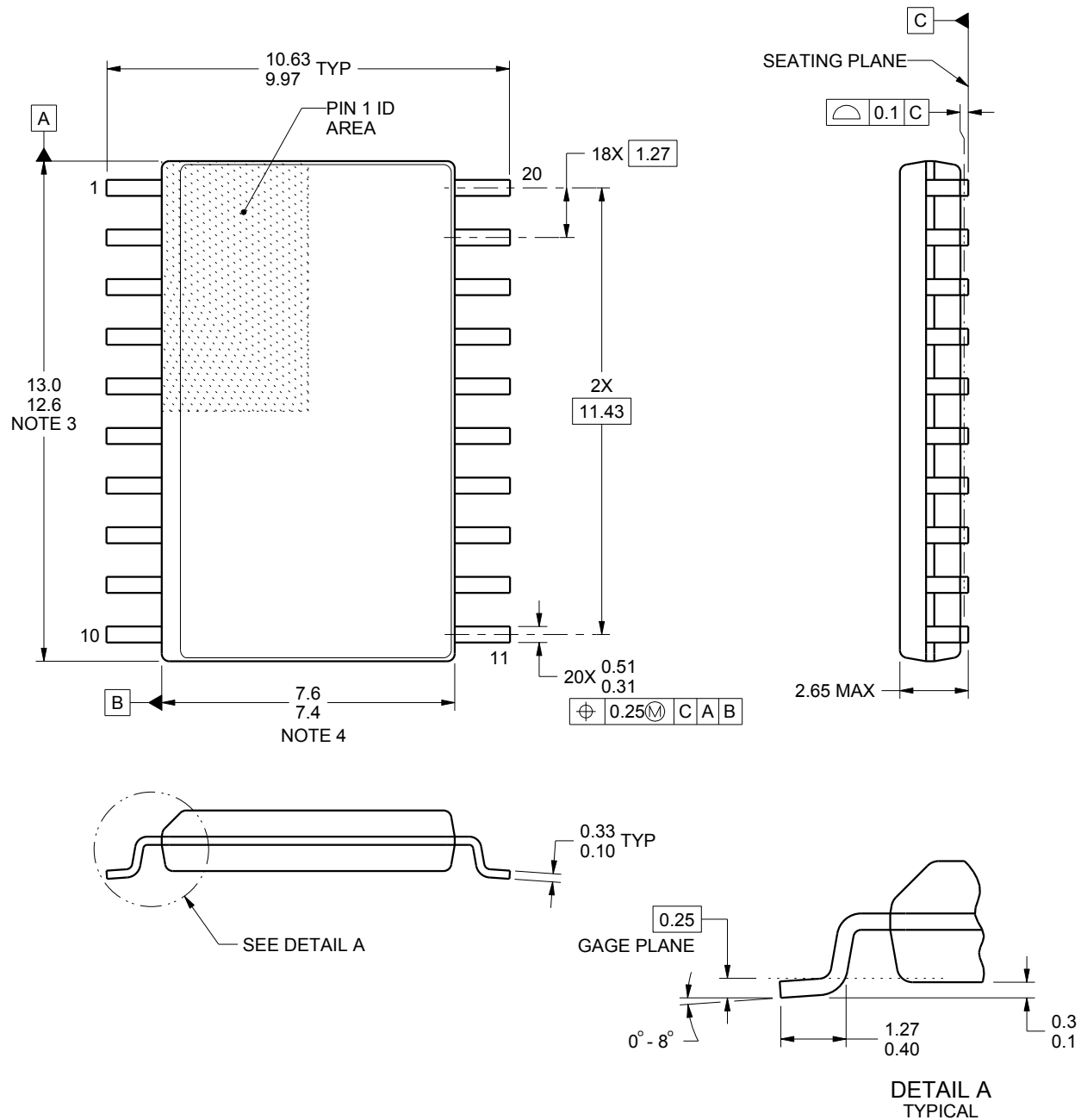
- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

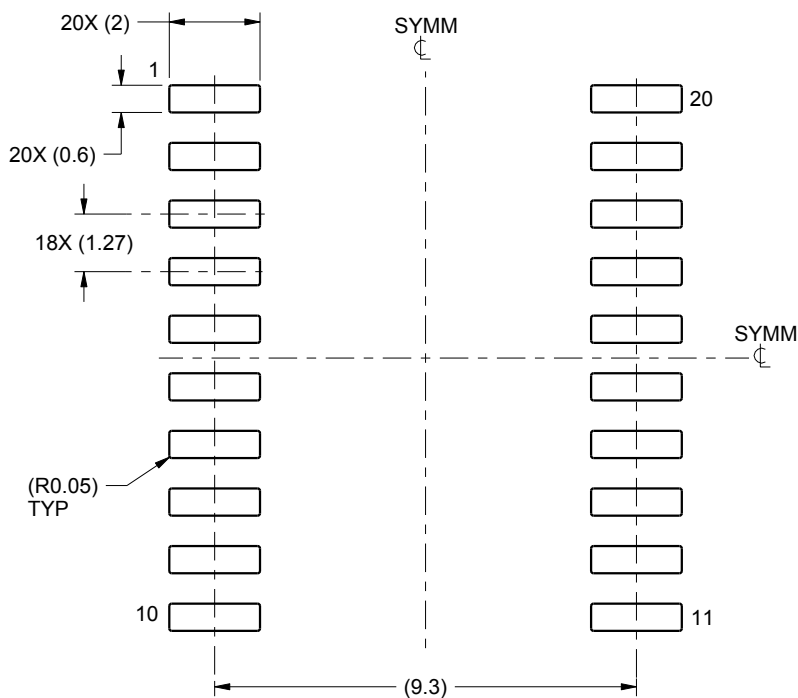
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

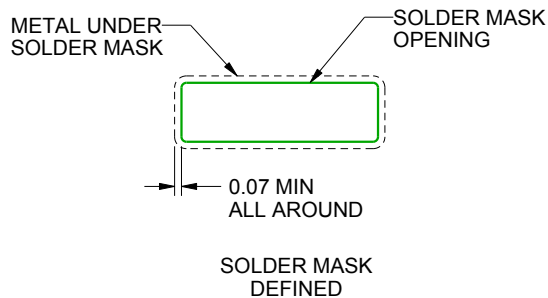
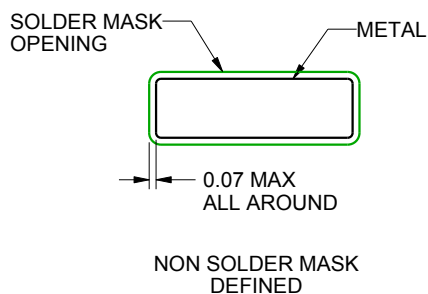
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

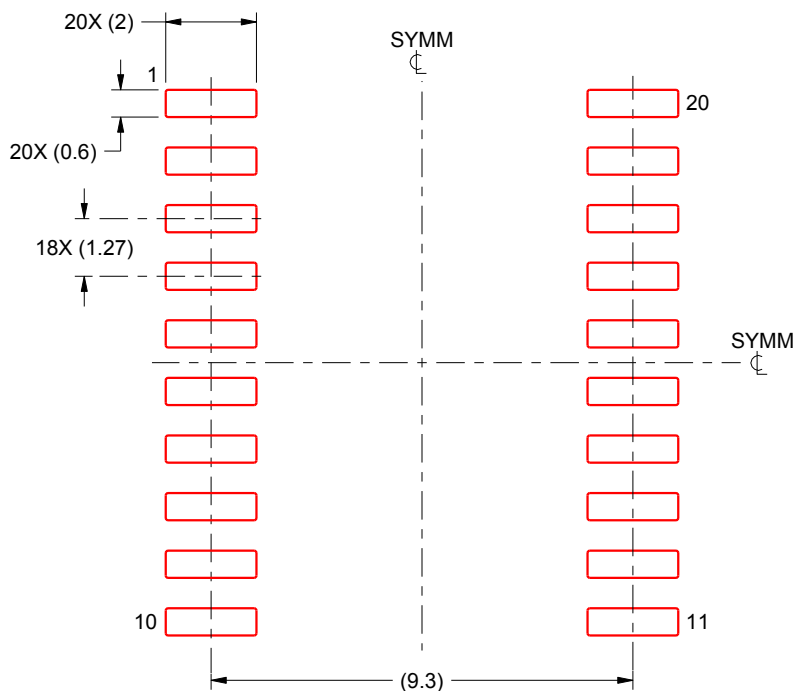
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

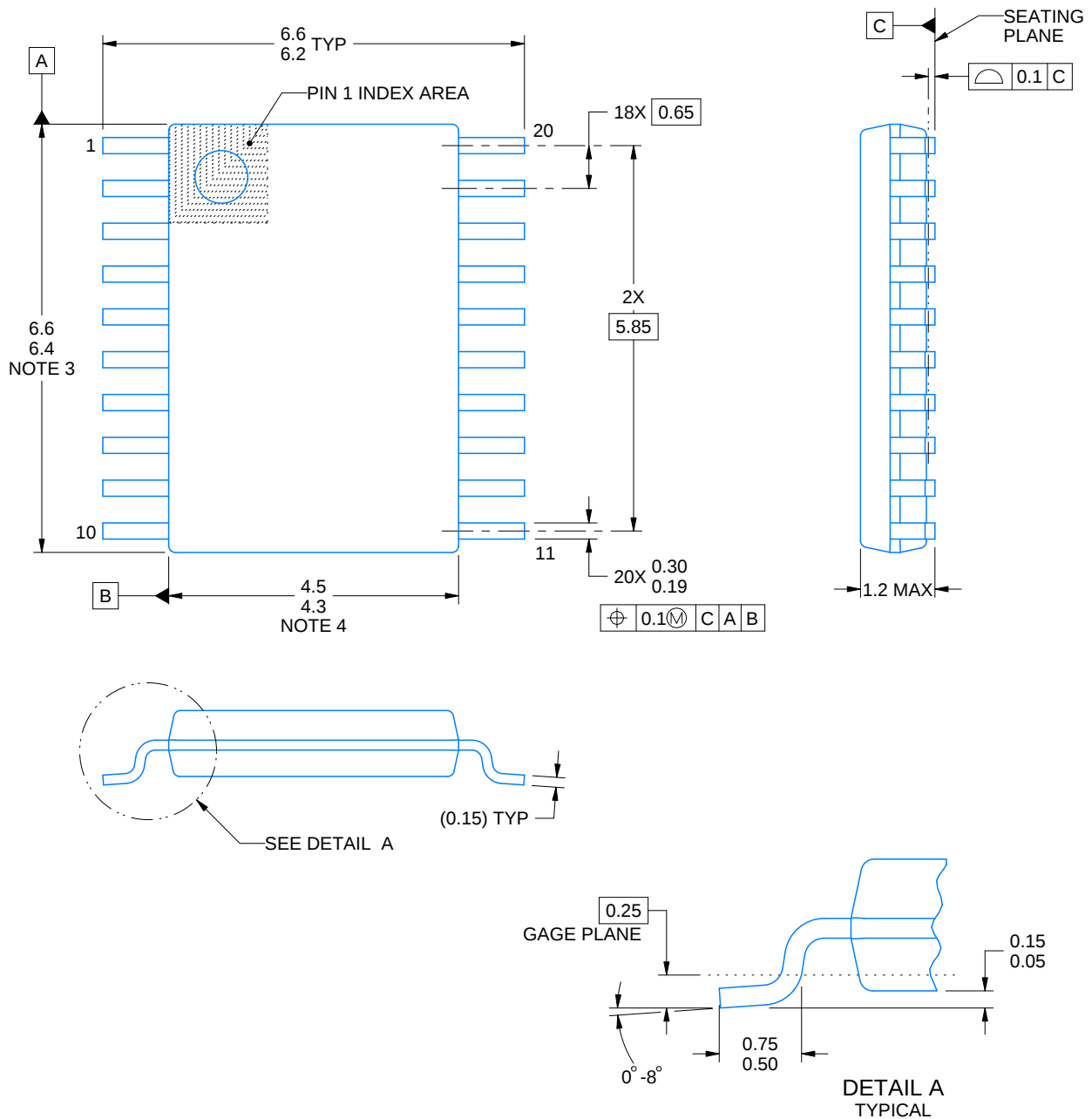
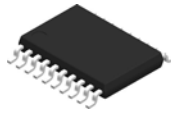


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220206/A 02/2017

NOTES:

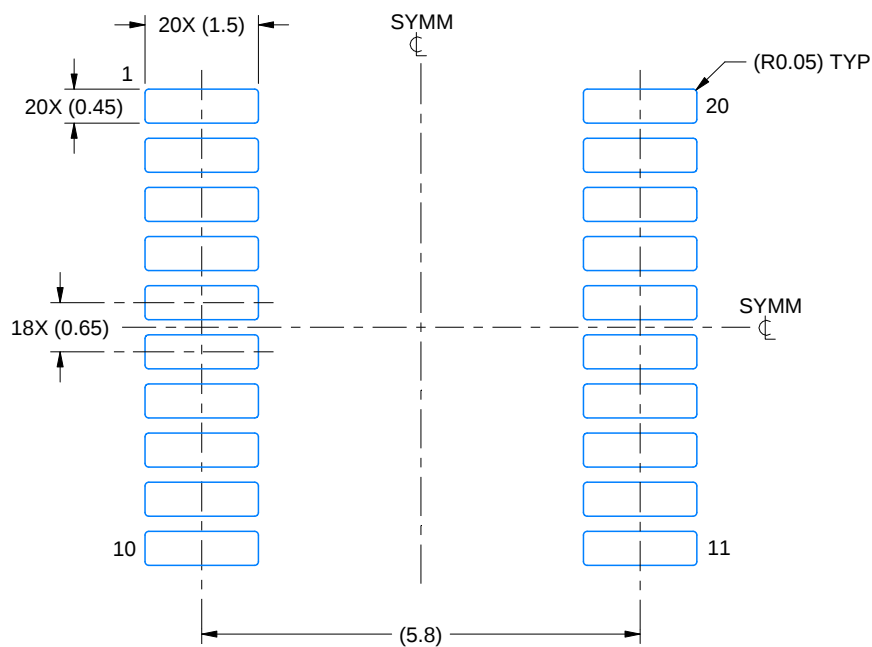
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

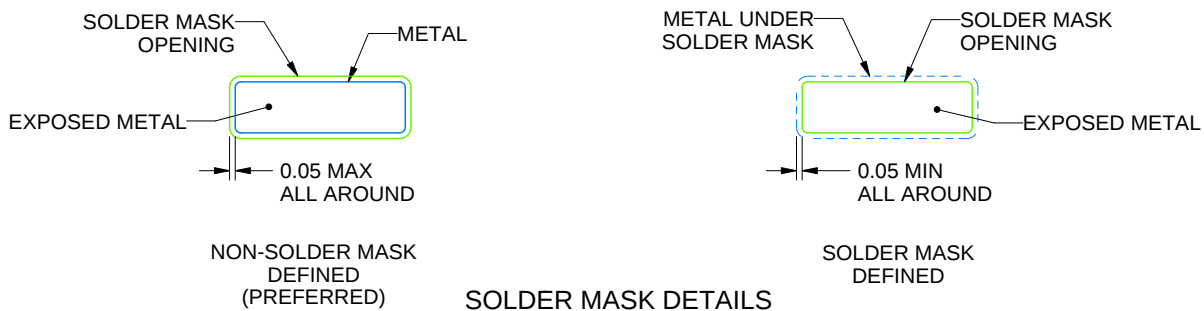
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

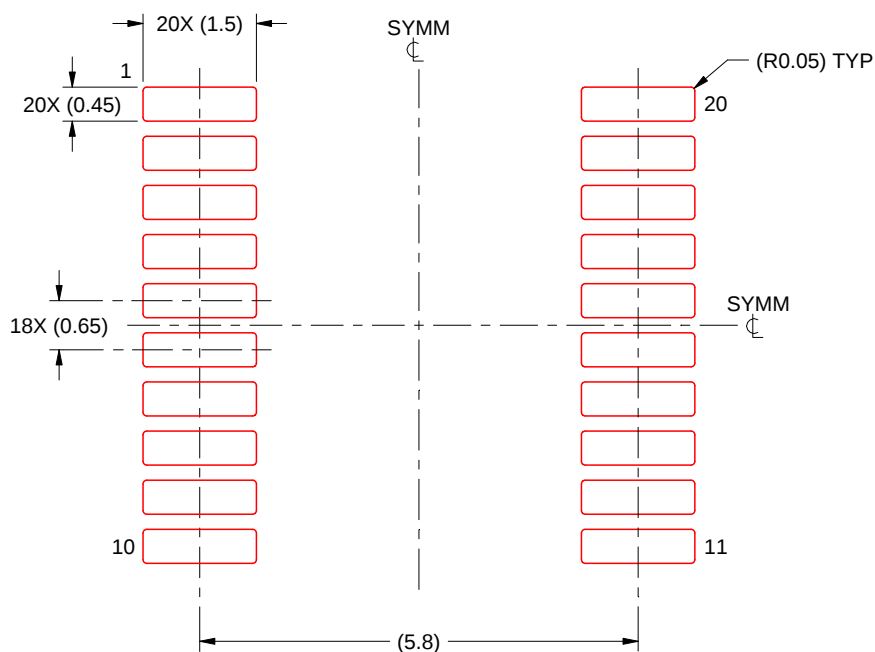
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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