# SN74ACT132 Quadruple Positive-NAND Gates With Schmitt-Trigger Inputs

## 1 Features

- Operating voltage range of 4.5V to 5.5V
- TTL-compatible Schmitt-trigger inputs support slow and noisy input signals
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Fast operation with delay of 10.2ns

## 2 Applications

- Alarm and tamper detect circuit
- S-R latch

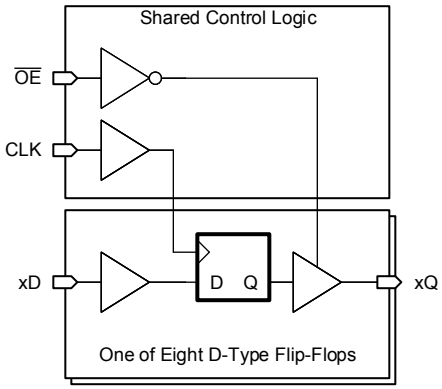
## 3 Description

The SN74ACT132 contains four independent 2-input NAND gates. Each gate performs the Boolean function $Y = \overline{A \cdot B}$.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN74ACT132 | PW (TSSOP, 14) | 5mm × 6.4mm | 5mm × 4.4mm |
| | BQA (WQFN, 14) | 3mm × 2.5mm | 3mm × 2.5mm |

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Functional Block Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

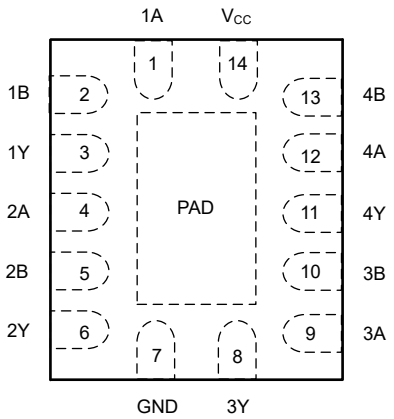


**Figure 4-1. SN74ACT132 BQA Package (Top View)**

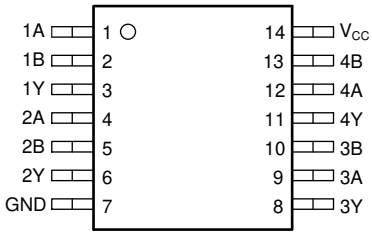


**Figure 4-2. SN74ACT132 , PW Package (Top View)**

**Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | I | Channel 1, Input A |
| 1B | 2 | I | Channel 1, Input B |
| 1Y | 3 | O | Channel 1, Output Y |
| 2A | 4 | I | Channel 2, Input A |
| 2B | 5 | I | Channel 2, Input B |
| 2Y | 6 | O | Channel 2, Output Y |
| GND | 7 | G | Ground |
| 3Y | 8 | O | Channel 3, Output Y |
| 3A | 9 | I | Channel 3, Input A |
| 3B | 10 | I | Channel 3, Input B |
| 4Y | 11 | O | Channel 4, Output Y |
| 4A | 12 | I | Channel 4, Input A |
| 4B | 13 | I | Channel 4, Input B |
| $V_{CC}$ | 14 | P | Positive Supply |
| Thermal Pad[2] | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply. |

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.
(2) BQA package only.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 7 | V |
| $V_I$ | Input voltage range[2] | | -0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | Output voltage range[2] | | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V | | ±20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V | | ±50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±50 | mA |
| | Continuous output current through $V_{CC}$ or GND | | | ±200 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2] | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | V |
| $V_I$ | Input Voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output Voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

## 5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC[1] | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $R_{\theta JA}$ | $R_{\theta JC(top)}$ | $R_{\theta JB}$ | $\Psi_{JT}$ | $\Psi_{JB}$ | $R_{\theta JC(bot)}$ | |
| PW (TSSOP) | 14 | 149.8 | 81.6 | 106.0 | 23.5 | 104.7 | N/A | °C/W |
| BQA (WQFN) | 14 | 95.2 | 106.6 | 64.8 | 19.8 | 64.6 | 40.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.


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## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive-going input threshold voltage | 4.5V | 1.28 | 1.54 | 1.83 | V |
| | | 5.5V | 1.46 | 1.72 | 2.02 | V |
| $V_{T-}$ | Negative-going input threshold voltage | 4.5V | 0.65 | 0.91 | 1.2 | V |
| | | 5.5V | 0.71 | 0.99 | 1.29 | V |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ - $V_{T-}$) | 4.5V | 0.51 | | 0.75 | V |
| | | 5.5V | 0.59 | | 0.88 | V |
| $V_{OH}$ | $I_{OH}$ = -50µA | 4.5V | 4.4 | 4.49 | | V |
| | | 5.5V | 5.4 | 5.49 | | |
| | $I_{OH}$ = -24mA | 4.5V | 3.7 | | | |
| | $I_{OH}$ = -24mA | 5.5V | 4.7 | | | |
| | $I_{OH}$ = -75mA(1) | 5.5V | 3.85 | | | |
| $V_{OL}$ | $I_{OL}$ = 50µA | 4.5V | | 0.01 | 0.1 | V |
| | | 5.5V | | 0.01 | 0.1 | |
| | $I_{OL}$ = 24mA | 4.5V | | | 0.5 | |
| | $I_{OL}$ = 24mA | 5.5V | | | 0.5 | |
| | $I_{OL}$ = 75mA(1) | 5.5V | | | 1.65 | |
| $I_I$ | $V_I$ = 5.5V or GND | 0V to 5.5V | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5V | | 0.1 | 2 | µA |
| $\Delta I_{CC}$ | $V_I$ = $V_{CC}$ – 2.1V; Any Input | 4.5V to 5.5V | | | 1.5 | mA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 5V | | 2 | | pF |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms

## 5.6 Switching Characteristics

over operating free-air temperature range; $C_L$ = 50pF typical values measured at $T_A$ = 25°C (unless otherwise noted). See Section 6

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $t_{pd}$ | A or B | Y | 1.5V | | 16.6 | 27.3 | ns |
| | | | 3.3V ± 0.3V | | 6.8 | 10.5 | ns |
| | | | 5V ± 0.5V | | 5.1 | 7.8 | ns |
| | | | 6V | | 4.5 | 6.7 | ns |
| $t_{sk(o)}$ | | Y | 1.5V | | 0.5 | 1.1 | ns |
| | | | 6V | | 0.1 | 0.2 | ns |
| $C_{PD}$ (1) | Any | | 5V | | 15 | | pF |

(1) Power dissipation capacitance is calculated using the method described in CMOS Power Consumption and Cpd Calculation.

## 5.7 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

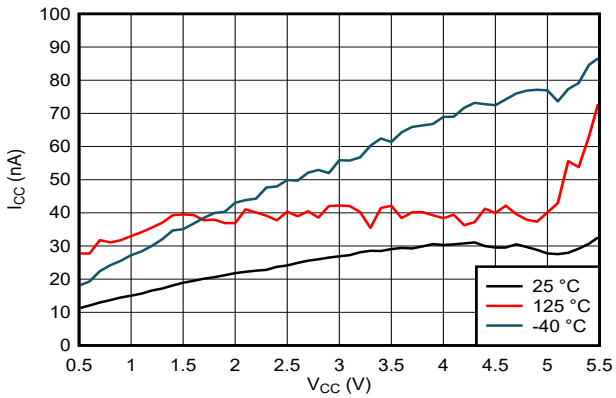


**Figure 5-1. Supply Current Across Supply Voltage**

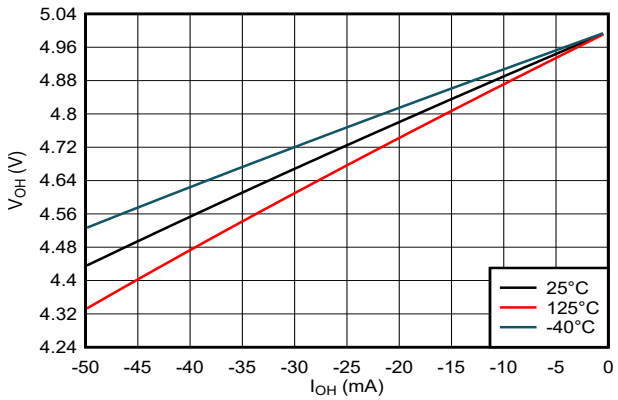


**Figure 5-2. Output Voltage vs Current in HIGH State; 5V Supply**

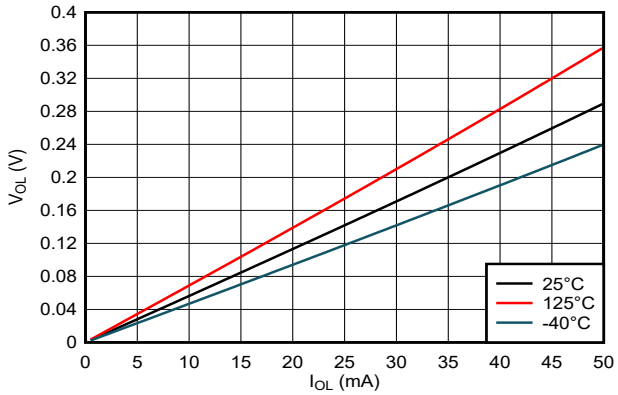


**Figure 5-3. Output Voltage vs Current in LOW State; 5V Supply**


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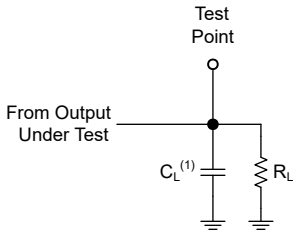
## 6 Parameter Measurement Information

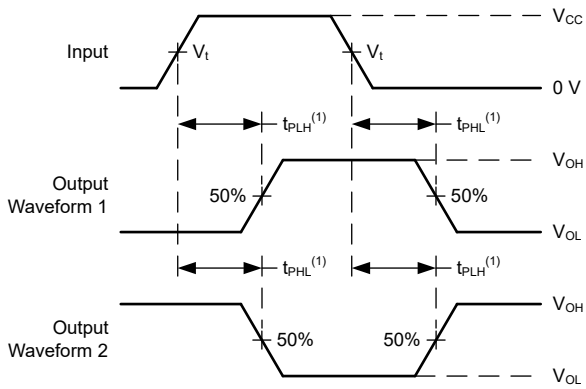
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O$ = 50Ω, $t_t$ < 2.5ns, $V_t$ = 1.5V. For push-pull outputs, $R_L$ = 500Ω.

The outputs are measured individually with one input transition per measurement.



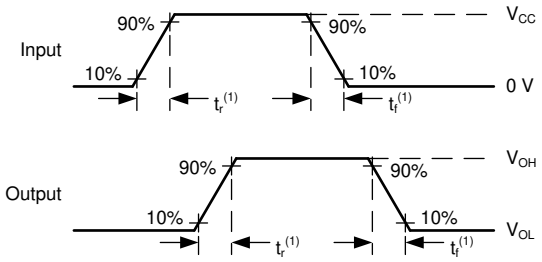

(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Push-Pull Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**Figure 6-2. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

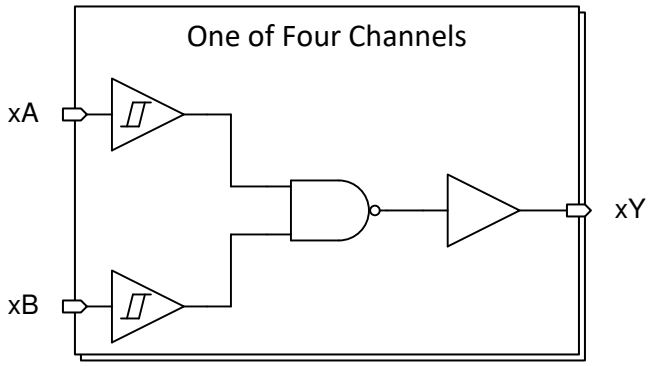
**Figure 6-3. Voltage Waveforms, Input and Output Transition Times**

# 7 Detailed Description

## 7.1 Overview

This device contains four independent 2-input NAND gates with Schmitt-trigger input architecture. Each gate performs the Boolean function $Y = \overline{A \bullet B}$ in positive logic.

## 7.2 Functional Block Diagram





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## 7.3 Feature Description

### *7.3.1 Balanced CMOS Push-Pull Outputs*

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

### *7.3.2 TTL-Compatible Schmitt-Trigger CMOS Inputs*

This device includes TTL-compatible CMOS inputs with Schmitt-trigger architecture. These inputs are specifically designed to interface with TTL logic devices by having reduced input voltage thresholds.

TTL-compatible Schmitt-trigger CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a 10kΩ resistor is recommended and will typically meet all requirements.

### *7.3.3 Clamp Diode Structure*

As shown in Figure 7-1, the inputs and outputs to this device have both positive and negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

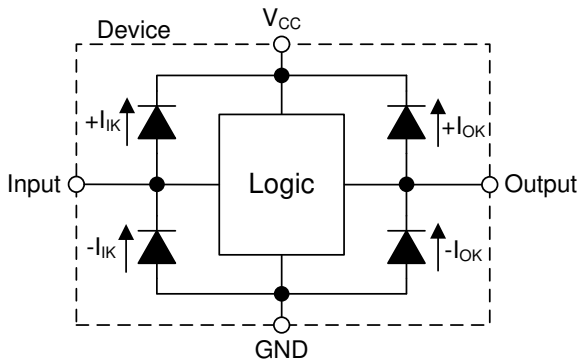


**Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output**

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | H | L |
| L | X | H |
| X | L | H |


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

In this application, two 2-input NAND gates are used to create an active-low SR latch as shown in Figure 8-1. The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The SN74ACT132 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the $\overline{R}$ input which returns the Q output back to LOW.

The inputs of this active-low SR latch can often be driven by open-drain outputs which can produce slow input transition rates when they transition from LOW to Hi-Z. This makes the SN74ACT132 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

## 8.2 Typical Application

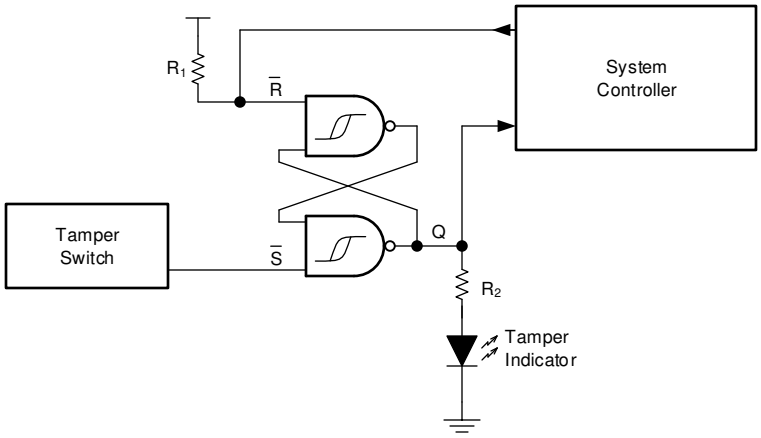


**Figure 8-1. Typical Application Block Diagram**

### 8.2.1 Design Requirements

#### 8.2.1.1 Power Considerations

Ensure that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics of the device, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74ACT132 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74ACT132 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74ACT132 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74ACT132 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74ACT132 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.


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Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74ACT132 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

### 8.2.3 Application Curves

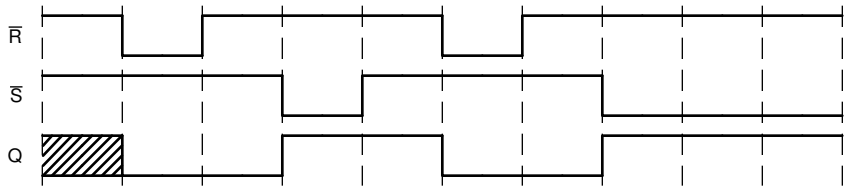


**Figure 8-2. Application Timing Diagram**


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## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.4 Layout

### *8.4.1 Layout Guidelines*

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

### *8.4.2 Layout Example*

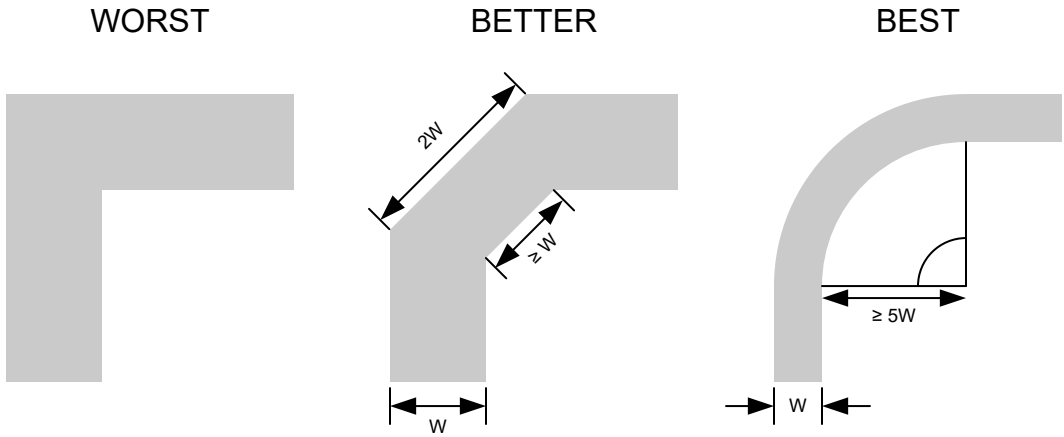


**Figure 8-3. Example Trace Corners for Improved Signal Integrity**

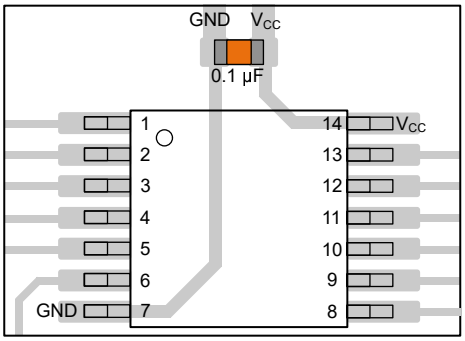


**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

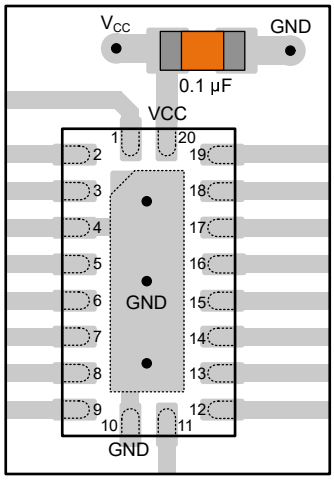


**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**

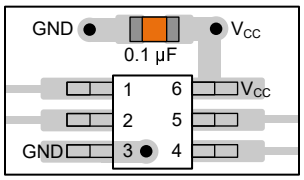


**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

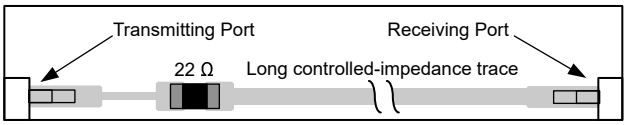


**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**


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# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| November 2025 | * | Initial Release |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74ACT132BQAR | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ACT132 |
| SN74ACT132PWR | Active | Production | TSSOP (PW) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ACT132 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74ACT132 :**

- Automotive : SN74ACT132-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# GENERIC PACKAGE VIEW

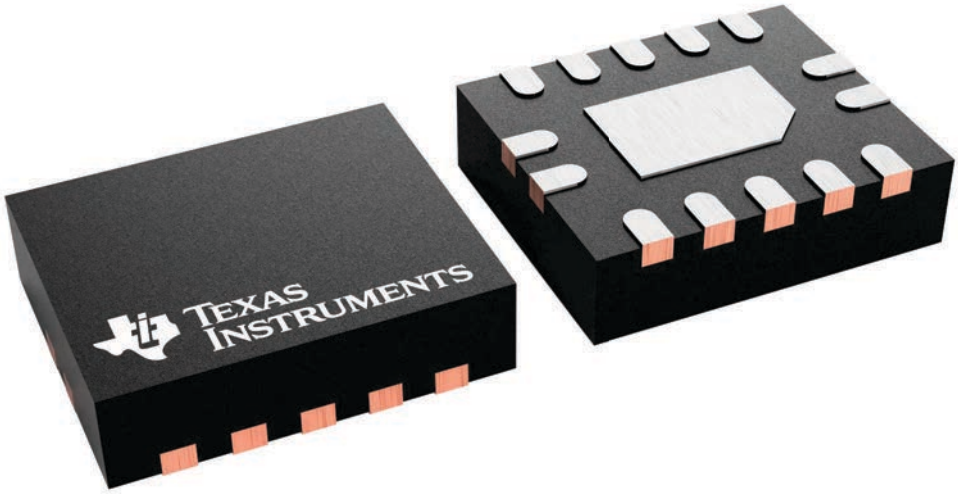
## BQA 14

## WQFN - 0.8 mm max height

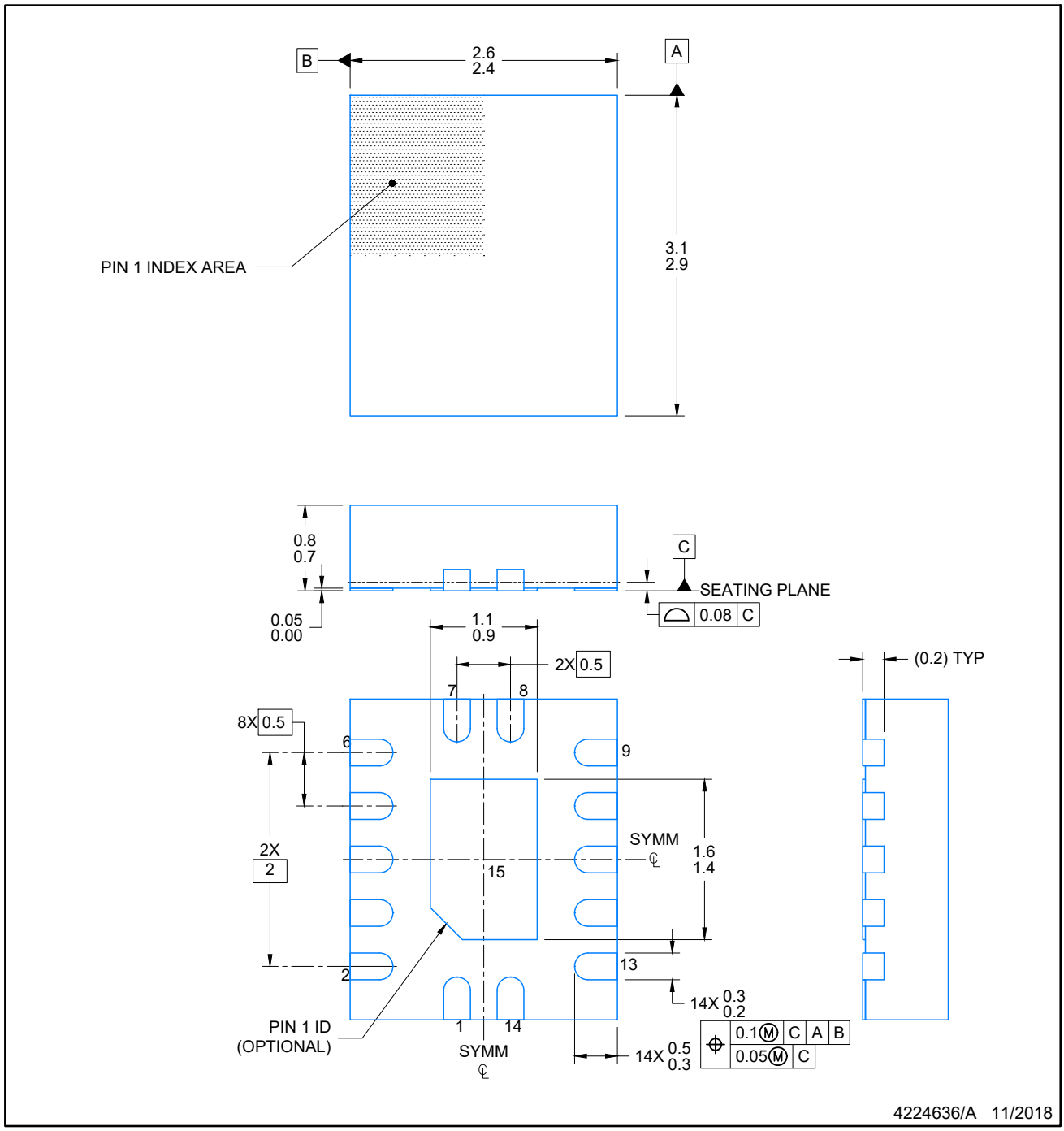
**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

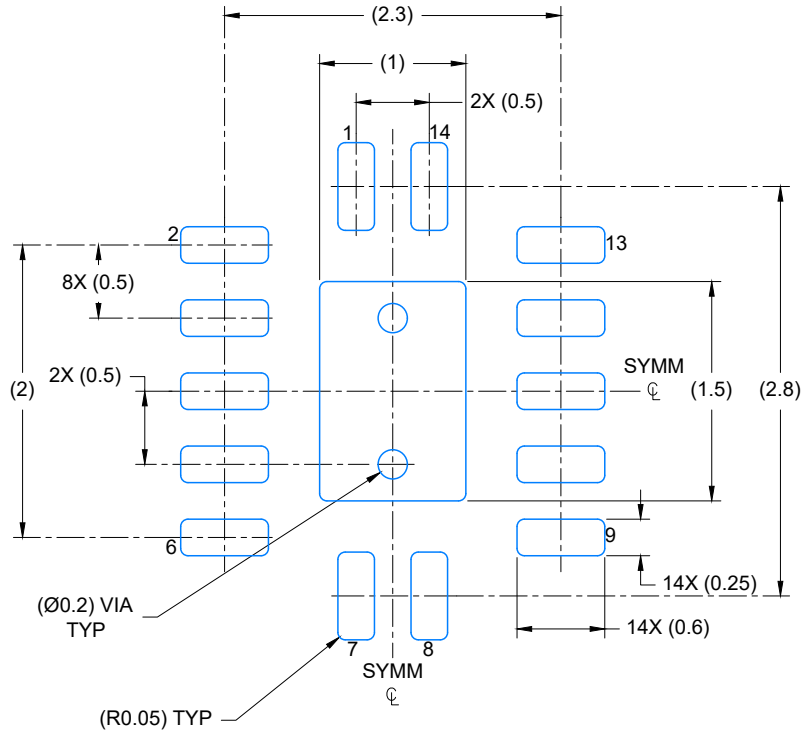



4227145/A

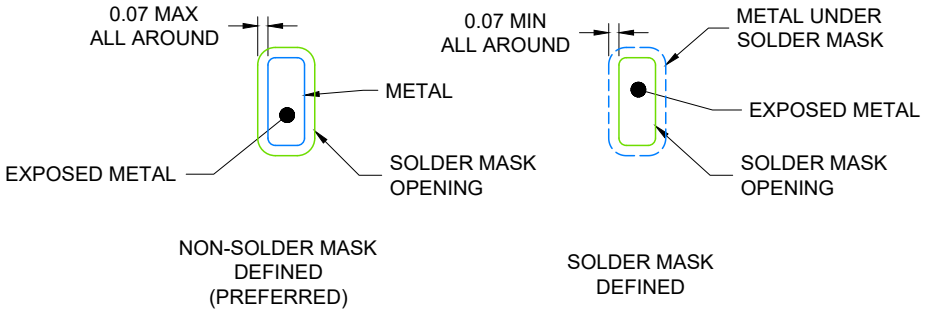



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



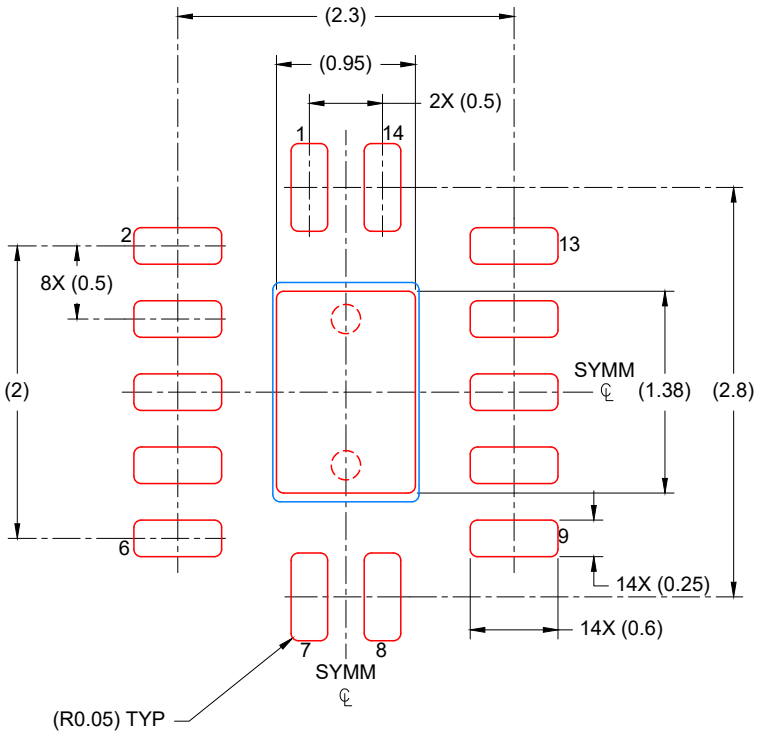

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

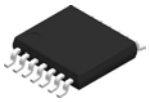
EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

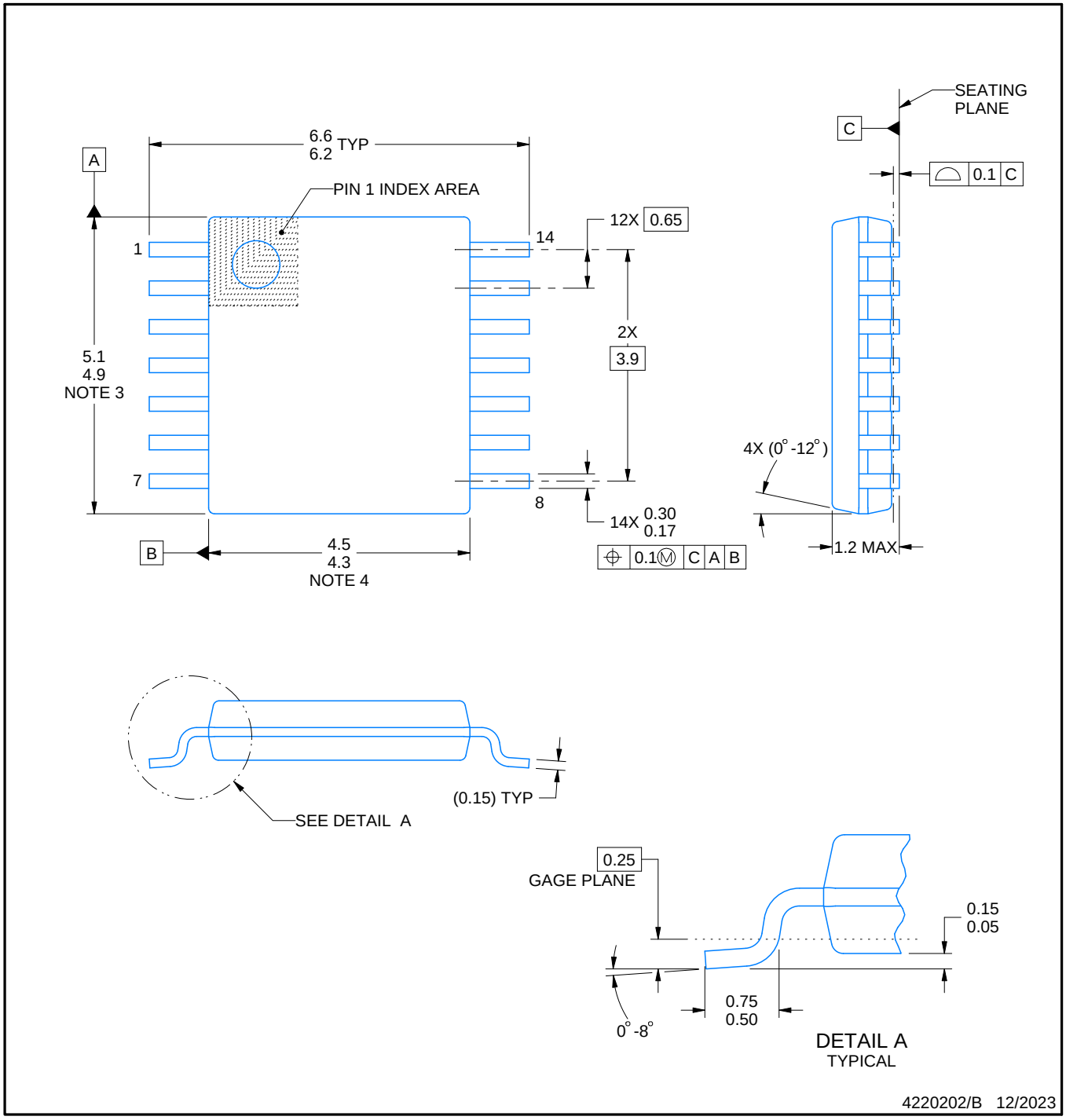
# PW0014A



# PACKAGE OUTLINE

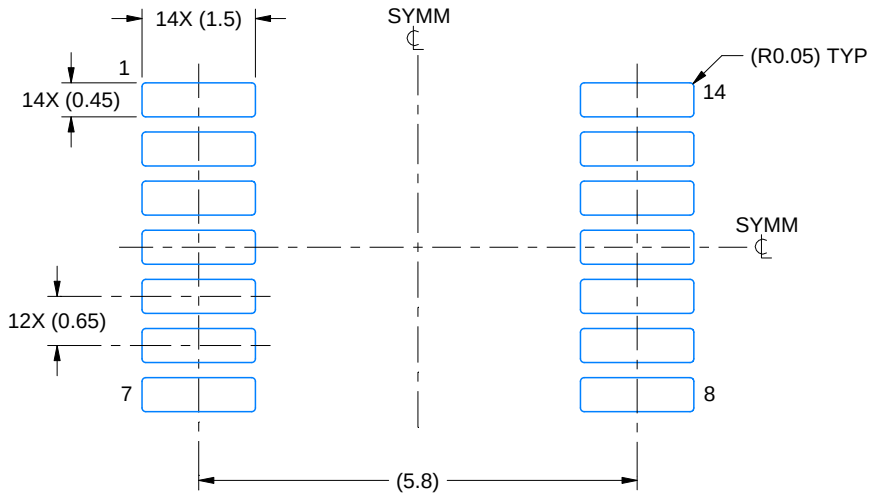
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

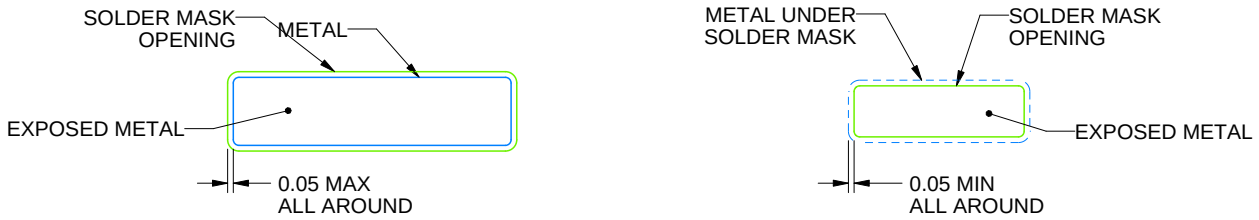



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK DEFINED (PREFERRED)

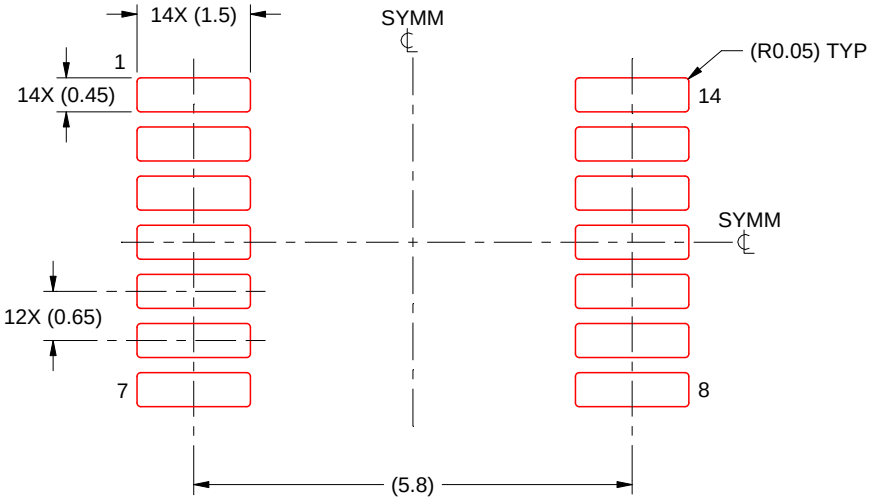
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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