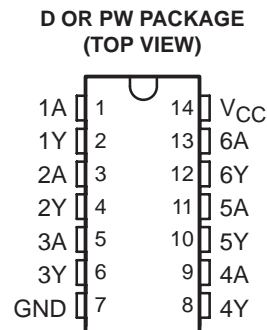


- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V_{CC}**
- **ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 150 V Using Machine Model (C = 200 pF, R = 0)**



† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description/ordering information

The SN74AHC04 contains six independent inverters. This device performs the Boolean function $Y = \bar{A}$.

ORDERING INFORMATION

| T _A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| –55°C to 125°C | SOIC – D | Tape and reel | SN74AHC04MDREP | AHC04MEP |
| | TSSOP – PW | Tape and reel | SN74AHC04MPWREP | AHC04EP |

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |



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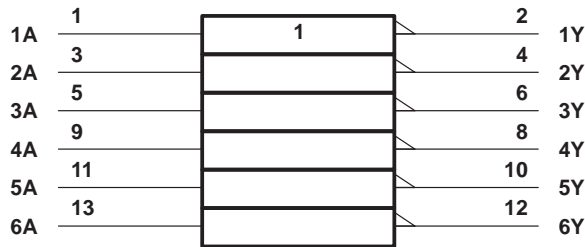
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SN74AHC04-EP
HEX INVERTER

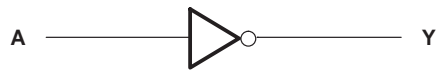
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|------------------------------------------------------------------|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | | MIN | MAX | UNIT |
|---------------------|------------------------------------|------------------------------------------|------|----------|--------------------|
| V_{CC} | Supply voltage | | 2 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | | V |
| | | $V_{CC} = 3\text{ V}$ | 2.1 | | |
| | | $V_{CC} = 5.5\text{ V}$ | 3.85 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | | 0.5 | V |
| | | $V_{CC} = 3\text{ V}$ | | 0.9 | |
| | | $V_{CC} = 5.5\text{ V}$ | | 1.65 | |
| V_I | Input voltage | | 0 | 5.5 | V |
| V_O | Output voltage | | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2\text{ V}$ | | -50 | μA |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | -4 | mA |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | -8 | |
| I_{OL} | Low-level output current | $V_{CC} = 2\text{ V}$ | | 50 | μA |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 4 | mA |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 100 | ns/V |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | 20 | |
| T_A | Operating free-air temperature | | -55 | 125 | $^{\circ}\text{C}$ |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AHC04-EP HEX INVERTER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-----------------|-------------------------------------------------------------|-----------------|-----------------------|-----|------|------|-----|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = -50 µA | 2 V | 1.9 | 2 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | | 2.48 | | |
| | I _{OH} = -8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| V _{OL} | I _{OL} = 50 µA | 2 V | | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | I _{OL} = 4 mA | 3 V | | | 0.36 | | 0.5 | |
| | I _{OL} = 8 mA | 4.5 V | | | 0.36 | | 0.5 | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | µA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | | 20 | µA |
| C _i | V _I = V _{CC} or GND | 5 V | | 2 | 10 | | | pF |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|------|-----|------|------|
| | | | | MIN | TYP | MAX | | | |
| t _{PLH} | A | Y | C _L = 15 pF | | 5 | 8.9 | 1 | 10.5 | ns |
| t _{PHL} | | | | | 5 | 8.9 | 1 | 10.5 | |
| t _{PLH} | A | Y | C _L = 50 pF | | 7.5 | 11.4 | 1 | 13 | ns |
| t _{PHL} | | | | | 7.5 | 11.4 | 1 | 13 | |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|-----|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t _{PLH} | A | Y | C _L = 15 pF | | 3.8 | 5.5 | 1 | 6.5 | ns |
| t _{PHL} | | | | | 3.8 | 5.5 | 1 | 6.5 | |
| t _{PLH} | A | Y | C _L = 50 pF | | 5.3 | 7.5 | 1 | 8.5 | ns |
| t _{PHL} | | | | | 5.3 | 7.5 | 1 | 8.5 | |

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------------------------|-----|------|-----|------|
| V _{OL(P)} | Quiet output, maximum dynamic V _{OL} | | 0.4 | | V |
| V _{OL(V)} | Quiet output, minimum dynamic V _{OL} | | -0.4 | | V |
| V _{OH(V)} | Quiet output, minimum dynamic V _{OH} | | 4.8 | | V |
| V _{IH(D)} | High-level dynamic input voltage | | 3.5 | | V |
| V _{IL(D)} | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are for surface-mount packages only.

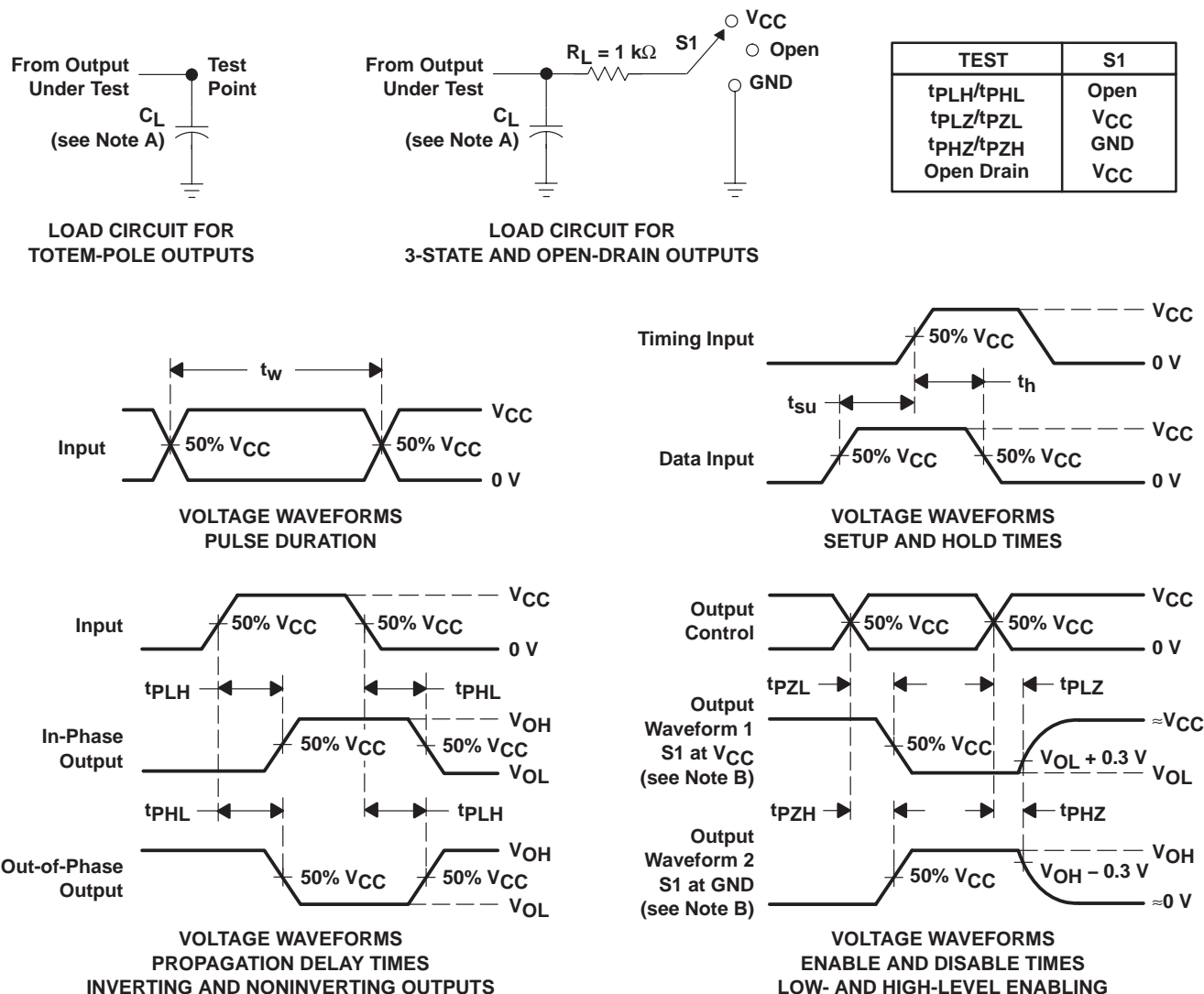


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operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|----------------------------------------|-----------------------------|-----|------|
| C_{pd} Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 12 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74AHC04MDREP | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC04MEP |
| SN74AHC04MDREP.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC04MEP |
| SN74AHC04MPWREP | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC04EP |
| SN74AHC04MPWREP.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC04EP |
| V62/03646-01XE | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC04EP |
| V62/03646-01YE | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AHC04MEP |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AHC04-EP :

- Catalog : [SN74AHC04](#)
- Automotive : [SN74AHC04-Q1](#)
- Military : [SN54AHC04](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC04MDREP | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHC04MPWREP | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC04MDREP | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74AHC04MPWREP | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

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