SCLS332F - MARCH 1996 - REVISED JANUARY 2000

- Members of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'AHC16541 devices are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

SN54AHC16541 . . . WD PACKAGE SN74AHC16541 . . . DGG, DGV, OR DL PACKAGE (TOP VIEW)

			П		1
1 0E 1	[]1		\cup	48	1 0 E2
1Y1	Q_2	2		47] 1A1
1Y2	Qз	3		46	1A2
GND	\mathbb{Q}_4	ļ		45	GND
1Y3	Q 5	,			1A3
1Y4	[]6	6] 1A4
V_{CC}					$]v_{cc}$
1Y5					1A5
1Y6)			1A6
GND	_	0			GND
1Y7		•			1A7
1Y8	_			37	1A8
2Y1	<u>]</u> 1	3			2A1
2Y2	_			35	2A2
GND	_				GND
2Y3	<u>]</u> 1	6			2A3
2Y4	<u>]</u> 1	7			2A4
V_{CC}					v_{cc}
2Y5	_				2A5
2Y6	_				2A6
GND	_				GND
2Y7	_				2A7
2Y8	<u>]</u> 2	23		26	2 <u>A8</u>
2OE1	$\frac{1}{2}$	24		25	2 0 E2

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC16541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC16541 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 8-bit buffer/driver)

	INPUTS		ОИТРИТ
OE1	OE2	Y	
L	L	L	L
L	L	Н	Н
Н	X	Χ	Z
Х	Н	Χ	Z

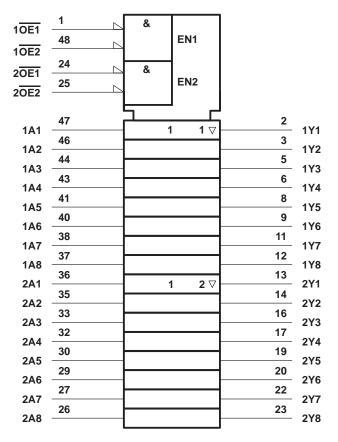


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

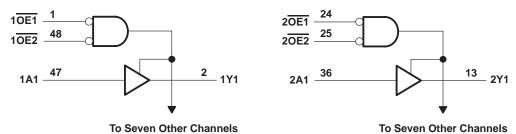


logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCLS332F - MARCH 1996 - REVISED JANUARY 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}		0	.5 V to 7 V
Input voltage range, V _I (see Note 1)		0	.5 V to 7 V
Output voltage range, VO (see Note 1)		–0.5 V to V	CC + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)			–20 mA
Output clamp current, IOK (VO < 0 or VO > VO	cc)		±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CO}	;)		±25 mA
Continuous current through each V _{CC} or GNI	D		±75 mA
Package thermal impedance, θ_{JA} (see Note 2	2): DGG package	9	70°C/W
	DGV package)	58°C/W
	DL package		63°C/W
Storage temperature range, T _{sto}			C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

			SN54AH	C16541	SN74AH0	C16541	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2	5.5	2	5.5	V
		V _{CC} = 2 V	1.5		1.5		
VIH	High-level input voltage	V _{CC} = 3 V	2.1		2.1		V
		V _{CC} = 5.5 V	3.85		3.85		
		V _{CC} = 2 V		0.5		0.5	
VIL	Low-level input voltage	V _{CC} = 3 V		0.9		0.9	V
		V _{CC} = 5.5 V		1.65		1.65	1
٧ı	Input voltage	-	0.0	5.5	0	5.5	V
٧o	Output voltage		.0	Vcc	0	Vcc	V
		V _{CC} = 2 V	20	-50		- 50	μΑ
ЮН	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	8	-4		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8		-8	mA
		V _{CC} = 2 V		50		50	μΑ
lOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4		4	A
		$V_{CC} = 5 V \pm 0.5 V$		8		8	mA
44/4		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100		100	//
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20		20	ns/V
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

SN54AHC16541, SN74AHC16541 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS332F - MARCH 1996 - REVISED JANUARY 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	Vaa	T,	ղ = 25°C	;	SN54AH0	C16541	SN74AHC	16541	LINUT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		2 V	1.9	2		1.9		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		2.9		
Voн		4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8	N.	3.8		
		2 V			0.1		0.1		0.1	
	I _{OL} = 50 μA	3 V			0.1	Ġ	0.1		0.1	
V _{OL}		4.5 V			0.1	6	0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36	70	0.5		0.44	
	I _{OL} = 8 mA	4.5 V			0.36	06	0.5		0.44	
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1	Q	±1*		±1	μΑ
loz	$V_O = V_{CC}$ or GND, $V_I (\overline{OE}) = V_{IL}$ or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μΑ
C _i	V _I = V _{CC} or GND	5 V		2	10				10	pF
Co	$V_O = V_{CC}$ or GND	5 V		3						pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	Δ = 25°(C	SN54AH	C16541	SN74AH0	16541	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	А	Y	C ₁ = 15 pF		5**	8.4**	1**	10**	1	10	ns
t _{PHL}	^	'	C[= 15 μΓ		5**	8.4**	1**	10**	1	10	115
^t PZH	ŌĒ	Y	C 15 pE		6**	10.6**	1**	12.5**	1	12.5	ns
t _{PZL}	OE	<u>'</u>	C _L = 15 pF		6**	10.6**	1**	12.5**	1	12.5	115
t _{PHZ}	ŌĒ	Y	C: 15 pF		7**	11.5**	1**	12.5**	1	12.5	
t _{PLZ}	OE	<u>'</u>	C _L = 15 pF		7**	11.5**	1**	12.5**	1	12.5	ns
t _{PLH}	А	Y	C _I = 50 pF		7.5	11.9	1	13.5	1	13.5	no
t _{PHL}	A	<u>'</u>	CL = 50 pr		7.5	11.9	25	13.5	1	13.5	ns
^t PZH	ŌĒ	Y	C ₁ = 50 pF		8	14.1	0 1	16	1	16	ns
tPZL	OE	1	CL = 50 pr		8	14.1	Q 1	16	1	16	115
t _{PHZ}	ŌĒ	Y	C: - 50 pF		9	14	1	16	1	16	no
tPLZ	OE	l r	C _L = 50 pF		9	14	1	16	1	16	ns
^t sk(o)			C _L = 50 pF			1.5***		·		1.5	ns

 $^{^{\}star\star}$ On products compliant to MIL-PRF-38535, this parameter is not production tested.



^{***} On products compliant to MIL-PRF-38535, this parameter does not apply.

SCLS332F - MARCH 1996 - REVISED JANUARY 2000

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	TA	√ = 25°C	;	SN54AH0	C16541	SN74AHC	16541	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
t _{PLH}	Α	Y	C _I = 15 pF		3.5*	6*	1*	7*	1	6.5	ns
t _{PHL}	ζ.	'	CL = 13 pr		3.5*	6*	1*	7*	1	6.5	115
^t PZH	ŌĒ	Y	C _L = 15 pF		4.7*	7.3*	1*	8.5*	1	8.5	ns
tPZL	OE	'	GL = 13 pr		4.7*	7.3*	1*	8.5*	1	8.5	115
^t PHZ	ŌĒ	Y	C: -15 pE		5*	7.2*	1*	8.5*	1	8.5	ns
t _{PLZ}	OE	'	C _L = 15 pF		5*	7.2*	1* 4	8.5*	1	8.5	115
tPLH	Α	Y	C ₁ = 50 pF		5	8	1	9	1	8.5	ns
t _{PHL}	ζ.	'	CL = 30 pr		5	8	251	9	1	8.5	115
^t PZH	ŌĒ	Y	C _I = 50 pF		6.2	9.3	0 1	10.5	1	10.5	ns
t _{PZL}	OE	'	CL = 30 pr		6.2	9.3	2 1	10.5	1	10.5	115
t _{PHZ}	ŌĒ	Y	C _L = 50 pF		6	9.2	1	10.5	1	10.5	ns
tPLZ	OE	ſ	GL = 50 pr		6	9.2	1	10.5	1	10.5	115
tsk(o)		·	C _L = 50 pF			1**				1	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^{\circ}\text{C}$ (see Note 4)

	PARAMETER	SN74	541	UNIT	
	FARAWETER	MIN	TYP	MAX	ONIT
V _{OL(P)}	Quiet output, maximum dynamic VOL		0.7		V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.3		V
VOH(V)	Quiet output, minimum dynamic VOH		4.7		V
VIH(D)	High-level dynamic input voltage	3.5			V
V _{IL(D)}	Low-level dynamic input voltage			1.5	V

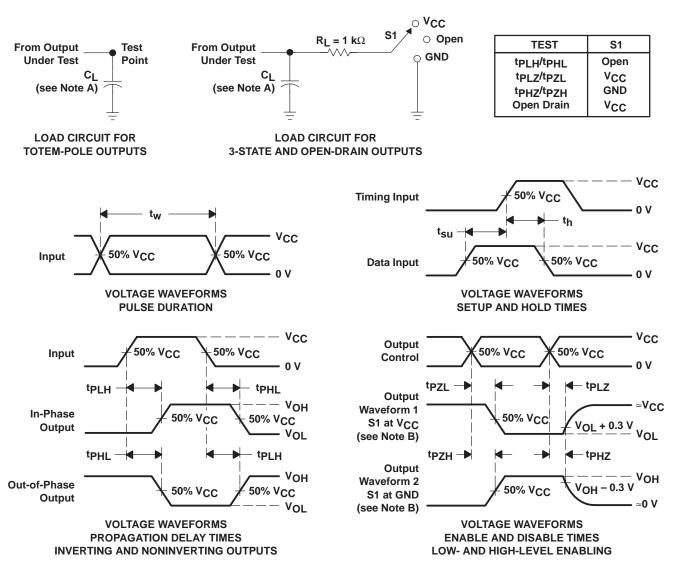
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER				
C _{pd} Power dissipation capa	citance	No load,	f = 1 MHz	12	pF

^{**} On products compliant to MIL-PRF-38535, this parameter does not apply.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AHC16541DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16541
SN74AHC16541DGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16541
SN74AHC16541DGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE541
SN74AHC16541DGVR.A	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HE541
SN74AHC16541DL	Obsolete	Production	SSOP (DL) 48	-	-	Call TI	Call TI	-40 to 85	AHC16541
SN74AHC16541DLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16541
SN74AHC16541DLR.A	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC16541

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

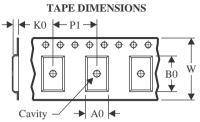
www.ti.com 11-Nov-2025

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC16541DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AHC16541DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74AHC16541DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

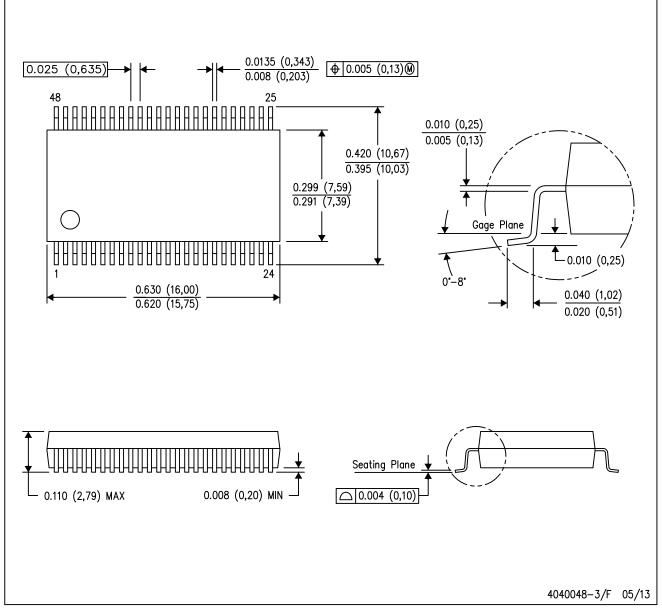


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC16541DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74AHC16541DGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74AHC16541DLR	SSOP	DL	48	1000	356.0	356.0	53.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025