

# SN74AUCH16244

## 16-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCES391E – MARCH 2002 – REVISED DECEMBER 2002

- Member of the Texas Instruments Widebus™ Family
- Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max  $t_{pd}$  of 1.8 ns at 1.8 V
- Low Power Consumption, 20- $\mu$ A Max  $I_{CC}$
- $\pm 8$ -mA Output Drive at 1.8 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description/ordering information

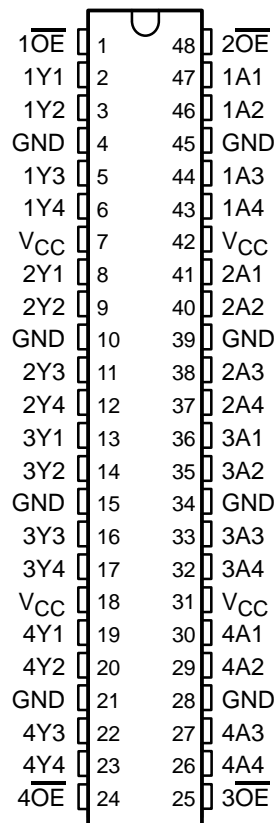
This 16-bit buffer/driver is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUCH16244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### DGG OR DGV PACKAGE (TOP VIEW)



#### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AUCH16244DGGR	AUCH16244
	TVSOP – DGV	Tape and reel	SN74AUCH16244DGV	MJ244
	VFBGA – GQL	Tape and reel	SN74AUCH16244GQLR	MJ244

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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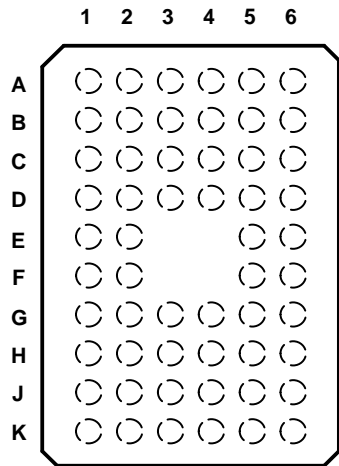
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description/ordering information (continued)

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

GQL PACKAGE  
(TOP VIEW)



terminal assignments

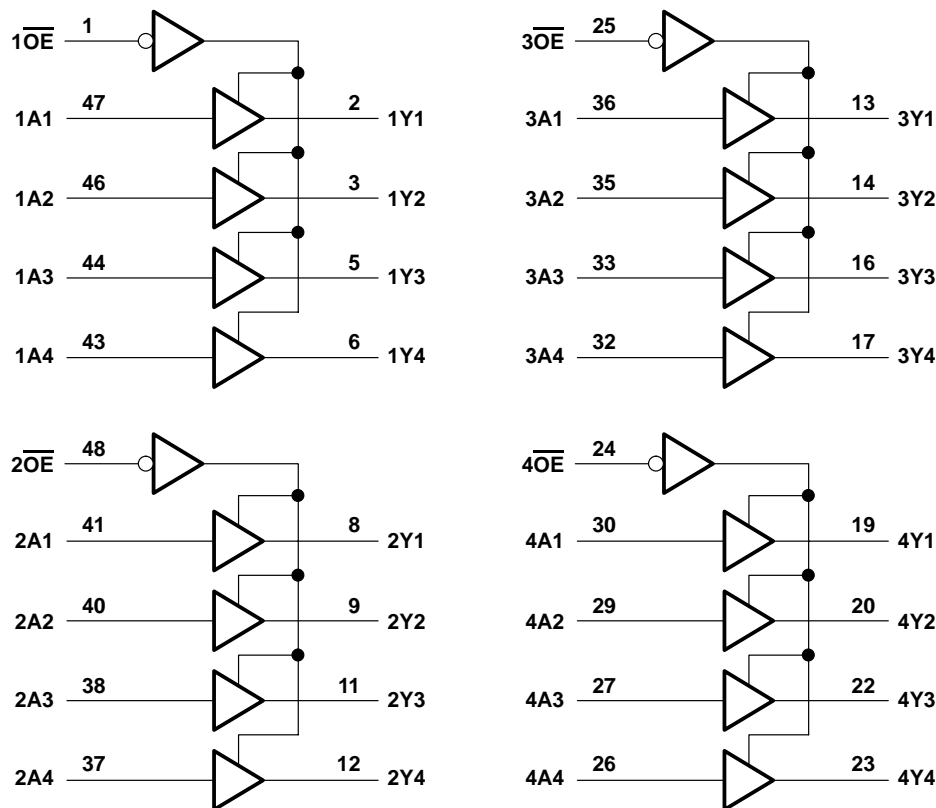
	1	2	3	4	5	6
A	1 $\overline{\text{OE}}$	NC	NC	NC	NC	2 $\overline{\text{OE}}$
B	1Y2	1Y1	GND	GND	1A1	1A2
C	1Y4	1Y3	V <sub>CC</sub>	V <sub>CC</sub>	1A3	1A4
D	2Y2	2Y1	GND	GND	2A1	2A2
E	2Y4	2Y3			2A3	2A4
F	3Y1	3Y2			3A2	3A1
G	3Y3	3Y4	GND	GND	3A4	3A3
H	4Y1	4Y2	V <sub>CC</sub>	V <sub>CC</sub>	4A2	4A1
J	4Y3	4Y4	GND	GND	4A4	4A3
K	4 $\overline{\text{OE}}$	NC	NC	NC	NC	3 $\overline{\text{OE}}$

NC – No internal connection

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT Y
$\overline{\text{OE}}$	A	
L	H	H
L	L	L
H	X	Z

**logic diagram (positive logic)**



Pin numbers shown are for the DGG and DGV packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 3.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 3.6 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±20 mA
Continuous current through $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	70°C/W
DGV package	58°C/W
GQL package	42°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

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## 16-BIT BUFFER/DRIVER

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#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	0.8	2.7	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8\text{ V}$	$V_{CC}$	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 0.8\text{ V}$	–0.7	mA
		$V_{CC} = 1.1\text{ V}$	–3	
		$V_{CC} = 1.4\text{ V}$	–5	
		$V_{CC} = 1.65\text{ V}$	–8	
		$V_{CC} = 2.3\text{ V}$	–9	
$I_{OL}$	Low-level output current	$V_{CC} = 0.8\text{ V}$	0.7	mA
		$V_{CC} = 1.1\text{ V}$	3	
		$V_{CC} = 1.4\text{ V}$	5	
		$V_{CC} = 1.65\text{ V}$	8	
		$V_{CC} = 2.3\text{ V}$	9	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8\text{ V}$	20	ns/V
		$V_{CC} = 1.3\text{ V}$	15	
		$V_{CC} = 1.6\text{ V, }1.95\text{ V, and }2.7\text{ V}$	10	
$T_A$	Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = –100 µA	0.8 V to 2.7 V	V <sub>CC</sub> –0.1			V
		I <sub>OH</sub> = –0.7 mA	0.8 V	0.55			
		I <sub>OH</sub> = –3 mA	1.1 V	0.8			
		I <sub>OH</sub> = –5 mA	1.4 V	1			
		I <sub>OH</sub> = –8 mA	1.65 V	1.2			
		I <sub>OH</sub> = –9 mA	2.3 V	1.8			
V <sub>OL</sub>		I <sub>OL</sub> = 100 µA	0.8 V to 2.7 V	0.2			V
		I <sub>OL</sub> = 0.7 mA	0.8 V	0.25			
		I <sub>OL</sub> = 3 mA	1.1 V	0.3			
		I <sub>OL</sub> = 5 mA	1.4 V	0.4			
		I <sub>OL</sub> = 8 mA	1.65 V	0.45			
		I <sub>OL</sub> = 9 mA	2.3 V	0.6			
I <sub>I</sub>	A or $\overline{OE}$ inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	0 to 2.7 V			±5	µA
I <sub>BHL</sub> ‡		V <sub>I</sub> = 0.35 V	1.1 V	10			µA
		V <sub>I</sub> = 0.47 V	1.4 V	15			
		V <sub>I</sub> = 0.57 V	1.65 V	20			
		V <sub>I</sub> = 0.7 V	2.3 V	40			
I <sub>BHH</sub> §		V <sub>I</sub> = 0.8 V	1.1 V	–10			µA
		V <sub>I</sub> = 0.9 V	1.4 V	–15			
		V <sub>I</sub> = 1.07 V	1.65 V	–20			
		V <sub>I</sub> = 1.7 V	2.3 V	–40			
I <sub>BHLO</sub> ¶		V <sub>I</sub> = 0 to V <sub>CC</sub>	1.3 V	75			µA
			1.6 V	125			
			1.95 V	175			
			2.7 V	275			
I <sub>BHHO</sub> #		V <sub>I</sub> = 0 to V <sub>CC</sub>	1.3 V	–75			µA
			1.6 V	–125			
			1.95 V	–175			
			2.7 V	–275			
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 2.7 V	0			±10	µA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	2.7 V			±10	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	0.8 V to 2.7 V			20	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V		3	4.5	pF
C <sub>o</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	2.5 V		4	7	pF

† All typical values are at T<sub>A</sub> = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.

¶ An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.

# An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.



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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

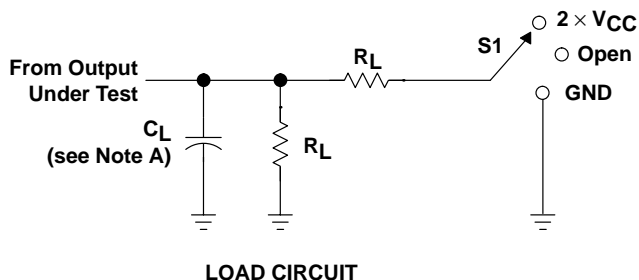
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V			V <sub>CC</sub> = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	5.4	0.8	2.8	0.6	1.9	0.7	1.3	1.8	0.5	1.8	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	8	1	4.4	0.7	2.6	0.8	1.4	2.5	0.6	1.9	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	12	1.9	4.9	1	4.6	1.5	2.6	4	0.5	2	ns

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C <sub>pd</sub> Power dissipation capacitance	Outputs enabled	f = 10 MHz		21	22	23	25	30	pF
	Outputs disabled			1	1	1	1	1	

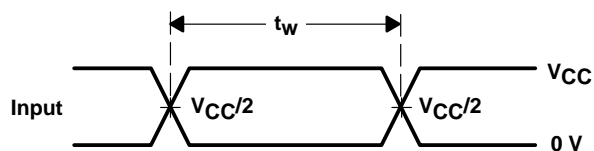


## PARAMETER MEASUREMENT INFORMATION

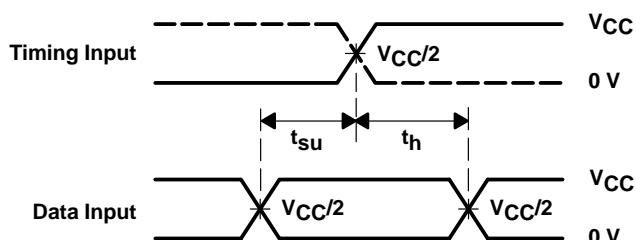


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

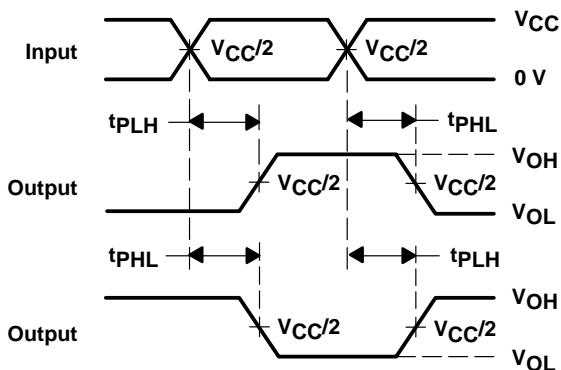
$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



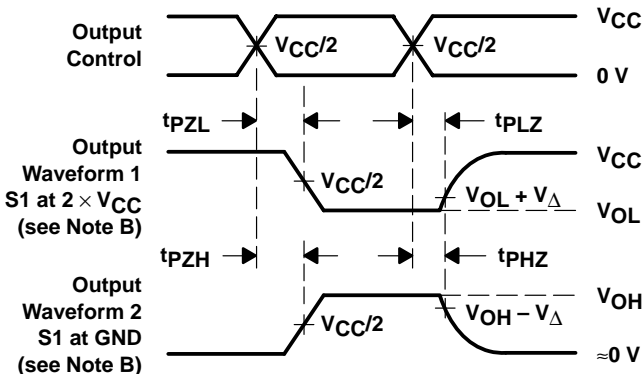
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AUCH16244DGVRG4	Active	Production	TVSOP (DGV)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MJ244
74AUCH16244DGVRG4.B	Active	Production	TVSOP (DGV)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MJ244
<a href="#">SN74AUCH16244DGGR</a>	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AUCH16244
SN74AUCH16244DGGR.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AUCH16244
<a href="#">SN74AUCH16244DGVR</a>	Active	Production	TVSOP (DGV)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MJ244
SN74AUCH16244DGVR.B	Active	Production	TVSOP (DGV)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MJ244

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AUCH16244DGVRG4	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74AUCH16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AUCH16244DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AUCH16244DGVRG4	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74AUCH16244DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74AUCH16244DGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0

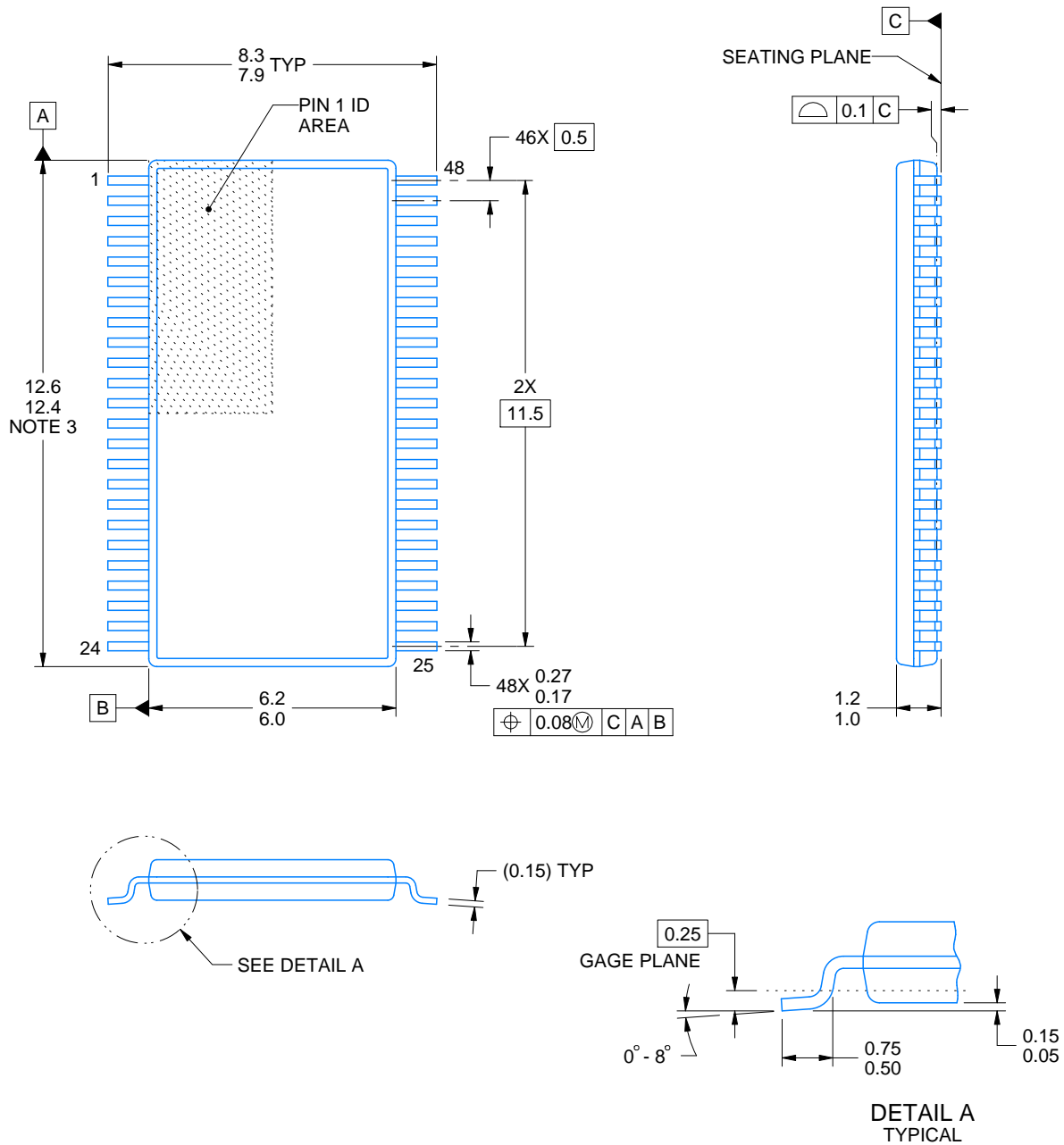
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



4214859/B 11/2020

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

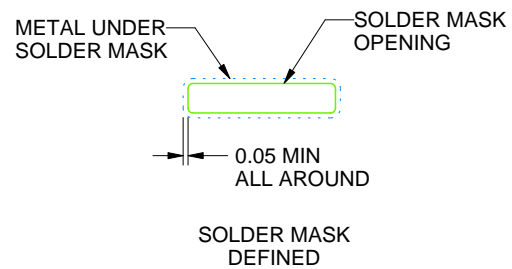
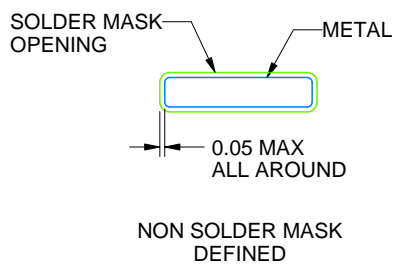
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

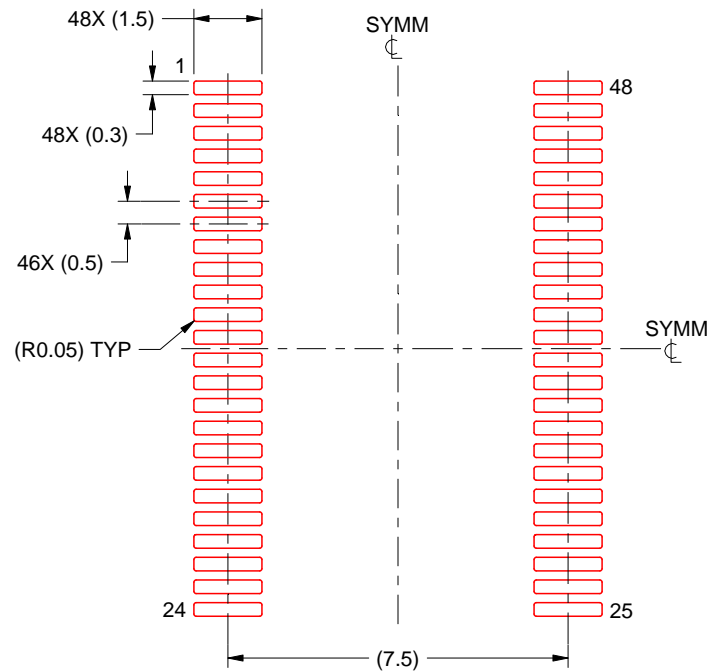
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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Last updated 10/2025