

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- DOC™ (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Less Than 2-ns Maximum Propagation Delay at 2.5-V and 3.3-V  $V_{CC}$
- Dynamic Drive Capability Is Equivalent to Standard Outputs With  $I_{OH}$  and  $I_{OL}$  of  $\pm 24$  mA at 2.5-V  $V_{CC}$
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

## DESCRIPTION

A Dynamic Output Control (DOC™) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

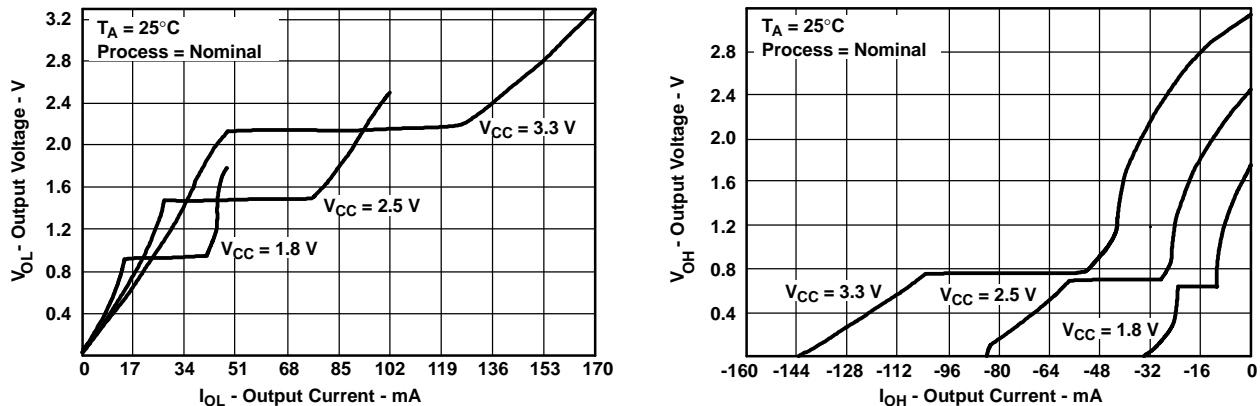


Figure 1. Output Voltage vs Output Current

This 20-bit noninverting buffer/driver is operational at 1.2-V to 3.6-V  $V_{CC}$ , but is designed specifically for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74AVC16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1OE1 and 1OE2 or 2OE1 and 2OE2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16827 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

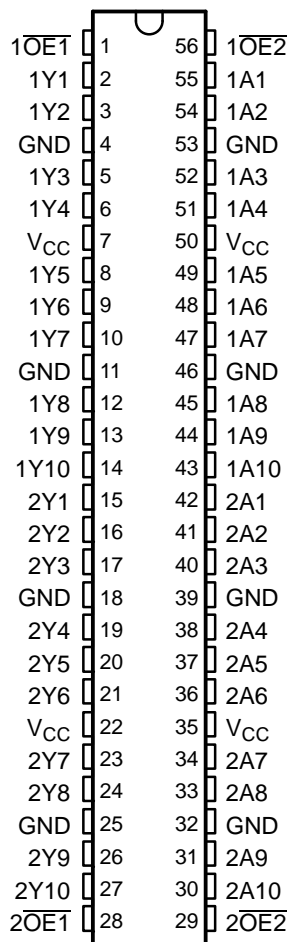


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## TERMINAL ASSIGNMENTS

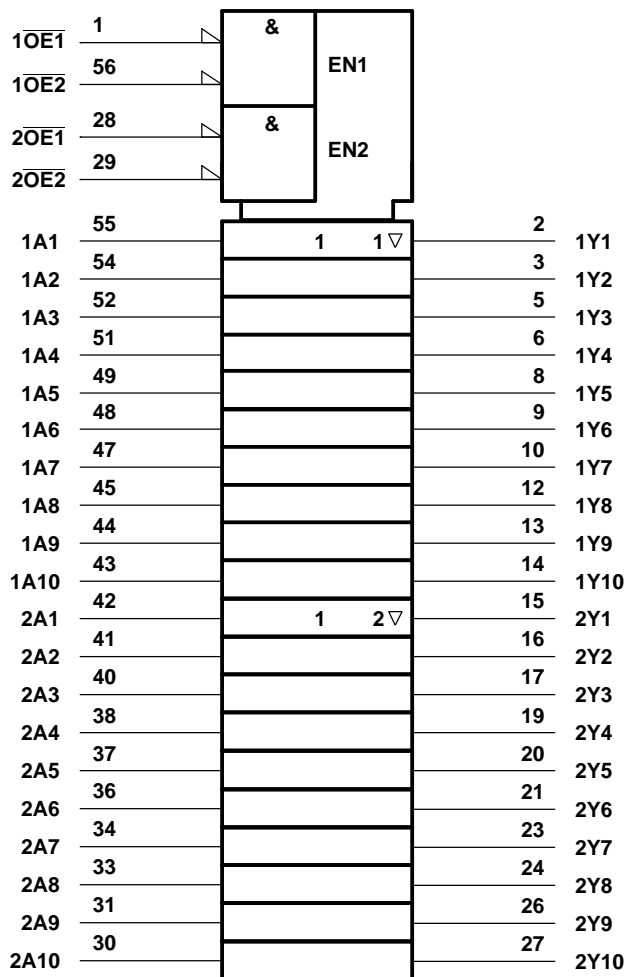
DGG OR DGV PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(EACH 10-BIT BUFFER/DRIVER)

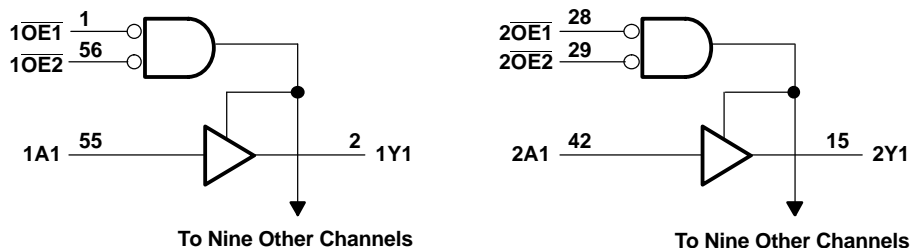
INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

LOGIC SYMBOL<sup>(1)</sup>



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



# SN74AVC16827

## 20-BIT BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCES176I–DECEMBER 1998–REVISED JUNE 2005



#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	4.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	4.6	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through each $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	64	°C/W
		DGV package	48	
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

#### Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	1.2	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.2$ V	$V_{CC}$	V
		$V_{CC} = 1.4$ V to 1.6 V	$0.65 \times V_{CC}$	
		$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	1.7	
		$V_{CC} = 3$ V to 3.6 V	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.2$ V	GND	V
		$V_{CC} = 1.4$ V to 1.6 V	$0.35 \times V_{CC}$	
		$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
		$V_{CC} = 3$ V to 3.6 V	0.8	
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	Active state	0	V
		3-state	0	
$I_{OHS}$	Static high-level output current <sup>(1)</sup>	$V_{CC} = 1.4$ V to 1.6 V	–2	mA
		$V_{CC} = 1.65$ V to 1.95 V	–4	
		$V_{CC} = 2.3$ V to 2.7 V	–8	
		$V_{CC} = 3$ V to 3.6 V	–12	
$I_{OLS}$	Static low-level output current <sup>(1)</sup>	$V_{CC} = 1.4$ V to 1.6 V	2	mA
		$V_{CC} = 1.65$ V to 1.95 V	4	
		$V_{CC} = 2.3$ V to 2.7 V	8	
		$V_{CC} = 3$ V to 3.6 V	12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.4$ V to 3.6 V	5	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

- (1) Dynamic drive capability is equivalent to standard outputs with  $I_{OH}$  and  $I_{OL}$  of ±24 mA at 3.3-V  $V_{CC}$ . See Figure 1 for  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  characteristics. Refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OHS</sub> = –100 µA, V <sub>IH</sub> = V <sub>CC</sub>	1.4 V to 3.6 V	V <sub>CC</sub> – 0.2			V
		I <sub>OHS</sub> = –2 mA, V <sub>IH</sub> = 0.91 V	1.4 V	1.05			
		I <sub>OHS</sub> = –4 mA, V <sub>IH</sub> = 1.07 V	1.65 V	1.2			
		I <sub>OHS</sub> = –8 mA, V <sub>IH</sub> = 1.7 V	2.3 V	1.75			
		I <sub>OHS</sub> = –12 mA, V <sub>IH</sub> = 2 V	3 V	2.3			
V <sub>OL</sub>		I <sub>OLS</sub> = 100 µA	1.4 V to 3.6 V			0.2	V
		I <sub>OLS</sub> = 2 mA, V <sub>IL</sub> = 0.49 V	1.4 V			0.4	
		I <sub>OLS</sub> = 4 mA, V <sub>IL</sub> = 0.57 V	1.65 V			0.45	
		I <sub>OLS</sub> = 8 mA, V <sub>IL</sub> = 0.7 V	2.3 V			0.55	
		I <sub>OLS</sub> = 12 mA, V <sub>IL</sub> = 0.8 V	3 V			0.7	
I <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±2.5	µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0			±10	µA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>IH</sub> = V <sub>CC</sub>	3.6 V			±12.5	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	µA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V	4			pF
			3.3 V	4			
	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V	2.5			
			3.3 V	2.5			
C <sub>O</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	2.5 V	6.5			pF
			3.3 V	6.5			

(1) Typical values are measured at T<sub>A</sub> = 25°C.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2 through Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.2 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			TYP		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	3		0.4	3.2	0.9	2.9	0.8	1.9	0.5	1.7	ns
t <sub>en</sub>	$\overline{OE}$	Y	8.7		2.3	9.1	2.1	8	1.4	5.6	1.2	5.1	ns
t <sub>dis</sub>	$\overline{OE}$	Y	7.5		2.7	8.3	2.5	7.3	0.9	4.9	1	4.7	ns

## Switching Characteristics<sup>(1)</sup>

T<sub>A</sub> = 0°C to 85°C, C<sub>L</sub> = 0 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t <sub>pd</sub>	A	Y	0.09	0.67	ns

(1) Texas Instruments SPICE simulation data

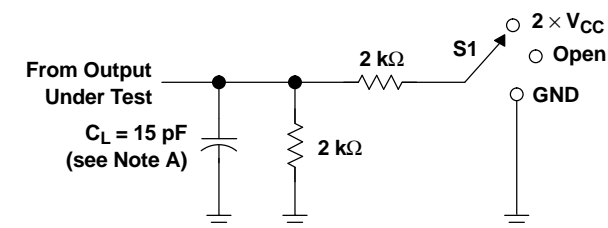
## Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	31	35	40	pF
		Outputs disabled	6	6	6	

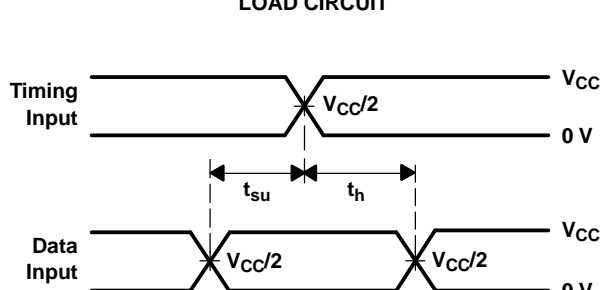
# PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2\text{ V AND } 1.5\text{ V} \pm 0.1\text{ V}$

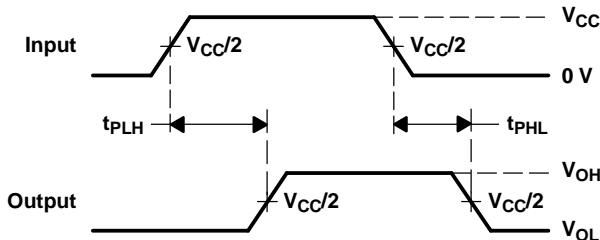


LOAD CIRCUIT

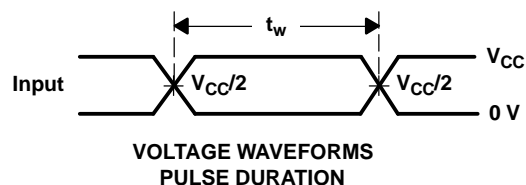
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



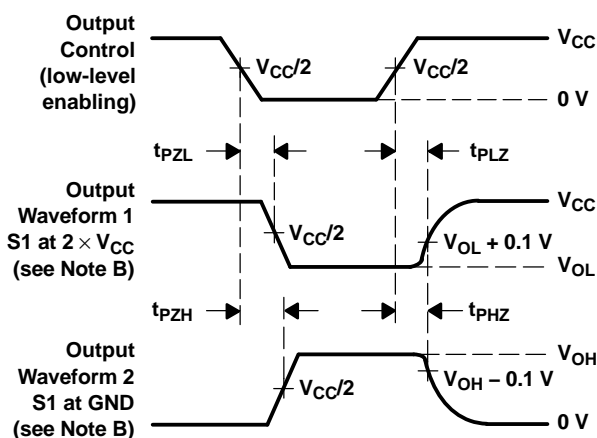
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



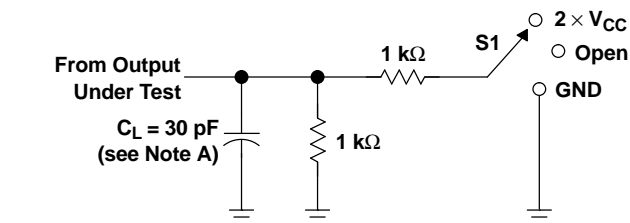
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

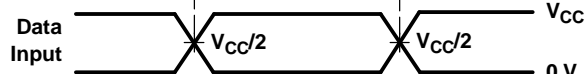
# PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$

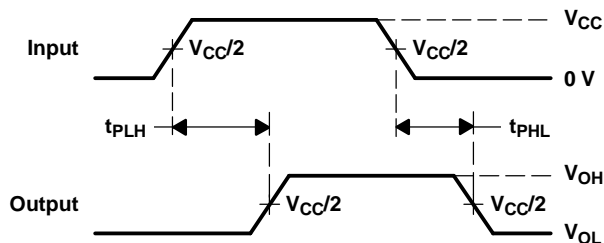


LOAD CIRCUIT

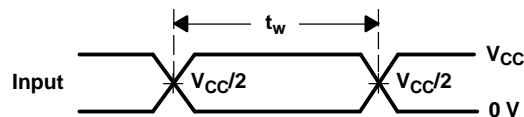
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 × $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



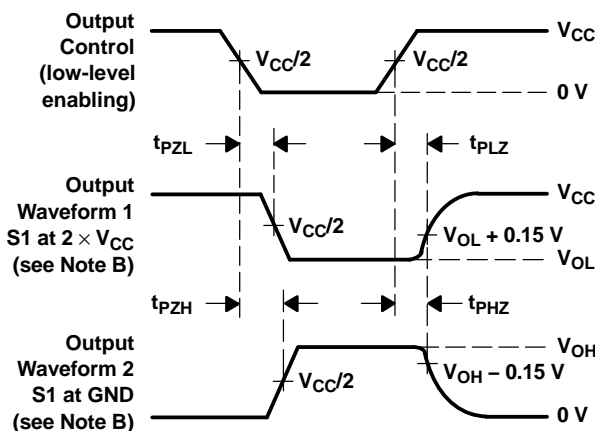
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



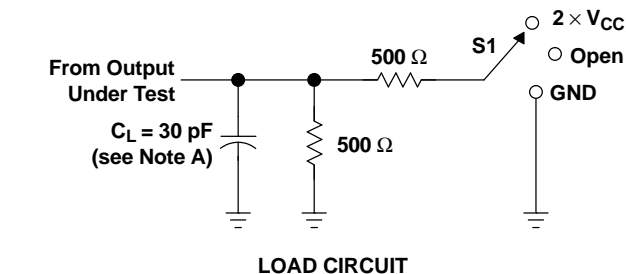
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

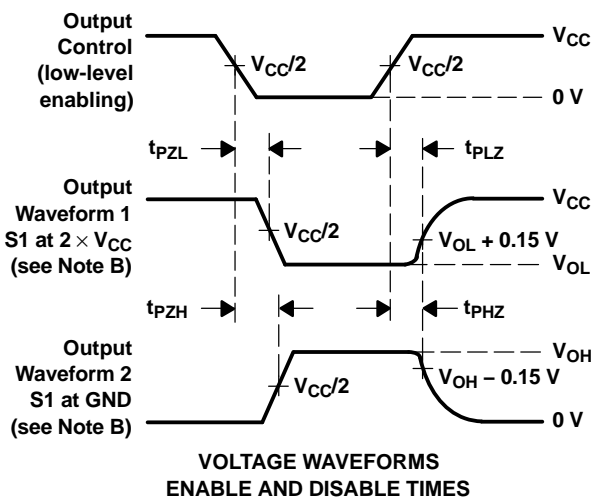
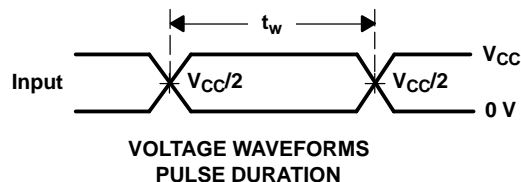
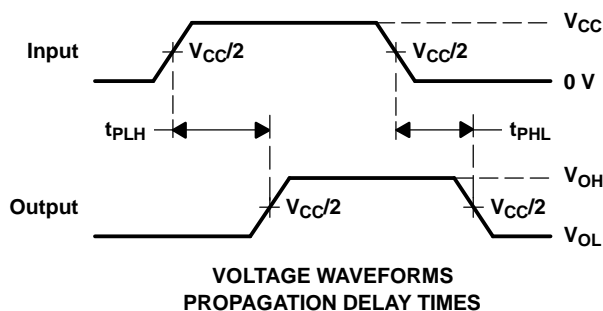
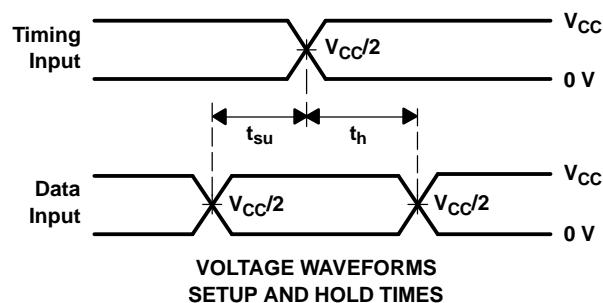
Figure 3. Load Circuit and Voltage Waveforms

# **PARAMETER MEASUREMENT INFORMATION**

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



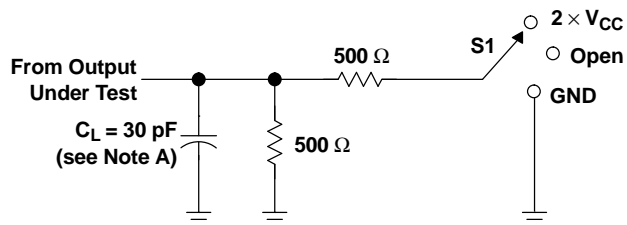
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 4. Load Circuit and Voltage Waveforms**



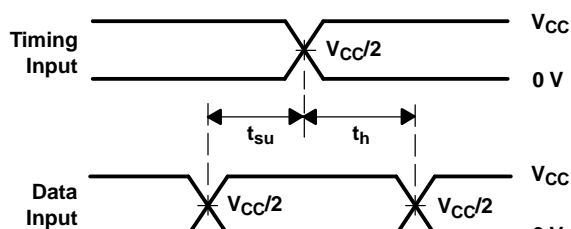
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$

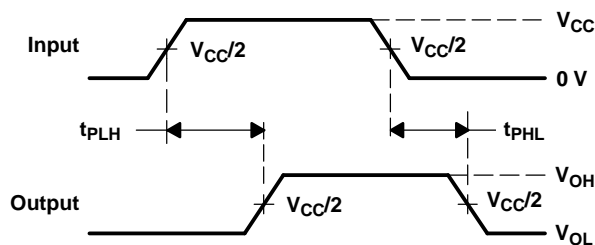


LOAD CIRCUIT

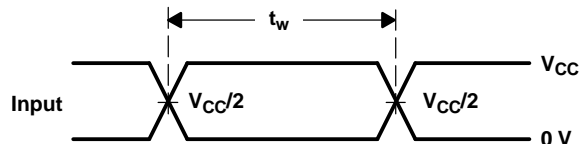
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PHL}$	GND



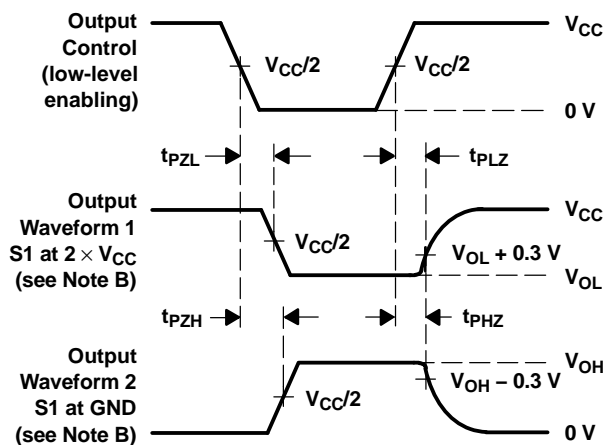
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 5. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AVC16827DGGR</a>	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC16827
SN74AVC16827DGGR.B	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC16827
SN74AVC16827DGGRG4	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC16827
SN74AVC16827DGGRG4.B	Active	Production	TSSOP (DGG)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC16827
<a href="#">SN74AVC16827DGVR</a>	Active	Production	TVSOP (DGV)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVA827
SN74AVC16827DGVR.B	Active	Production	TVSOP (DGV)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVA827
SN74AVC16827DGVRG4	Active	Production	TVSOP (DGV)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVA827
SN74AVC16827DGVRG4.B	Active	Production	TVSOP (DGV)   56	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CVA827

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC16827DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74AVC16827DGGRG4	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74AVC16827DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74AVC16827DGVRG4	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC16827DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74AVC16827DGGRG4	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74AVC16827DGVR	TVSOP	DGV	56	2000	356.0	356.0	45.0
SN74AVC16827DGVRG4	TVSOP	DGV	56	2000	356.0	356.0	45.0

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

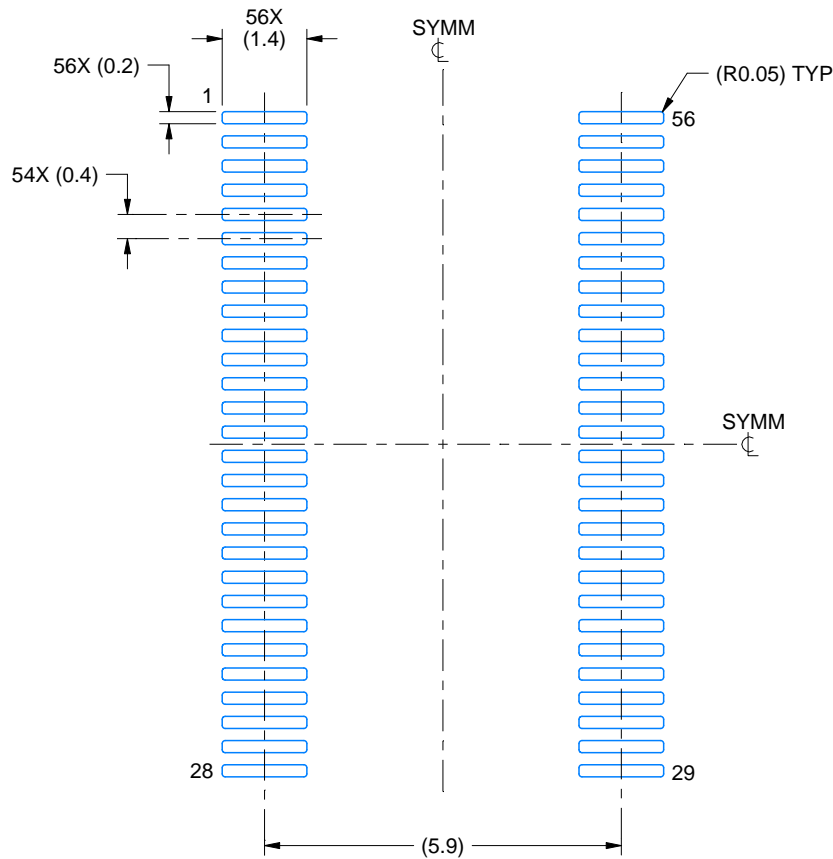


# EXAMPLE BOARD LAYOUT

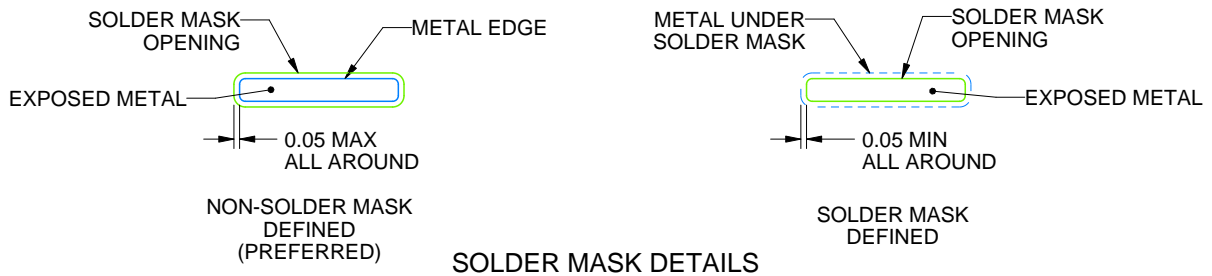
DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 8X



SOLDER MASK DETAILS

4220240/B 12/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

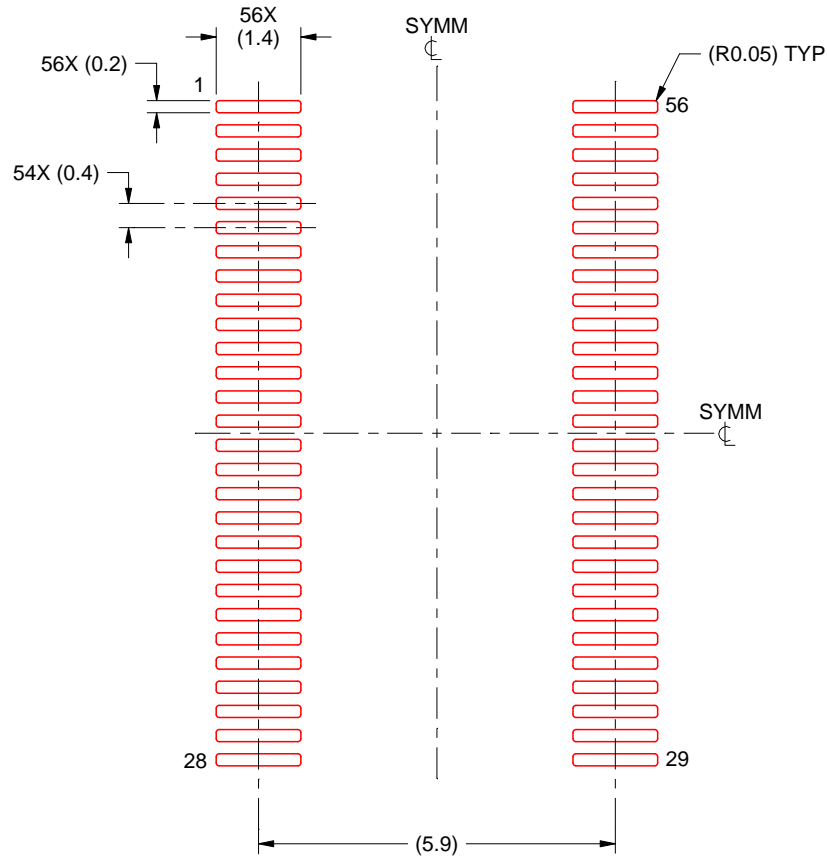


# EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

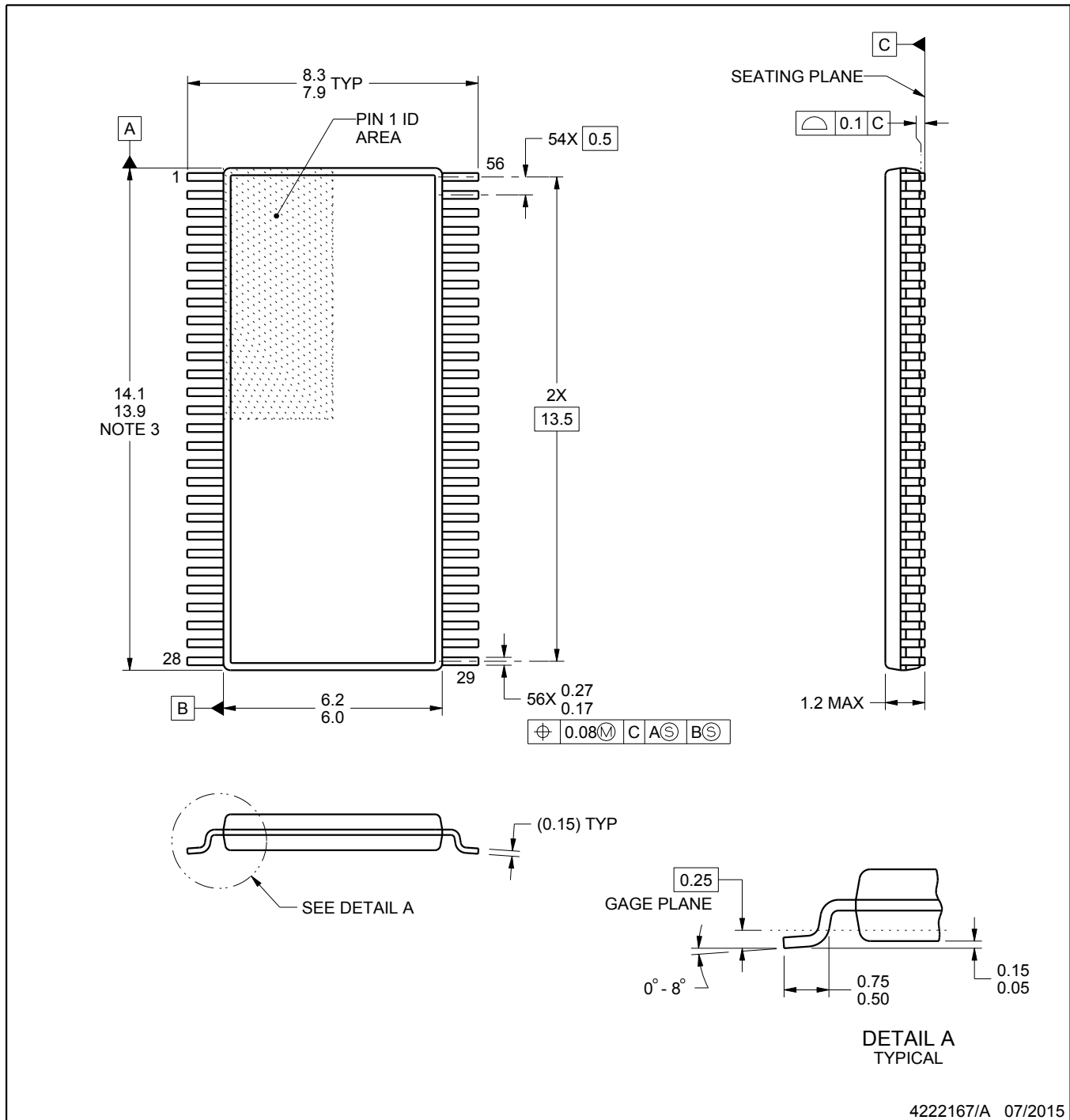


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 8X

4220240/B 12/2020

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4222167/A 07/2015

## NOTES:

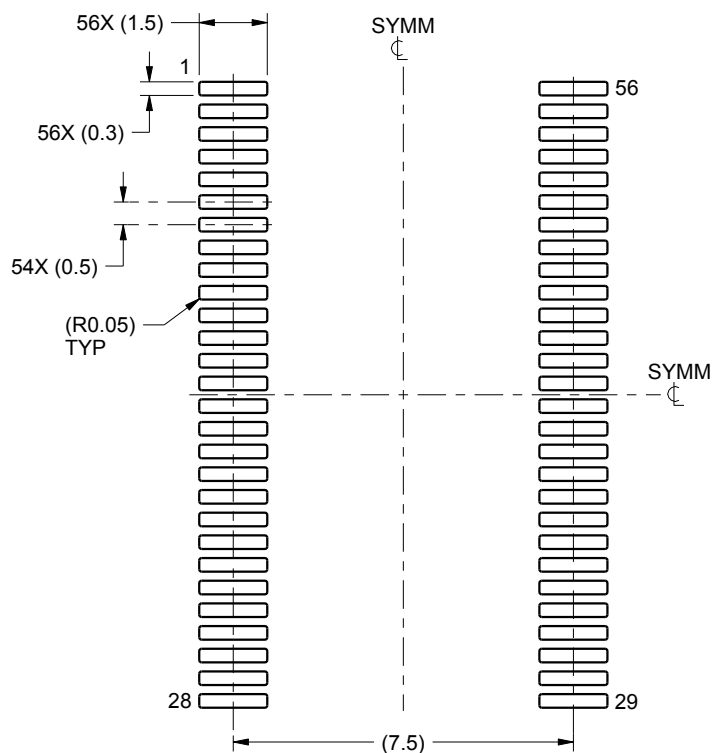
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

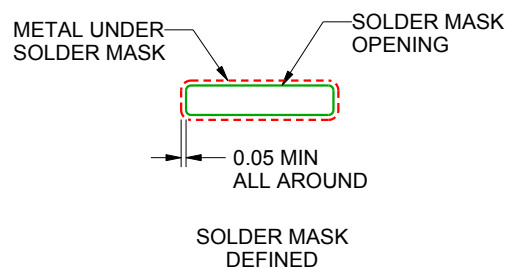
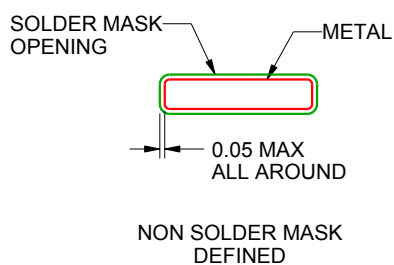
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

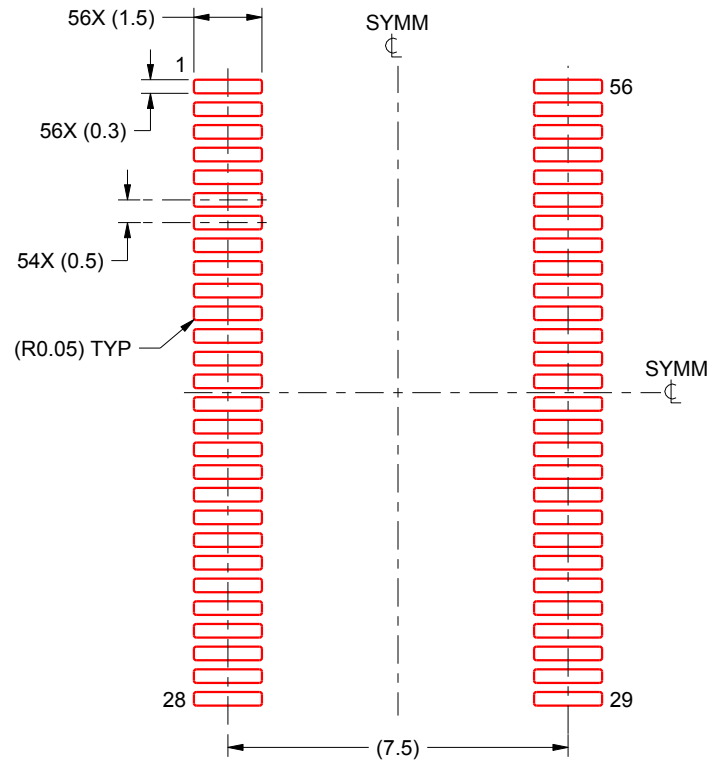
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025