

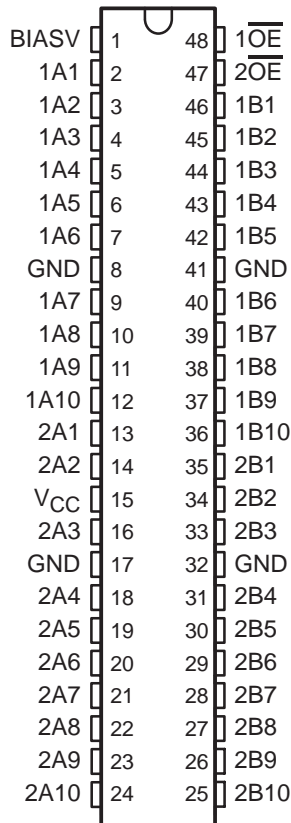
# SN74CBT16800C

## 20-BIT FET BUS SWITCH WITH PRECHARGED OUTPUTS 5-V BUS SWITCH WITH $-2$ -V UNDERSHOOT PROTECTION

SCDS117C – JANUARY 2003 – REVISED OCTOBER 2003

- Member of the Texas Instruments Widebus™ Family
- Undershoot Protection for Off-Isolation on A and B Ports Up To  $-2$  V
- B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging
- Supports PCI Hot Plug
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 3 \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{iO(OFF)} = 5.5$  pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 3 \mu A$  Max)
- $V_{CC}$  Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



### description/ordering information

The SN74CBT16800C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT16800C provides protection for undershoot up to  $-2$  V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.



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**description/ordering information (continued)**

The SN74CBT16800C is organized as two 10-bit bus switches with separate output-enable ( $\overline{1OE}$ ,  $\overline{2OE}$ ) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When  $\overline{OE}$  is low, the associated 10-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 10-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to BIASV through the equivalent of a 10-k $\Omega$  resistor when  $\overline{OE}$  is high, or if the device is powered down ( $V_{CC} = 0$  V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16800CDL	CBT16800C
		Tape and reel	SN74CBT16800CDLR	
	TSSOP – DGG	Tube	SN74CBT16800CDGG	CBT16800C
		Tape and reel	SN74CBT16800CDGGR	
	TVSOP – DGV	Tape and reel	SN74CBT16800CDGVR	CY800C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**  
**(each 10-bit bus switch)**

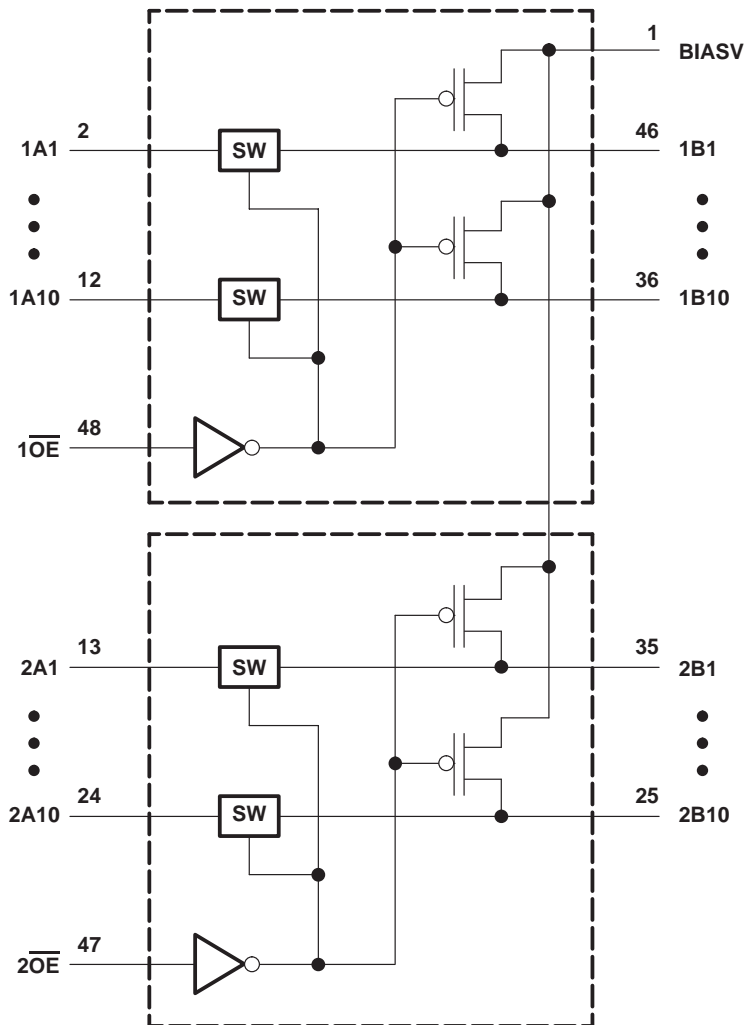
INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV



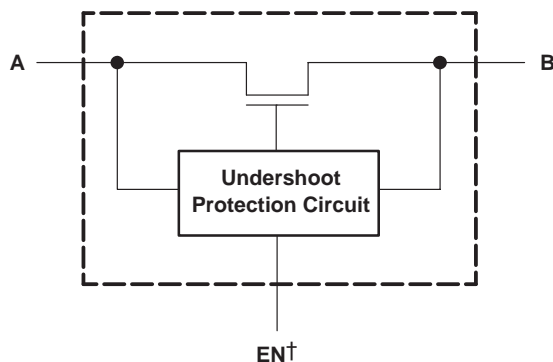
**SN74CBT16800C**  
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**5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

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logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Bias supply voltage range, BIASV	-0.5 V to 7 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2)	-0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	-0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )	-50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ )	-50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	$\pm 128$ mA
Continuous current through $V_{CC}$ or GND terminals	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
  2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  5. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 6)**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
BIASV Bias supply voltage	0	$V_{CC}$	V
$V_{IH}$ High-level control input voltage	2	5.5	V
$V_{IL}$ Low-level control input voltage	0	0.8	V
$V_{I/O}$ Data input/output voltage	0	5.5	V
$T_A$ Operating free-air temperature	-40	85	°C

NOTE 6: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Control inputs	V <sub>CC</sub> = 4.5 V,	I <sub>IN</sub> = -18 mA			-1.8	V
V <sub>IKU</sub>	Data inputs	V <sub>CC</sub> = 5 V,	0 mA > I <sub>I</sub> ≥ -50 mA, V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch OFF			-2	V
V <sub>O(USP)‡</sub>		V <sub>CC</sub> = BIASV = 5 V,	I <sub>I</sub> = -10 mA, V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch OFF	3			V
V <sub>O</sub>	B port	V <sub>CC</sub> = 0 V,	BIASV = V <sub>X</sub> , I <sub>O</sub> = 0	V <sub>X</sub> -0.1		V <sub>X</sub>	V
I <sub>IN</sub>	Control inputs	V <sub>CC</sub> = 5.5 V,	V <sub>IN</sub> = V <sub>CC</sub> or GND			±1	μA
I <sub>O</sub>	B port	V <sub>CC</sub> = 4.5 V,	BIASV = 2.4 V, V <sub>O</sub> = 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND		0.25		mA
I <sub>OZ</sub> §		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			±10	μA
I <sub>off</sub>		V <sub>CC</sub> = 0,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0			10	μA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	I <sub>I/O</sub> = 0, V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch ON or OFF			3	μA
ΔI <sub>CC</sub> ¶	Control inputs	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			2.5	mA
C <sub>in</sub>	Control inputs	V <sub>IN</sub> = 3 V or 0			4.5		pF
C <sub>iO(OFF)</sub>	A port	V <sub>I/O</sub> = 3 V or 0,	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			5.5	pF
C <sub>iO(ON)</sub>		V <sub>I/O</sub> = 3 V or 0,	Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND			15.5	pF
r <sub>on</sub> #		V <sub>CC</sub> = 4 V, TYP at V <sub>CC</sub> = 4 V	V <sub>I</sub> = 2.4 V, I <sub>O</sub> = -15 mA		8	12	Ω
		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>O</sub> = 64 mA	3	6	
				I <sub>O</sub> = 30 mA	3	6	
			V <sub>I</sub> = 2.4 V, I <sub>O</sub> = -15 mA	5	10		

V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

† All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

‡ V<sub>O(USP)</sub> = A-port undershoot static protection.

§ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t <sub>pd</sub>		A or B	B or A		0.24		0.15	ns
t <sub>PZH</sub>	BIASV = GND	$\overline{\text{OE}}$	A or B		6.5	1.5	6	ns
t <sub>PZL</sub>	BIASV = 3 V				6.5	1.5	6	
t <sub>PHZ</sub>	BIASV = GND	$\overline{\text{OE}}$	A or B		6.5	1.5	6	ns
t <sub>PLZ</sub>	BIASV = 3 V				6.5	1.5	6	

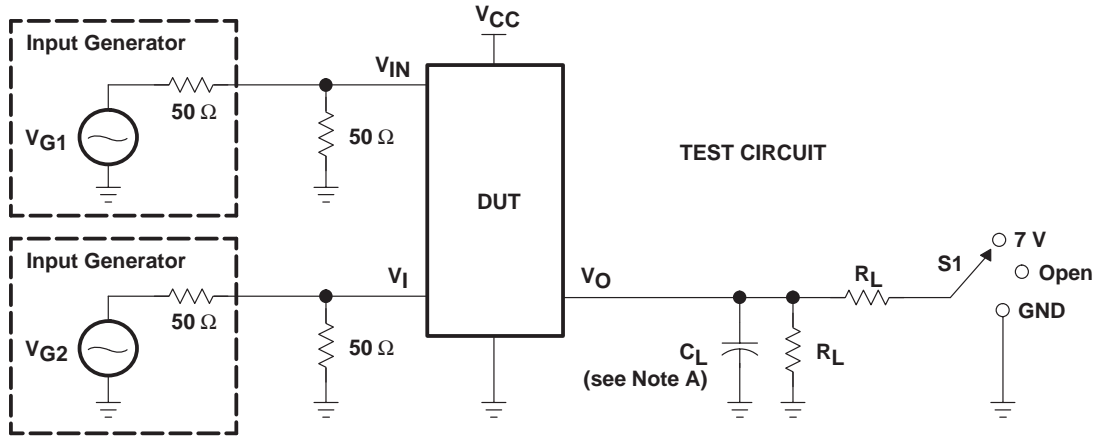
|| The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



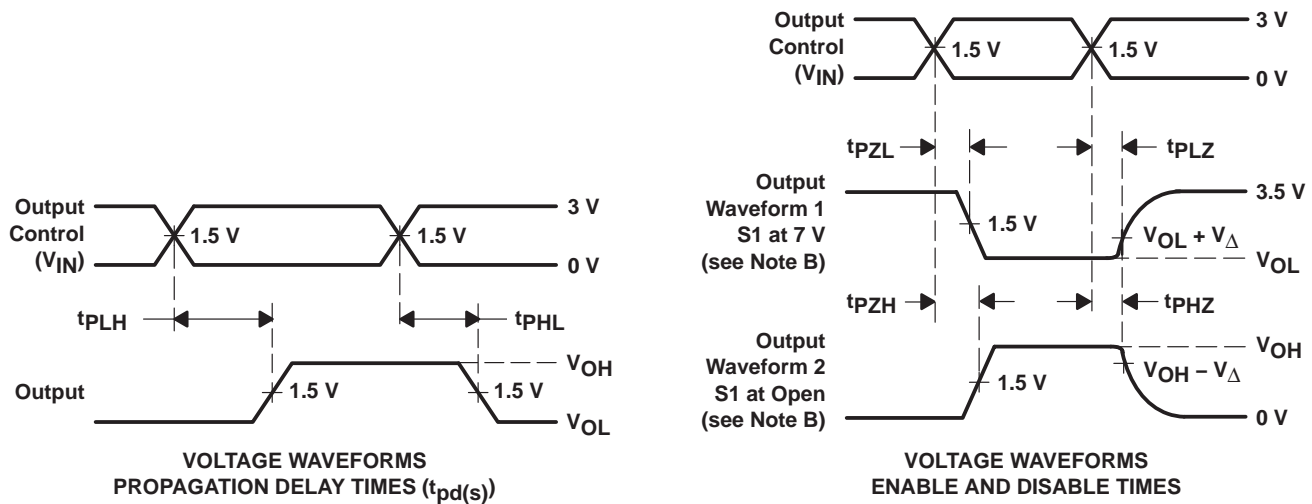
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**PARAMETER MEASUREMENT INFORMATION**



TEST	VCC	S1	RL	VI	CL	VΔ
t <sub>pd</sub> (s)	5 V ± 0.5 V	Open	500 Ω	VCC or GND	50 pF	
	4 V	Open	500 Ω	VCC or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
	4 V	7 V	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	5 V ± 0.5 V	Open	500 Ω	VCC	50 pF	0.3 V
	4 V	Open	500 Ω	VCC	50 pF	0.3 V



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Test Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74CBT16800CDGGR</a>	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16800C
SN74CBT16800CDGGR.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16800C
<a href="#">SN74CBT16800CDL</a>	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16800C
SN74CBT16800CDL.B	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16800C

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16800CDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16800CDGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT16800CDL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74CBT16800CDL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



# EXAMPLE BOARD LAYOUT

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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