

SN74HCS20 Dual 4-Input NAND Gate with Schmitt-Trigger Inputs

1 Features

- Wide operating voltage range: 2V to 6V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
 - Typical I_{CC} of 100nA
 - Typical input leakage current of ± 100 nA
- ± 7.8 mA output drive at 5V
- Extended ambient temperature range: -40°C to $+125^{\circ}\text{C}$, T_A

2 Applications

- [Alarm / tamper detect circuit](#)
- S-R latch

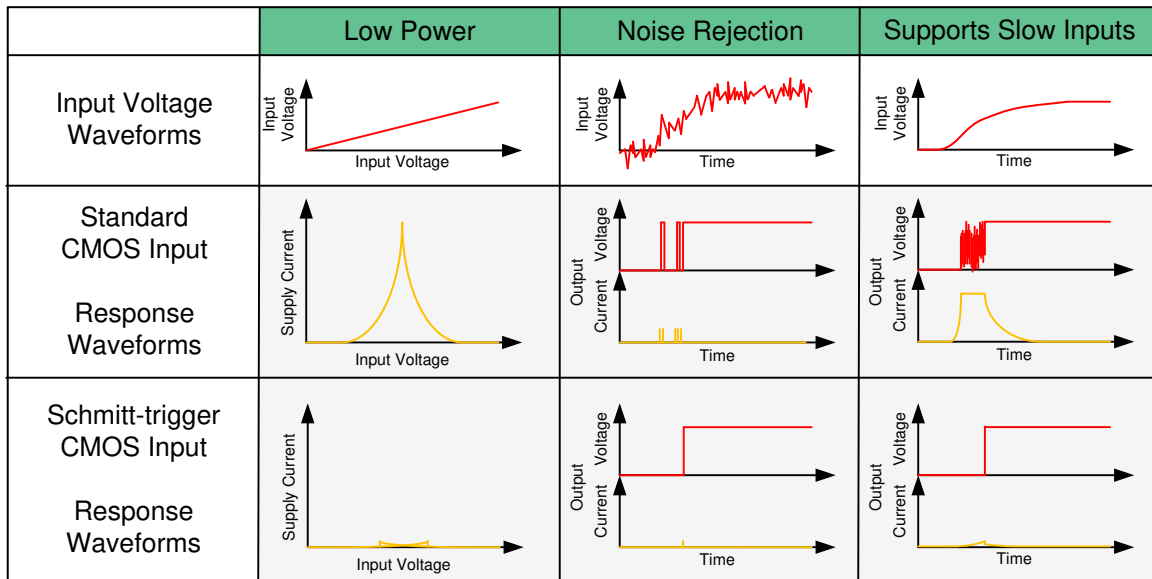
3 Description

This device contains two independent 4-input NAND gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = \overline{A \bullet B \bullet C \bullet D}$ in positive logic.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74HCS20PWR	TSSOP (14)	5.00mm × 4.40mm
SN74HCS20DR	SOIC (14)	8.70mm × 3.90mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Benefits of Schmitt-trigger Inputs



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4 Pin Configuration and Functions

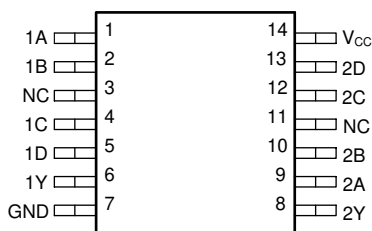


Figure 4-1. D or PW Package 14-Pin SOIC or TSSOP Top View

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
1C	4	I	Channel 1, Input C
1D	5	I	Channel 1, Input D
1Y	6	O	Channel 1, Output Y
2A	9	I	Channel 2, Input A
2B	10	I	Channel 2, Input B
2C	12	I	Channel 2, Input C
2D	13	I	Channel 2, Input D
2Y	8	O	Channel 2, Output Y
GND	7	—	Ground
NC	3, 11	—	Not internally connected
V _{CC}	14	—	Positive Supply

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		–0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < –0.5 or V _I > V _{CC} + 0.5		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < –0.5 or V _O > V _{CC} + 0.5		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35	mA
	Continuous current through V _{CC} or GND			±70	mA
T _J	Junction temperature ⁽³⁾			150	°C
T _{stg}	Storage temperature		–65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings can be exceeded if the input and output current ratings are observed. Do not exceed the absolute maximum voltage supply rating.
- (3) Verified by design.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2		6	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
Δt/Δv	Input transition rise and fall rate			Unlimited	ns/V
T _A	Ambient temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74HCS20		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	94.1	89.1	°C/W

5.4 Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		SN74HCS20		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2V	1.13	1.26	1.37	V
				4.5V	2.31	2.47	2.66	
				6V	2.99	3.18	3.44	
V_{T-}	Negative switching threshold			2V	0.55	0.62	0.71	V
				4.5V	1.21	1.36	1.5	
				6V	1.56	1.79	1.99	
ΔV_T	$V_{T+} - V_{T-}$			2V	0.54	0.64	0.71	V
				4.5V	0.94	1.11	1.27	
				6V	1.20	1.38	1.57	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2V to 6V	$V_{CC} - 0.1$ $V_{CC} - 0.002$			V
			$I_{OH} = -6\text{mA}$	4.5V	4.0	4.3		
			$I_{OH} = -7.8\text{mA}$	6V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2V to 6V		0.002	0.1	V
			$I_{OL} = 4\text{mA}$	4.5V		0.18	0.30	
			$I_{OL} = 7.8\text{mA}$	6V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6V		± 100	± 1000	nA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6V		0.1	2	μA
C_i	Input capacitance			2V to 6V			5	pF

5.6 Switching Characteristics

over operating free-air temperature range; typical ratings measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See the [Parameter Measurement Information](#).

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	A or B	Y	2V		19	56	ns
				4.5V		8	22	
				6V		7	19	
t_t	Transition-time		Y	2V		9	17	ns
				4.5V		5	8	
				6V		4	7	

5.7 Typical Characteristics

$T_A = 25^\circ\text{C}$

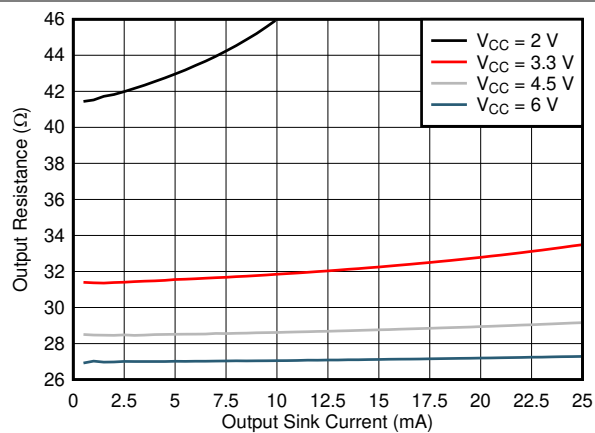


Figure 5-1. Output driver resistance in Low state

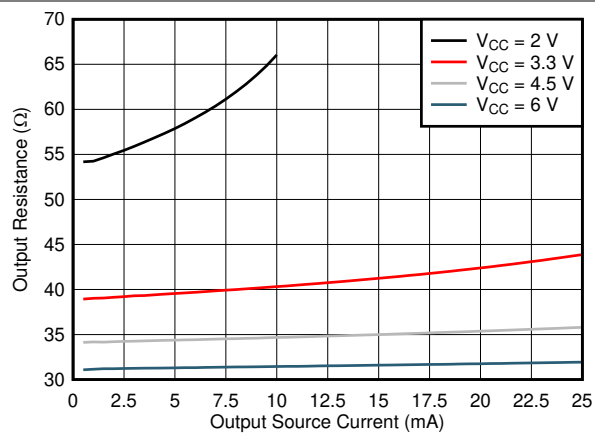


Figure 5-2. Output driver resistance in High state

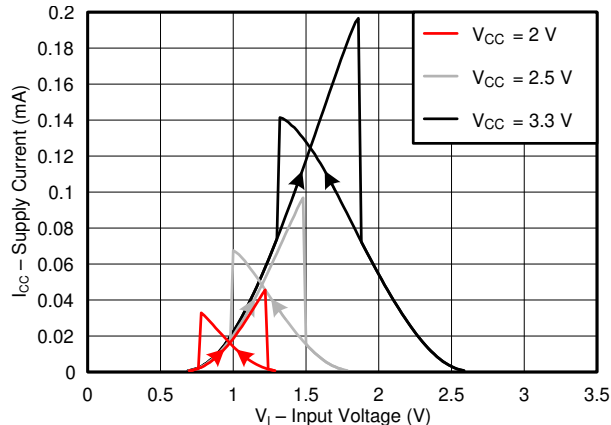


Figure 5-3. Typical supply current versus input voltage across common supply values (2V to 3.3V)

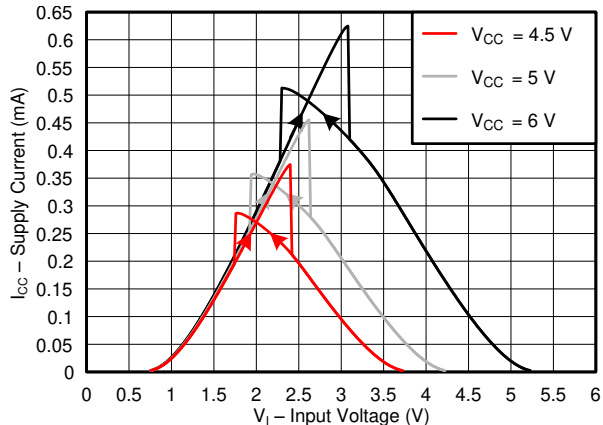
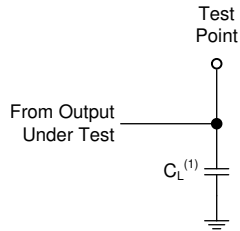


Figure 5-4. Typical supply current versus input voltage across common supply values (4.5V to 6V)

6 Parameter Measurement Information

- Phase relationships between waveforms are chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_f < 2.5\text{ns}$.
- The outputs are measured one at a time, with one input transition per measurement.



A. $C_L = 50\text{pF}$ and includes probe and jig capacitance.

Figure 6-1. Load Circuit

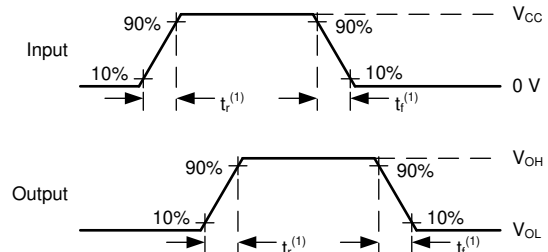
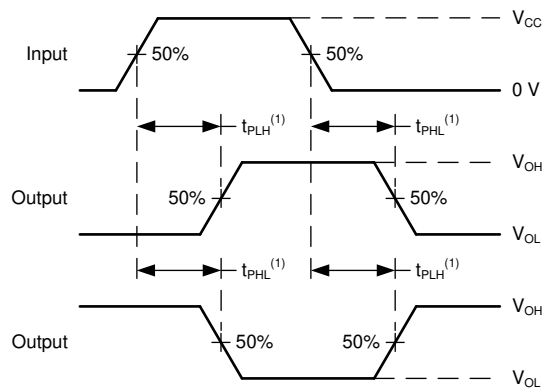


Figure 6-2. Voltage Waveforms Transition Times



A. The maximum between t_{PLH} and t_{PHL} is used for t_{pd} .

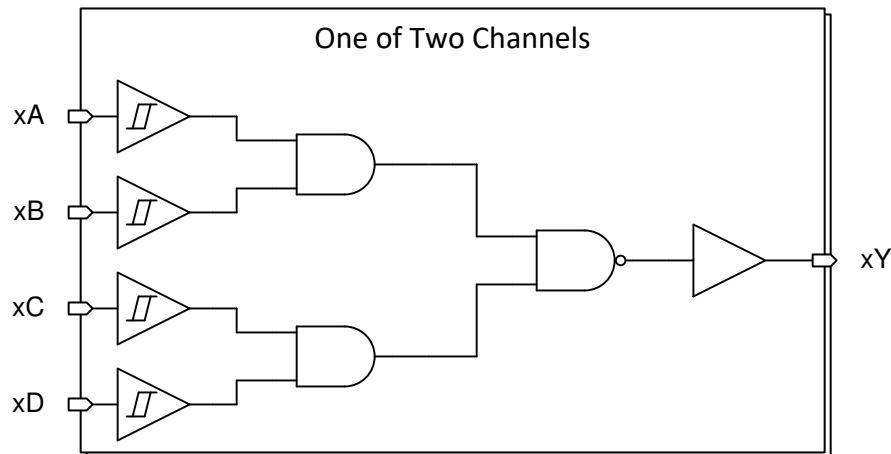
Figure 6-3. Voltage Waveforms Propagation Delays

7 Detailed Description

7.1 Overview

This device contains two independent 4-input NAND gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = \overline{A \bullet B \bullet C \bullet D}$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Section 5.1](#) must be followed at all times.

7.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the [Electrical Characteristics](#), which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Figure 7-1](#).

CAUTION

Voltages beyond the values specified in the [Section 5.1](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

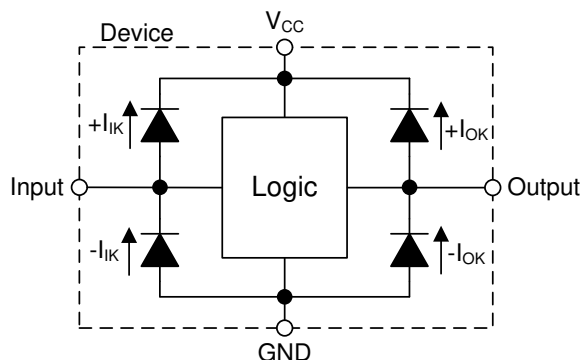


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

[Table 7-1](#) lists the functional modes of SN74HCS20.

Table 7-1. Function Table

INPUTS				OUTPUT T Y
A	B	C	D	
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, two 4-input NAND gates are used to create an active-low SR latch as shown in [Figure 8-1](#).

The SN74HCS20 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

8.2 Typical Application

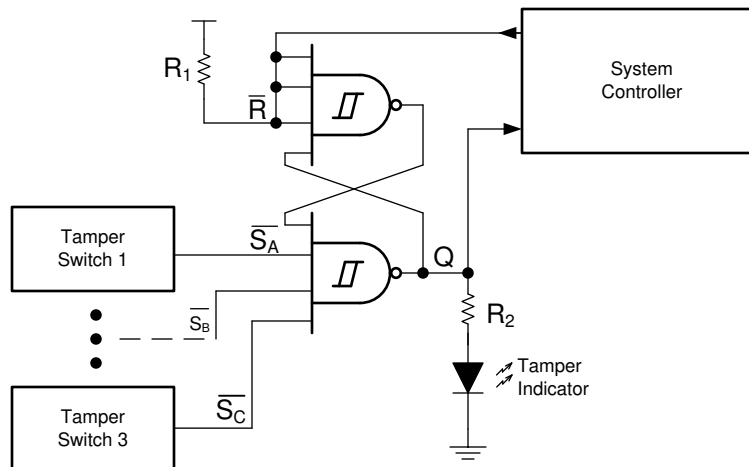


Figure 8-1. Typical application block diagram

8.2.1 Design Requirements

- All signals in the system operate at 5V
- Avoid unstable state by not having LOW signals on both inputs
- Conditions for output
 - Q output is HIGH when $\bar{S}$ is LOW
 - Q output remains High until $\bar{R}$ is LOW

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS20 plus the maximum supply current, I_{CC} , listed in the [Electrical Characteristics](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the [Absolute Maximum Ratings](#).

The SN74HCS20 can drive a load with a total capacitance less than or equal to 50pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70pF.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_J(\text{max})$ listed in the [Section 5.1](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Section 5.1](#). These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{L(\text{min})}$ to be considered a logic LOW, and $V_{H(\text{min})}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the [Section 5.1](#).

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS20, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10k Ω resistor value is often used due to these factors.

The SN74HCS20 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_T(\text{min})$ in the [Electrical Characteristics](#). This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the [Typical Characteristics](#).

Refer to the [Feature Description](#) for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the [Electrical Characteristics](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the [Electrical Characteristics](#).

Unused outputs can be left floating.

Refer to [Feature Description](#) for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the [Layout](#).
2. Ensure the capacitive load at the output is $\leq 70\text{pF}$. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS20 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / 25\text{mA}) \Omega$. This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

8.2.3 Application Curves

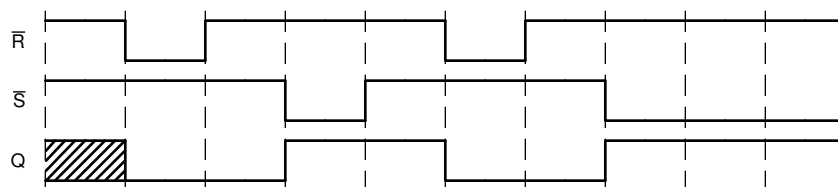


Figure 8-2. Application timing diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 5.3](#). Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results, as shown in [Figure 8-3](#).

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

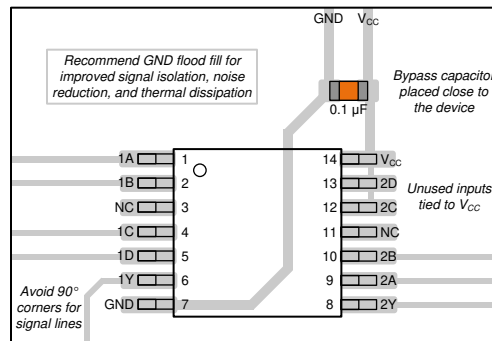


Figure 8-3. Example layout for the SN74HCS20

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- [Reduce Noise and Save Power with the New HCS Logic Family](#)
- [CMOS Power Consumption and CPD Calculation](#)
- [Designing with Logic](#)

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 30, 2020 to September 29, 2026 (from Revision A (June 2020) to Revision B (October 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Deleted "I _{CC} " and "output" from "Continuous current through V _{CC} or GND" row for clarity.....	4
• Changed V _{T+} limits at 2V V _{CC} from 0.7V (min), 1.5V (max) to 1.13V (min), 1.37V (max)	5
• Added V _{T+} typical values at 2V V _{CC}	5
• Changed V _{T+} limits at 4.5V V _{CC} from 1.7V (min), 3.15V (max) to 2.31V (min), 2.66V (max)	5
• Added V _{T+} typical values at 4.5V V _{CC}	5
• Changed V _{T+} limits at 6V V _{CC} from 2.1V (min), 4.2V (max) to 2.99V (min), 3.44V (max)	5
• Added V _{T+} typical values at 6V V _{CC}	5
• Changed V _{T-} limits at 2V V _{CC} from 0.3V (min), 1.0V (max) to 0.55V (min), 0.71V (max).....	5
• Added V _{T-} typical values at 2V V _{CC}	5
• Changed V _{T-} limits at 4.5V V _{CC} from 0.9V (min), 2.2V (max) to 1.21V (min), 1.50V (max)	5
• Added V _{T-} typical values at 4.5V V _{CC}	5
• Changed V _{T-} limits at 6V V _{CC} from 1.2V (min), 3.0V (max) to 1.56V (min), 1.99V (max).....	5
• Added V _{T-} typical values at 6V V _{CC}	5
• Changed ΔV _T limits at 2V V _{CC} from 0.2V (min), 1.0V (max) to 0.54V (min), 0.71V (max).....	5
• Added ΔV _T typical values at 2V V _{CC}	5
• Changed ΔV _T limits at 4.5V V _{CC} from 0.4V (min), 1.4V (max) to 0.94V (min), 1.27V (max).....	5
• Added ΔV _T typical values at 4.5V V _{CC}	5

• Changed ΔV_T limits at 6V V_{CC} from 0.6V (min), 1.6V (max) to 1.20V (min), 1.57V (max).....	5
• Added ΔV_T typical values at 6V V_{CC}	5

Changes from Revision * (March 2020) to Revision A (June 2020)	Page
• Added D package to data sheet	1
• Added D Package to <i>Thermal Information Table</i>	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS20DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS20
SN74HCS20DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS20
SN74HCS20PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS20
SN74HCS20PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS20
SN74HCS20PWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS20
SN74HCS20PWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS20

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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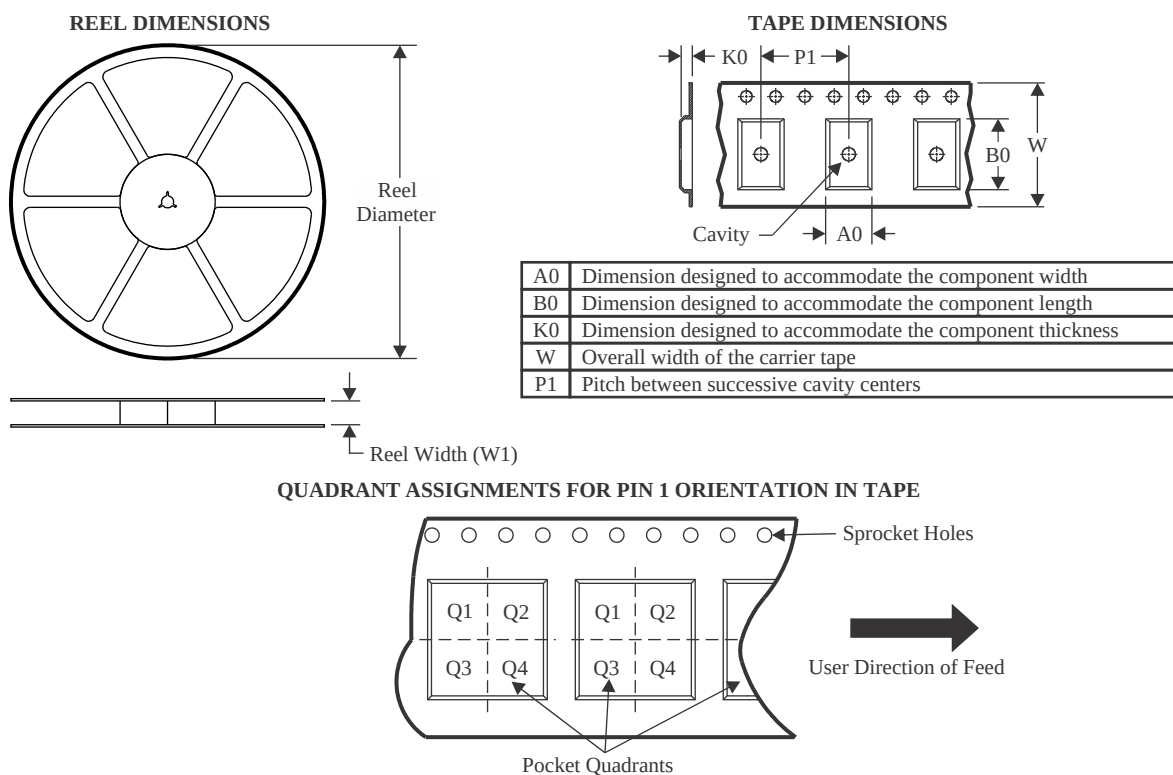
OTHER QUALIFIED VERSIONS OF SN74HCS20 :

- Automotive : [SN74HCS20-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

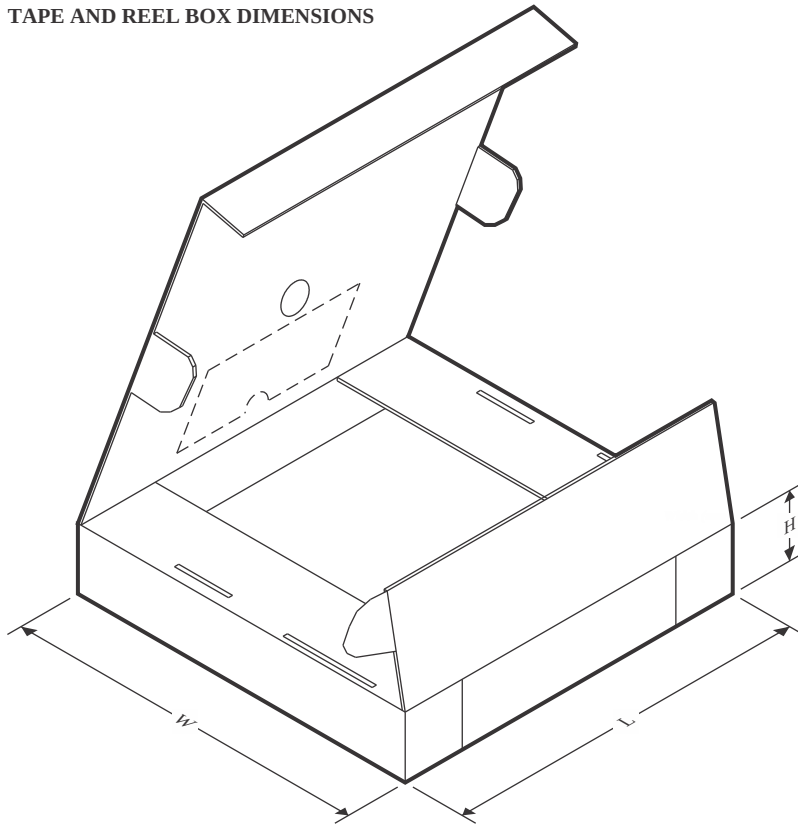
TAPE AND REEL INFORMATION



*All dimensions are nominal

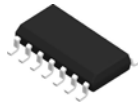
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS20DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS20PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS20PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

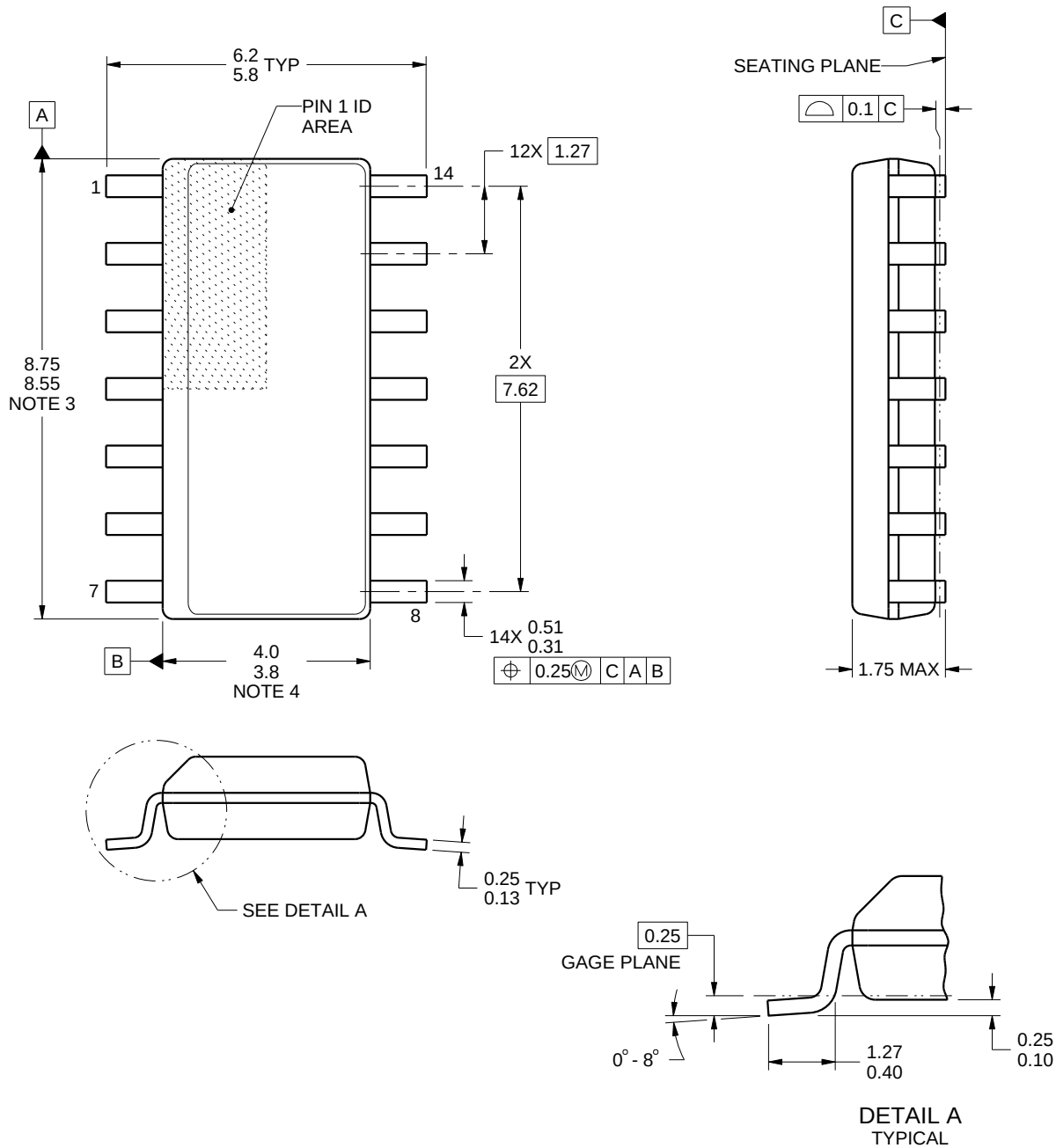


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS20DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCS20PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCS20PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

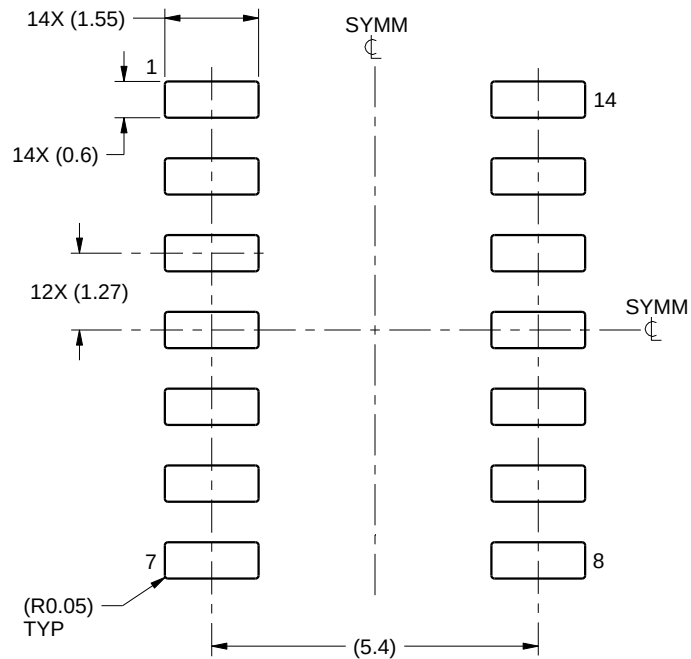
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

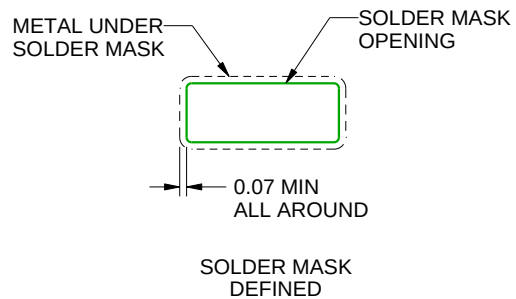
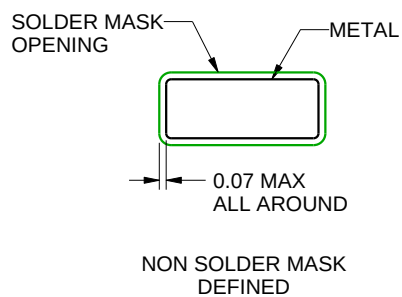
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

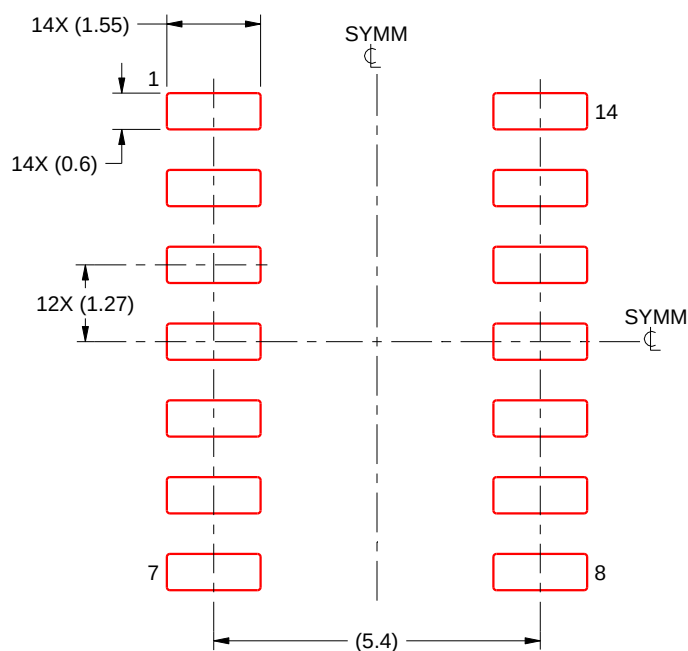
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

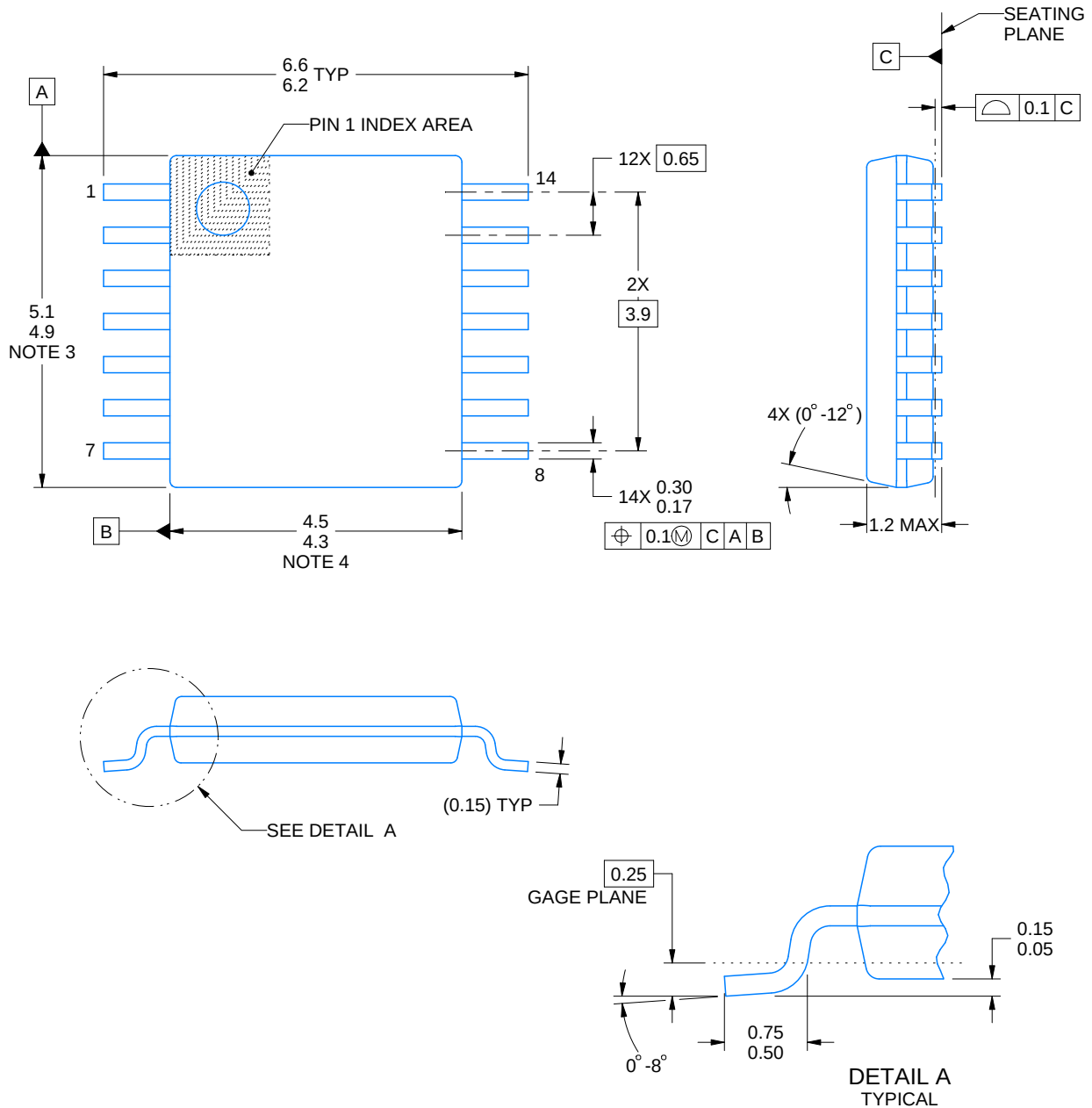
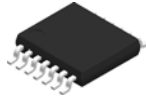


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

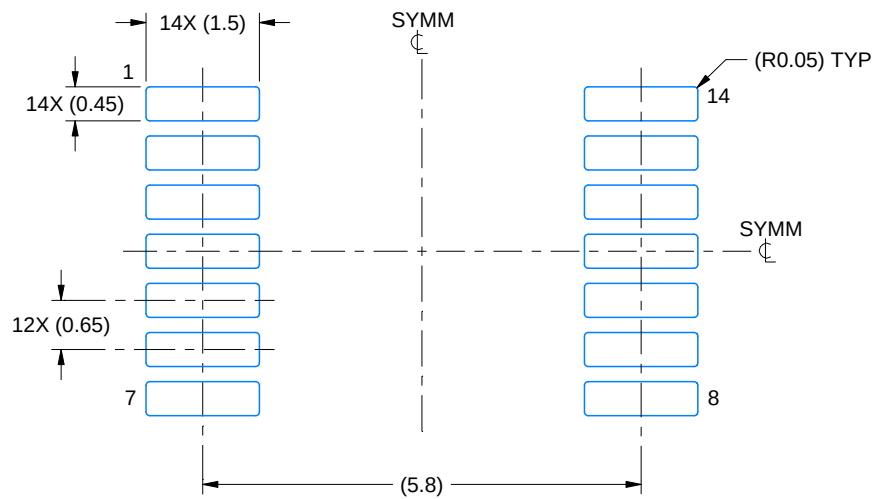
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

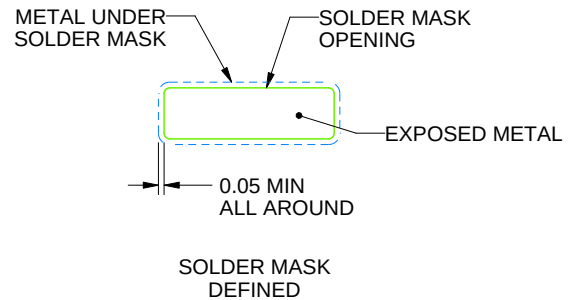
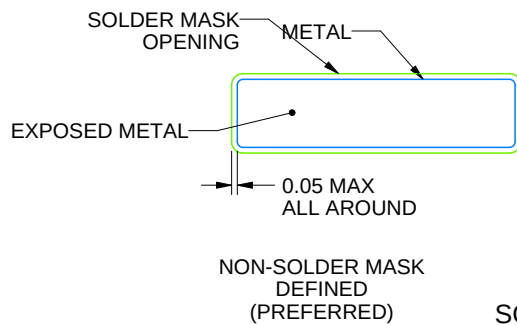
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

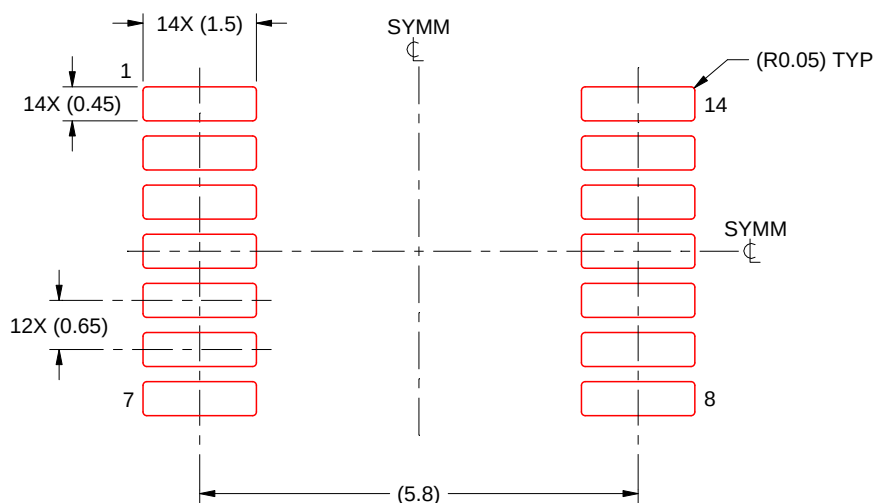
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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