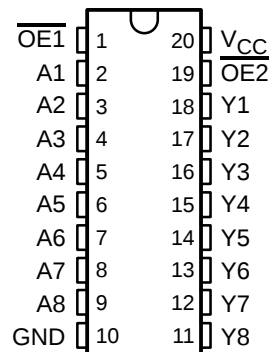


# SN54HCT540, SN74HCT540 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS008C – MARCH 1984 – REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)

SN54HCT540 . . . J PACKAGE  
SN74HCT540 . . . DW OR N PACKAGE  
(TOP VIEW)



## description/ordering information

These octal buffers and line drivers are designed to have the performance of the 'HCT240 devices and a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR. If either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state. The 'HCT540 devices provide inverted data at the outputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$          | PACKAGE <sup>†</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | PDIP – N             | Tube          | SN74HCT540N           | SN74HCT540N      |
|                | SOIC – DW            | Tube          | SN74HCT540DW          | HCT540           |
|                |                      | Tape and reel | SN74HCT540DWR         |                  |
| -55°C to 125°C | CDIP – J             | Tube          | SNJ54HCT540J          | SNJ54HCT540J     |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each buffer/driver)

| INPUTS           |                  |   | OUTPUT<br>Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A |             |
| L                | L                | L | H           |
| L                | L                | H | L           |
| H                | X                | X | Z           |
| X                | H                | X | Z           |



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 **TEXAS  
INSTRUMENTS**

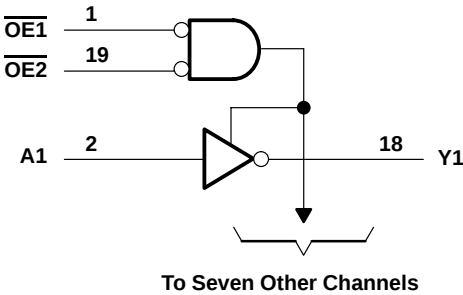
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# SN54HCT540, SN74HCT540 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                             |                |
|-----------------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                              | –0.5 V to 7 V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)  | ±20 mA         |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) | ±20 mA         |
| Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )                  | ±35 mA         |
| Continuous current through $V_{CC}$ or GND                                  | ±70 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package           | 58°C/W         |
| N package                                                                   | 69°C/W         |
| Storage temperature range, $T_{stg}$                                        | –65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

|          |                                       |                                         | SN54HCT540 |     |          | SN74HCT540 |     |          | UNIT |
|----------|---------------------------------------|-----------------------------------------|------------|-----|----------|------------|-----|----------|------|
|          |                                       |                                         | MIN        | NOM | MAX      | MIN        | NOM | MAX      |      |
| $V_{CC}$ | Supply voltage                        |                                         | 4.5        | 5   | 5.5      | 4.5        | 5   | 5.5      | V    |
| $V_{IH}$ | High-level input voltage              | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 2          |     |          | 2          |     |          | V    |
| $V_{IL}$ | Low-level input voltage               | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ |            |     | 0.8      |            |     | 0.8      | V    |
| $V_I$    | Input voltage                         |                                         | 0          |     | $V_{CC}$ | 0          |     | $V_{CC}$ | V    |
| $V_O$    | Output voltage                        |                                         | 0          |     | $V_{CC}$ | 0          |     | $V_{CC}$ | V    |
| $t_t$    | Input transition (rise and fall) time |                                         |            |     | 500      |            |     | 500      | ns   |
| $T_A$    | Operating free-air temperature        |                                         | –55        |     | 125      | –40        |     | 85       | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54HCT540, SN74HCT540

## OCTAL BUFFERS AND LINE DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                     | TEST CONDITIONS                                                                            | V <sub>CC</sub> | T <sub>A</sub> = 25°C    |      |     | SN54HCT540 |       | SN74HCT540 |      | UNIT |
|-------------------------------|--------------------------------------------------------------------------------------------|-----------------|--------------------------|------|-----|------------|-------|------------|------|------|
|                               |                                                                                            |                 | MIN                      | TYP  | MAX | MIN        | MAX   | MIN        | MAX  |      |
| V <sub>OH</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                        | 4.5 V           | I <sub>OH</sub> = –20 µA |      |     | 4.4        | 4.499 | 4.4        | 4.4  | V    |
|                               |                                                                                            |                 | I <sub>OH</sub> = –6 mA  |      |     | 3.98       | 4.3   | 3.7        | 3.84 |      |
| V <sub>OL</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                        | 4.5 V           | I <sub>OL</sub> = 20 µA  |      |     | 0.001      | 0.1   | 0.1        | 0.1  | V    |
|                               |                                                                                            |                 | I <sub>OL</sub> = 6 mA   |      |     | 0.17       | 0.26  | 0.4        | 0.33 |      |
| I <sub>I</sub>                | V <sub>I</sub> = V <sub>CC</sub> or 0                                                      | 5.5 V           | ±0.1                     | ±100 |     | ±1000      |       | ±1000      |      | nA   |
| I <sub>OZ</sub>               | V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 5.5 V           | ±0.01                    | ±0.5 |     | ±10        |       | ±5         |      | µA   |
| I <sub>CC</sub>               | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0                                  | 5.5 V           |                          | 8    |     | 160        |       | 80         |      | µA   |
| ΔI <sub>CC</sub> <sup>†</sup> | One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>                          | 5.5 V           |                          | 1.4  | 2.4 | 3          |       | 2.9        |      | mA   |
| C <sub>i</sub>                |                                                                                            | 4.5 V to 5.5 V  |                          | 3    | 10  | 10         |       | 10         |      | pF   |

<sup>†</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)           | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54HCT540 |     | SN74HCT540 |     | UNIT |
|------------------|------------------------|-------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
|                  |                        |             |                 | MIN                   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>pd</sub>  | A                      | Y           | 4.5 V           |                       | 13  | 20  |            | 30  |            | 25  | ns   |
|                  |                        |             | 5.5 V           |                       | 12  | 18  |            | 27  |            | 23  |      |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Y           | 4.5 V           |                       | 20  | 30  |            | 45  |            | 38  | ns   |
|                  |                        |             | 5.5 V           |                       | 18  | 27  |            | 41  |            | 34  |      |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | Y           | 4.5 V           |                       | 19  | 30  |            | 45  |            | 38  | ns   |
|                  |                        |             | 5.5 V           |                       | 18  | 27  |            | 41  |            | 34  |      |
| t <sub>t</sub>   |                        | Y           | 4.5 V           |                       | 8   | 12  |            | 18  |            | 15  | ns   |
|                  |                        |             | 5.5 V           |                       | 7   | 11  |            | 16  |            | 14  |      |

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 150 pF (unless otherwise noted) (see Figure 1)

| PARAMETER       | FROM (INPUT)           | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54HCT540 |     | SN74HCT540 |     | UNIT |
|-----------------|------------------------|-------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
|                 |                        |             |                 | MIN                   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>pd</sub> | A                      | Y           | 4.5 V           |                       | 20  | 30  |            | 45  |            | 38  | ns   |
|                 |                        |             | 5.5 V           |                       | 19  | 27  |            | 41  |            | 34  |      |
| t <sub>en</sub> | $\overline{\text{OE}}$ | Y           | 4.5 V           |                       | 26  | 40  |            | 60  |            | 50  | ns   |
|                 |                        |             | 5.5 V           |                       | 25  | 36  |            | 54  |            | 45  |      |
| t <sub>t</sub>  |                        | Y           | 4.5 V           |                       | 17  | 42  |            | 63  |            | 53  | ns   |
|                 |                        |             | 5.5 V           |                       | 14  | 38  |            | 57  |            | 48  |      |

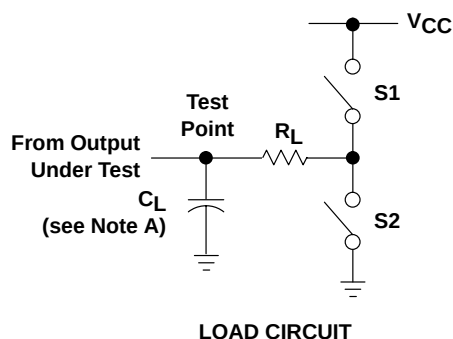
operating characteristics, T<sub>A</sub> = 25°C

| PARAMETER                                                       | TEST CONDITIONS | TYP | UNIT |
|-----------------------------------------------------------------|-----------------|-----|------|
| C <sub>pd</sub> Power dissipation capacitance per buffer/driver | No load         | 35  | pF   |

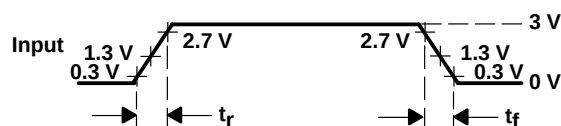
# SN54HCT540, SN74HCT540 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS008C – MARCH 1984 – REVISED MARCH 2003

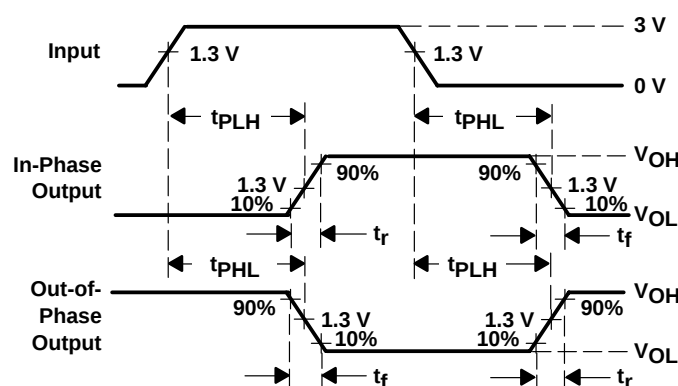
## PARAMETER MEASUREMENT INFORMATION



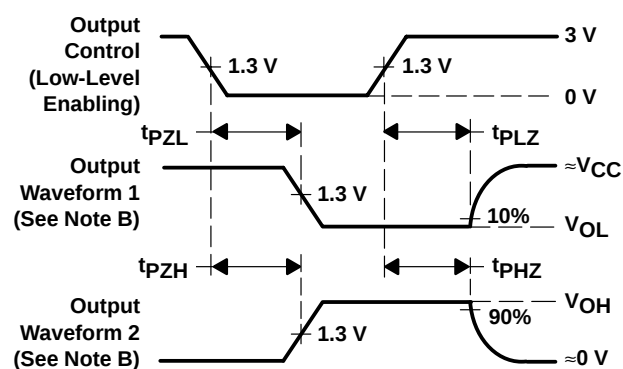
| PARAMETER         | $R_L$        | $C_L$           | S1     | S2     |
|-------------------|--------------|-----------------|--------|--------|
| $t_{en}$          | 1 k $\Omega$ | 50 pF or 150 pF | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{dis}$         | 1 k $\Omega$ | 50 pF           | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{pd}$ or $t_t$ | --           | 50 pF or 150 pF | Open   | Open   |



VOLTAGE WAVEFORM  
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)  |
|----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------|
| <a href="#">JM38510/65760BRA</a> | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>65760BRA |
| JM38510/65760BRA.A               | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>65760BRA |
| <a href="#">M38510/65760BRA</a>  | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | JM38510/<br>65760BRA |
| <a href="#">SN54HCT540J</a>      | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HCT540J          |
| SN54HCT540J.A                    | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HCT540J          |
| <a href="#">SN74HCT540DWR</a>    | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HCT540               |
| SN74HCT540DWR.A                  | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HCT540               |
| SN74HCT540DWRG4                  | Active        | Production           | SOIC (DW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HCT540               |
| <a href="#">SN74HCT540N</a>      | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HCT540N          |
| SN74HCT540N.A                    | Active        | Production           | PDIP (N)   20  | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HCT540N          |
| <a href="#">SNJ54HCT540J</a>     | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SNJ54HCT540J         |
| SNJ54HCT540J.A                   | Active        | Production           | CDIP (J)   20  | 20   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SNJ54HCT540J         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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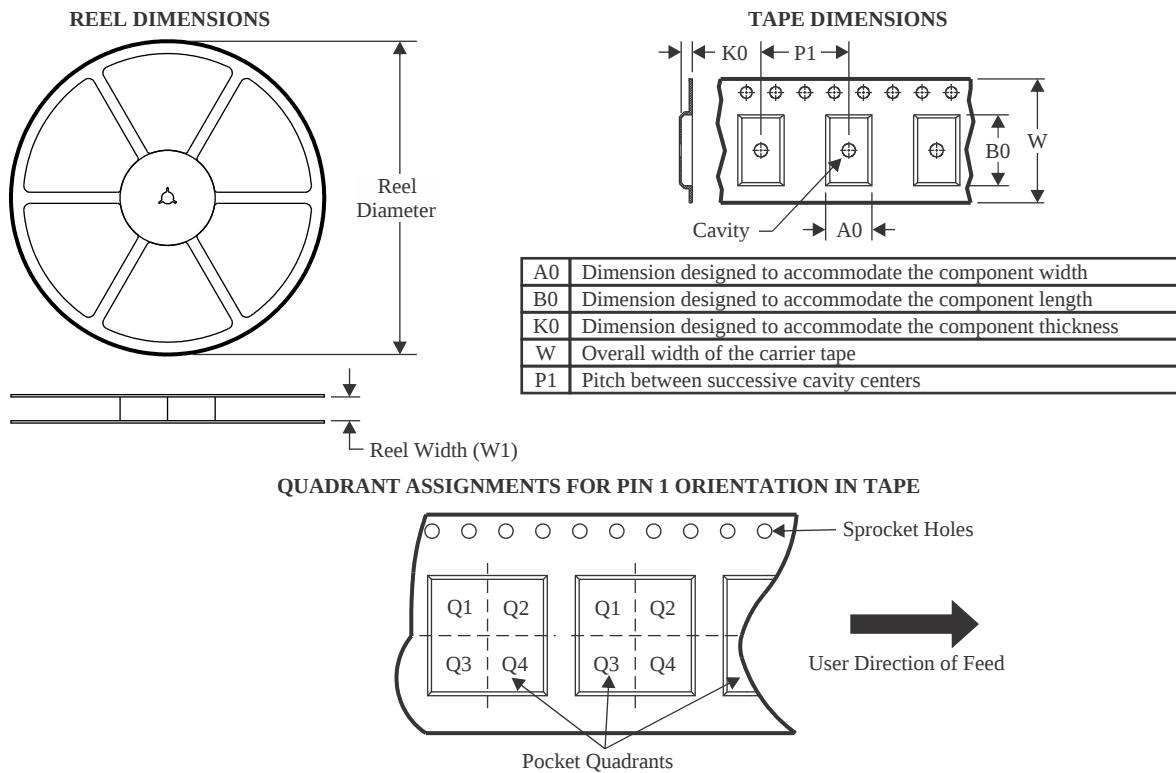
**OTHER QUALIFIED VERSIONS OF SN54HCT540, SN74HCT540 :**

- Catalog : [SN74HCT540](#)
- Military : [SN54HCT540](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

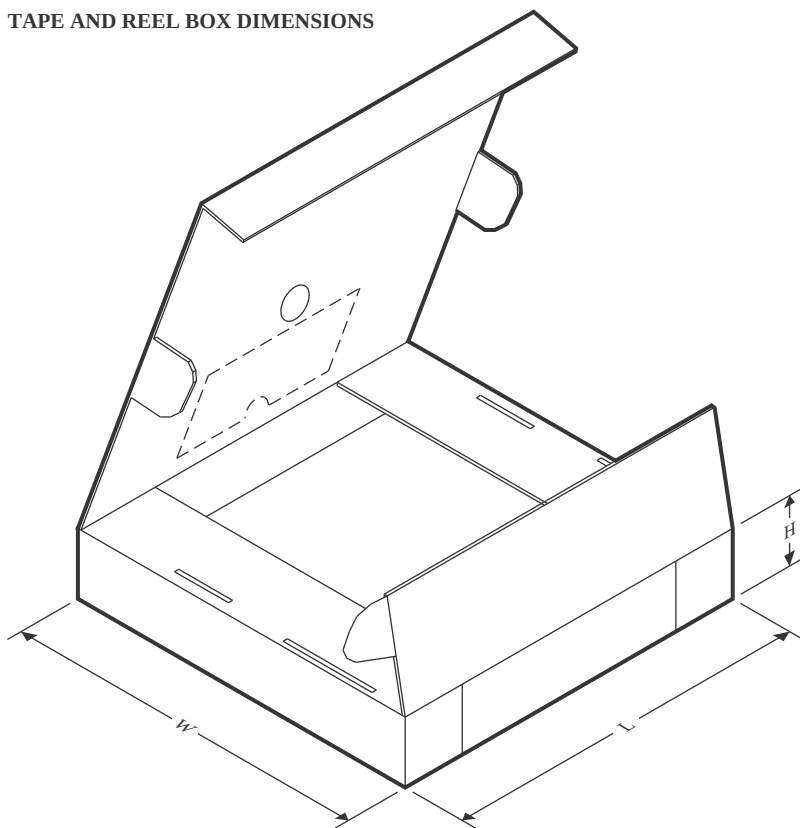
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HCT540DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74HCT540DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |

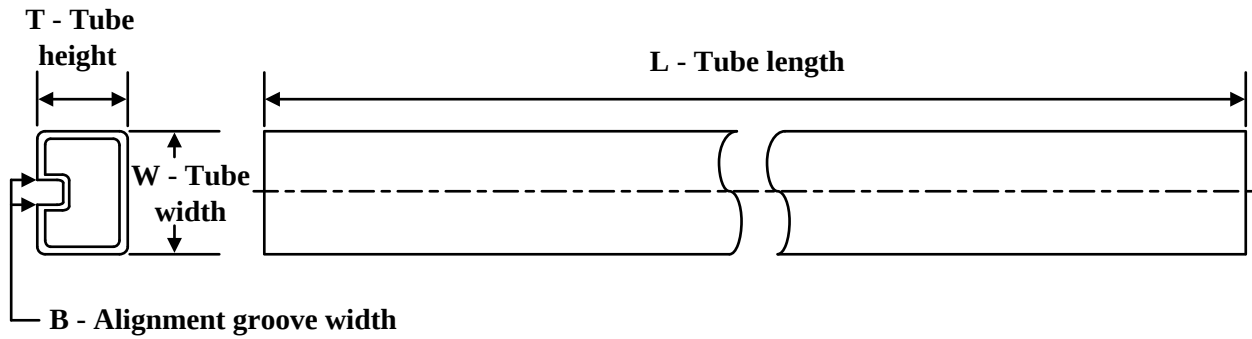
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT540DWR | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74HCT540DWR | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |

## TUBE



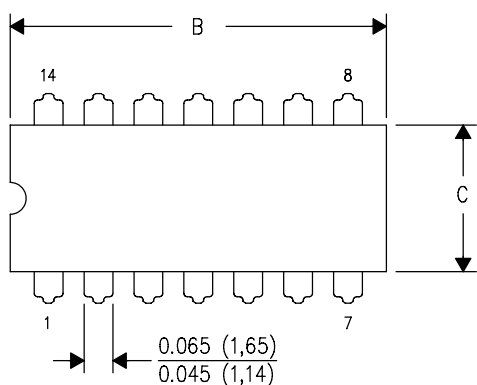
\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74HCT540N   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74HCT540N.A | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |

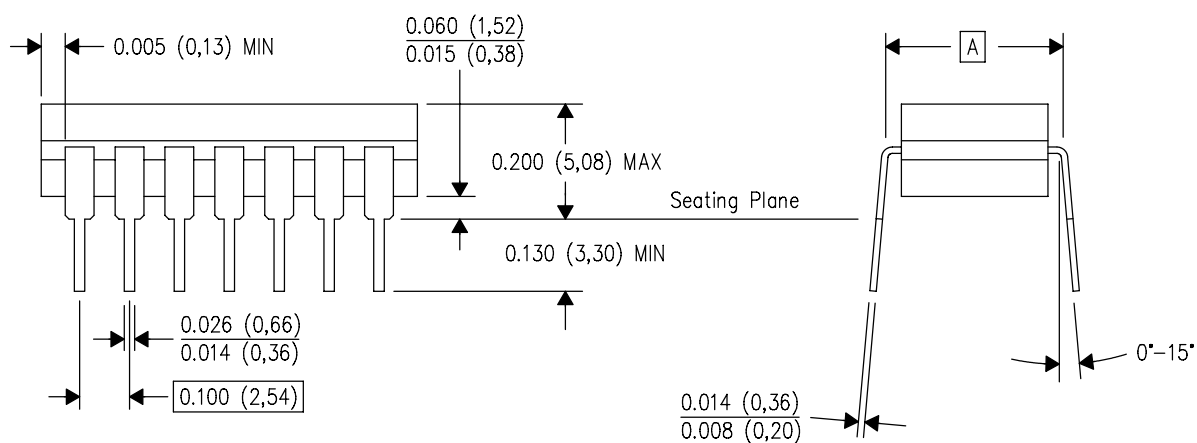
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



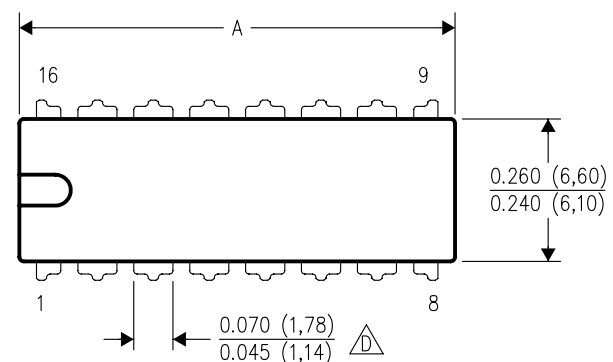
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

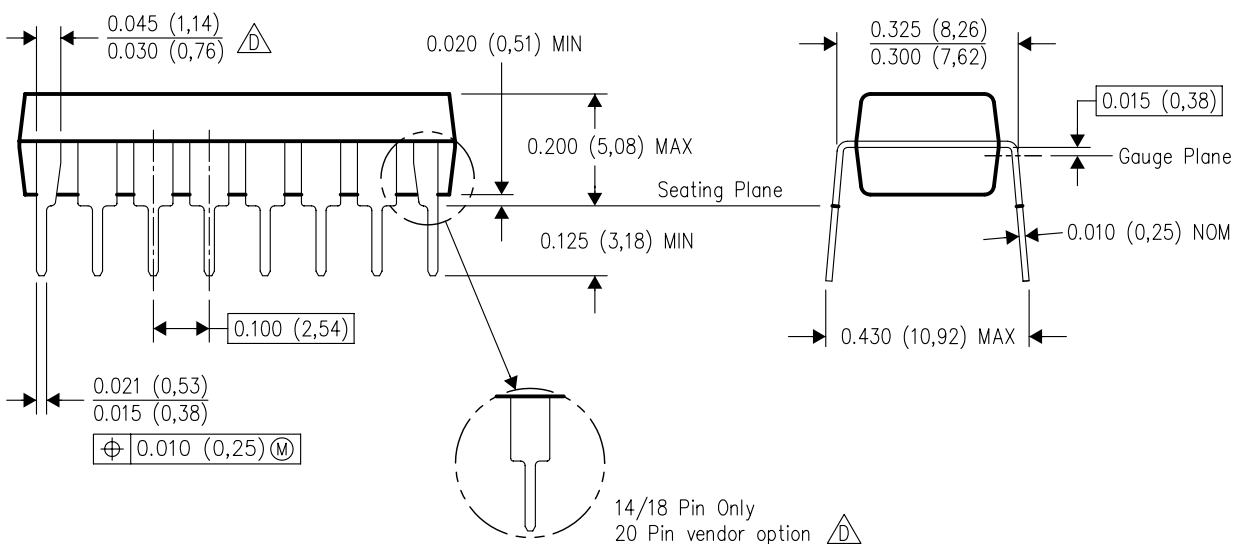
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



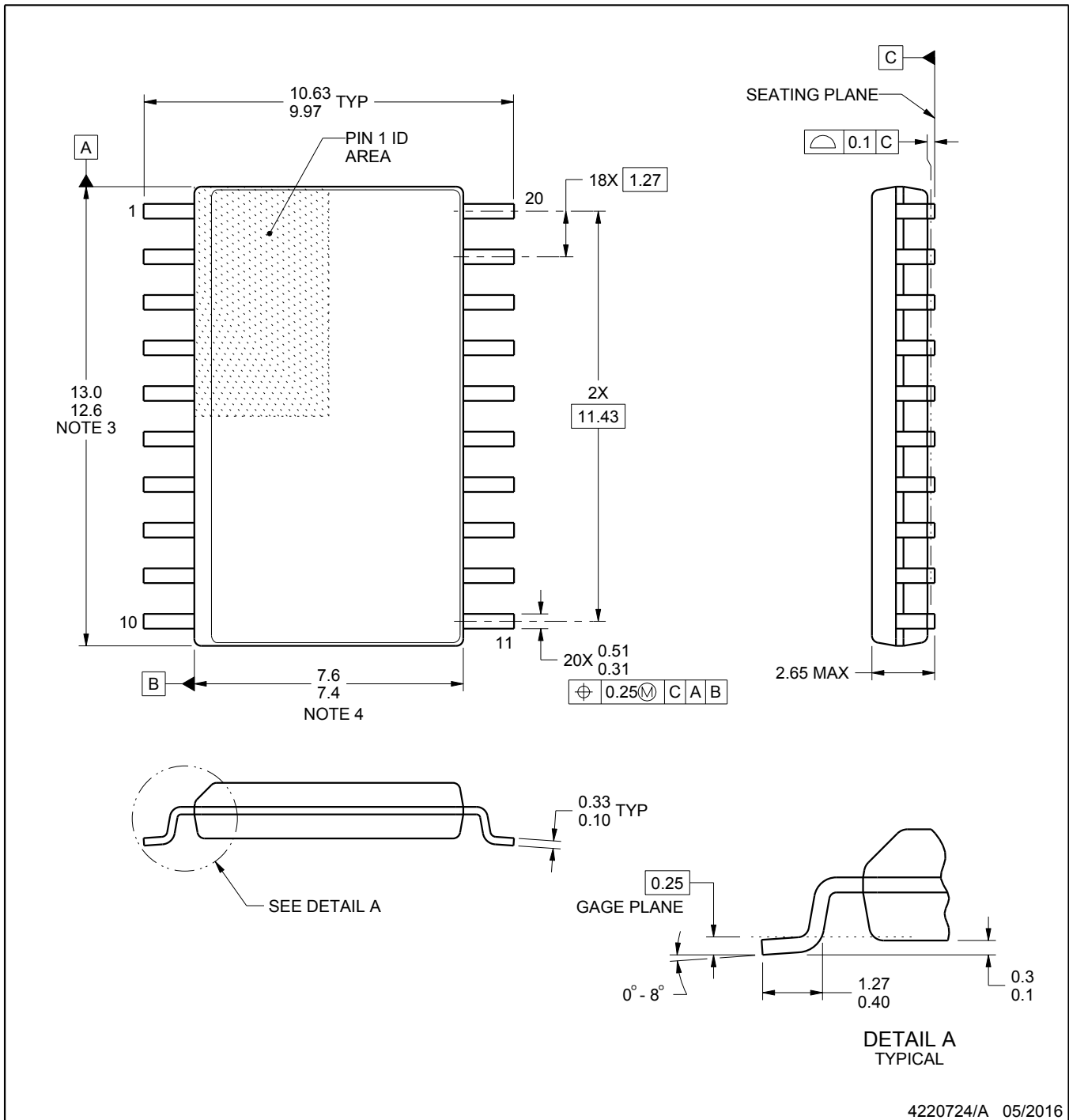
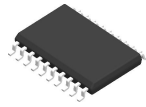
| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



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## NOTES:

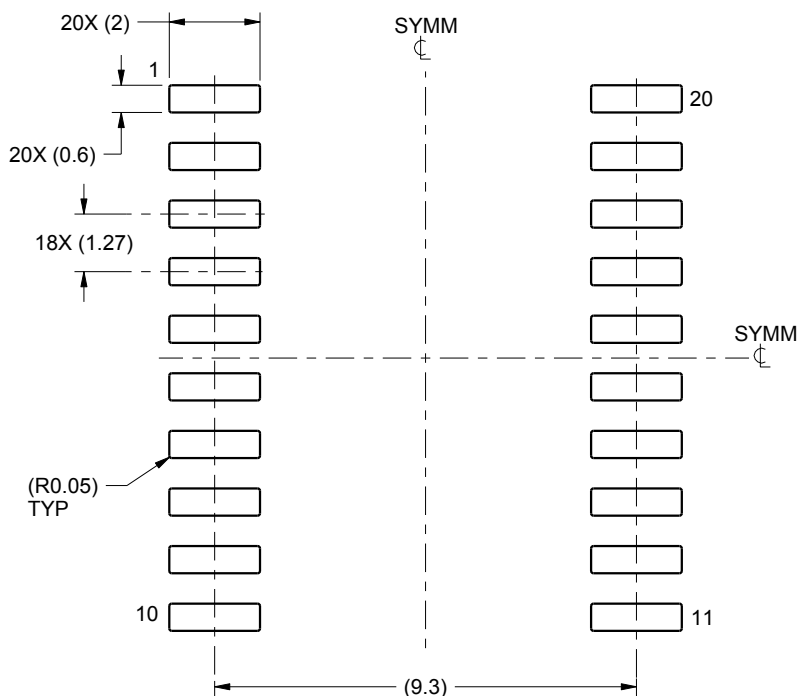
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

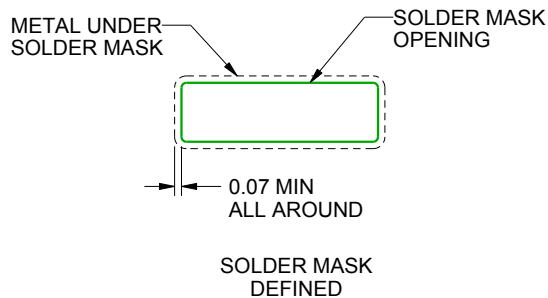
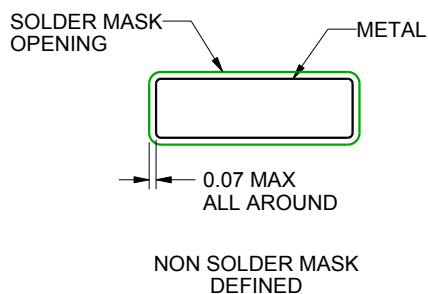
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

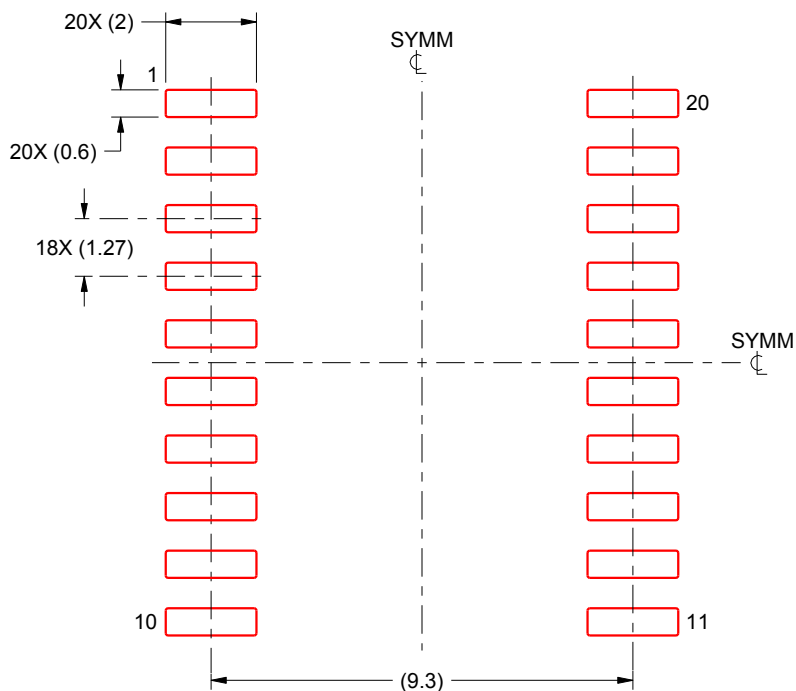
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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