# SNx4LS06 Hex Inverter Buffers and Drivers With Open-Collector High-Voltage Outputs

## 1 Features

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

## 2 Applications

- Factory Automation
- Building Automation
- Line Drivers
- Electronic Point of Sale
- Desktop or Notebook PCs

## 3 Description

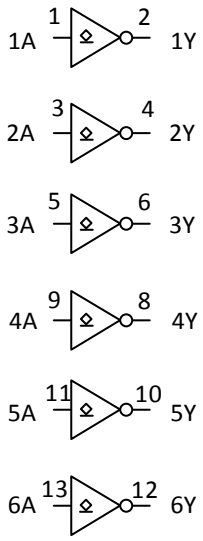
The SNx4LS06 devices feature high-voltage, open-collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The SNx4LS06 devices have a rated output voltage of 30 V.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN54LS06 | CDIP (14) | 19.50 mm × 6.92 mm |
| | LCCC (20) | 8.89 mm × 8.89 mm |
| SN74LS06D | SOIC (14) | 8.65 mm × 3.91 mm |
| SN74LS06DB | SSOP (14) | 5.30 mm × 6.20 mm |
| SN74LS06N | PDIP (14) | 19.30 mm × 6.35 mm |
| SN74LS06NS | SOP (14) | 5.30 mm × 10.20 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**




Pin numbers shown are for the D, DB, J, N, and NS packages.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (February 2004) to Revision F | Page |
|---|---|
| • Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Added Military Disclaimer to Features list | 1 |
| • Added Applications. | 1 |
| • Changed values in the *Thermal Information* table to align with JEDEC standards | 5 |


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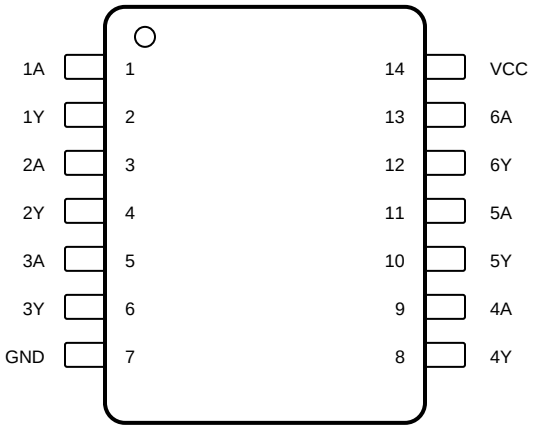
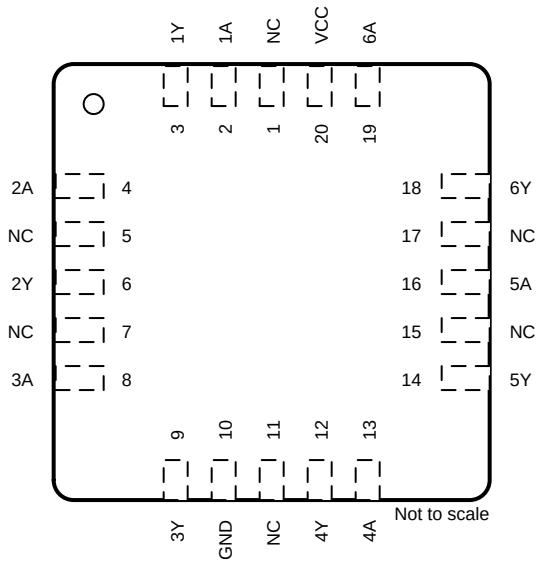
# 5 Pin Configuration and Functions

**D, DB, J, N, and NS Package**
**14-Pin SOIC, SSOP, CDIP, PDIP, and SOP**
**Top View**




Not to scale

**FK Package**
**20-Pin LCCC**
**Top View**




Not to scale

**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, SSOP, CDIP, PDIP, SOP | LCCC | | |
| 1A | 1 | 2 | I | 1A Input |
| 1Y | 2 | 3 | O | 1Y Output |
| 2A | 3 | 4 | I | 2A Input |
| 2Y | 4 | 6 | O | 2Y Output |
| 3A | 5 | 8 | I | 3A Input |
| 3Y | 6 | 9 | O | 3Y Output |
| 4A | 9 | 13 | I | 4A Input |
| 4Y | 8 | 12 | O | 4Y Output |
| 5A | 11 | 16 | I | 5A Input |
| 5Y | 10 | 14 | O | 5Y Output |
| 6A | 13 | 19 | I | 6A Input |
| 6Y | 12 | 18 | O | 6Y Output |
| GND | 7 | 10 | — | Ground |
| NC | — | 1, 5, 7, 11, 15, 17 | — | No internal connection |
| $V_{CC}$ | 14 | 20 | — | Power pin |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 7 | V |
| Input voltage, $V_I$(2) | | 7 | V |
| Output voltage, $V_O$ (SNx4LS06)(2)(3) | | 30 | V |
| Absolute maximum junction temperature, $T_J$ | | 150 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) This is the maximum voltage that must be applied to any output when it is in the off state.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±2000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Tested on N package

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage (SNx4LS06) | | | | 30 | V |
| $I_{OL}$ | Low-level output current | SN54LS06 | | | 30 | mA |
| | | SN74LS06 | | | 40 | |
| $T_A$ | Operating free-air temperature | SN54LS06 | –55 | | 125 | °C |
| | | SN74LS06 | 0 | | 70 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74LS06 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 85.8 | 97.4 | 50.2 | 82.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 44 | 49.8 | 37.5 | 40.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 40.3 | 44.5 | 30 | 41.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 11.1 | 16.5 | 22.3 | 12.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.1 | 44 | 29.9 | 41.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS[1] | | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = MIN, $I_I$ = –12 mA | | | | –1.5 | V |
| $I_{OH}$ | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{OH}$ = 30 V, SNx4LS06 | | | | 0.25 | mA |
| $V_{OL}$ | $V_{CC}$ = MIN, $V_{IH}$ = 2 V | $I_{OL}$ = 16 mA | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 30 mA | | | 0.7 | |
| | | $I_{OL}$ = 40 mA, SN74LS06 | | | 0.7 | |
| $I_I$ | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 1 | mA |
| $I_{IH}$ | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | –0.2 | mA |
| $I_{CCH}$ | $V_{CC}$= MAX | | | | 18 | mA |
| $I_{CCL}$ | $V_{CC}$= MAX | | | | 60 | mA |

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Recommended Operating Conditions*.
(2) All typical values are at $V_{CC}$ = 5 V, and $T_A$ = 25°C.

## 6.6 Switching Characteristics

$V_{CC}$ = 5 V and $T_A$ = 25°C (see Figure 2)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{PLH}$ | From A (input) to Y (output), $R_L$= 110 Ω, $C_L$ = 15 pF | 7 | | 15 | ns |
| $t_{PHL}$ | From A (input) to Y (output), $R_L$= 110 Ω, $C_L$ = 15 pF | 10 | | 20 | |

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## 6.7 Typical Characteristics

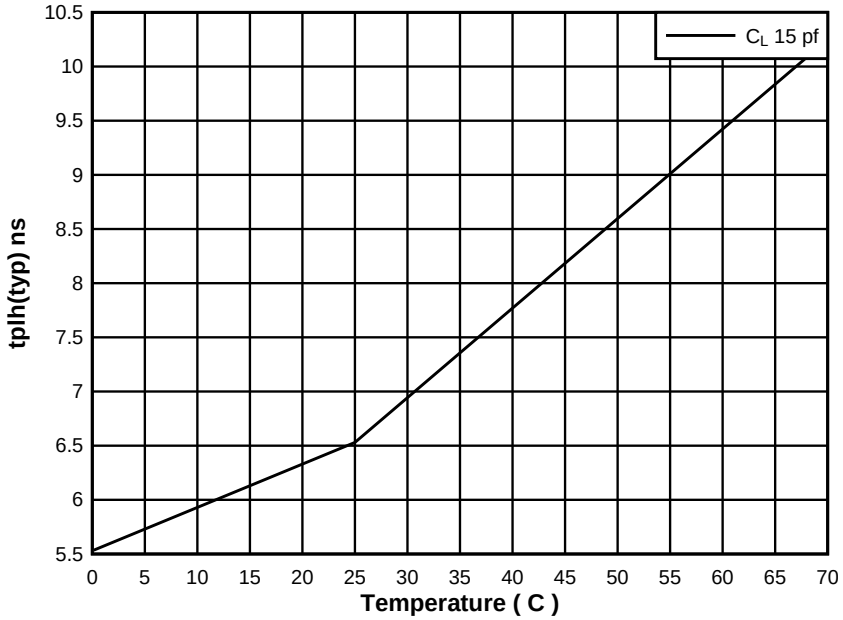


**Figure 1. Propagation Delay vs Temperature**


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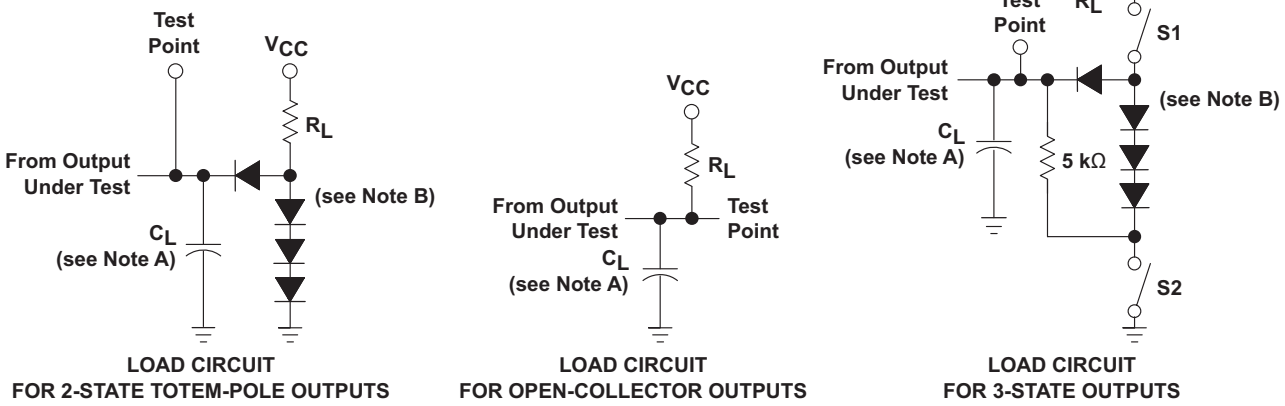
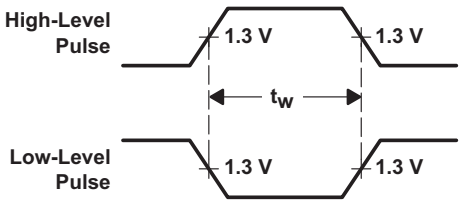
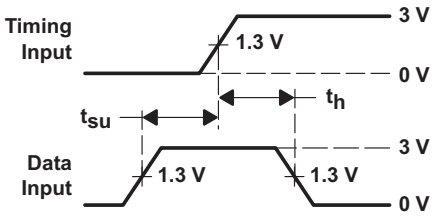
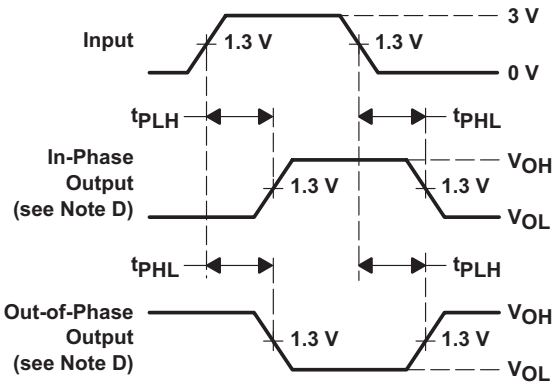
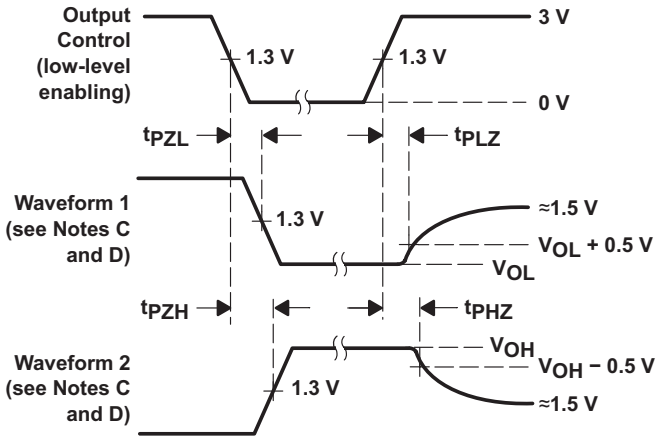
# 7 Parameter Measurement Information




A. $C_L$ includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

D. S1 and S2 are closed for $t_{PLH}$, $t_{PHL}$, $t_{PHZ}$, and $t_{PLZ}$; S1 is open and S2 is closed for $t_{PZH}$; S1 is closed and S2 is open for $t_{PZL}$.

E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ ≈ 50 Ω, $t_r$≤ 1.5 ns, $t_f$≤ 2.6 ns.

G. The outputs are measured one at a time, with one input transition per measurement.

**Figure 2. Load Circuits and Voltage Waveforms**

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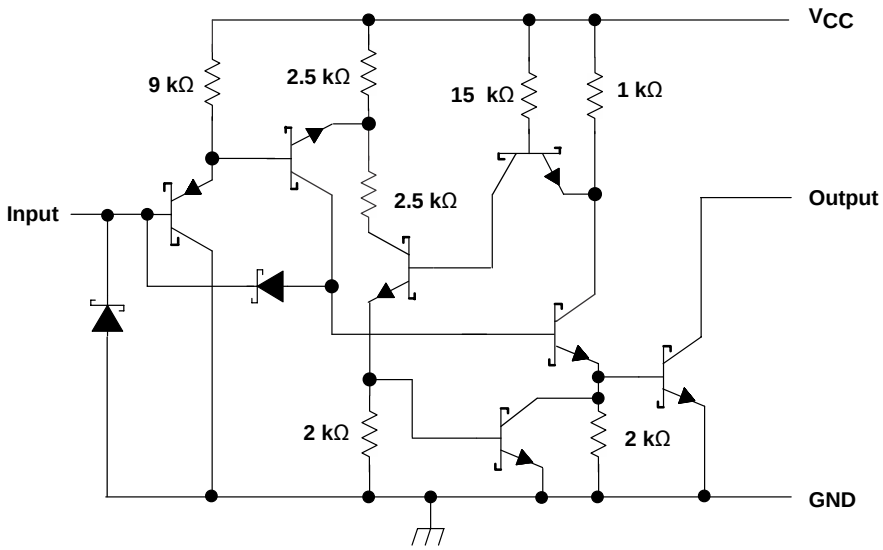
# 8 Detailed Description

## 8.1 Overview

The SNx4LS06 devices are open-collector output inverters. The maximum sink current for the SN54LS06 device is 30 mA, and for the SN74LS06 device it is 40 mA. These devices are compatible with most TTL families. Inputs are diode-clamped to minimize transmission effects, which simplifies design. Typical power dissipation is 175 mW, and average propagation delay time is 8 ns.

## 8.2 Functional Block Diagram

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## 8.3 Feature Description

The SNx4LS06 devices can convert most TTL voltage circuit voltage level to MOS levels. The devices have high sink-current capability of up to 40 mA. The open-collector driver can be used for typical applications including Indicator lamps and relays.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4LS06 devices.

**Table 1. Function Table**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | Hi-Z |


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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The open-collector device is suitable for high-drive and high-voltage translation applications.

## 9.2 Typical Application

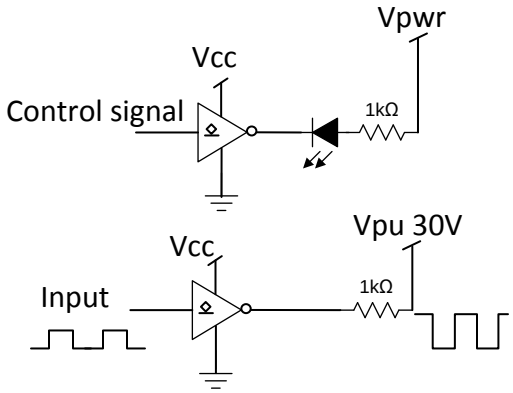


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**Figure 3. Application Schematic**

### 9.2.1 Design Requirements

The SNx4LS06 are open-collector devices which can sink current (up to 40 mA on SN74LS06). The devices can be used in applications such as LED drivers and voltage translation using pullup resistors.

### 9.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in the *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommended output conditions:
   - Load currents must not exceed ($I_O$ max) per output.
   - Outputs can be pulled up to 30 V.

## Typical Application (continued)

### 9.2.3 Application Curve

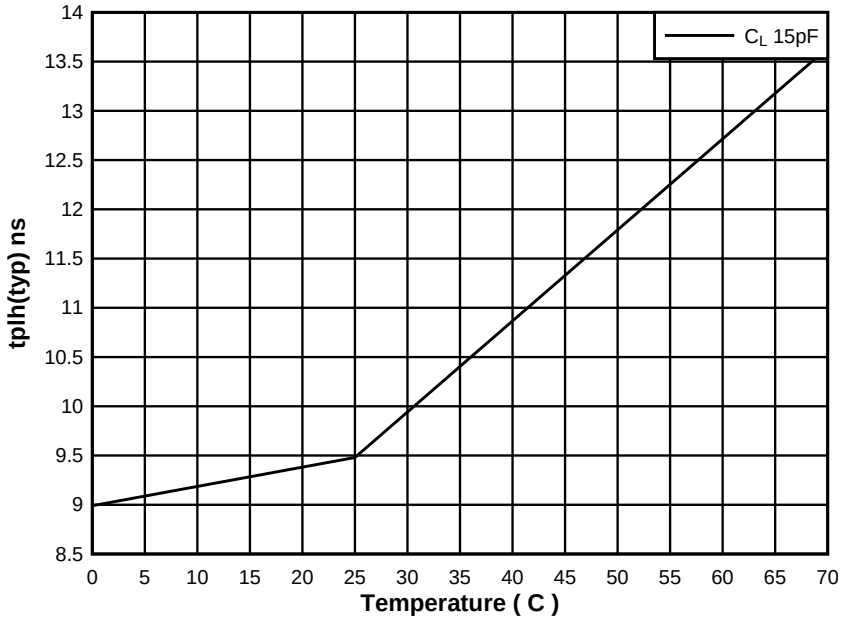


**Figure 4. Propagation Delay vs Temperature**


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# 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor, and if there are multiple $V_{CC}$ pins, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input and gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following rules must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or $V_{CC}$ whichever make more sense or is more convenient. TI recommends keeping the signal lines as short and as straight as possible (see Figure 6). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1" long. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω as required by the application.

## 11.2 Layout Examples

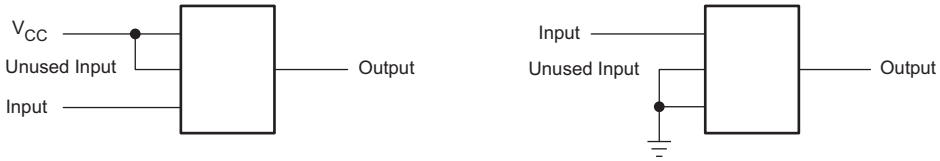


**Figure 5. Layout Schematic**

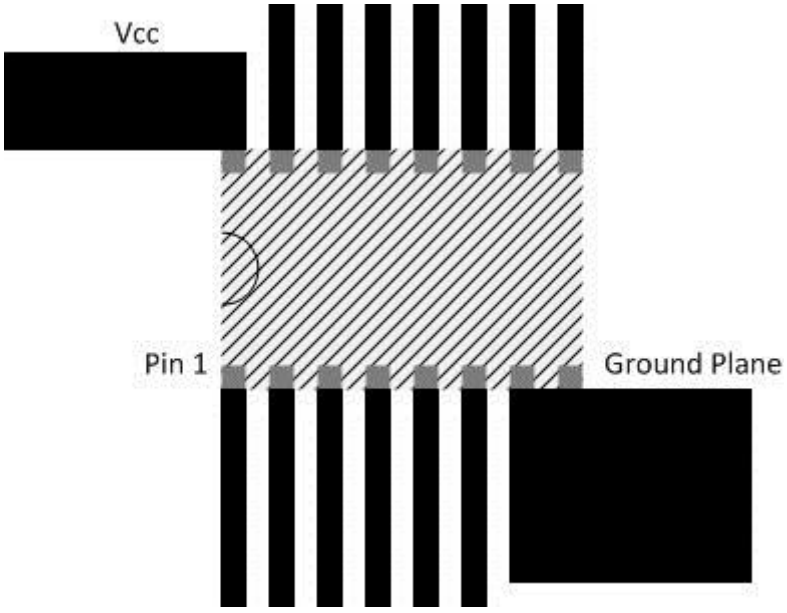


**Figure 6. Signal Line Layout**

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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

*Implications of Slow or Floating CMOS Inputs* (SCBA004)

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54LS06 | Click here | Click here | Click here | Click here | Click here |
| SN74LS06 | Click here | Click here | Click here | Click here | Click here |
| SN74LS16 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9861701Q2A | NRND | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9861701Q2A SNJ54LS 06FK |
| 5962-9861701QCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9861701QCA SNJ54LS06J |
| SN54LS06J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS06J |
| SN54LS06J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54LS06J |
| SN74LS06D | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS06 |
| SN74LS06D.A | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS06 |
| SN74LS06DBR | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS06 |
| SN74LS06DBR.A | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS06 |
| SN74LS06DG4 | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS06 |
| SN74LS06DR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS06 |
| SN74LS06DR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS06 |
| SN74LS06DRE4 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS06 |
| SN74LS06N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS06N |
| SN74LS06N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS06N |
| SN74LS06NE4 | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS06N |
| SN74LS06NS.A | Active | Production | SOP (NS) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS06 |
| SN74LS06NSR | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS06 |
| SN74LS06NSR.A | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS06 |
| SN74LS06NSRG4 | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS06 |
| SNJ54LS06FK | NRND | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9861701Q2A SNJ54LS 06FK |
| SNJ54LS06FK.A | NRND | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9861701Q2A SNJ54LS 06FK |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SNJ54LS06J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9861701QCA SNJ54LS06J |
| SNJ54LS06J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9861701QCA SNJ54LS06J |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LS06, SN74LS06 :**

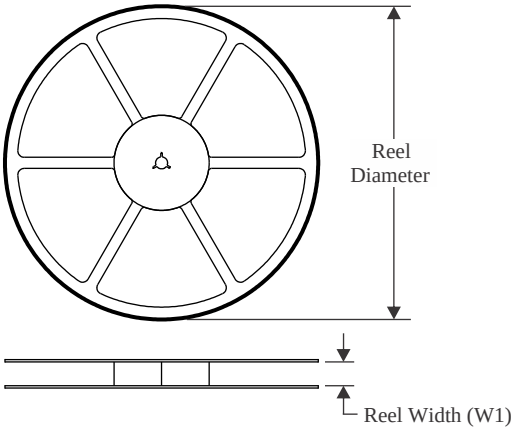
- Catalog : SN74LS06
- Military : SN54LS06

NOTE: Qualified Version Definitions:

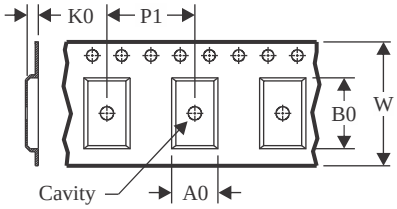
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

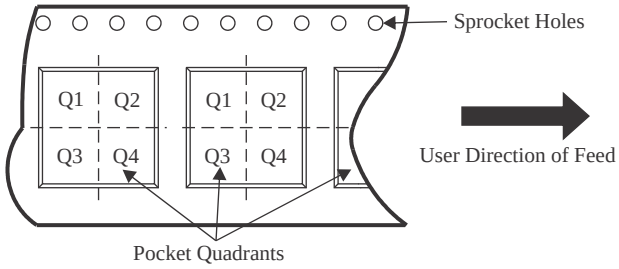



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

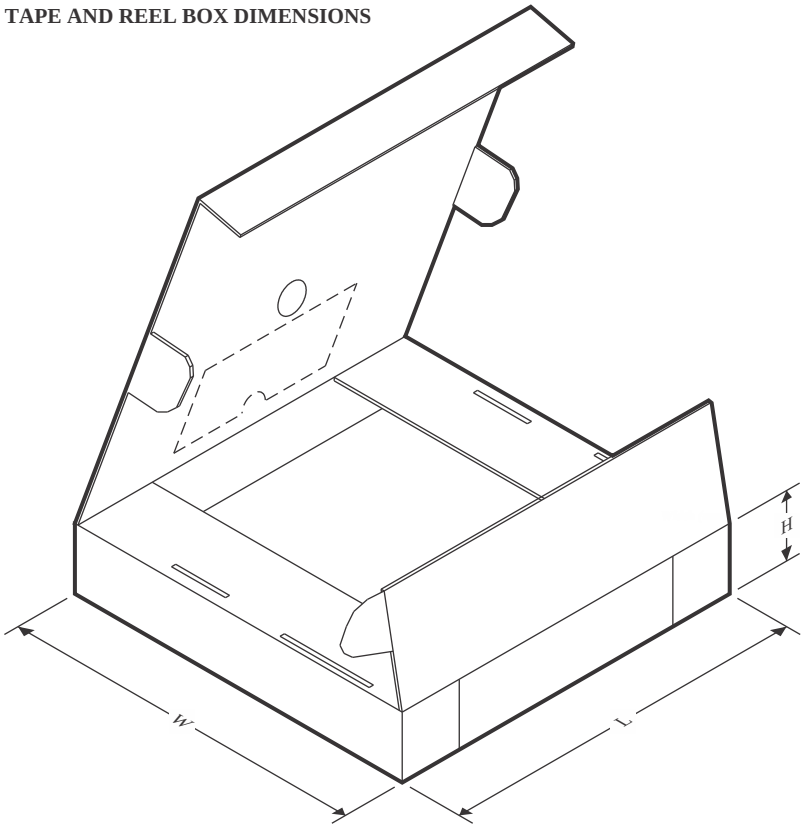
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS06DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LS06DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS06NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |

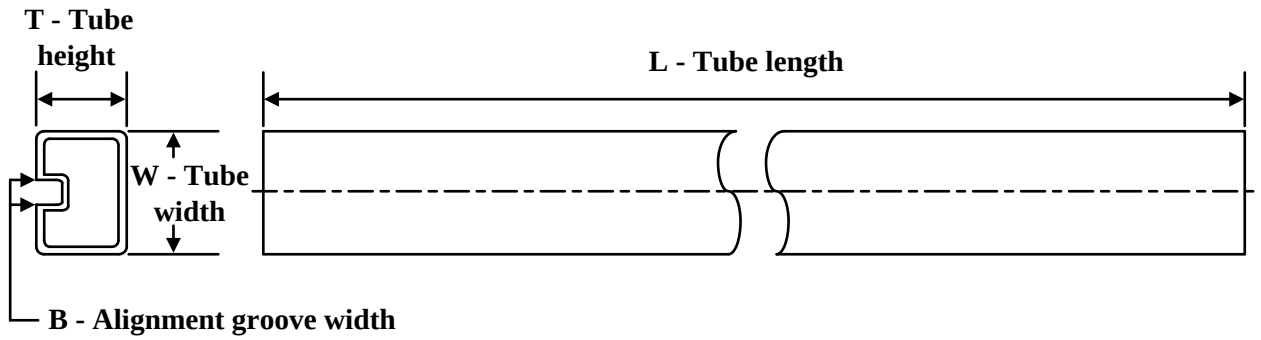
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

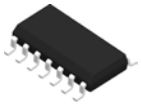
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS06DBR | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LS06DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74LS06NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9861701Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74LS06D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LS06D.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LS06DG4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LS06N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS06N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS06N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS06N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS06NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS06NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS06NS.A | NS | SOP | 14 | 50 | 530 | 10.5 | 4000 | 4.1 |
| SNJ54LS06FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LS06FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

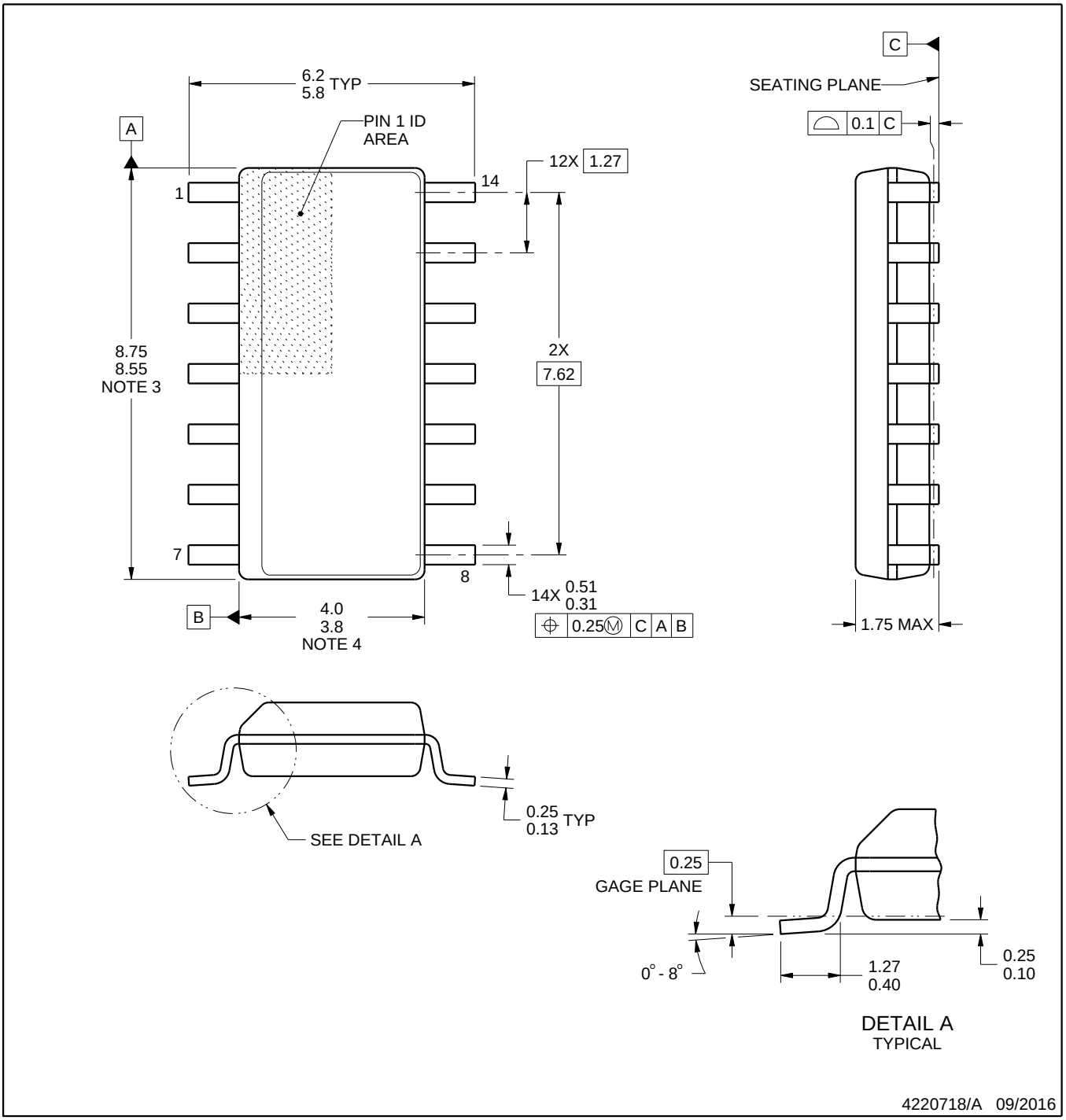


# PACKAGE OUTLINE

## D0014A

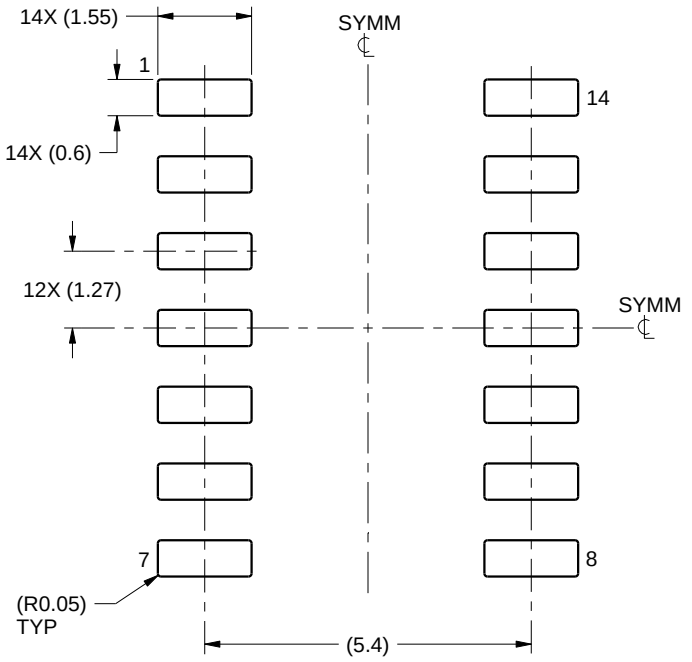
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

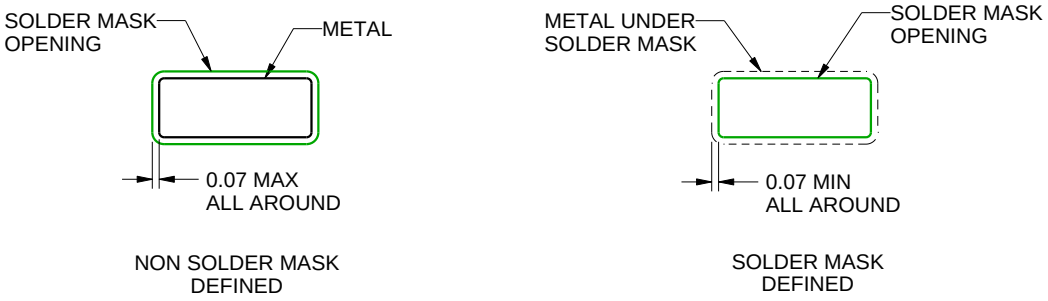



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

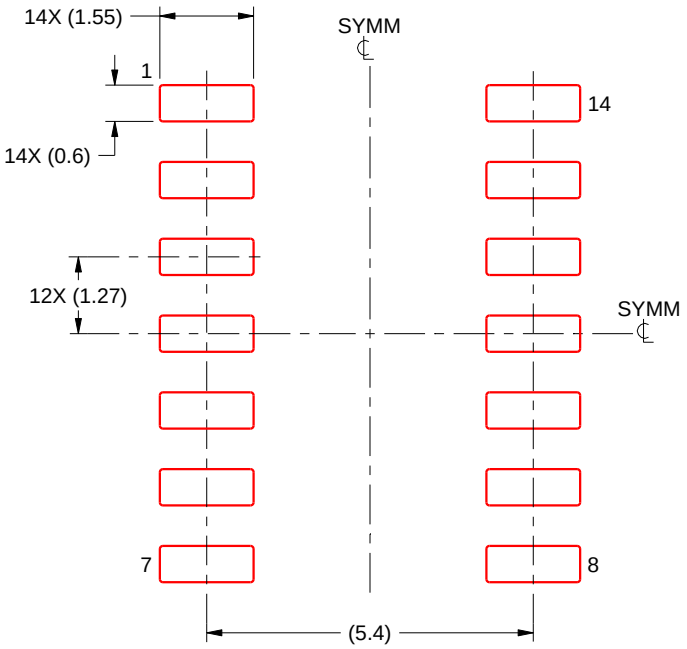
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

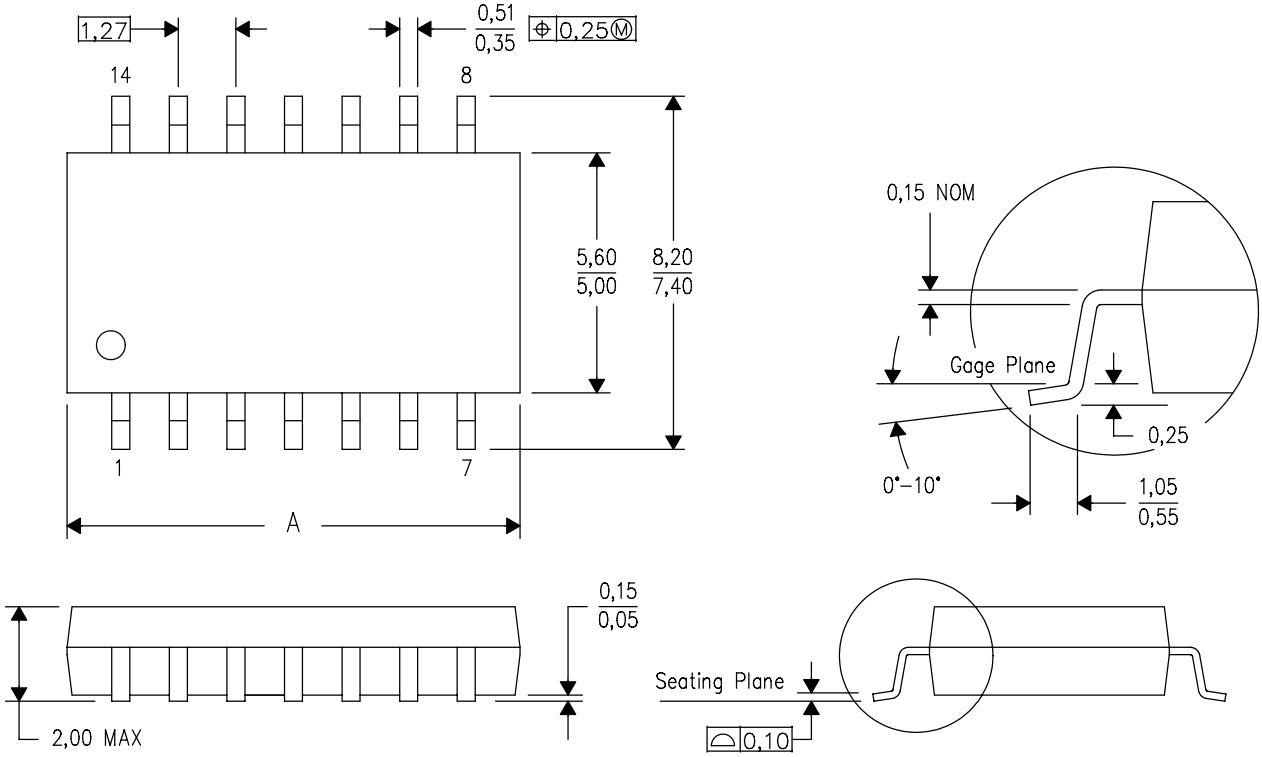
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

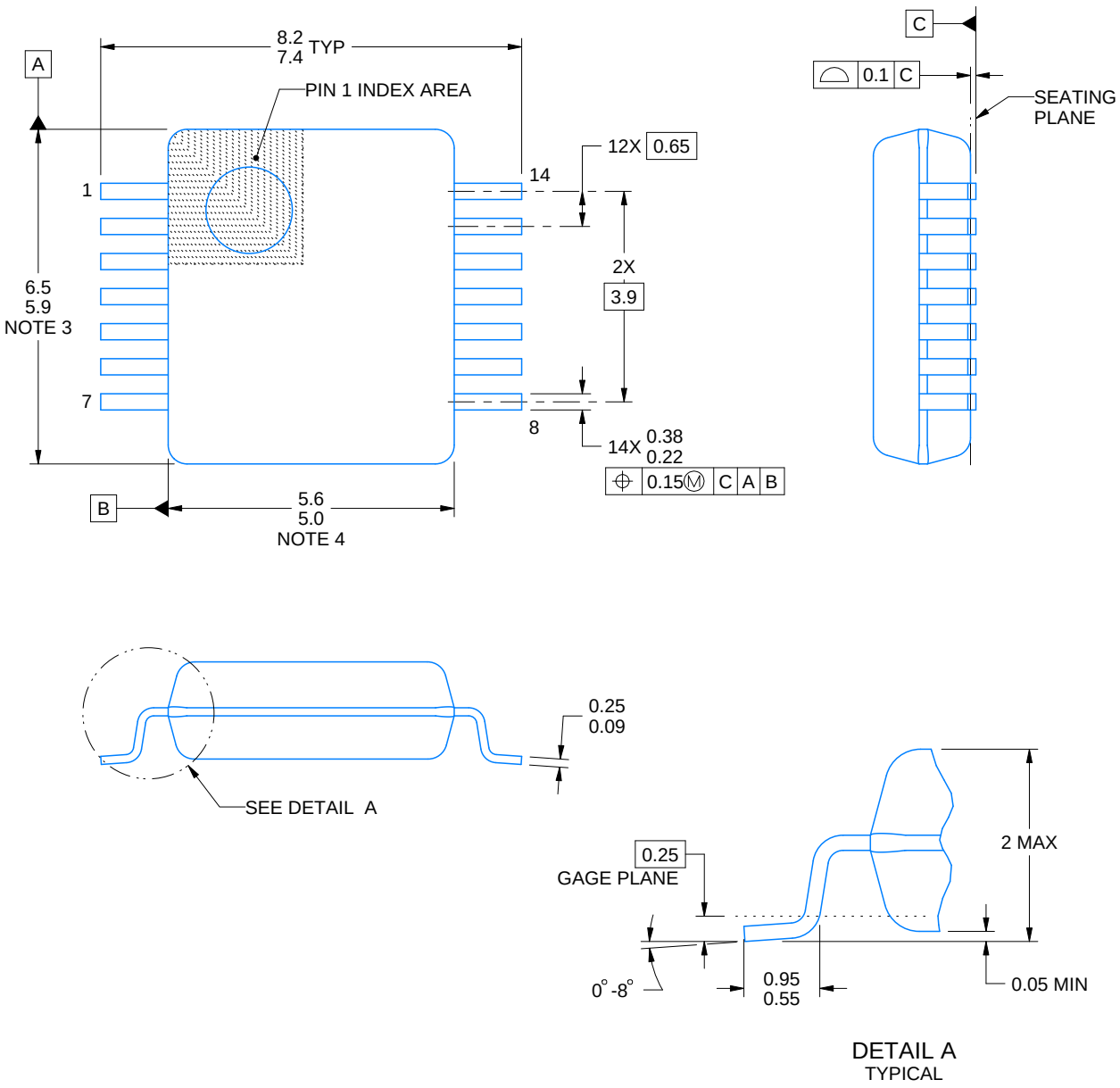
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# PACKAGE OUTLINE

## DB0014A

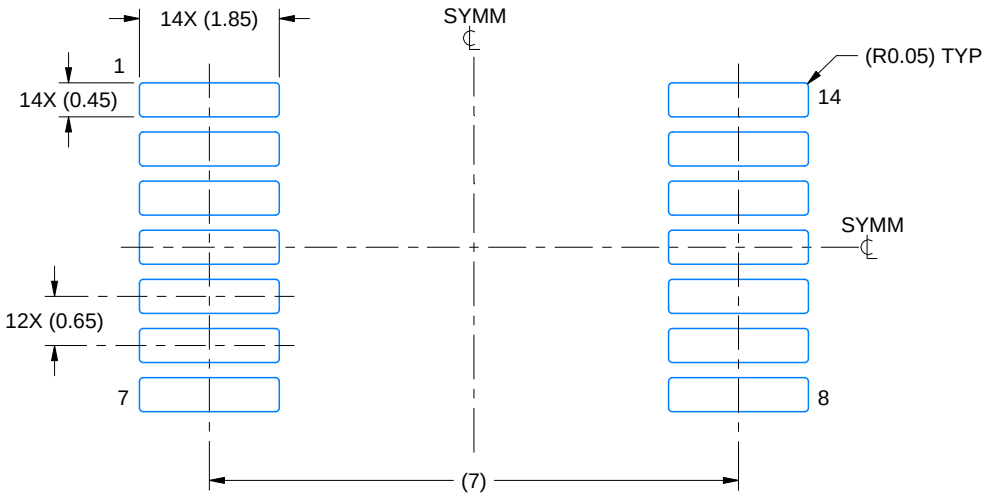
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

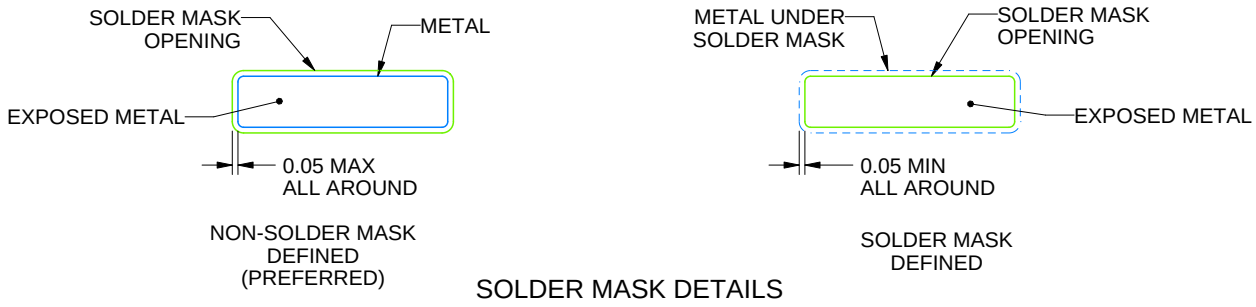



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

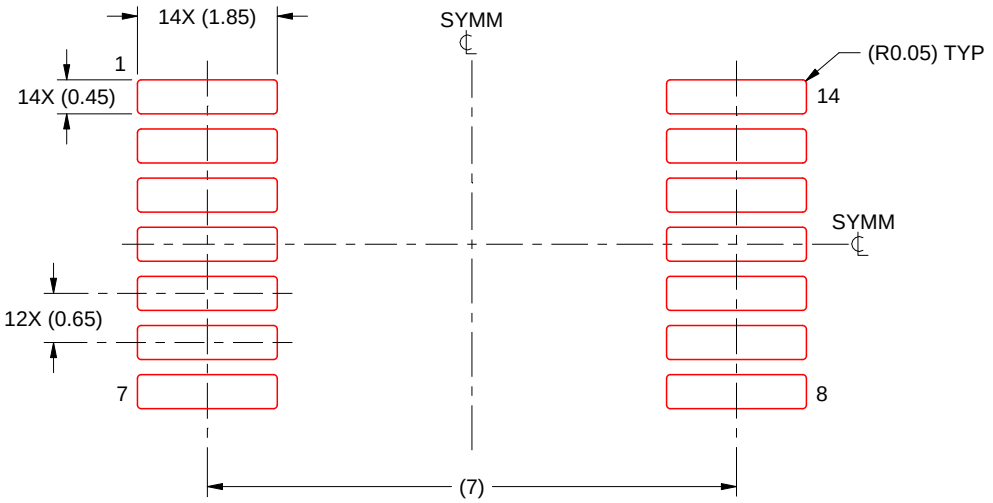



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

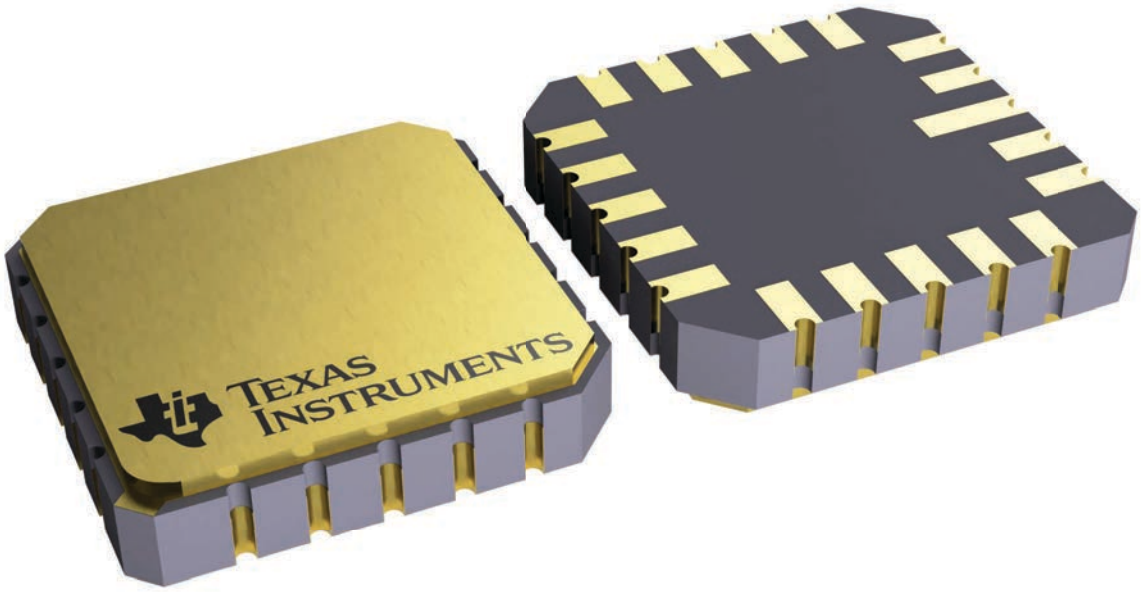
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

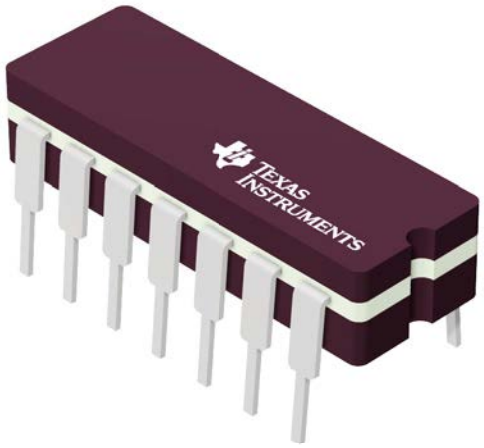



4229370VA\

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

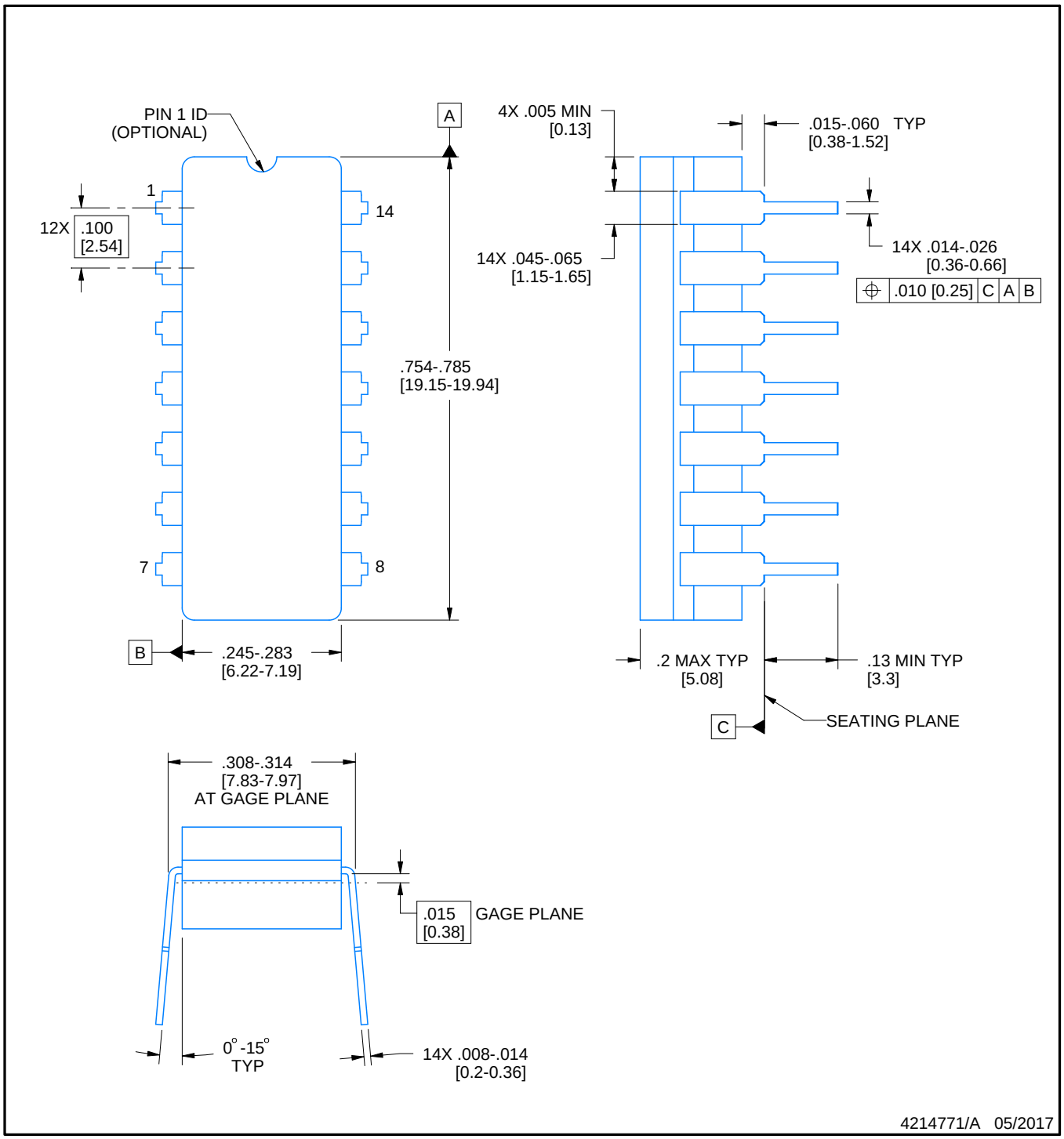
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

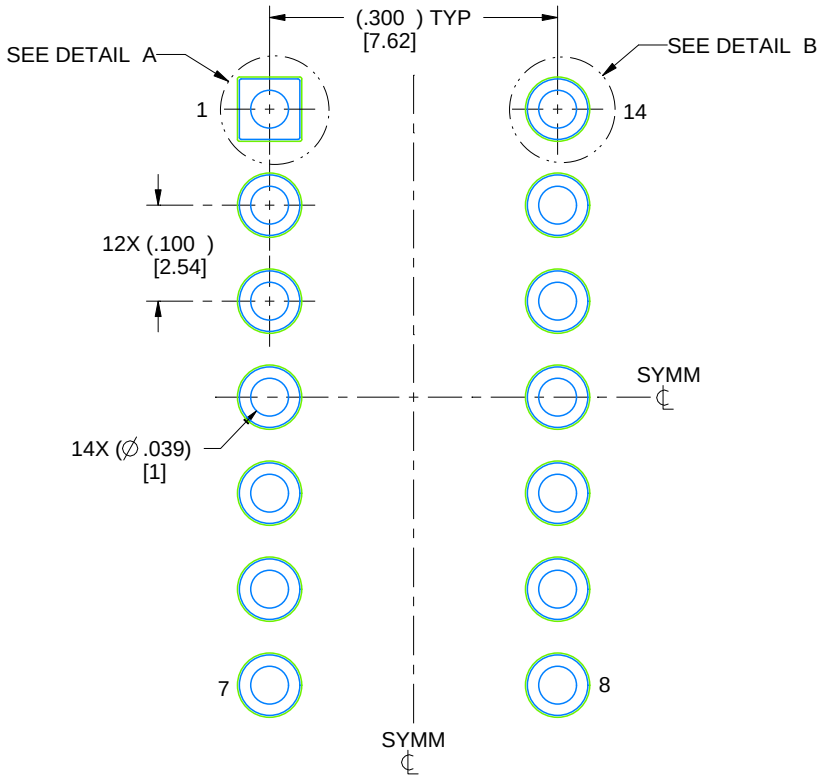
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

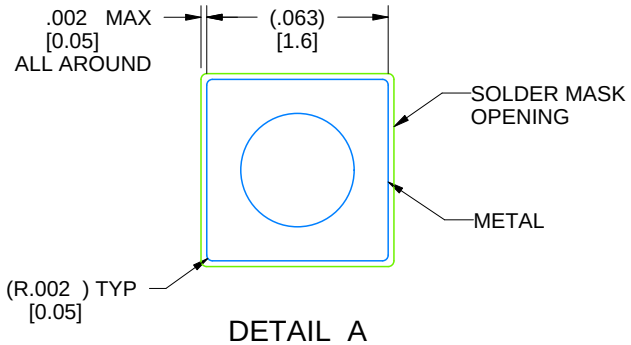
## J0014A

## CDIP - 5.08 mm max height

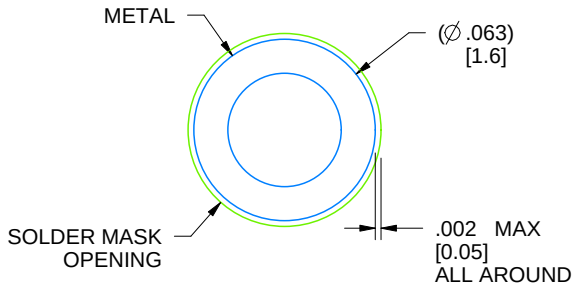
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X



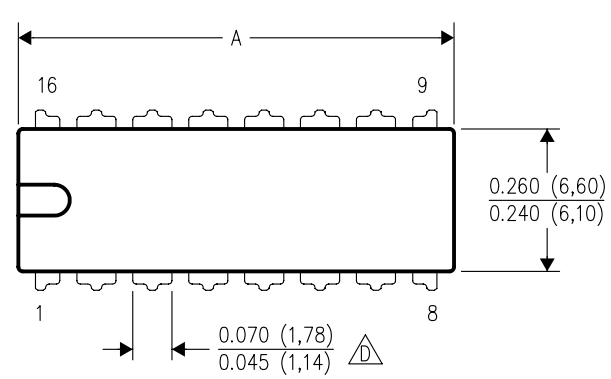

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

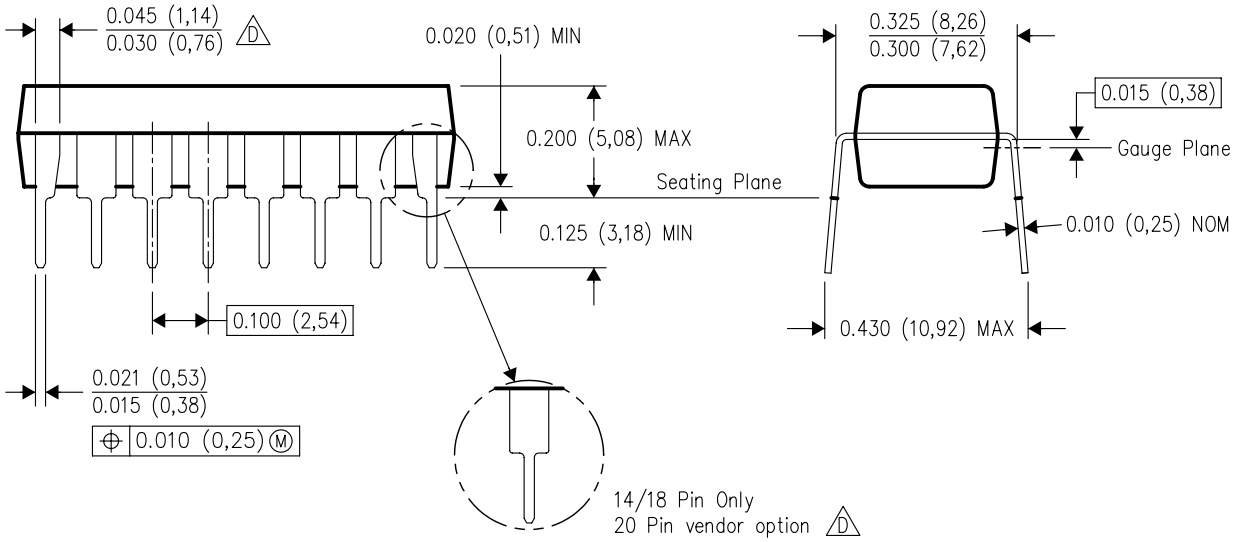
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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