

SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

SDLS007

D2635. JANUARY 1981 - REVISED MARCH 1988

- 8-Bit Parallel Storage Register Inputs ('LS597)
- Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('LS598)
- Shift Register has Direct Overriding Load and Clear
- Accurate Shift-Frequency . . . DC to 20 MHz

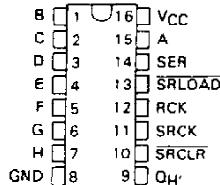
description

The 'LS597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

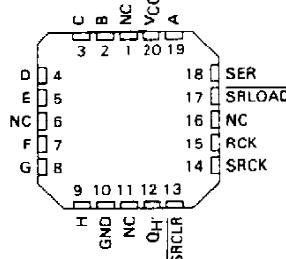
The 'LS598 comes in a 20-pin package and has all the features of the 'LS597 plus 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

SN54LS597 . . . J OR W PACKAGE
SN74LS597 . . . N PACKAGE

(TOP VIEW)

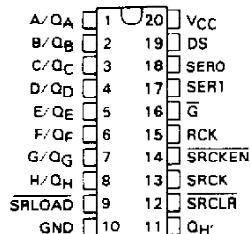


SN54LS597 . . . FK PACKAGE
(TOP VIEW)

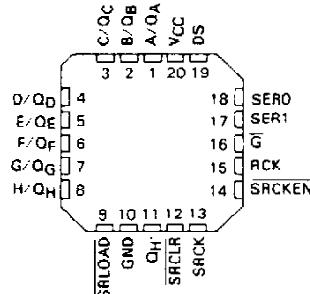


SN54LS598 . . . J OR W PACKAGE
LS598 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS598 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

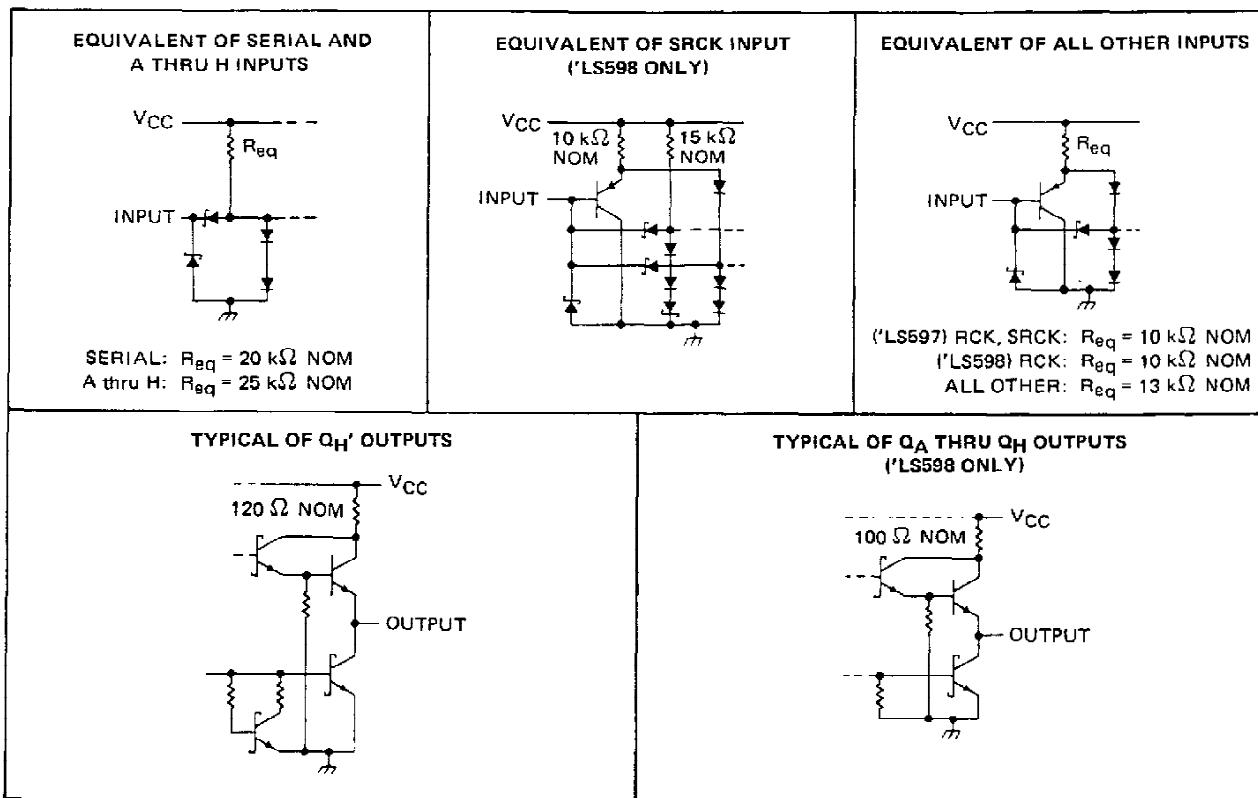
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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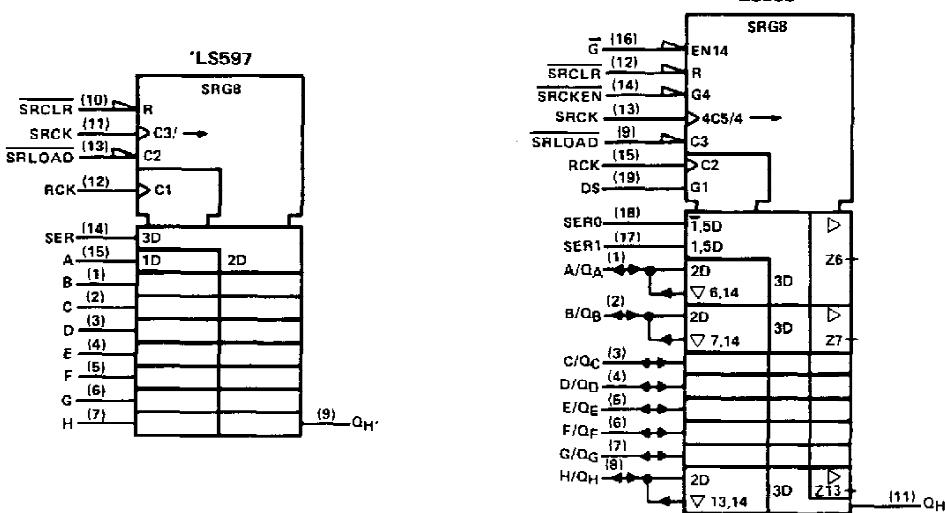
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SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

schematics of inputs and outputs



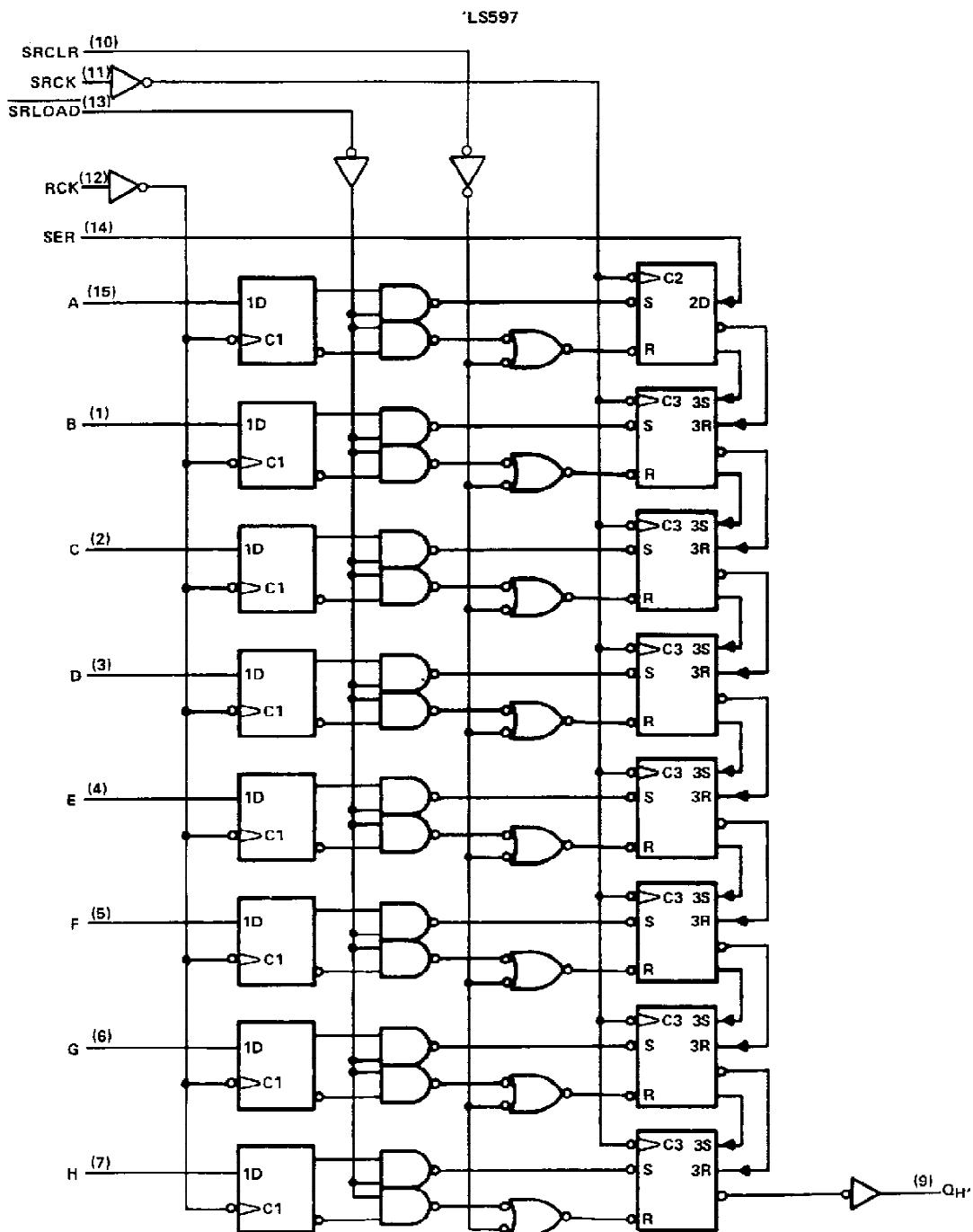
logic symbols[†]



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

SN54LS597, SN74LS597
8-BIT SHIFT REGISTERS WITH INPUT LATCHES

logic diagram (positive logic)



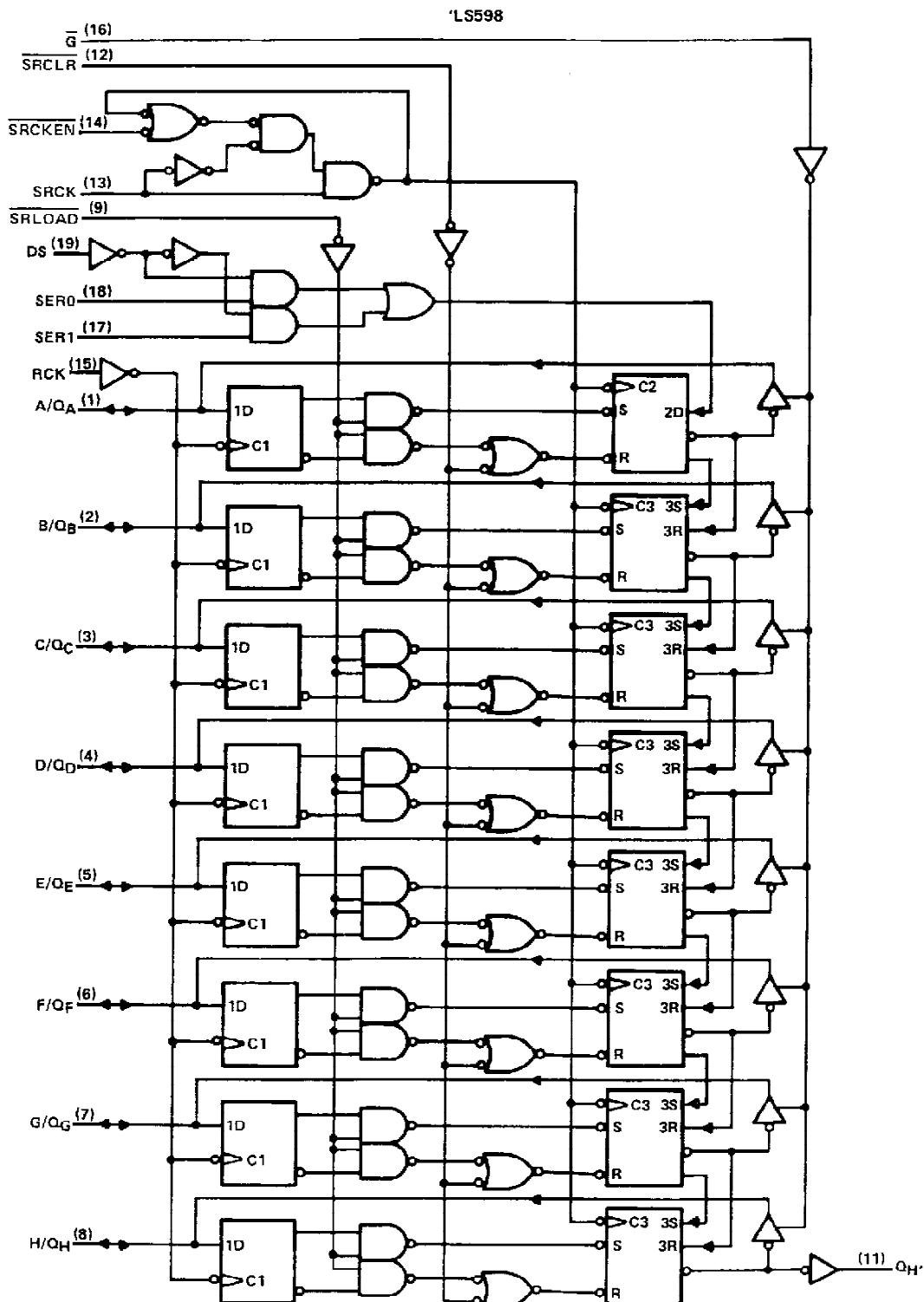
Pin numbers shown are for DW, J, N, and W packages.

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SN54LS598, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

logic diagram (positive logic)



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SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (excluding I/O ports)	7 V
Off-state output voltage (including I/O ports)	5.5 V
Operating free-air temperature range: SN54LS597, SN54LS598	-55°C to 125°C
SN74LS597, SN74LS598	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current	Q _H '			-1		-1	mA
		Q _A thru Q _H , 'LS598 only			-1		-2.6	
I _{OL}	Low-level output current	Q _H '			8		16	mA
		Q _A thru Q _H , 'LS598 only			12		24	
f _{SCK}	Shift clock frequency	0		20	0		20	MHz
t _W	Pulse duration	SRCK	high	15	15			ns
			low	35	35			
		RCK		20	20			
		SRCLR		20	20			
		SRLOAD		40	40			
t _{su}	Setup time	Data before RCK↑		20	20			ns
		DS before SRCK↑ ('LS598 only)		30	30			
		SRCKEN low before SRCK↑ ('LS598 only)		20	20			
		SRCLR inactive before SRCK↑		25	25			
		SRLOAD inactive before SRCK↑		30	30			
		RCK↑ before SRLOAD↑ (see Note 2)		40	40			
		SER before SRCK↑		20	20			
t _h	Hold time	0		0	0			ns
TA	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: The RCK↑ before SRLOAD↑ setup time ensures the data saved by RCK↑ will also be loaded into the shift register.

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SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]			SN54LS [‡]			SN74LS [‡]			UNIT
					MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IK}		V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5			V
V _{OH}	'LS598 Q	V _{CC} = MIN, V _{IH} = 2 V,		I _{OH} = -1 mA	2.4	3.2					V
		V _{IIL} = MAX		I _{OH} = -2.6 mA				2.4	3.1		
	Q _H			I _{OH} = -1 mA	2.4	3.2		2.4	3.2		
V _{OL}	'LS598 Q	V _{CC} = MIN, V _{IH} = 2 V,		I _{OL} = 12 mA	0.25 0.4			0.25	0.4		V
		V _{IIL} = MAX		I _{OL} = 24 mA				0.35	0.5		
	Q _H			I _{OL} = 8 mA	0.25 0.4			0.25	0.4		
				I _{OL} = 16 mA				0.35	0.5		
I _{OZH}	'LS598 Q	V _{CC} = MAX, V _{IH} = 2 V,		V _{IIL} = MAX,	20			20	20		μA
I _{OZL}	'LS598 Q	V _{CC} = MAX, V _{IH} = 2 V,		V _{IIL} = MAX,	-0.4			-0.4	-0.4		mA
I _I	'LS598 Q	V _{CC} = MAX		V _I = 5.5 V	0.1			0.1	0.1		mA
	Others			V _I = 7 V	0.1			0.1	0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V		20		20			20	20		μA
I _{IL}	'LS598 SRCK			-0.8			-0.8	-0.8			mA
	SER, A Thru H	V _{CC} = MAX, V _I = 0.4 V		-0.4			-0.4	-0.4			
	Others			-0.2			-0.2	-0.2			
I _{OS} [§]	'LS598 Q	V _{CC} = MAX, V _O = 0 V		-30	-130	-30	-130				mA
	Q _H			-20	-100	-20	-100				
I _{CC}	'LS597	I _{CCH}			35	53		35	53		mA
		I _{CCL}			35	53		35	53		
		I _{CCH}			45	68		45	68		
	'LS598	I _{CCL}			54	80		54	80		
		I _{CCZ}			56	85		56	85		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C

[§] Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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8-BIT SHIFT REGISTERS WITH INPUT LATCHES

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS597			'LS598			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	SRCK	Q	$R_L = 667 \Omega$, $C_L = 45 \text{ pF}$	20	35		20	35		MHz
f_{max}	SRCK	Q_H'	$R_L = 1 \text{ k}\Omega$, $C_L = 30 \text{ pF}$	20	35					MHz
t_{PLH}	SRCK \uparrow	Q_H'			15	23		11	17	ns
t_{PHL}	SPCK \uparrow	Q_H'			20	30		15	23	ns
t_{PLH}	$\overline{SRLOAD}\downarrow$	Q_H'			38	57		28	42	ns
t_{PHL}	$\overline{SRLOAD}\downarrow$	Q_H'			29	44		20	30	ns
t_{PHL}	SRCLR \uparrow	Q_H'			24	36		18	27	ns
t_{PLH}	RCK \uparrow	Q_H'	$R_L = 1 \text{ k}\Omega$, $C_L = 30 \text{ pF}$		41	60		32	48	ns
t_{PHL}	RCK \uparrow	Q_H'	$SRLOAD = L$		32	48		24	36	ns
t_{PLH}	SRCK \uparrow	Q						12	18	ns
t_{PHL}	SRCK \uparrow	Q						19	28	ns
t_{PLH}	$\overline{SRLOAD}\downarrow$	Q						32	48	ns
t_{PHL}	$\overline{SRLOAD}\downarrow$	Q						27	40	ns
t_{PHL}	SRCLR \uparrow	Q						25	38	ns
t_{PZH}	G \downarrow	Q						26	31	ns
t_{PZL}	G \downarrow	Q						29	43	ns
t_{PHZ}	G \uparrow	Q	$R_L = 667 \Omega$, $C_L = 5 \text{ pF}$					25	38	ns
t_{PLZ}	G \uparrow	Q						20	30	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

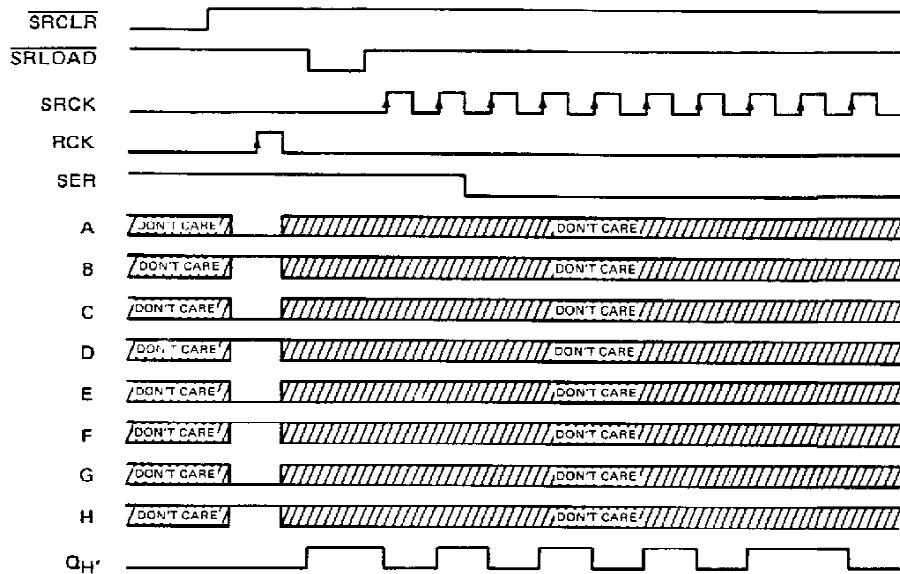
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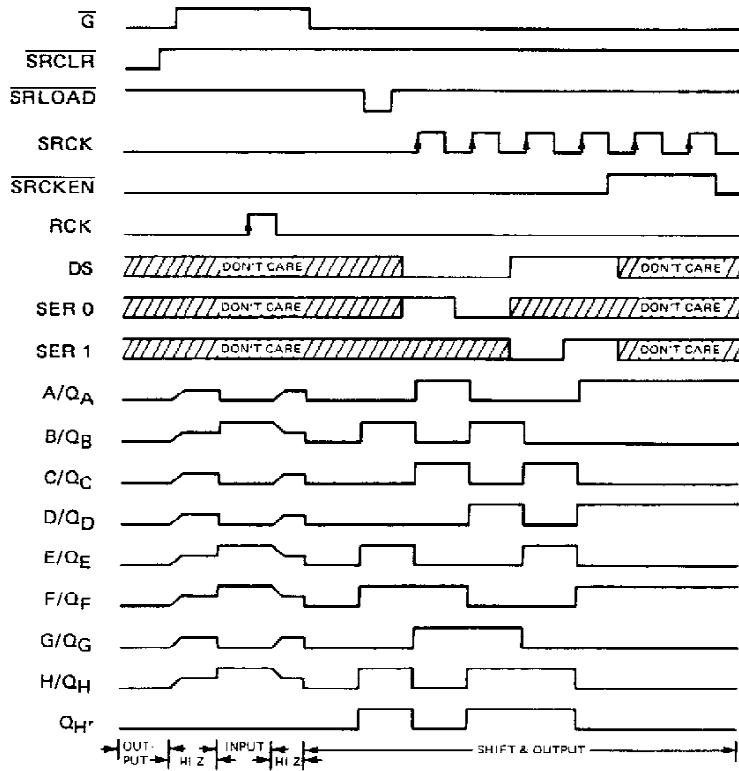
SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

typical operating sequences

'LS597



'LS598



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-89444012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89444012A SNJ54LS597FK
5962-8944401EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J
5962-8944401EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J
5962-8944401FA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W
5962-8944401FA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W
SN74LS597D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS597
SN74LS597D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS597
SN74LS597D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS597
SN74LS597D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS597
SN74LS597N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS597N
SN74LS597N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS597N
SN74LS597N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS597N
SN74LS597N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS597N
SN74LS598N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS598N
SN74LS598N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS598N
SN74LS598N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS598N
SN74LS598N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS598N
SNJ54LS597FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89444012A SNJ54LS597FK
SNJ54LS597FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89444012A SNJ54LS597FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS597FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89444012A SNJ54LS597FK
SNJ54LS597FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89444012A SNJ54LS597FK
SNJ54LS597J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J
SNJ54LS597J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J
SNJ54LS597J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J
SNJ54LS597J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401EA SNJ54LS597J
SNJ54LS597W	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W
SNJ54LS597W	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W
SNJ54LS597W.A	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W
SNJ54LS597W.A	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8944401FA SNJ54LS597W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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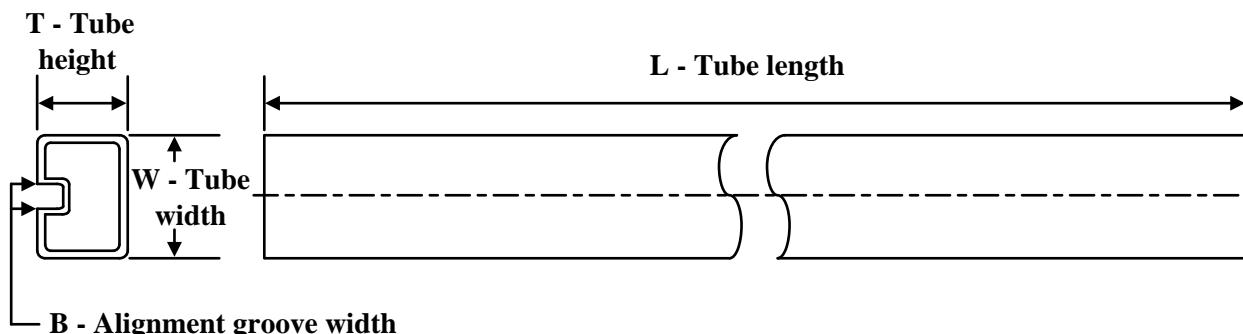
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OTHER QUALIFIED VERSIONS OF SN54LS597, SN74LS597 :

- Catalog : [SN74LS597](#)
- Military : [SN54LS597](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

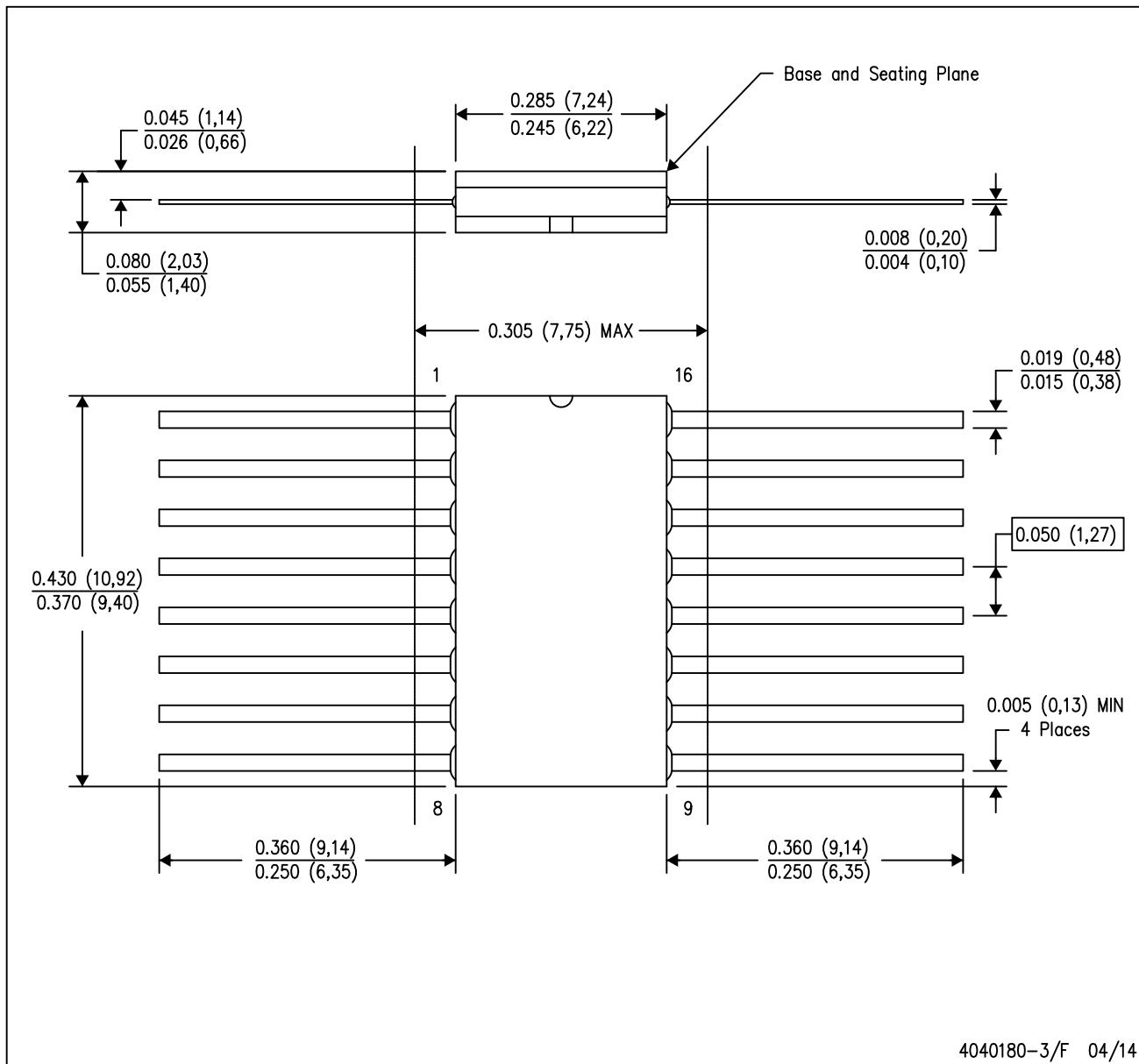
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-89444012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8944401FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS597D	D	SOIC	16	40	507	8	3940	4.32
SN74LS597D.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS597N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS597N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS597N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS597N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS598N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS598N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS597FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS597FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS597W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS597W.A	W	CFP	16	25	506.98	26.16	6220	NA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/F 04/14

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

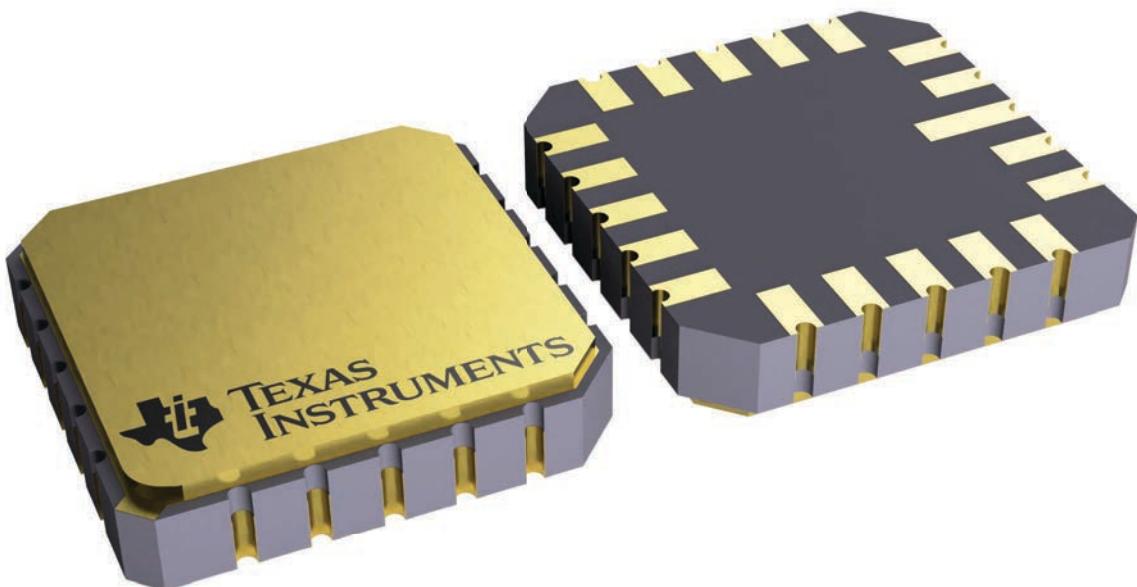
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

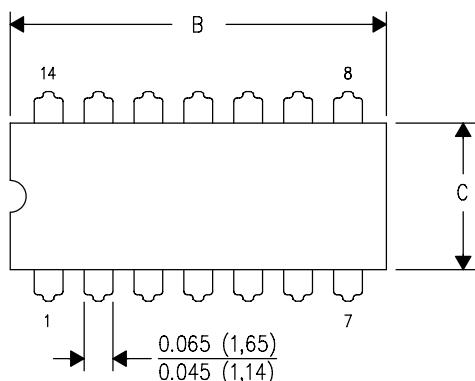


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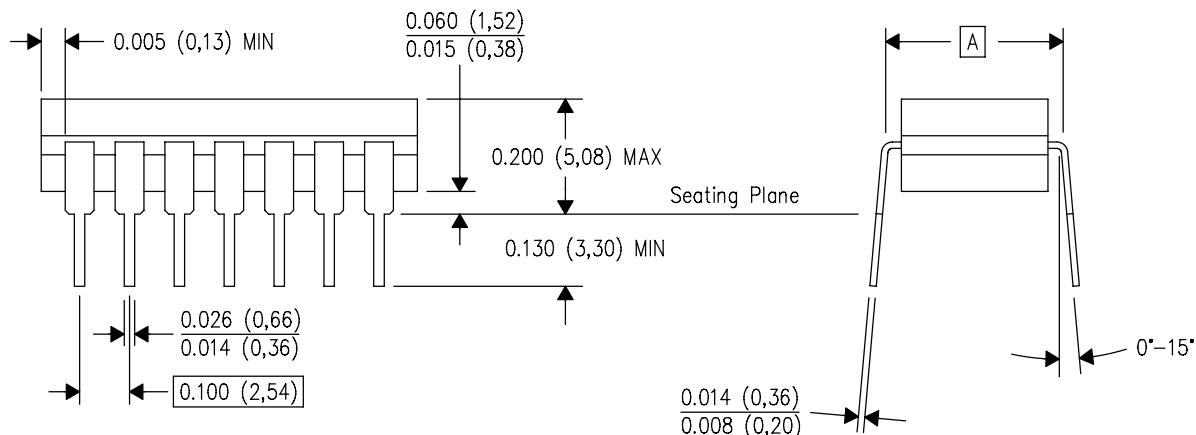
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



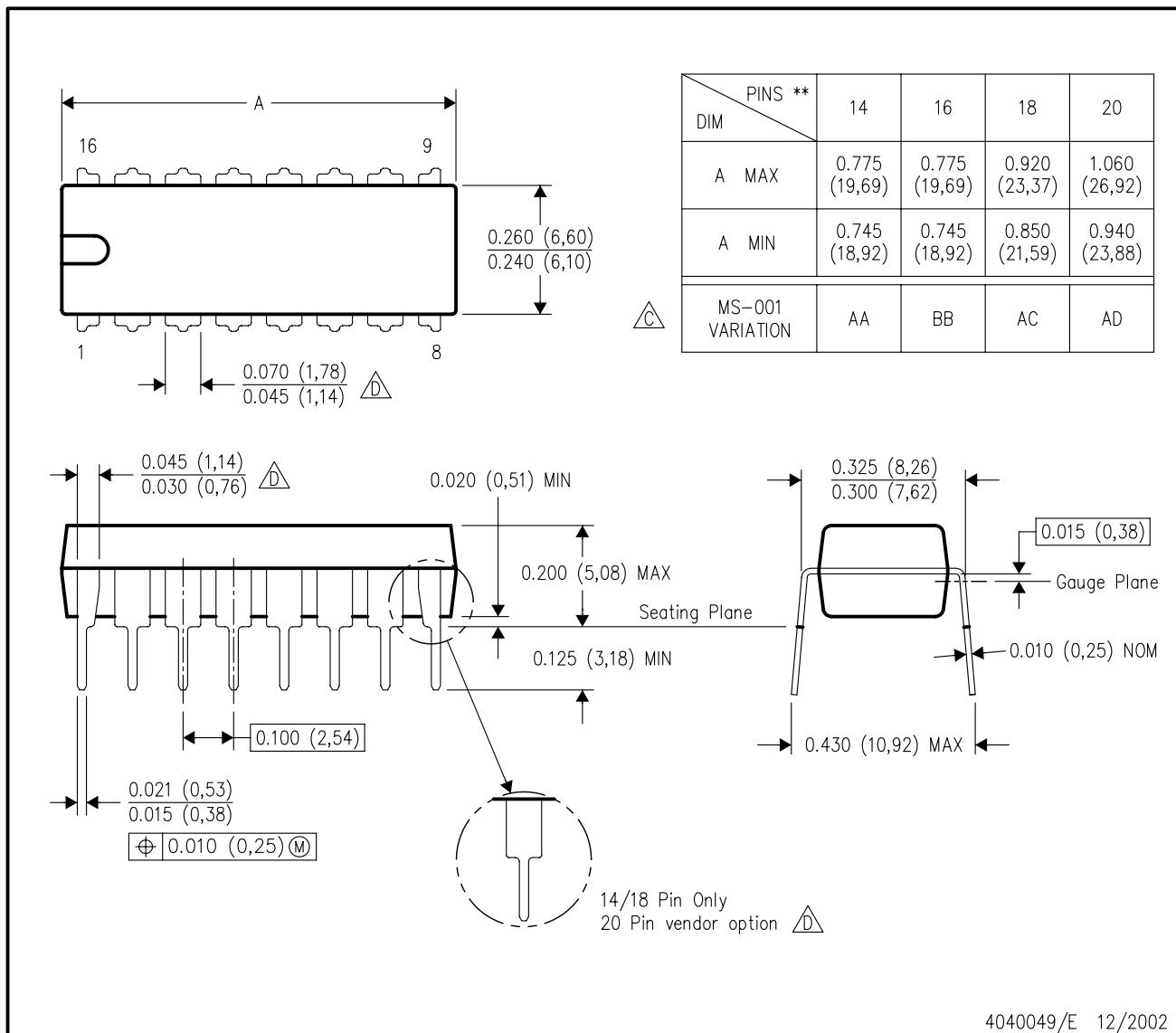
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

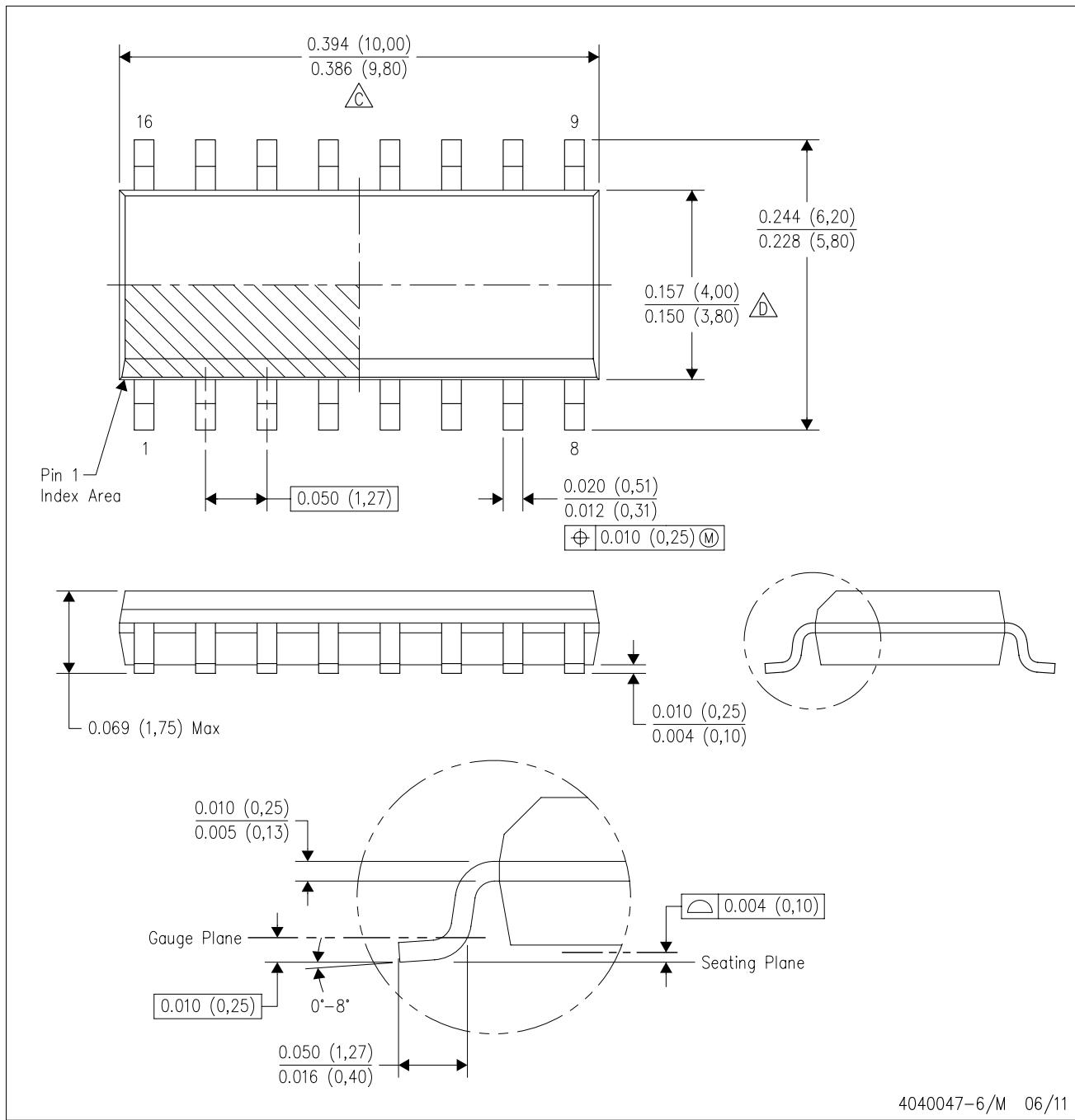
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

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