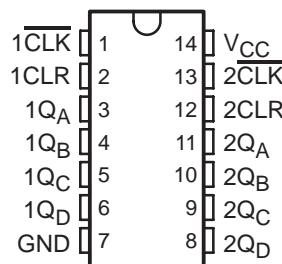


- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of -40°C to 105°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree[†]**
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 14.5 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce)**
 $<0.8 \text{ V at } \text{V}_{\text{CC}} = 3.3 \text{ V, } T_A = 25^{\circ}\text{C}$

[†] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74LV393A contains eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. This device is designed for 2-V to 5.5-V V_{CC} operation.

This device comprises two independent 4-bit binary counters, each having a clear (CLR) and a clock ($\overline{\text{CLK}}$) input. The device changes state on the negative-going transition of the $\overline{\text{CLK}}$ pulse. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The SN74LV393A has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV393ATPWREP	LV393EP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		FUNCTION
$\overline{\text{CLK}}$	CLR	
\uparrow	L	No change
\downarrow	L	Advance to next stage
X	H	All outputs L



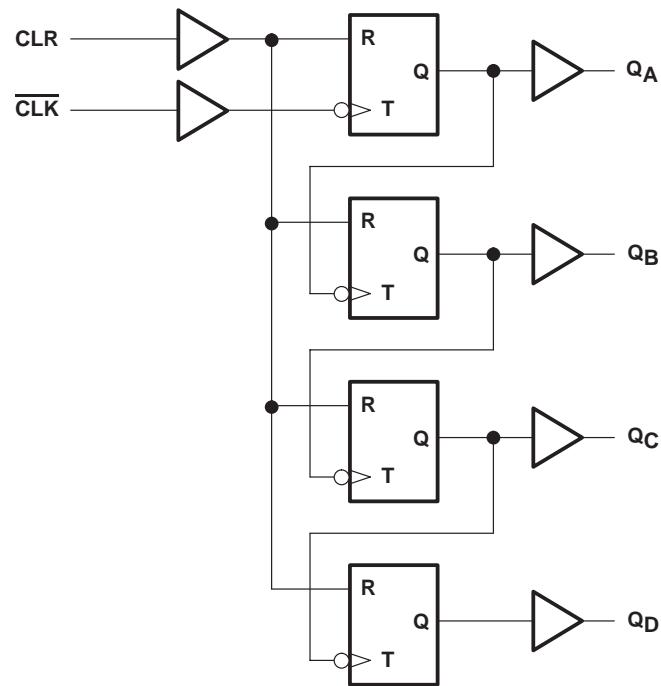
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LV393A-EP

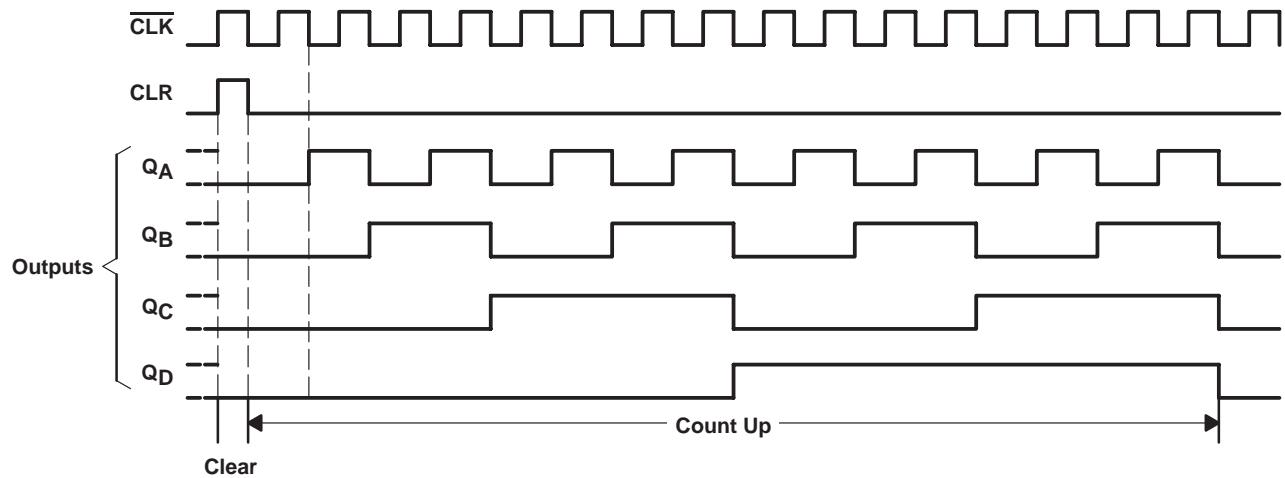
DUAL 4-BIT BINARY COUNTER

SCLS566A – JANUARY 2004 – REVISED MAY 2004

logic diagram, each counter (positive logic)



timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range applied in high or low state, V_O (see Notes 1 and 2)	–0.5 V to V_{CC} + 0.5 V
Output voltage range applied in power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3)	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 7 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 2.3$ V to 2.7 V	–2	
		$V_{CC} = 3$ V to 3.6 V	–6	
		$V_{CC} = 4.5$ V to 5.5 V	–12	
I_{OL}	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 2.3$ V to 2.7 V	2	
		$V_{CC} = 3$ V to 3.6 V	6	
		$V_{CC} = 4.5$ V to 5.5 V	12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	100	
		$V_{CC} = 4.5$ V to 5.5 V	20	
T_A	Operating free-air temperature	–40	105	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LV393A-EP

DUAL 4-BIT BINARY COUNTER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{OH}	I _{OH} = -50 µA	2 V to 5.5 V	V _{CC} -0.1			V
	I _{OH} = -2 mA	2.3 V	2			
	I _{OH} = -6 mA	3 V	2.48			
	I _{OH} = -12 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 50 µA	2 V to 5.5 V		0.1		V
	I _{OL} = 2 mA	2.3 V		0.4		
	I _{OL} = 6 mA	3 V		0.44		
	I _{OL} = 12 mA	4.5 V		0.55		
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±1	µA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		20	µA	
I _{off}	V _I or V _O = 0 to 5.5 V	0		5	µA	
C _i	V _I = V _{CC} or GND	3.3 V		1.8	pF	

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	CLK high or low	5	5		ns
		CLR high	5	5		
t _{su}	Setup time	CLR inactive before CLK↓	6	6		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	CLK high or low	5	5		ns
		CLR high	5	5		
t _{su}	Setup time	CLR inactive before CLK↓	5	5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t _w	Pulse duration	CLK high or low	5	5		ns
		CLR high	5	5		
t _{su}	Setup time	CLR inactive before CLK↓	4	4		ns

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50 \text{ pF}$	30	70	25			MHz
t_{pd}	$\overline{\text{CLK}}$	Q_A	$C_L = 50 \text{ pF}$	9.3	21.3	1	24.5	ns	
		Q_B		10.9	23.9	1	27.5		
		Q_C		12.3	26.1	1	30		
		Q_D		13.4	27.8	1	32		
t_{PHL}	CLR	Q_n	$C_L = 50 \text{ pF}$	9.1	17.4	1	20	ns	

switching characteristics over recommended operation free-air temperature range,
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50 \text{ pF}$	45	105	35			MHz
t_{pd}	$\overline{\text{CLK}}$	Q_A	$C_L = 50 \text{ pF}$	6.7	16.7	1	19	ns	
		Q_B		7.8	19.3	1	22		
		Q_C		8.7	21.5	1	24.5		
		Q_D		9.5	23.2	1	26.5		
t_{PHL}	CLR	Q_n	$C_L = 50 \text{ pF}$	6.8	15.8	1	18	ns	

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{max}			$C_L = 50 \text{ pF}$	85	150	75			MHz
t_{pd}	$\overline{\text{CLK}}$	Q_A	$C_L = 50 \text{ pF}$	4.9	10.5	1	12	ns	
		Q_B		5.6	11.8	1	13.5		
		Q_C		6.2	13.2	1	15		
		Q_D		6.6	14.5	1	16.5		
t_{PHL}	CLR	Q_n	$C_L = 50 \text{ pF}$	5.2	10.1	1	11.5	ns	

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DUAL 4-BIT BINARY COUNTER

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noise characteristics, $V_{CC} = 3.3$ V, $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ (see Note 5)

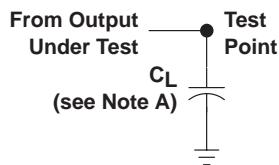
PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}	0.3	0.8		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}	-0.2	-0.8		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	2.8			V
$V_{IH(D)}$ High-level dynamic input voltage	2.31			V
$V_{IL(D)}$ Low-level dynamic input voltage	0.99			V

NOTE 5: Characteristics are for surface-mount packages only.

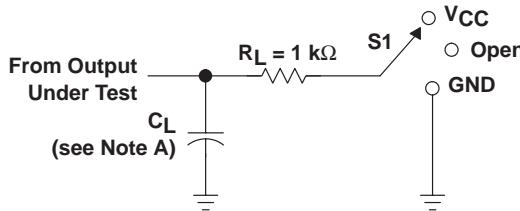
operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50$ pF, $f = 10$ MHz	3.3 V	15.2	pF
		5 V	17.3	

PARAMETER MEASUREMENT INFORMATION

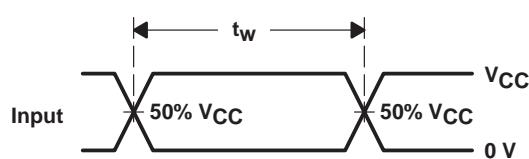


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

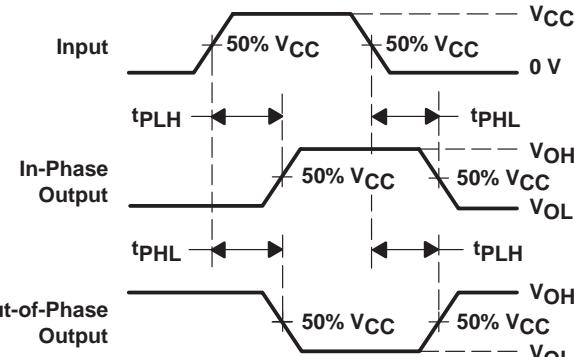


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

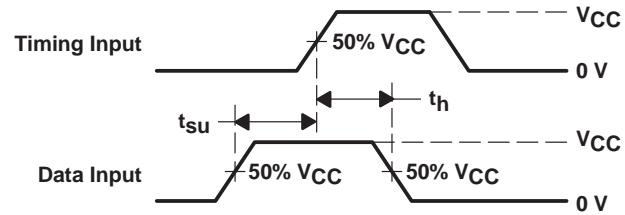
TEST	S1
tPLH/tPHL	Open
tPZL/tPZL	V _{CC}
tPHZ/tPZH	GND
Open Drain	V _{CC}



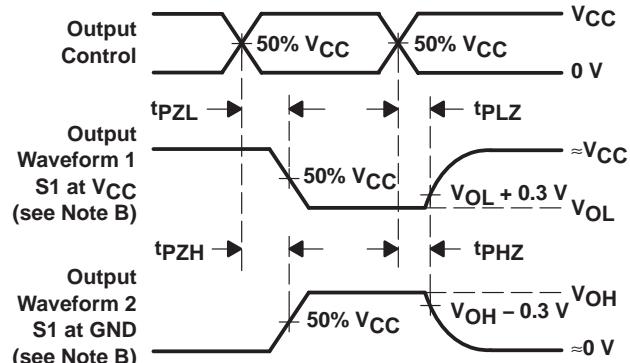
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV393ATPWREP	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 105	LV393EP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LV393A-EP :

- Catalog : [SN74LV393A](#)

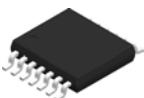
- Automotive : [SN74LV393A-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

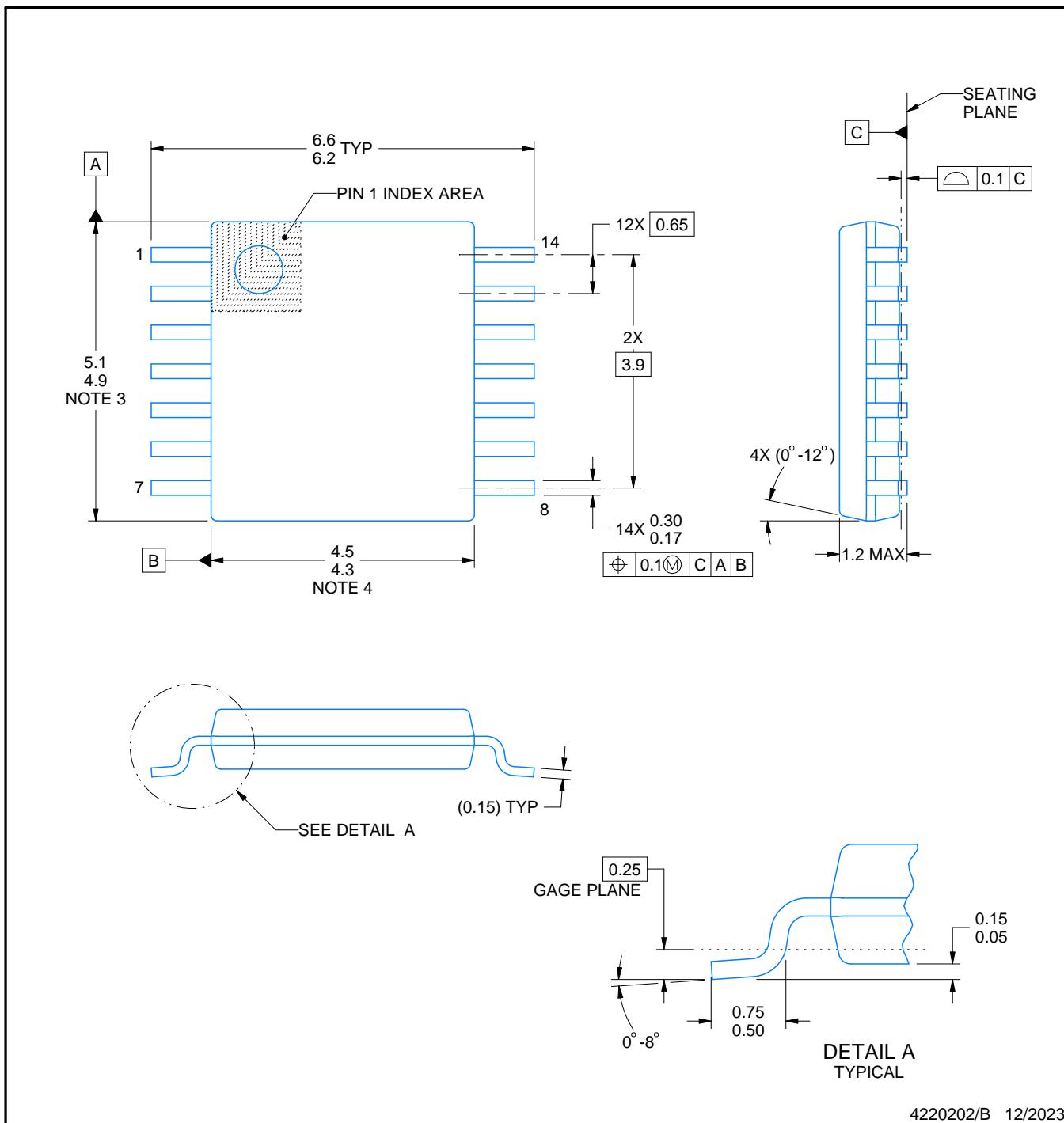
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

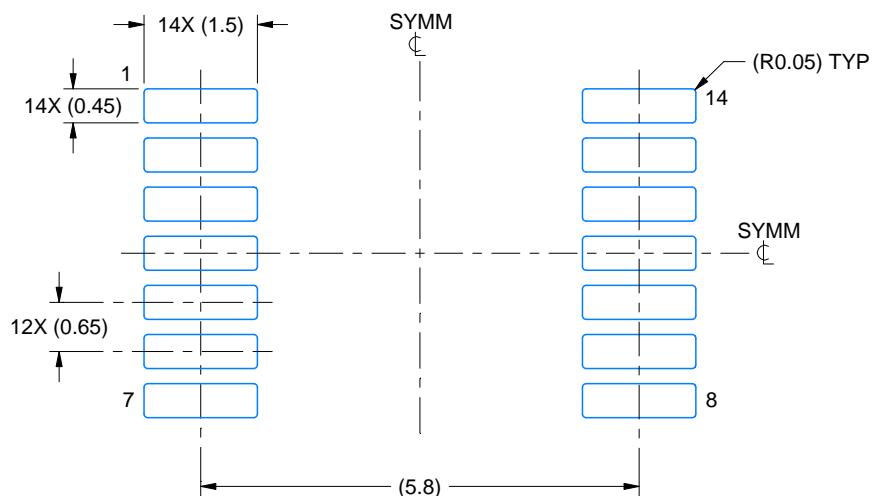
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

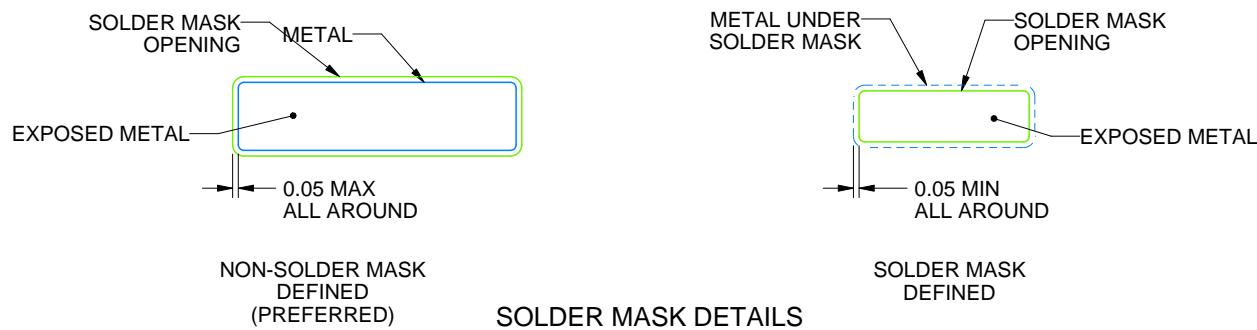
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

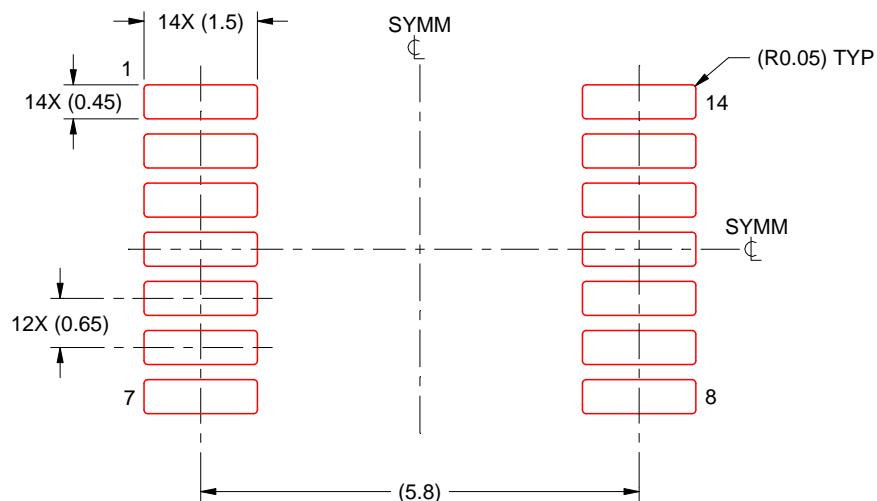
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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