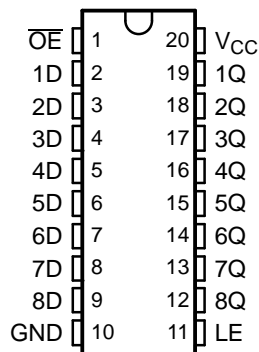


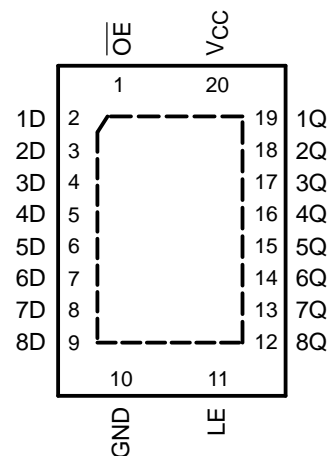
## FEATURES

- Inputs Are TTL-Voltage Compatible
- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Typical  $t_{pd} = 5.1$  ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2.3$  V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The SN74LV573AT is an octal transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74LV573ATRGYR	VV573
	SOIC – DW	Tube	SN74LV573ATDW	LV573AT
		Tape and reel	SN74LV573ATDWR	
	SOP – NS	Tape and reel	SN74LV573ATNSR	74LV573AT
	SSOP – DB	Tape and reel	SN74LV573ATDBR	LV573AT
	TSSOP – PW	Tube	SN74LV573ATPW	LV573AT
		Tape and reel	SN74LV573ATPWR	
TVSOP – DGV	Tape and reel	SN74LV573ATDGV	LV573AT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**SN74LV573AT**  
**OCTAL TRANSPARENT D-TYPE LATCH**  
**WITH 3-STATE OUTPUTS**

SCES574C–JUNE 2004–REVISED AUGUST 2005

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  shall be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

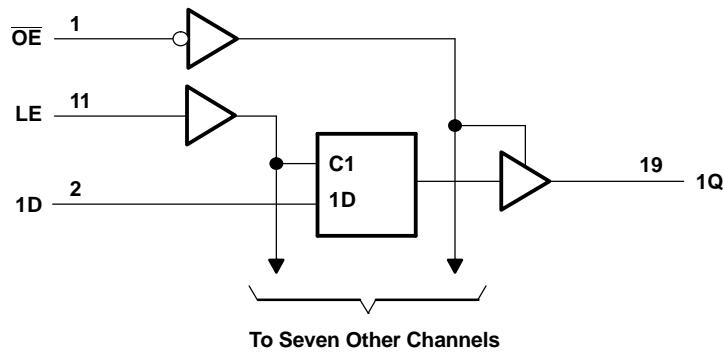
$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**FUNCTION TABLE**  
**(EACH LATCH)**

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

**LOGIC DIAGRAM (POSTIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	7	V
$V_O$	Output voltage range applied in the high or low state <sup>(2)(3)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	–20	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–50	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$	±35	mA
	Continuous current through $V_{CC}$ or GND		±70	mA
$\theta_{JA}$	Package thermal impedance	DB package <sup>(4)</sup>	70	°C/W
		DGV package <sup>(4)</sup>	92	
		DW package <sup>(4)</sup>	58	
		NS package <sup>(4)</sup>	60	
		PW package <sup>(4)</sup>	83	
		RGYpackage <sup>(5)</sup>	37	
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2	V
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	0.8	V
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$
		3-state	0	5.5
$I_{OH}$	High-level output current	$V_{CC} = 4.5$ V to 5.5 V	–16	mA
$I_{OL}$	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V	16	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 4.5$ V to 5.5 V	20	ns/V
$T_A$	Operating free-air temperature	–40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LV573AT

## OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES574C–JUNE 2004–REVISED AUGUST 2005

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4	V	
	I <sub>OH</sub> = -16 mA	4.5 V	3.8			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0	0.1	0.1	V	
	I <sub>OL</sub> = 16 mA	4.5 V			0.55	0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±0.1	±1	μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25	±2.5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2	20	μA	
ΔI <sub>CC</sub> ( <sup>1</sup> )	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35	1.5	mA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			0.5	5	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			4.5			pF	

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

### Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	6.5		8.5		ns
t <sub>su</sub>	Setup time, data before LE↓	1.5		1.5		ns
t <sub>h</sub>	Hold time, data after LE↓	3.5		3.5		ns

### Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF	2.6	5.1	8.5	1	9.5	ns
t <sub>PHL</sub>				3	5.1	8.5	1	9.5	
t <sub>PLH</sub>	LE	Q	C <sub>L</sub> = 15 pF	3	7.7	12.3	1	14.5	ns
t <sub>PHL</sub>				3.5	7.7	12.3	1	14.5	
t <sub>PZH</sub>	OE	Q	C <sub>L</sub> = 15 pF	3	6.3	10.9	1	12.5	ns
t <sub>PZL</sub>				3.3	6.3	10.9	1	12.5	
t <sub>PHZ</sub>	OE	Q	C <sub>L</sub> = 15 pF	2.8	5.5	8	1	11	ns
t <sub>PLZ</sub>				1.6	5.4	8	1	9.5	
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 50 pF	3.7	5.9	9.5	1	10.5	ns
t <sub>PHL</sub>				5.5	5.9	9.5	1	10.5	
t <sub>PLH</sub>	LE	Q	C <sub>L</sub> = 50 pF	4.3	8.5	13.3	1	14.5	ns
t <sub>PHL</sub>				5.9	8.5	13.3	1	14.5	
t <sub>PZH</sub>	OE	Q	C <sub>L</sub> = 50 pF	4.5	7.1	11.9	1	13.5	ns
t <sub>PZL</sub>				5.4	7.1	11.9	1	13.5	
t <sub>PHZ</sub>	OE	Q	C <sub>L</sub> = 50 pF	3.3	8.8	11.2	1	12	ns
t <sub>PLZ</sub>				2.6	8.8	11.2	1	12	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			1.5		1.5	ns

**Noise Characteristics<sup>(1)</sup>**
 $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ 

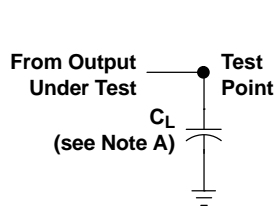
		$T_A = 25^\circ\text{C}$			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		1.1	1.5	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-1.1	-1.5	V
$V_{OH(V)}$	Quiet output, maximum dynamic $V_{OH}$		4		V
$V_{IH(D)}$	High-level dynamic input voltage	2			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

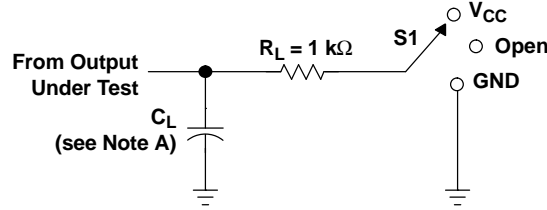
**Operating Characteristics**
 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	8	pF

**PARAMETER MEASUREMENT INFORMATION**

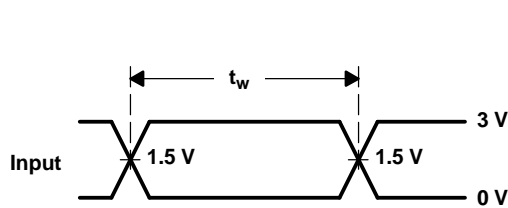


**LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS**

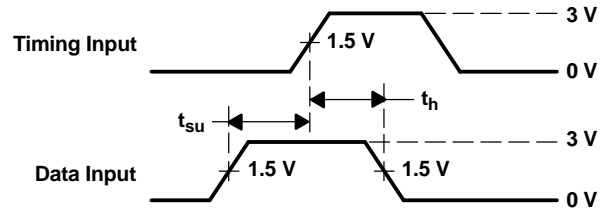


**LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS**

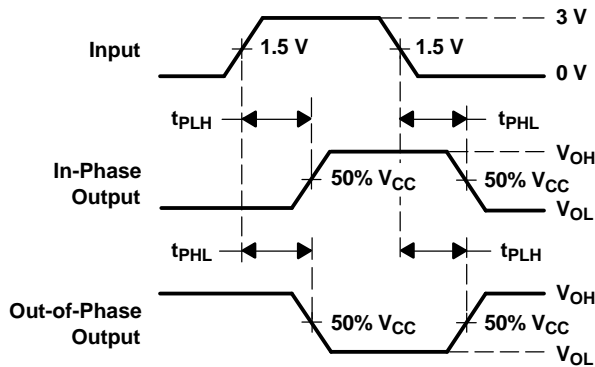
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$



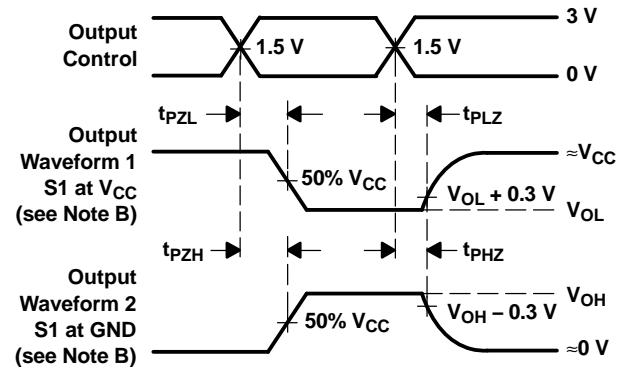
**VOLTAGE WAVEFORMS PULSE DURATION**



**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
D. The outputs are measured one at a time, with one input transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LV573ATDWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT
SN74LV573ATDWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT
<a href="#">SN74LV573ATPW</a>	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 85	LV573AT
<a href="#">SN74LV573ATPWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT
SN74LV573ATPWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573AT

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV573ATDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV573ATPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV573ATDWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV573ATPWR	TSSOP	PW	20	2000	353.0	353.0	32.0

PW0020A



# PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025