# SN74LVC04B-Q1 Automotive 6-Channel, 1.1V to 3.6V Inverters

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Operating range from 1.1V to 3.6V
- Over-voltage tolerant inputs support up to 5.5V independent of $V_{CC}$
- Maximum propagation delay of 4.8ns at 3.3V $V_{CC}$, $C_L$ = 50pF
- Supports partial-power-down with back drive protection ($I_{off}$)
- High output drive strength:
  - ±24mA at 3.3V
  - ±8mA at 2.3V
  - ±4mA at 1.65V

## 2 Applications

- Advanced driver assistance systems (ADAS)
- Body electronics and lighting
- Infotainment and cluster

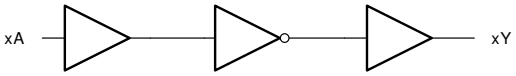
## 3 Description

This device contains six independent inverters, each gate performs the Boolean function $Y = \overline{A}$ in positive logic.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE (2) | BODY SIZE(3) |
|---|---|---|---|
| SN74LVC04B-Q1 | BQA ( WQFN, 14) | 3mm × 2.5mm | 3mm × 2.5mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram (One of Six Channels)**

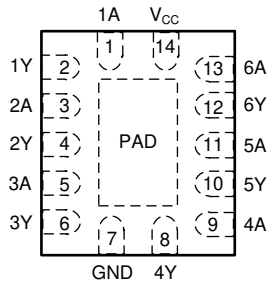
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# 4 Pin Configuration and Functions




**BQA Package,**
**14-Pin WQFN**
**(Top View)**

**Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | I | Channel 1, Input A |
| 1Y | 2 | O | Channel 1, Output Y |
| 2A | 3 | I | Channel 2, Input A |
| 2Y | 4 | O | Channel 2, Output Y |
| 3A | 5 | I | Channel 3, Input A |
| 3Y | 6 | O | Channel 3, Output Y |
| GND | 7 | G | Ground |
| 4Y | 8 | O | Channel 4, Output Y |
| 4A | 9 | I | Channel 4, Input A |
| 5Y | 10 | O | Channel 5, Output Y |
| 5A | 11 | I | Channel 5, Input A |
| 6Y | 12 | O | Channel 6, Output Y |
| 6A | 13 | I | Channel 6, Input A |
| $V_{CC}$ | 14 | P | Power Supply |
| Thermal Pad | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply |

(1) I = input, O = output, P = Positive Supply, G = Ground

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | -0.5 | 6.5 | V |
| $V_O$ | Output voltage range(2) | | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0V | | -50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0V | | -50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| $I_O$ | Continuous output current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | -65 | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B | ±1000 | |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.


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## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Specifications | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.1 | 3.6 | V |
| $V_I$ | Input voltage | | | 5.5 | V |
| $V_O$ | Output voltage | (High or low state) | | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.1V to 1.95V | 0.65 × Vcc | | V |
| | | $V_{CC}$ = 2.3V to 2.7V | 1.7 | | |
| | | $V_{CC}$ = 2.7V to 3.6V | 2 | | |
| $V_{IL}$ | Low-Level input voltage | $V_{CC}$ = 1.1V to 1.95V | | 0.35 × Vcc | V |
| | | $V_{CC}$ = 2.3V to 2.7V | | 0.7 | |
| | | $V_{CC}$ = 2.7V to 3.6V | | 0.8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.8V | | 4 | mA |
| | | $V_{CC}$ = 2.3V | | 8 | |
| | | $V_{CC}$ = 2.7V | | 12 | |
| | | $V_{CC}$ = 3V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 125 | °C |

## 5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC(1) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $R_{\theta JA}$ | $R_{\theta JC(top)}$ | $R_{\theta JB}$ | $\Psi_{JT}$ | $\Psi_{JB}$ | $R_{\theta JC(bot)}$ | |
| BQA (WQFN, 14) | 14 | 91.3 | 99.4 | 61.0 | 14.5 | 60.8 | 37.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{OL}$ | $I_{OH}$= 100µA | 1.1V to 3.6V | | | 0.15 | V |
| | $I_{OH}$= 4mA | 1.65V | | | 0.45 | |
| | $I_{OH}$= 8mA | 2.3V | | | 0.7 | |
| | $I_{OH}$= 12mA | 2.7V | | | 0.4 | |
| | $I_{OH}$= 24mA | 3V | | | 0.55 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 3.6V | | | ±5 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = $V_{CC}$ | 0V | | | ±10 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6V | | | 40 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | 2.7V to 3.6V | | | 500 | µA |


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## 5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $V_{CC}$ | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{pd}$ | A | Y | $C_L$ = 15pF | 1.2V ± 0.1V | | | 22.6 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 15pF | 1.5V ± 0.12V | | | 8.5 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 15pF | 1.8V ± 0.15V | | | 6.2 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 15pF | 2.5V ± 0.2V | | | 4.1 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 15pF | 2.7V | | | 3.8 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 15pF | 3.3V ± 0.3V | | | 3.4 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 30pF | 1.8V ± 0.15V | | | 7.4 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 30pF | 2.5V ± 0.2V | | | 4.9 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 50pF | 2.7V | | | 5.3 | ns |
| $t_{pd}$ | A | Y | $C_L$ = 50pF | 3.3V ± 0.3V | | | 4.8 | ns |
| $C_{pd}$ | | | f = 10MHz | 1.8V | | 13.3 | | pF |
| $C_{pd}$ | | | f = 10MHz | 2.5V | | 15.6 | | pF |
| $C_{pd}$ | | | f = 10MHz | 3.3V | | 17.7 | | pF |

## 5.7 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

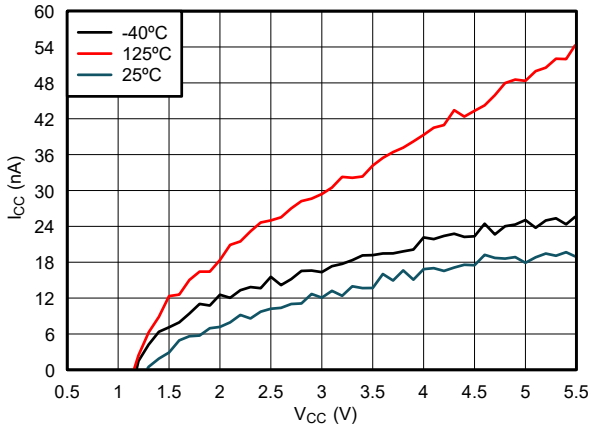



**Figure 5-1. Supply Current Across Supply Voltage and Temperature**

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## 5.7 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

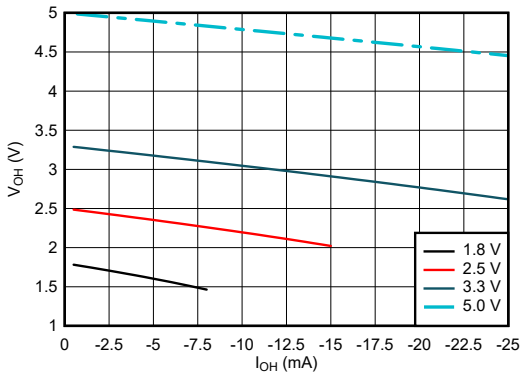



**Figure 5-2. Output Voltage vs Current in HIGH State**

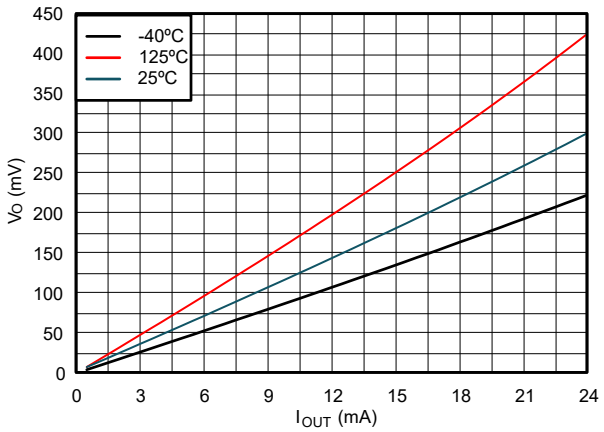



**Figure 5-3. Output Voltage vs Current in LOW State; 3V Supply**

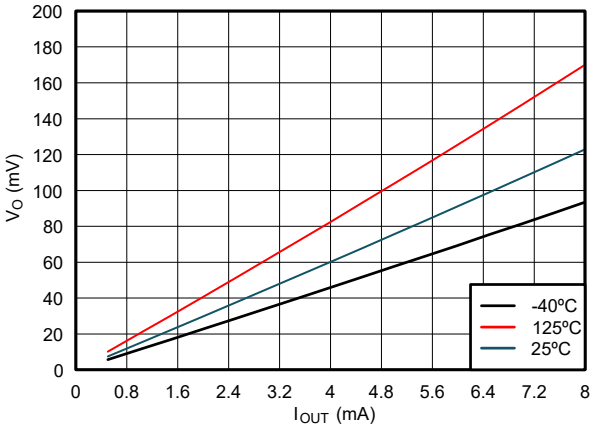



**Figure 5-4. Output Voltage vs Current in LOW State; 2.3V Supply**

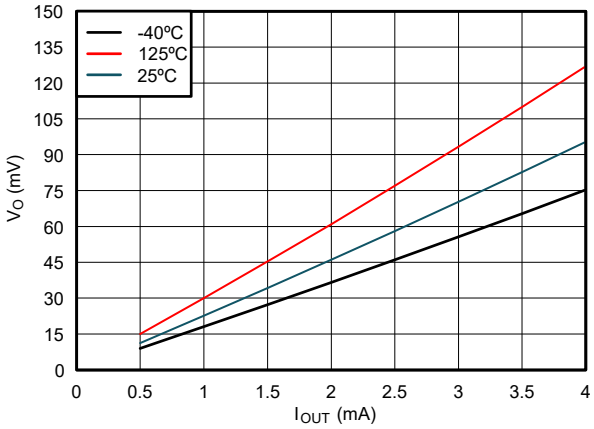



**Figure 5-5. Output Voltage vs Current in LOW State; 1.65V Supply**

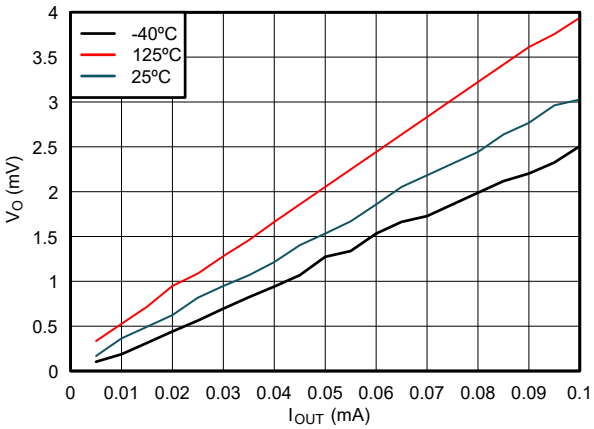



**Figure 5-6. Output Voltage vs Current in LOW State; 1.38V Supply**

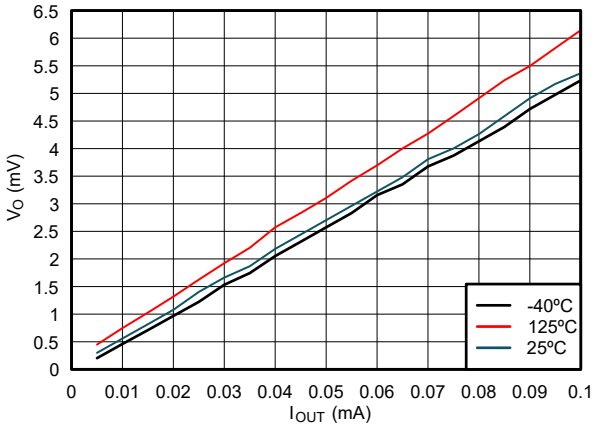



**Figure 5-7. Output Voltage vs Current in LOW State; 1.1V Supply**


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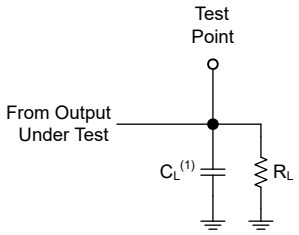
## 6 Parameter Measurement Information

Phase relationships between waveforms are chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O$ = 50Ω, $t_t$ ≤ 2.5ns.

The outputs are measured individually with one input transition per measurement.

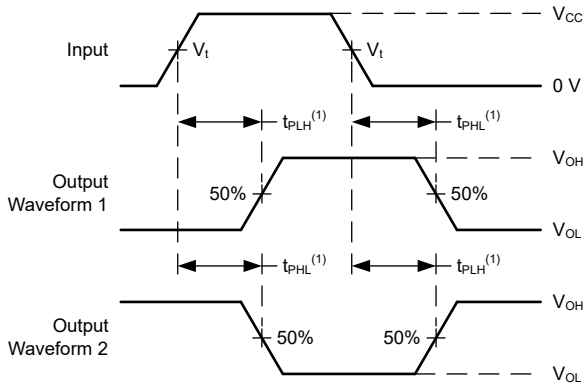
**Table 6-1. Push-Pull Outputs**

| $V_{CC}$ | $V_t$ | $R_L$ | $C_L$ | ΔV |
|---|---|---|---|---|
| 1.2V ± 0.1V | $V_{CC}$/2 | 2kΩ | 15pF | 0.1V |
| 1.5V ± 0.12V | $V_{CC}$/2 | 2kΩ | 15pF | 0.1V |
| 1.8V ± 0.15V | $V_{CC}$/2 | 1kΩ | 15pF/30pF | 0.15V |
| 2.5V ± 0.2V | $V_{CC}$/2 | 500Ω | 15pF/30pF | 0.15V |
| 2.7V | 1.5V | 500Ω | 15pF/50pF | 0.3V |
| 3.3V ± 0.3V | 1.5V | 500Ω | 15pF/50pF | 0.3V |



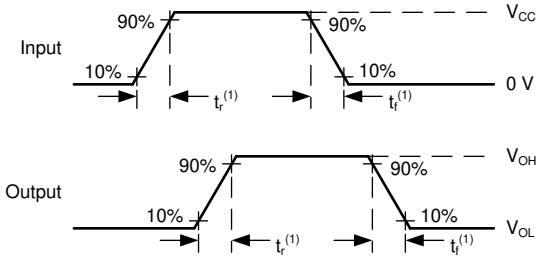

(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Push-Pull Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**Figure 6-2. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**Figure 6-3. Voltage Waveforms, Input and Output Transition Times**

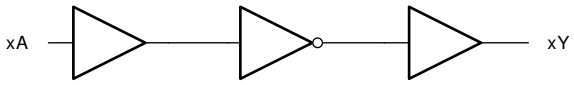
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# 7 Detailed Description

## 7.1 Overview

This device contains six independent inverters. Each gate performs the Boolean function Y = $\overline{A}$ in positive logic.

## 7.2 Logic Diagram




**One of Six Channels**

## 7.3 Feature Description

### *7.3.1 Balanced CMOS Push-Pull Outputs*

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

### *7.3.2 Partial Power Down ($I_{off}$)*

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the $I_{off}$ specification in the *Electrical Characteristics* table.

### *7.3.3 Standard CMOS Inputs*

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at $V_{CC}$ or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

### *7.3.4 Wettable Flanks*

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the datasheet where packages include this feature.


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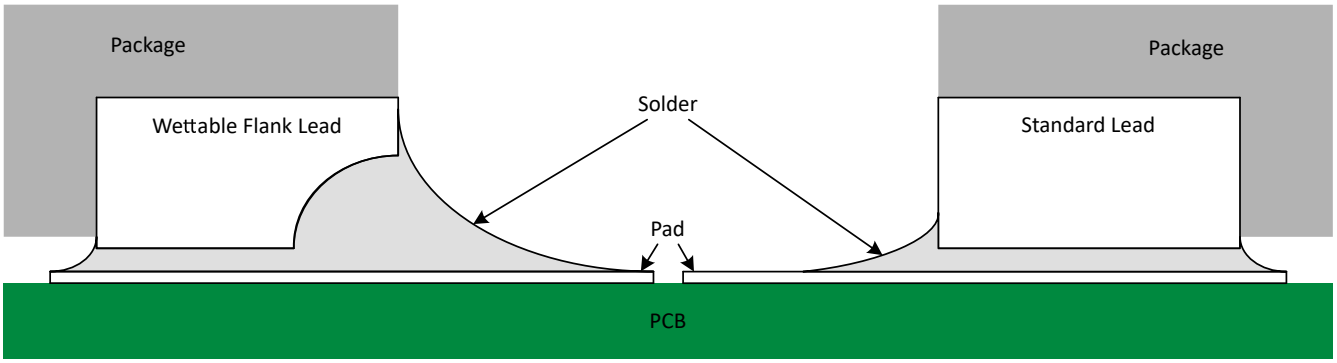



**Figure 7-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-1, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

### *7.3.5 Clamp Diode Structure*

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

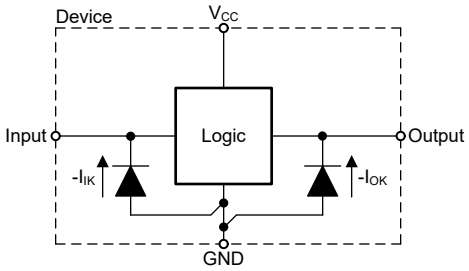



**Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output**

### *7.3.6 Over-Voltage Tolerant Inputs*

The SN74LVC04B-Q1 includes over-voltage tolerant inputs. The input pins support high-state input voltages larger than the supply voltage by utilizing an input protection circuit that does not include a standard positive clamp diode. See *Recommended Operating Conditions* for the recommended input voltage.

**CAUTION**

Do not exceed the maximum input voltage range provided in *Absolute Maximum Ratings*. Exceeding the maximum input voltage range rating can cause immediate and permanent damage to the device.

## 7.4 Device Functional Modes

Function Table lists the functional modes of the SN74LVC04B-Q1.

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**Table 7-1. Function Table**

| INPUTS[1] | OUTPUT |
|---|---|
| A | Y |
| L | H |
| H | L |

(1) H = High Voltage Level, L = Low Voltage Level


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The SN74LVC04B-Q1 can be used to add an additional stage to a counter with an external flip-flop. Because counters use a negative edge trigger, the flip-flop's clock input must be inverted to provide this function. This function only requires one of the six available inverters in the SN74LVC04B-Q1 device, so the remaining channels can be used for other applications needing an inverted signal. Unused inputs must be terminated at $V_{CC}$ or GND. Unused outputs can be left floating.

## 8.2 Typical Application

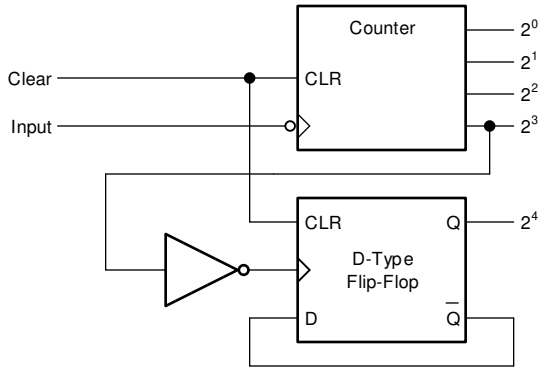



**Figure 8-1. Typical Application Block Diagram**

### *8.2.1 Design Requirements*

#### 8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC04B-Q1 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC04B-Q1 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC04B-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74LVC04B-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state,

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the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation application note*.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices application note*.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC04B-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC04B-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### *8.2.2 Detailed Design Procedure*

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74LVC04B-Q1 to the receiving device.
3. Verify that the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.


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4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation application note*.

### 8.2.3 Application Curves

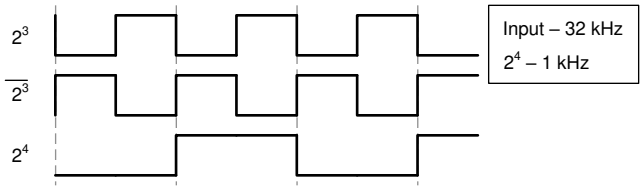



**Figure 8-2. Application Timing Diagram**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. A design can use multiple bypass capacitors in parallel to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

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### 8.4.2 Layout Example

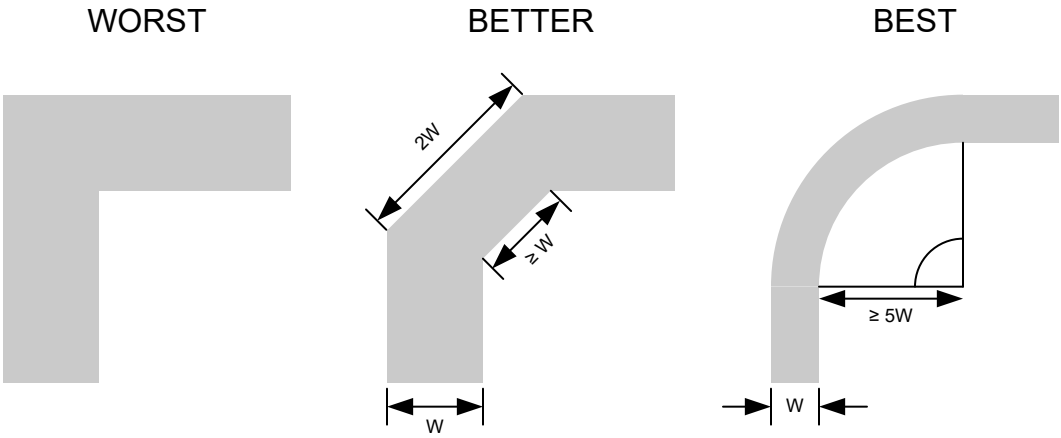



**Figure 8-3. Example Trace Corners for Improved Signal Integrity**

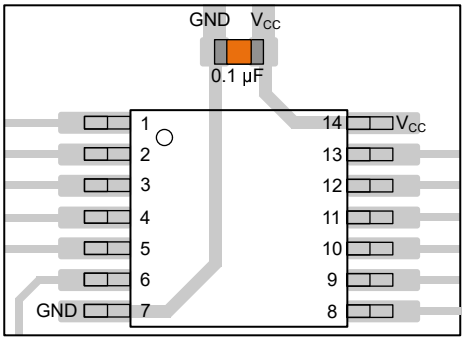



**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

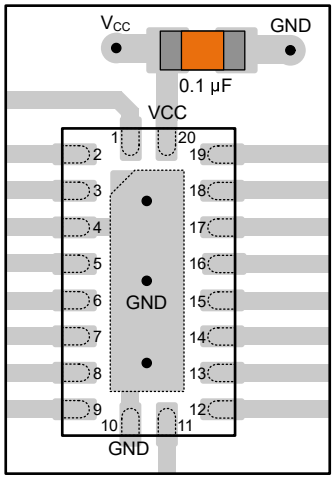



**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**

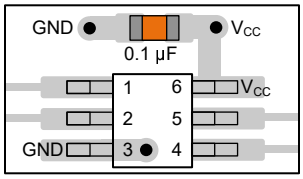



**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

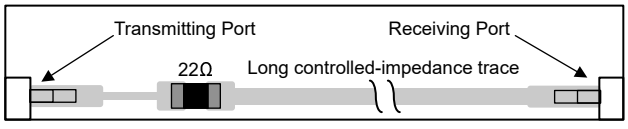



**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**


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# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application brief
- Texas Instruments, *Logic in Live-Insertion Applications With a Focus on GTLP* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Texas Instruments General Quality Guidelines*
- Texas Instruments, *Thermal Characteristics of SLL Packages and Devices* application note
- Texas Instruments, *Understanding Schmitt Triggers* application brief

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| September 2026 | * | Initial Release |

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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVC04BWBQARQ1 | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | LVC04Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC04B-Q1 :**

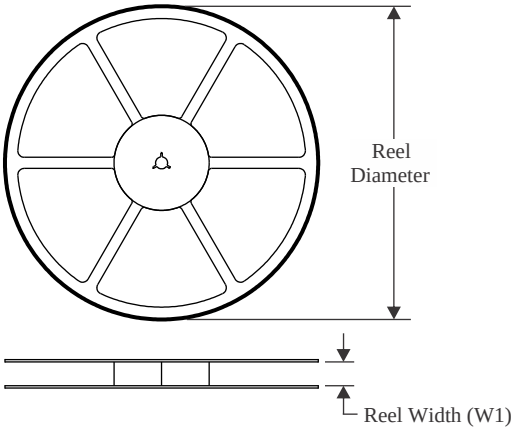
- Catalog : SN74LVC04B

NOTE: Qualified Version Definitions:

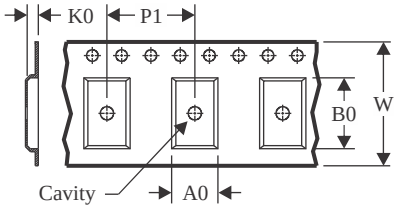
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

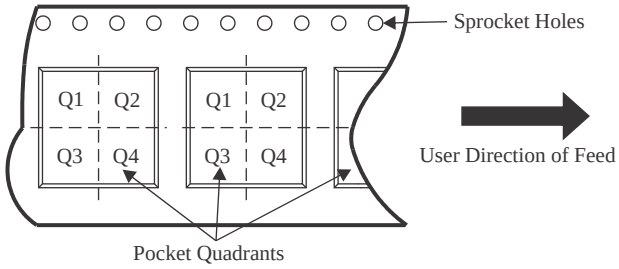



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

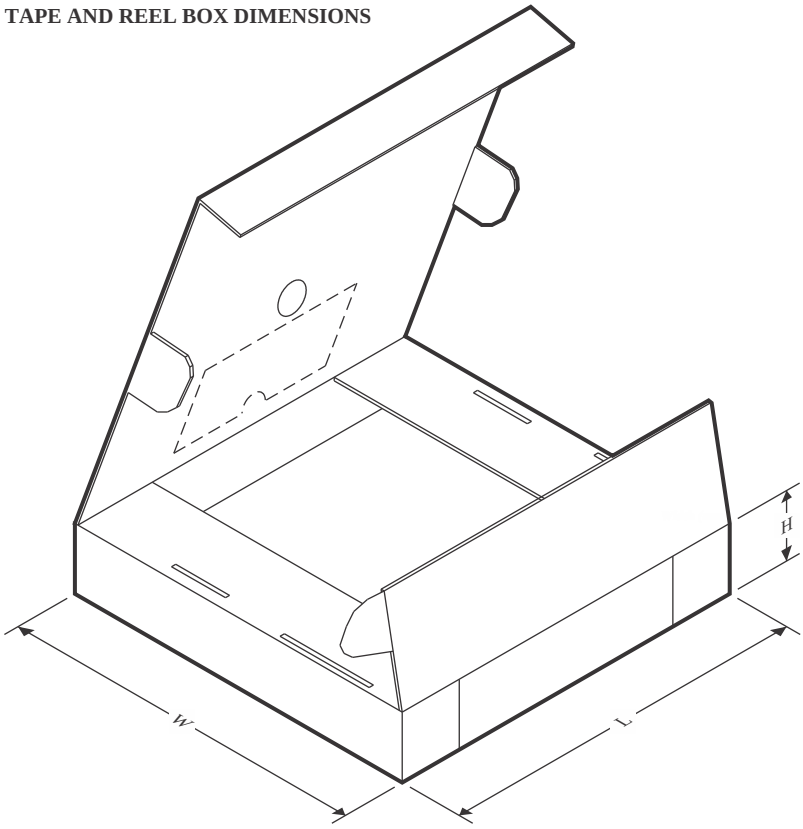
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC04BWBQARQ1 | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC04BWBQARQ1 | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

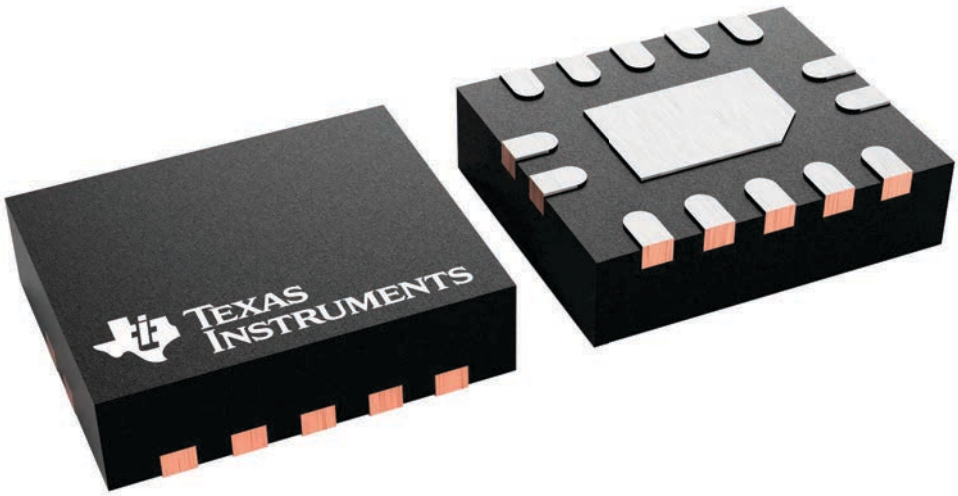
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

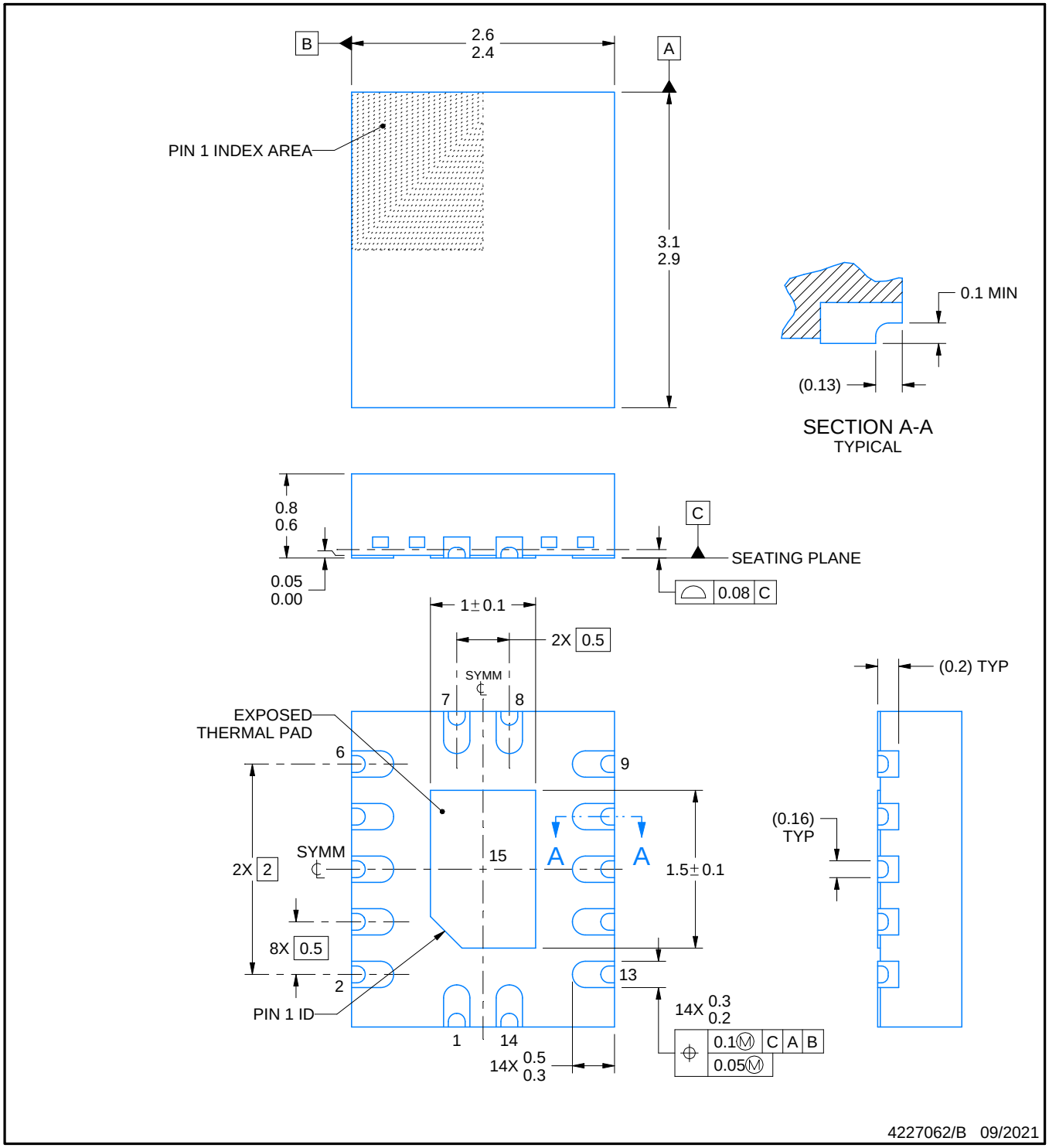


# BQA0014B

# PACKAGE OUTLINE

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

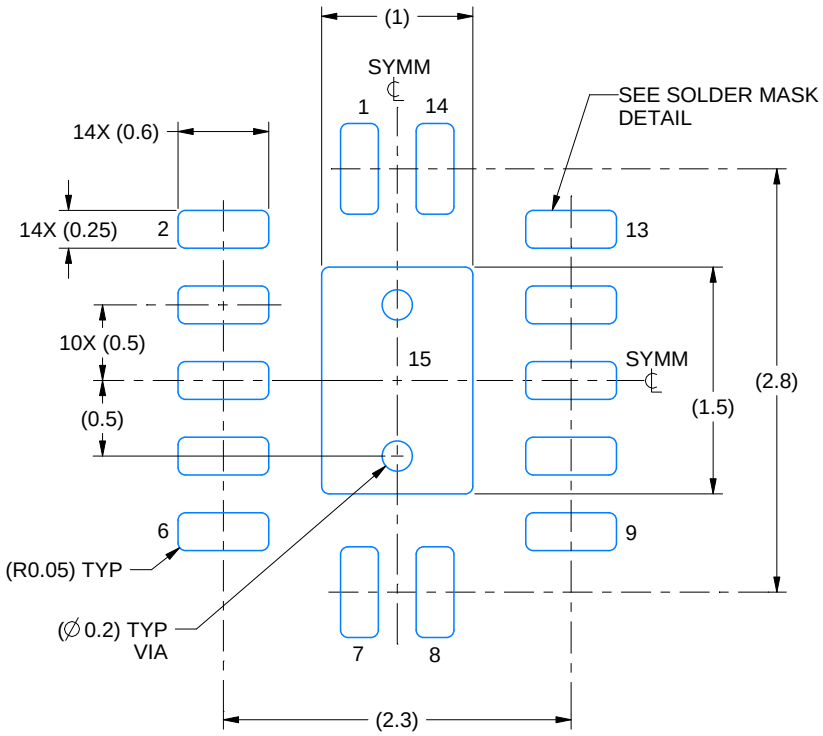
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

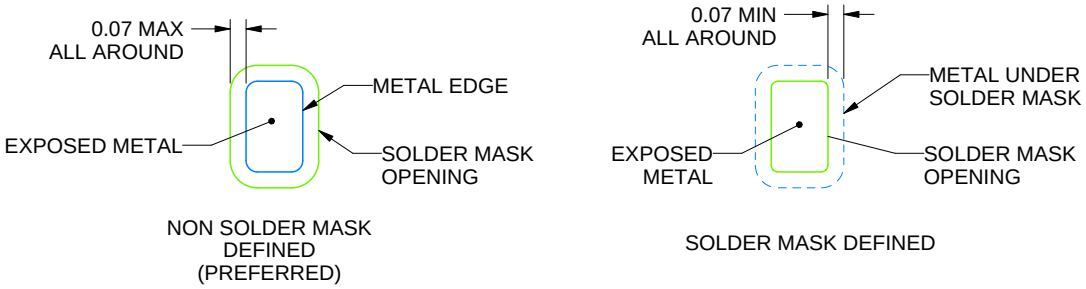
## BQA0014B

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

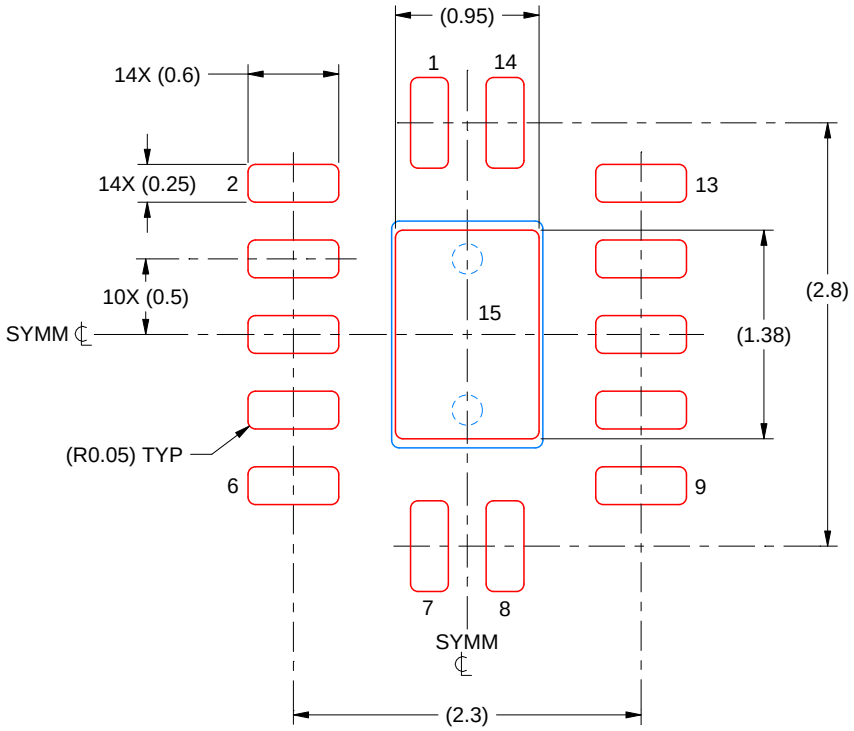



SOLDER MASK DETAILS

4227062/B 09/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025