

SN74LVC07A Hex Buffer and Driver With Open-Drain Outputs

1 Features

- Operates From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages Up to 5.5 V
- Max  $t_{pd}$  of 2.6 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- MP3 Player or Recorder
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD, Digital, and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

3 Description

The SN74LVC07A device is a hex buffer and driver that is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

Device Information<sup>(1)</sup>

| PART NUMBER   | PACKAGE    | BODY SIZE (NOM)    |
|---------------|------------|--------------------|
| SN74LVC07AD   | SOIC (14)  | 8.65 mm × 3.91 mm  |
| SN74LVC07ADB  | SSOP (14)  | 6.20 mm × 5.30 mm  |
| SN74LVC07ADGV | TVSOP (14) | 3.60 mm × 4.40 mm  |
| SN74LVC07APW  | TSSOP (14) | 5.00 mm × 4.40 mm  |
| SN74LVC07ANS  | SO (14)    | 10.30 mm × 5.30 mm |
| SN74LVC07ARGY | VQFN (14)  | 3.50 mm × 3.50 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision V (May 2015) to Revision W                                                          | Page |
|-----------------------------------------------------------------------------------------------------------|------|
| • Changed <i>Pin Functions</i> table .....                                                                | 4    |
| • Added Junction temperature to the <i>Absolute Maximum Ratings</i> table .....                           | 5    |
| • Reformatted the <i>Electrical Characteristics</i> and the <i>Switching Characteristics</i> tables ..... | 6    |
| • Changed <i>Typical Application Diagram</i> .....                                                        | 13   |
| • Added <i>Receiving Notification of Documentation Updates</i> section .....                              | 16   |

| Changes from Revision U (June 2014) to Revision V                                                    | Page |
|------------------------------------------------------------------------------------------------------|------|
| • Changed <i>Handling Ratings</i> table to <i>ESD Ratings</i> table .....                            | 5    |
| • Added industry standard terms to package designators in the <i>Thermal Information</i> table ..... | 6    |
| • Changed from "High" to "High-Z" in the <i>Function Table</i> .....                                 | 12   |

| Changes from Revision T (February 2011) to Revision U                                      | Page |
|--------------------------------------------------------------------------------------------|------|
| • Updated document to new TI data sheet format .....                                       | 1    |
| • Removed <i>Ordering Information</i> table .....                                          | 1    |
| • Added <i>Applications</i> .....                                                          | 1    |
| • Added $I_{off}$ <i>Features</i> bullet .....                                             | 1    |
| • Added <i>Device Information</i> table .....                                              | 1    |
| • Added <i>Handling Ratings</i> table .....                                                | 5    |
| • Changed MAX operating free-air temperature from 85°C to 125°C .....                      | 5    |
| • Updated <i>Thermal Information</i> table .....                                           | 6    |
| • Added –40°C TO +125°C temperature range to <i>Electrical Characteristics</i> table ..... | 6    |
| • Added <i>Switching Characteristics</i> table for –40°C TO 125°C temperature range .....  | 6    |

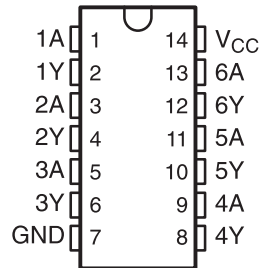
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|                                              |                   |
|----------------------------------------------|-------------------|
| • Added <i>Typical Characteristics</i> ..... | <a href="#">7</a> |
|----------------------------------------------|-------------------|

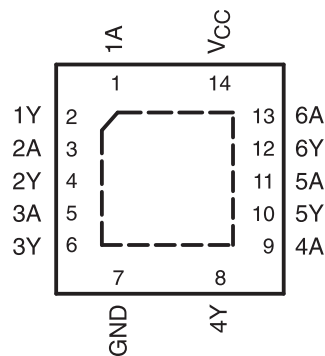
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## 5 Pin Configuration and Functions

**D, DB, DGV, NS, PW Package**  
**14-Pin SOIC, SSOP, TVSOP, SO, TSSOP**  
**Top View**



**RGY Package**  
**14-Pin VQFN**  
**Top View**



**Pin Functions**

| PIN |                 | I/O | DESCRIPTION |
|-----|-----------------|-----|-------------|
| NO. | NAME            |     |             |
| 1   | 1A              | I   | Input 1     |
| 2   | 1Y              | O   | Output 1    |
| 3   | 2A              | I   | Input 2     |
| 4   | 2Y              | O   | Output 2    |
| 5   | 3A              | I   | Input 3     |
| 6   | 3Y              | O   | Output 3    |
| 7   | GND             | —   | Ground pin  |
| 8   | 4Y              | O   | Output 4    |
| 9   | 4A              | I   | Input 4     |
| 10  | 5Y              | O   | Output 5    |
| 11  | 5A              | I   | Input 5     |
| 12  | 6Y              | O   | Output 6    |
| 13  | 6A              | I   | Input 6     |
| 14  | V <sub>CC</sub> | —   | Power pin   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                   |                    | MIN  | MAX  | UNIT |
|------------------|---------------------------------------------------|--------------------|------|------|------|
| V <sub>CC</sub>  | Supply voltage                                    |                    | –0.5 | 6.5  | V    |
| V <sub>I</sub>   | Input voltage <sup>(2)</sup>                      |                    | –0.5 | 6.5  | V    |
| V <sub>O</sub>   | Output voltage                                    |                    | –0.5 | 6.5  | V    |
| I <sub>IK</sub>  | Input clamp current                               | V <sub>I</sub> < 0 |      | –50  | mA   |
| I <sub>OK</sub>  | Output clamp current                              | V <sub>O</sub> < 0 |      | –50  | mA   |
| I <sub>O</sub>   | Continuous output current                         |                    |      | ±50  | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |                    |      | ±100 | mA   |
| T <sub>j</sub>   | Junction temperature                              |                    |      | 150  | °C   |
| T <sub>stg</sub> | Storage temperature                               |                    | –65  | 150  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±4000 |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                |                                    | MIN                    | MAX                    | UNIT |
|-----------------|--------------------------------|------------------------------------|------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage                 |                                    | 1.65                   | 5.5                    | V    |
| V <sub>IH</sub> | High-level input voltage       | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> |                        | V    |
|                 |                                | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |                        |      |
|                 |                                | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2                      |                        |      |
|                 |                                | V <sub>CC</sub> = 4.5 V to 5.5 V   | 0.7 × V <sub>CC</sub>  |                        |      |
| V <sub>IL</sub> | Low-level input voltage        | V <sub>CC</sub> = 1.65 V to 1.95 V |                        | 0.35 × V <sub>CC</sub> | V    |
|                 |                                | V <sub>CC</sub> = 2.3 V to 2.7 V   |                        | 0.7                    |      |
|                 |                                | V <sub>CC</sub> = 2.7 V to 3.6 V   |                        | 0.8                    |      |
|                 |                                | V <sub>CC</sub> = 4.5 V to 5.5 V   |                        | 0.3 × V <sub>CC</sub>  |      |
| V <sub>I</sub>  | Input voltage                  |                                    | 0                      | 5.5                    | V    |
| V <sub>O</sub>  | Output voltage                 |                                    | 0                      | 5.5                    | V    |
| I <sub>OL</sub> | Low-level output current       | V <sub>CC</sub> = 1.65 V           |                        | 4                      | mA   |
|                 |                                | V <sub>CC</sub> = 2.3 V            |                        | 12                     |      |
|                 |                                | V <sub>CC</sub> = 2.7 V            |                        | 12                     |      |
|                 |                                | V <sub>CC</sub> = 3 V              |                        | 24                     |      |
|                 |                                | V <sub>CC</sub> = 4.5 V            |                        | 24                     |      |
| T <sub>A</sub>  | Operating free-air temperature |                                    | –40                    | 125                    | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

**SN74LVC07A**

SCAS595W – OCTOBER 1997 – REVISED OCTOBER 2016

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## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LVC07A  |              |                |            |               |               | UNIT |
|-------------------------------|----------------------------------------------|-------------|--------------|----------------|------------|---------------|---------------|------|
|                               |                                              | D<br>(SOIC) | DB<br>(SSOP) | DGV<br>(TVSOP) | NS<br>(SO) | PW<br>(TSSOP) | RGY<br>(VQFN) |      |
|                               |                                              | 14 PINS     |              |                |            |               |               |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 177.4       | 135.1        | 157.7          | 120.3      | 160.3         | 80.6          | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 75.4        | 86.7         | 78.3           | 76.3       | 84.4          | 97.0          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 70.6        | 82.4         | 90.8           | 79.0       | 102.1         | 56.7          | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 34.7        | 43.7         | 21.0           | 36.2       | 24.3          | 16.7          | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 70.4        | 81.9         | 90.1           | 78.7       | 101.4         | 56.8          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | n/a         | n/a          | n/a            | n/a        | n/a           | 35.8          | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics—DC Limit Changes

T<sub>A</sub> = –40°C to +125°C, unless otherwise noted

| PARAMETER        | TEST CONDITIONS                                                                 | V <sub>CC</sub> | MIN | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|---------------------------------------------------------------------------------|-----------------|-----|--------------------|------|------|
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA                                                        | 1.65 V to 5.5 V |     |                    | 0.2  | V    |
|                  | I <sub>OL</sub> = 4 mA                                                          | 1.65 V          |     |                    | 0.45 |      |
|                  | I <sub>OL</sub> = 12 mA                                                         | 2.3 V           |     |                    | 0.7  |      |
|                  |                                                                                 | 2.7 V           |     |                    | 0.4  |      |
|                  | I <sub>OL</sub> = 24 mA                                                         | 3 V             |     |                    | 0.55 |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND                                                   | 3.6 V           |     |                    | ±5   | μA   |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                        | 0 V             |     |                    | ±10  | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                     | 3.6 V           |     |                    | 10   | μA   |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V,<br>Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  |     |                    | 500  | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                         | 3.3 V           |     | 5.0                |      | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) through [Figure 6](#))

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS |                                  | MIN | MAX | UNIT |
|-----------------|-----------------|----------------|-----------------|----------------------------------|-----|-----|------|
| t <sub>pd</sub> | A               | Y              | –40°C to 85°C   | V <sub>CC</sub> = 1.8 V ± 0.15 V | 1   | 5.6 | ns   |
|                 |                 |                |                 | V <sub>CC</sub> = 2.5 V ± 0.2 V  | 1   | 3.4 |      |
|                 |                 |                |                 | V <sub>CC</sub> = 2.7 V          | 1   | 3.3 |      |
|                 |                 |                |                 | V <sub>CC</sub> = 3.3 V ± 0.3 V  | 1   | 3.6 |      |
|                 |                 |                |                 | V <sub>CC</sub> = 5 V ± 0.5 V    | 1   | 2.6 |      |
|                 |                 |                | –40°C to 125°C  | V <sub>CC</sub> = 1.8 V ± 0.15 V | 1   | 6.1 |      |
|                 |                 |                |                 | V <sub>CC</sub> = 2.5 V ± 0.2 V  | 1   | 3.9 |      |
|                 |                 |                |                 | V <sub>CC</sub> = 2.7 V          | 1   | 3.8 |      |
|                 |                 |                |                 | V <sub>CC</sub> = 3.3 V ± 0.3 V  | 1   | 4.1 |      |
|                 |                 |                |                 | V <sub>CC</sub> = 5 V ± 0.5 V    | 1   | 3.1 |      |

## 6.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER                                                    | TEST CONDITIONS     | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|--------------------------------------------------------------|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
|                                                              |                     | TYP                     | TYP                     | TYP                     | TYP                   |      |
| $C_{pd}$ Power dissipation capacitance per buffer and driver | $f = 10\text{ MHz}$ | 1.8                     | 2                       | 2.5                     | 3.78                  | pF   |

## 6.8 Typical Characteristics

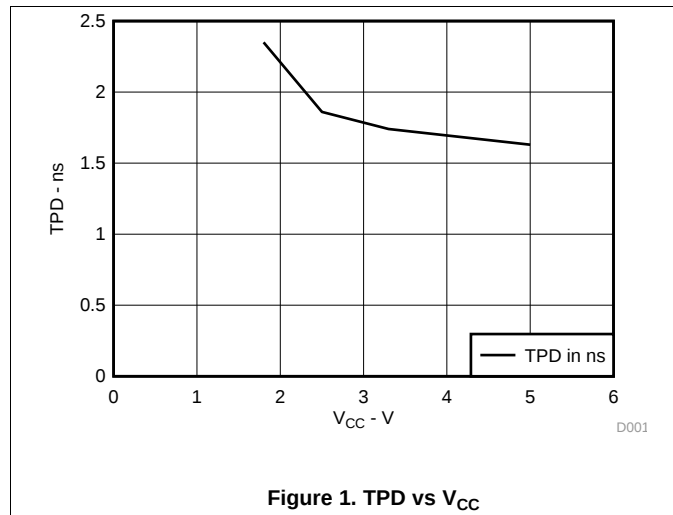


Figure 1. TPD vs  $V_{CC}$

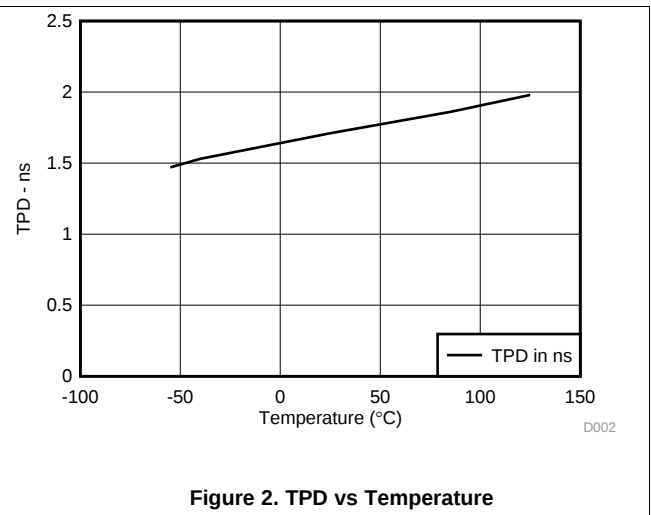
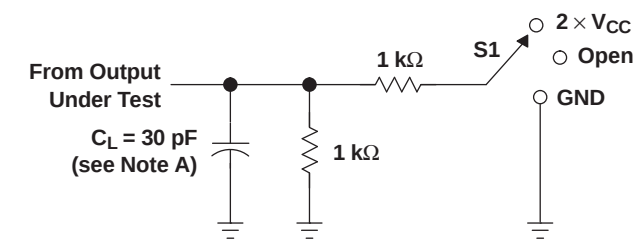


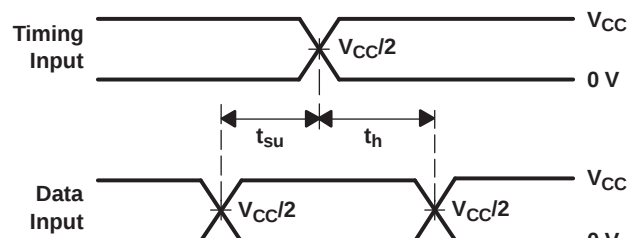
Figure 2. TPD vs Temperature

## 7 Parameter Measurement Information

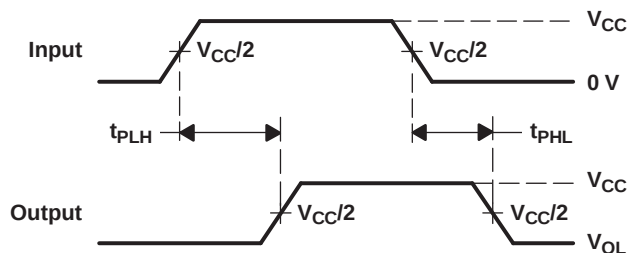
### 7.1 $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



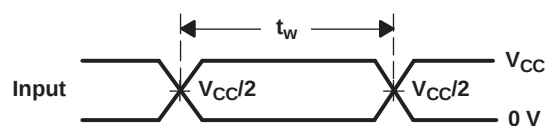
LOAD CIRCUIT



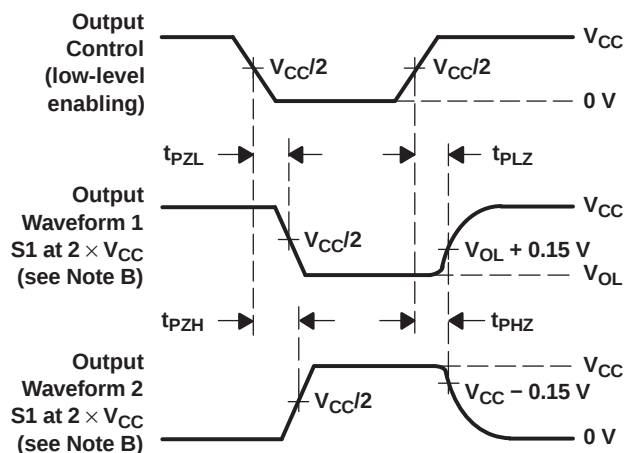
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION

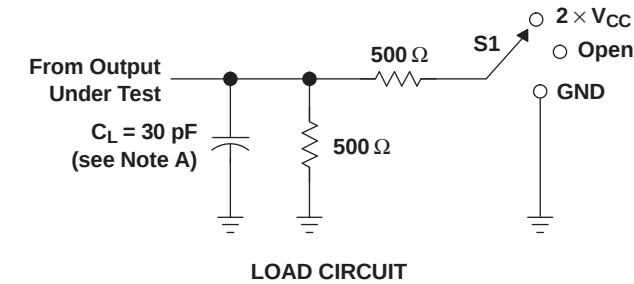


VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

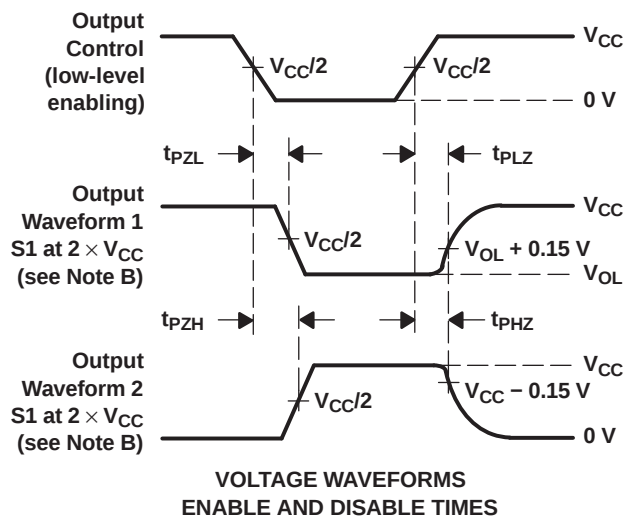
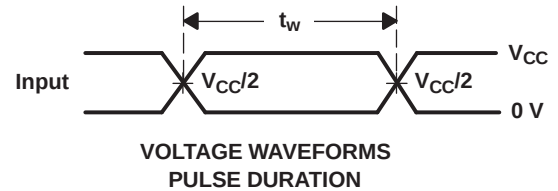
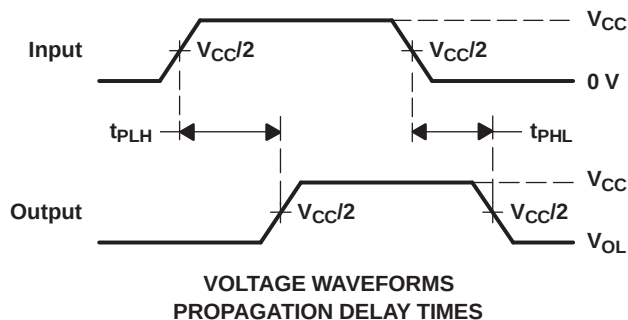
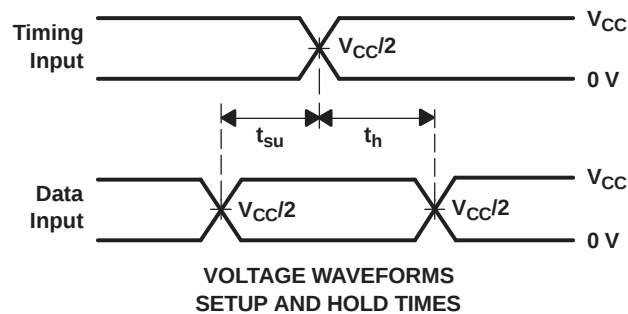
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  is measured at  $V_{CC}/2$ .
  - $t_{PLZ}$  is measured at  $V_{OL} + 0.15\text{ V}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

## 7.2 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



| TEST                   | S1                |
|------------------------|-------------------|
| $t_{PZL}$ (see Note F) | $2 \times V_{CC}$ |
| $t_{PLZ}$ (see Note G) | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$      | $2 \times V_{CC}$ |

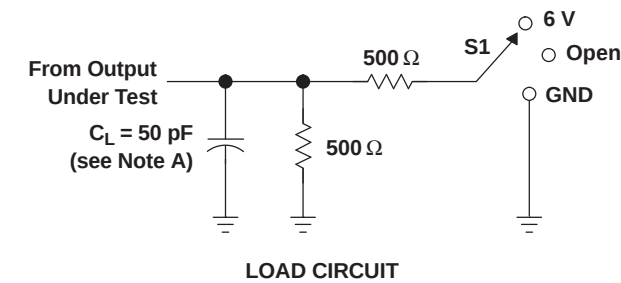


- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  is measured at  $V_{CC}/2$ .
  - $t_{PLZ}$  is measured at  $V_{OL} + 0.15\text{ V}$ .
  - All parameters and waveforms are not applicable to all devices.

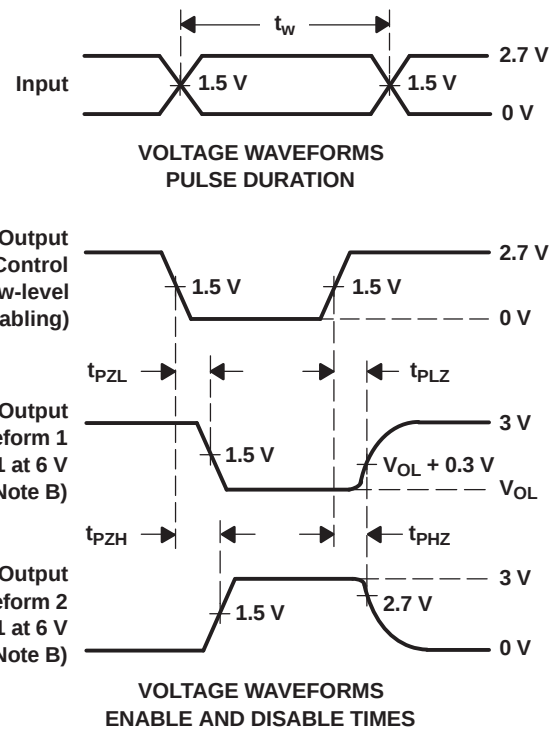
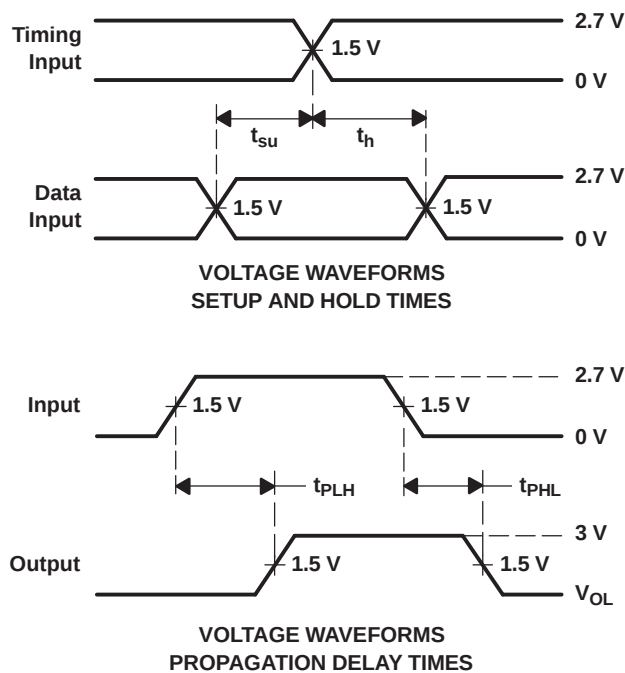
Figure 4. Load Circuit and Voltage Waveforms

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[www.ti.com](http://www.ti.com)
**7.3  $V_{CC} = 2.7$  and  $3.3\text{ V} \pm 0.3\text{ V}$** 


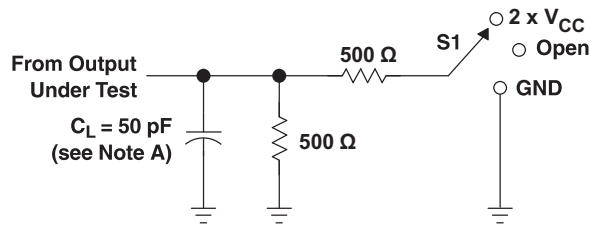
| TEST                   | S1  |
|------------------------|-----|
| $t_{PZL}$ (see Note F) | 6 V |
| $t_{PLZ}$ (see Note G) | 6 V |
| $t_{PHZ}/t_{PZH}$      | 6 V |



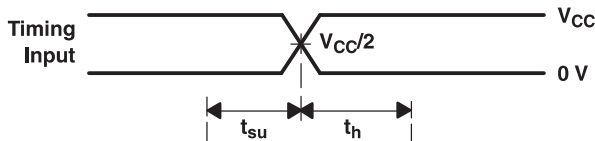
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  is measured at 1.5 V.
  - $t_{PLZ}$  is measured at  $V_{OL} + 0.3\text{ V}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 5. Load Circuit and Voltage Waveforms**

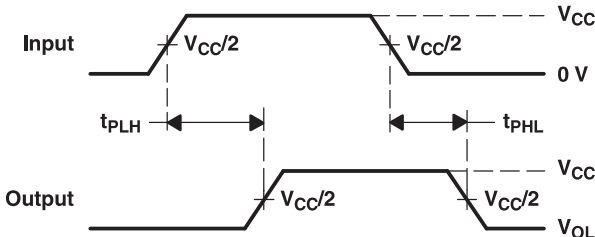
## 7.4 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$



LOAD CIRCUIT

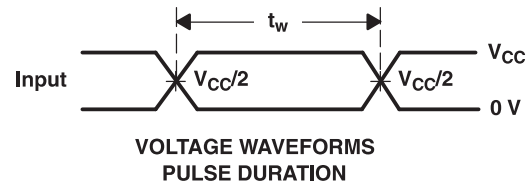


VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES

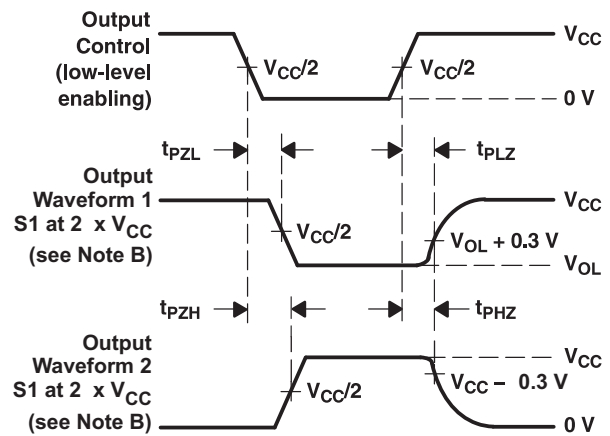


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

| TEST                   | S1           |
|------------------------|--------------|
| $t_{PZL}$ (see Note F) | 2 x $V_{CC}$ |
| $t_{PLZ}$ (see Note G) | 2 x $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$      | 2 x $V_{CC}$ |



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal connections such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal connections such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
  - $t_{PZL}$  is measured at  $V_{CC}/2$ .
  - $t_{PLZ}$  is measured at  $V_{OL} + 0.3\text{ V}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 6. Load Circuit and Voltage Waveforms

## 8 Detailed Description

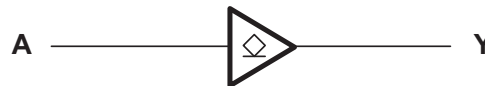
### 8.1 Overview

The outputs of the SN74LVC07A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 5.5 V
- Allows up or down voltage translation
  - Inputs and outputs accept voltages to 5.5 V
- $I_{off}$  feature
  - Allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

### 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC07A.

**Table 1. Function Table**

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | Hi-Z        |
| L          | L           |

## 9 Application and Implementation

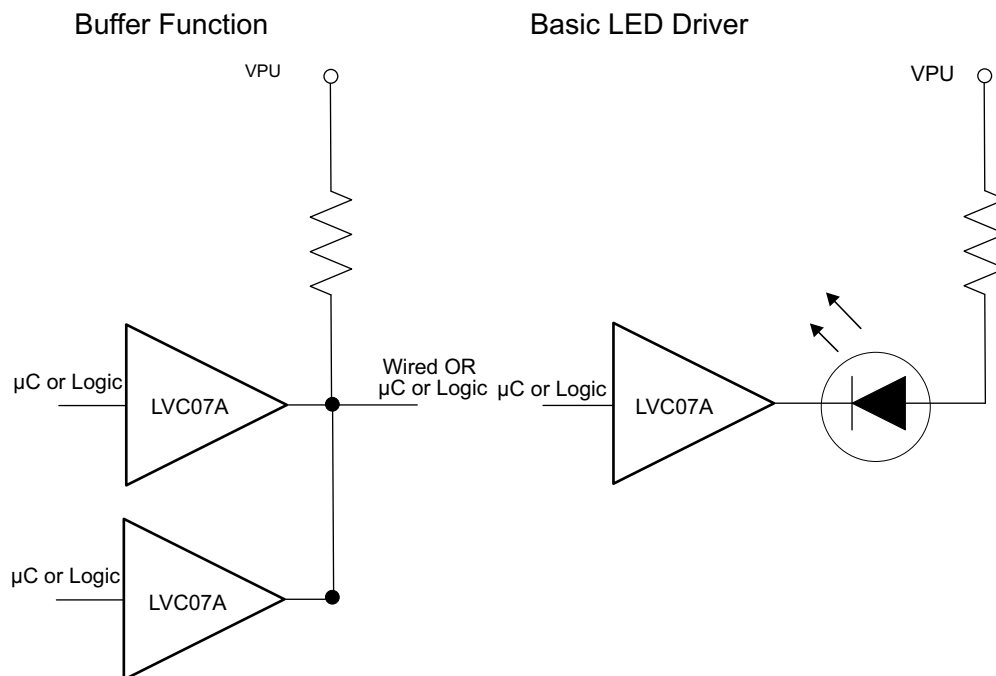
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LVC07A device is a high-drive, open-drain CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to translate up to 5.5 V or down to  $V_{CC}$ .

### 9.2 Typical Application



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**Figure 7. Typical Application Diagram**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions must be considered to prevent ringing.

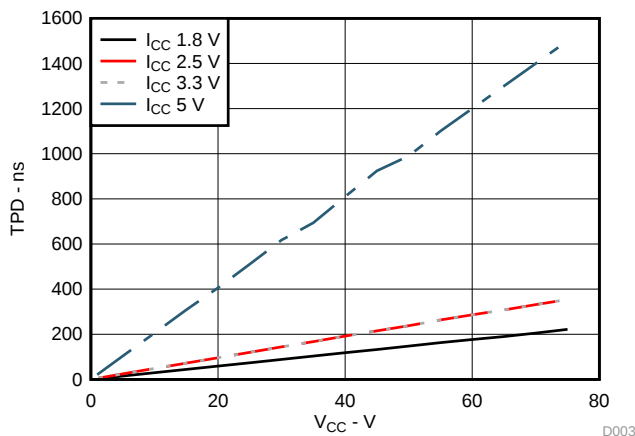
#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommended Output Conditions

## Typical Application (continued)

- Load currents must not exceed 25 mA per output and 50 mA total for the part.
- Outputs must not be pulled above 5.5 V.

### 9.2.3 Application Curve



**Figure 8.  $I_{CC}$  vs Frequency**

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{f}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{f}$  or 0.022  $\mu\text{f}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{f}$  and a 1  $\mu\text{f}$  are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 9](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

## 11.2 Layout Example

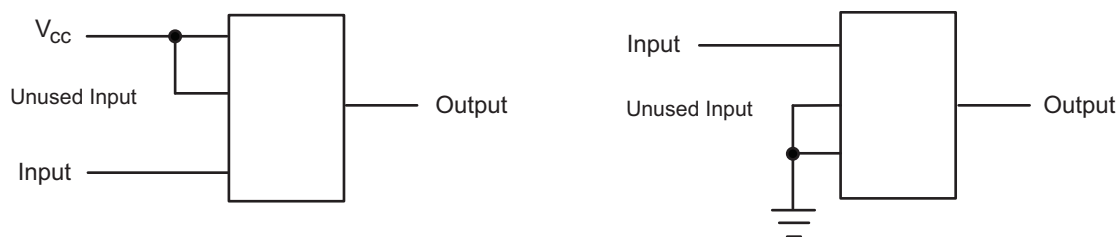


Figure 9. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [Implications of Slow or Floating CMOS Inputs](#), SCBA004.
- [Semiconductor and IC Package Thermal Metrics](#), SPRA953.

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LVC07AD</a>     | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| SN74LVC07AD.B                   | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| <a href="#">SN74LVC07ADBR</a>   | Active        | Production           | SSOP (DB)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07ADBR.B                 | Active        | Production           | SSOP (DB)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07ADE4                   | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| <a href="#">SN74LVC07ADGVR</a>  | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07ADGVR.B                | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07ADGVR1G4               | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07ADGVR1G4.B             | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| <a href="#">SN74LVC07ADR</a>    | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| SN74LVC07ADR.B                  | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| <a href="#">SN74LVC07ADRG3</a>  | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| SN74LVC07ADRG3.B                | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| <a href="#">SN74LVC07ADRG4</a>  | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| SN74LVC07ADRG4.B                | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| <a href="#">SN74LVC07ADT</a>    | Active        | Production           | SOIC (D)   14    | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| SN74LVC07ADT.B                  | Active        | Production           | SOIC (D)   14    | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| <a href="#">SN74LVC07ANSR</a>   | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| SN74LVC07ANSR.B                 | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC07A              |
| <a href="#">SN74LVC07APW</a>    | Active        | Production           | TSSOP (PW)   14  | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07APW.B                  | Active        | Production           | TSSOP (PW)   14  | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07APWE4                  | Active        | Production           | TSSOP (PW)   14  | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07APWG4                  | Active        | Production           | TSSOP (PW)   14  | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| <a href="#">SN74LVC07APWR</a>   | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07APWR.B                 | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07APWRE4                 | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| <a href="#">SN74LVC07APWRG3</a> | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07APWRG3.B               | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| <a href="#">SN74LVC07APWRG4</a> | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74LVC07APWRG4.B              | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| <a href="#">SN74LVC07APWT</a>  | Active        | Production           | TSSOP (PW)   14 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07APWT.B                | Active        | Production           | TSSOP (PW)   14 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| SN74LVC07APWTG4                | Active        | Production           | TSSOP (PW)   14 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC07A               |
| <a href="#">SN74LVC07ARGYR</a> | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | LC07A               |
| SN74LVC07ARGYR.B               | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | LC07A               |
| SN74LVC07ARGYRG4               | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | LC07A               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC07A :**

- Automotive : [SN74LVC07A-Q1](#)
- Enhanced Product : [SN74LVC07A-EP](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC07ADBR     | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74LVC07ADGVR    | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC07ADGVR1G4 | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC07ADR      | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC07ADRG3    | SOIC         | D               | 14   | 2500 | 330.0              | 16.8               | 6.5     | 9.5     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC07ADRG4    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC07ADRG4    | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC07ADT      | SOIC         | D               | 14   | 250  | 180.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC07ANSR     | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC07APWR     | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC07APWR     | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC07APWRG3   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC07APWRG4   | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC07APWT     | TSSOP        | PW              | 14   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC07ARGYR    | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC07ADBR     | SSOP         | DB              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC07ADGVR    | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC07ADGVR1G4 | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC07ADR      | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74LVC07ADRG3    | SOIC         | D               | 14   | 2500 | 364.0       | 364.0      | 27.0        |
| SN74LVC07ADRG4    | SOIC         | D               | 14   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74LVC07ADRG4    | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74LVC07ADT      | SOIC         | D               | 14   | 250  | 213.0       | 191.0      | 35.0        |
| SN74LVC07ANSR     | SOP          | NS              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC07APWR     | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC07APWR     | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74LVC07APWRG3   | TSSOP        | PW              | 14   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVC07APWRG4   | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC07APWT     | TSSOP        | PW              | 14   | 250  | 353.0       | 353.0      | 32.0        |
| SN74LVC07ARGYR    | VQFN         | RGY             | 14   | 3000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVC07AD    | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVC07AD.B  | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVC07ADE4  | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVC07APW   | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVC07APW.B | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVC07APWE4 | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVC07APWG4 | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |

## GENERIC PACKAGE VIEW

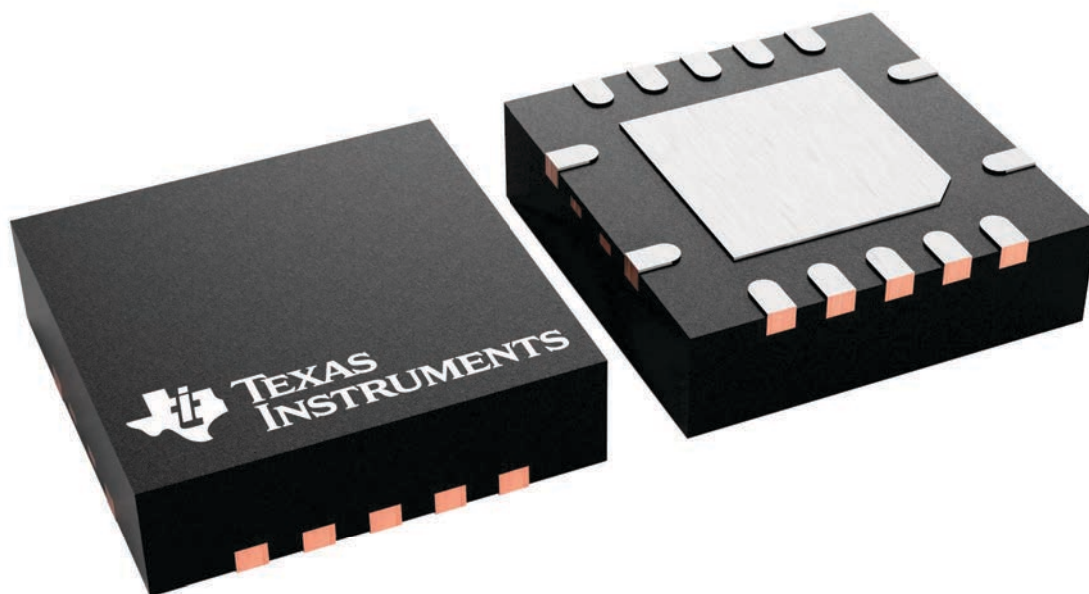
**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A

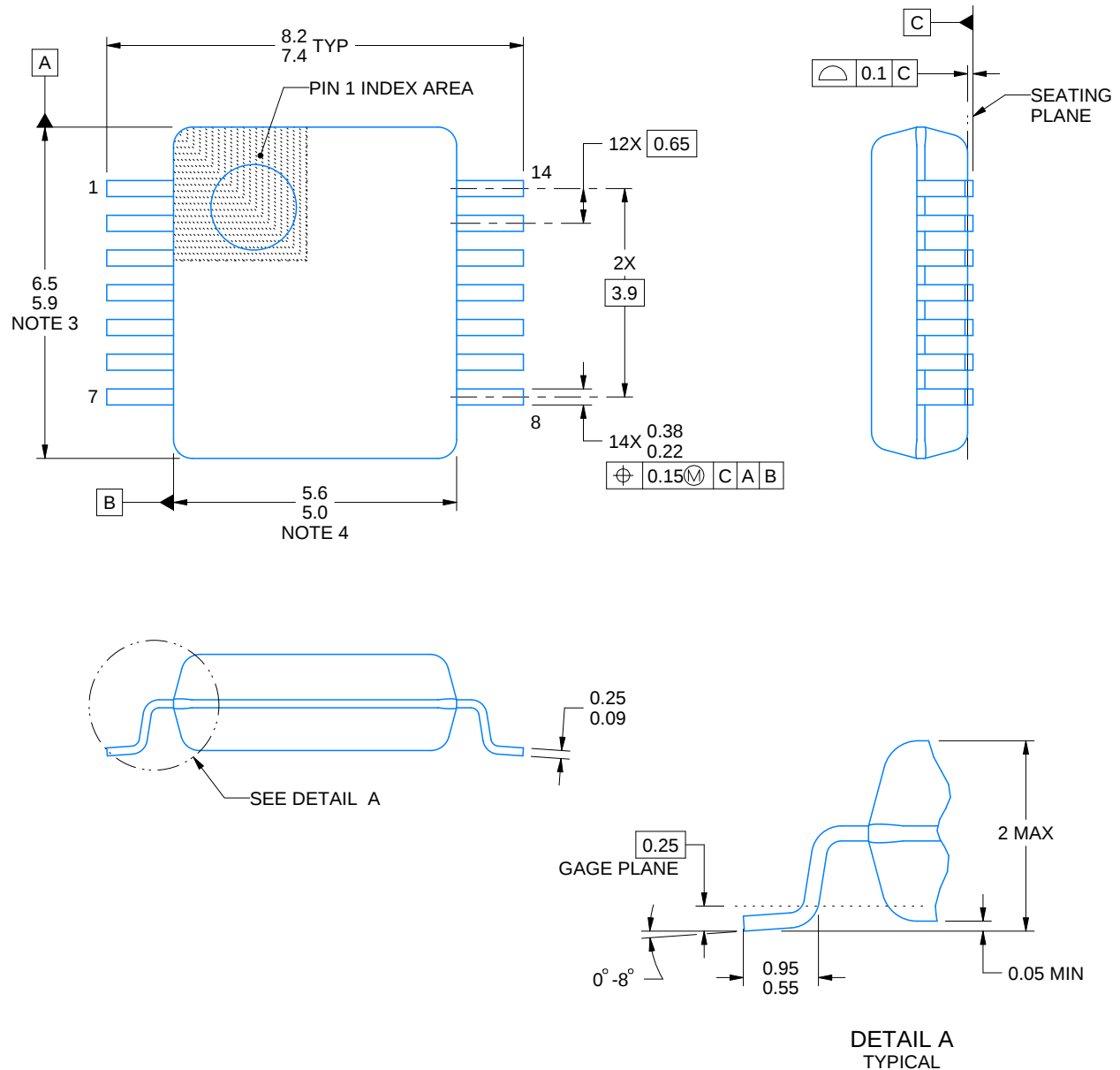
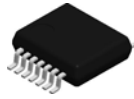
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



4220762/A 05/2024

## NOTES:

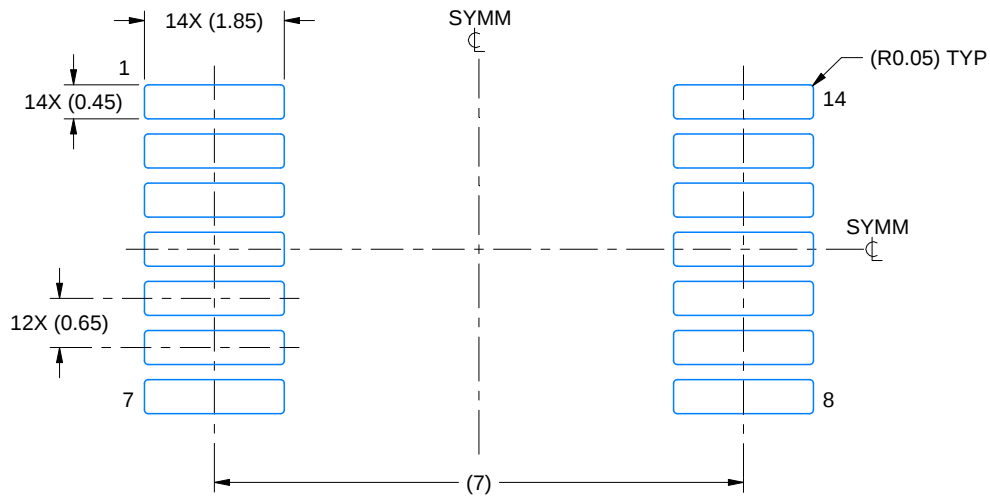
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

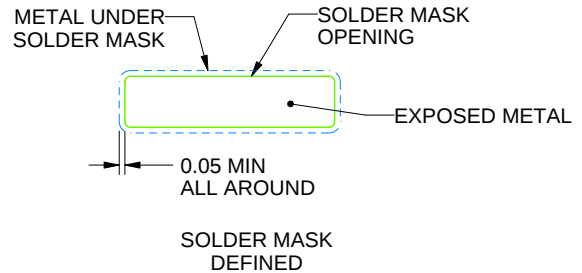
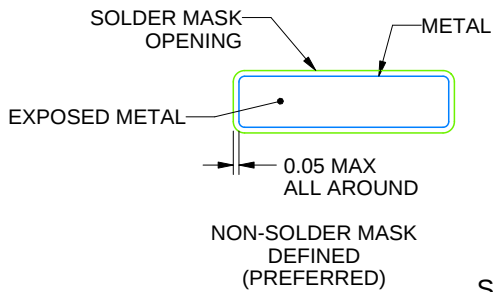
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

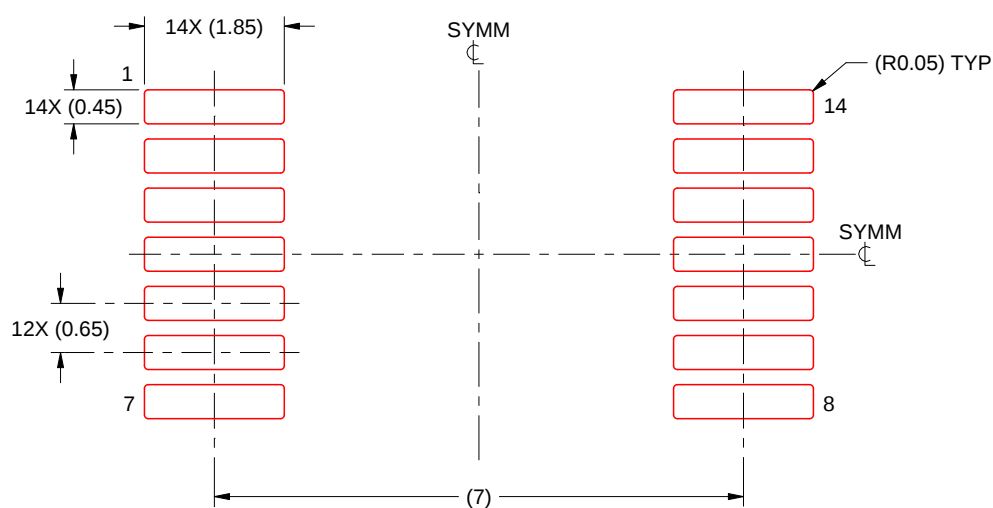
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

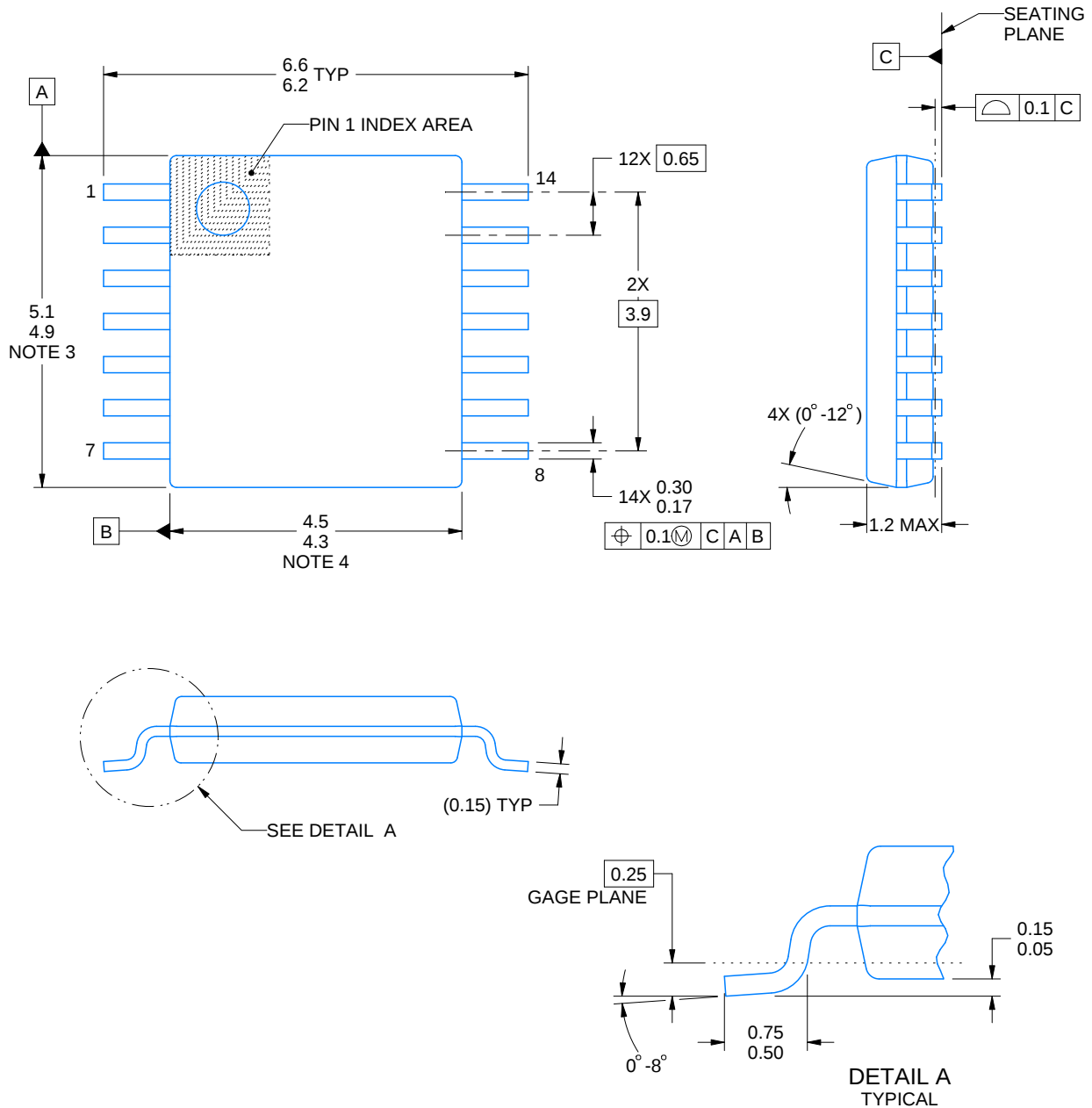
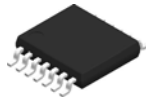


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

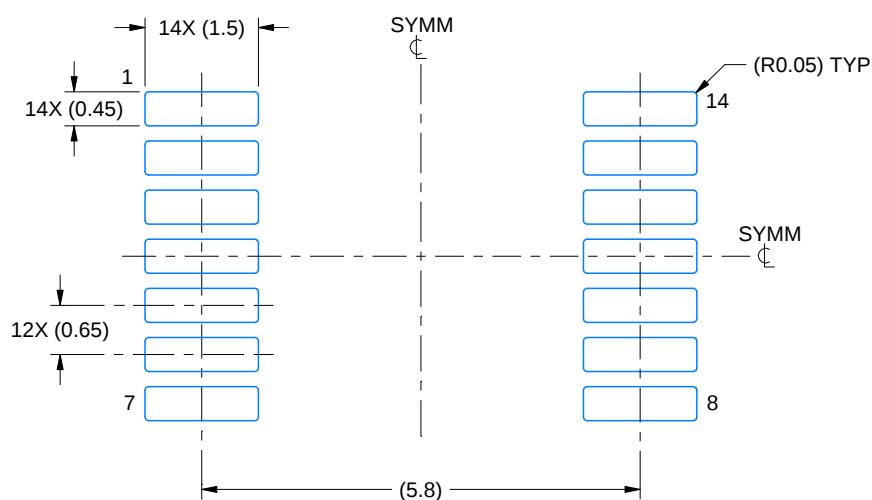
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

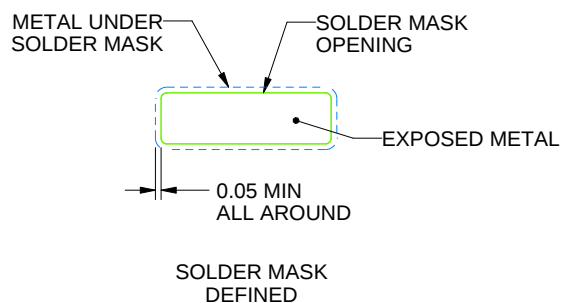
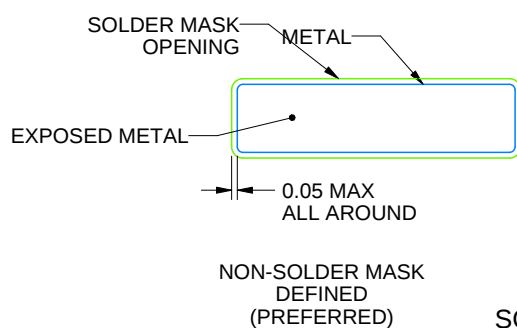
**PW0014A**

**TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

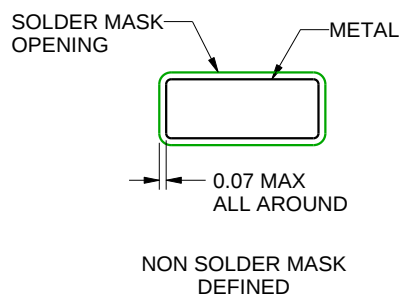
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

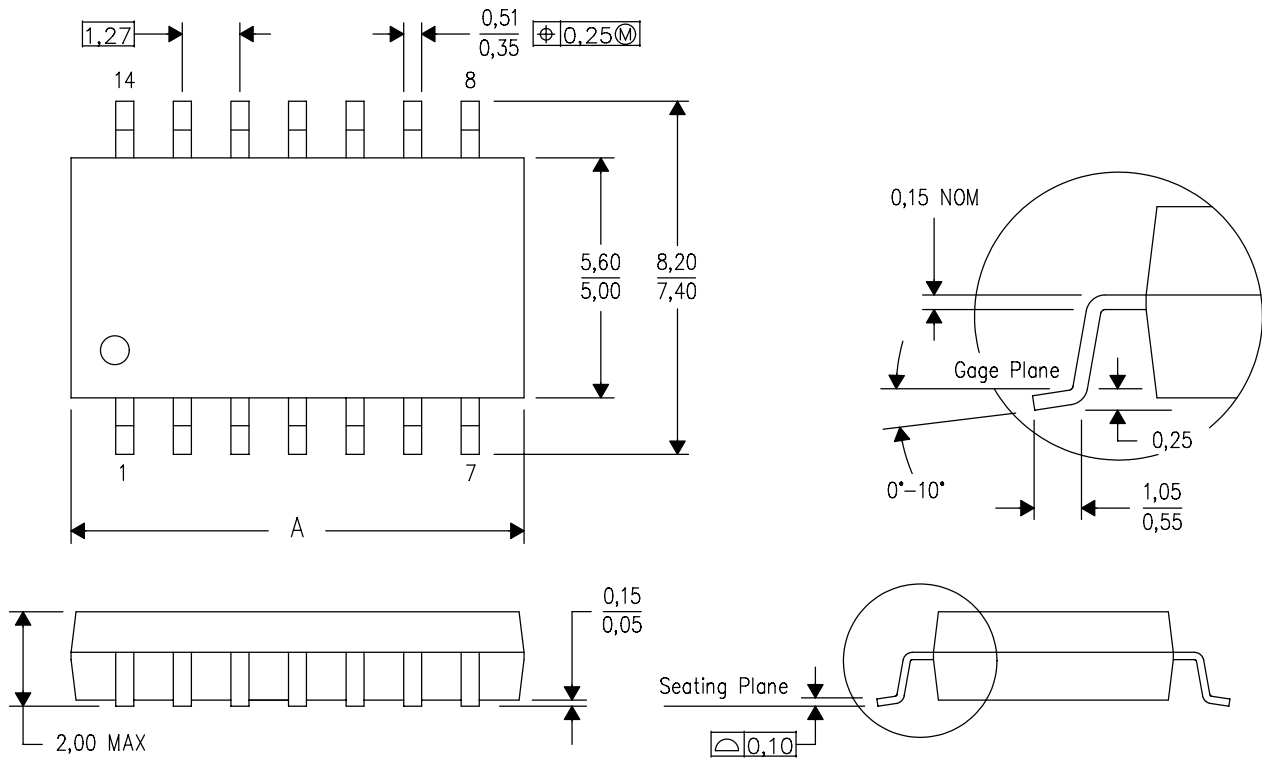
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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