SN74LVC1G04B-Q1 Automotive Single 1.1V to 5.5V Inverter

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Operating range from 1.1V to 5.5V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Supports partial-power-down with back drive protection (I_{off})
- High push-pull output drive strength:
  - ±32mA at 5V
  - ±24mA at 3.3V
  - ±8mA at 2.5V
  - ±4mA at 1.8V
- Maximum propagation delay of 3.6ns
- Latch-up performance exceeds 100mA per JESD78 and AEC-Q100-004

2 Applications

- Advanced driver assistance systems (ADAS)
- Body electronics and lighting
- Infotainment and cluster

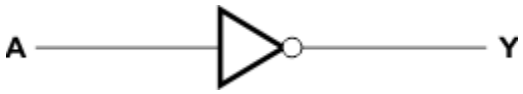
3 Description

The SN74LVC1G04B-Q1 device is a low-power single inverter that performs the Boolean function $Y = \overline{A}$.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
SN74LVC1G04B-Q1	DTX (X2SON, 5)	1.10mm × 0.85mm

(1) For more information, see Section 11.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

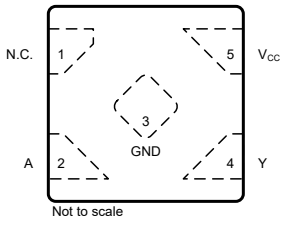


**Figure 4-1. or DTX Package,
5-Pin X2SON
(Top View)**

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	DTX		
N.C.	1	—	Not internally connected
A	2	I	Input A
GND	3	G	Ground pin
Y	4	O	Output Y
VCC	5	P	Power supply

(1) I = Input, O = Output, G = Ground, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range - High Impedance(2)		-0.5	6.5	V
I_{IK}	Input diode clamp current	V_I < -0.5V		-50	mA
I_{OK}	Output diode clamp current	V_O < -0.5V		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage - High or Low state		0	V_{CC}	V
I_{OH}(1)	High-level output current	V_{CC} = 1.2V		–1	mA
		V_{CC} = 1.5V		–4	
		V_{CC} = 1.8V		–6	
		V_{CC} = 2.5V		–16	
		V_{CC} = 3.3V		–32	
		V_{CC} = 5V		–50	
I_{OL}(1)	Low-level output current	V_{CC} = 1.2V		1	mA
		V_{CC} = 1.5V		4	
		V_{CC} = 1.8V		6	
		V_{CC} = 2.5V		16	
		V_{CC} = 3.3V		32	
		V_{CC} = 5V		50	
V_{IH}	High-level input voltage	V_{CC} = 1.1V to 1.95V	0.65x V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3.0V to 3.6V	2		
		V_{CC} = 4.5V to 5.5V	0.7x V_{CC}		
V_{IL}	Low-Level input voltage	V_{CC} = 1.1V to 1.95V		0.35x V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3.0V to 3.6V		0.8	
		V_{CC} = 4.5V to 5.5V		0.3x V_{CC}	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.1V to 2.7V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		5	
T_A	Operating free-air temperature		-40	125	°C

(1) Recommended maximum output current for continuous operation; see *Electrical Characteristics* for test current values to maintain V_{OH} and V_{OL} specifications. Operating with average output current greater than 32mA may impact device reliability and shorten the device lifetime.

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DTX (X2SON, 5)	5	393.6	103.2	331.8	69.8	331.9	179.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= –100µA	1.1V to 5.5V	V_{CC} - 0.1			V
	I_{OH}= –4mA	1.65V	1.2			
	I_{OH}= –8mA	2.3V	1.9			
	I_{OH}= –12mA	2.7V	2.2			
	I_{OH}= –16mA	3V	2.4			
	I_{OH}= –24mA	3V	2.3			
	I_{OH}= –32mA	4.5V	3.8			
V_{OL}	I_{OL}= 100µA	1.1V to 5.5V			0.2	V
	I_{OL}= 4mA	1.65V			0.45	
	I_{OL}= 8mA	2.3V			0.3	
	I_{OL}= 12mA	2.7V			0.4	
	I_{OL}= 16mA	3V			0.4	
	I_{OL}= 24mA	3V			0.55	
	I_{OL}= 32mA	4.5V			0.55	
I_I	V_I = V_{CC} or GND	V_{CC} = 0V to 5.5V		±0.01	±5	µA
I_{OFF}	V_I or V_O = V_{CC}	V_{CC} = 0V		±0.1	±10	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 1.1V to 5.5V		0.01	10	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	3.0V to 5.5V			500	µA
C_I	V_I = V_{CC} or GND	3.3V		3.5		pF
C_O	V_O = V_{CC} or GND	3.3V		6.3		pF

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5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A	Y	C_L = 15pF	1.2V ± 0.1V			31.3	ns
				1.5V ± 0.12V			8.4	
				1.8V ± 0.15V			5.5	
				2.5V ± 0.2V			3.6	
				3.3V ± 0.3V			2.9	
				5.0V ± 0.5V			2.5	
			C_L = 30pF	1.8V ± 0.15V			5.2	
				2.5V ± 0.2V			3.3	
			C_L = 50pF	3.3V ± 0.3V			3.6	
				5.0V ± 0.5V			2.9	
C_{pd}			f = 10MHz	1.8V		3		pF
				2.5V		3		
				3.3V		3		
				5.0V		4		

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5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

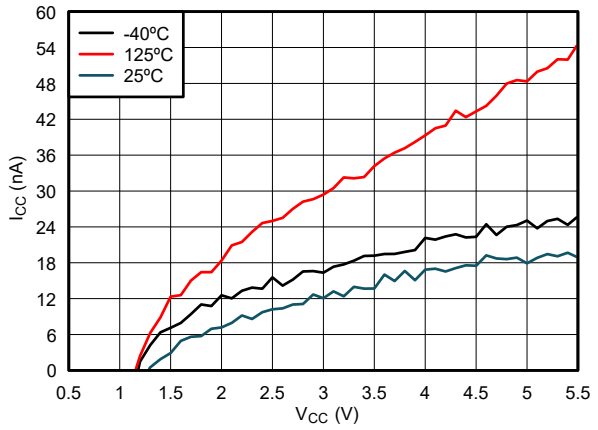


Figure 5-1. Supply Current Across Supply Voltage and Temperature

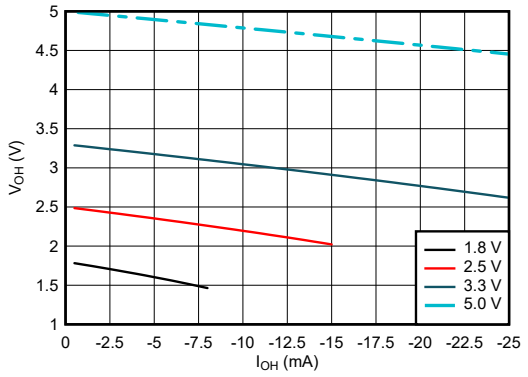


Figure 5-2. Output Voltage vs Current in HIGH State

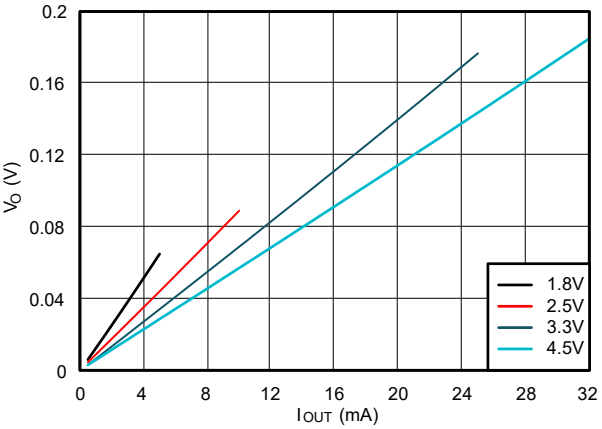


Figure 5-3. Output Voltage vs Current in LOW State

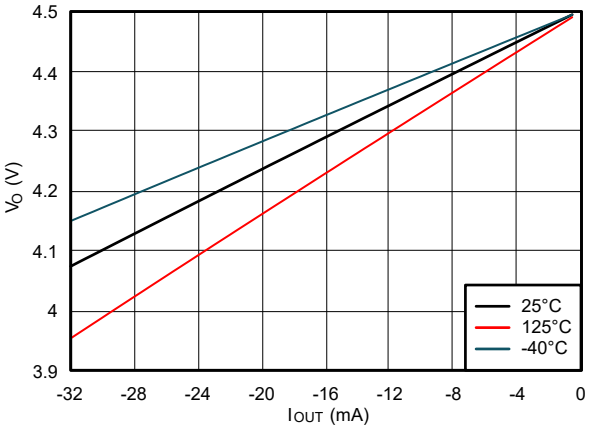


Figure 5-4. Output Voltage vs Current in HIGH State; 4.5V Supply

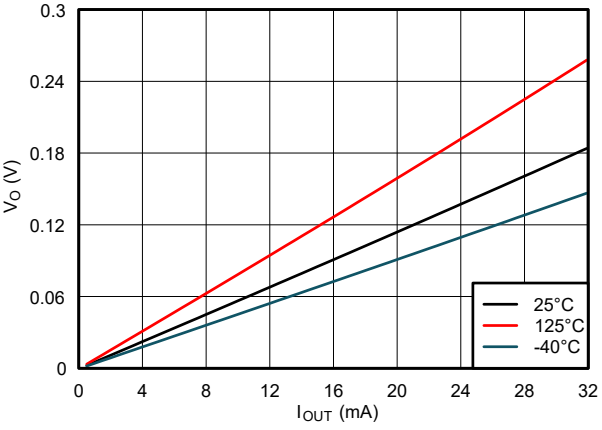


Figure 5-5. Output Voltage vs Current in LOW State; 4.5V Supply

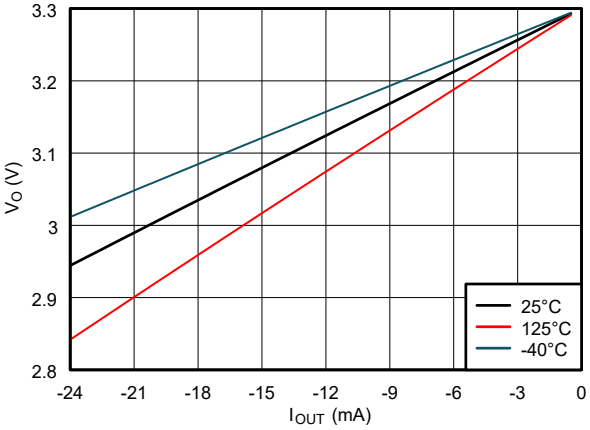


Figure 5-6. Output Voltage vs Current in HIGH State; 3.3V Supply

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5.7 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

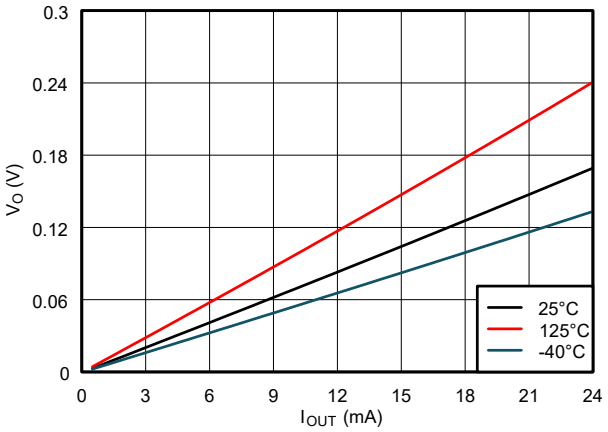


Figure 5-7. Output Voltage vs Current in LOW State; 3.3V Supply

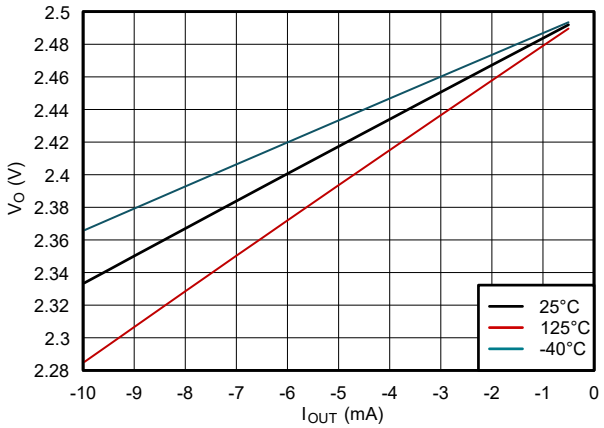


Figure 5-8. Output Voltage vs Current in HIGH State; 2.5V Supply

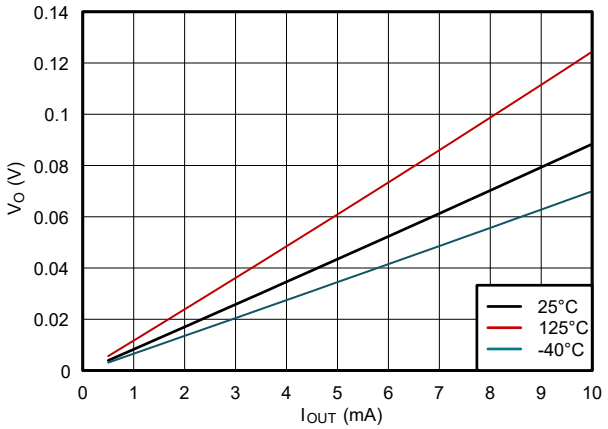


Figure 5-9. Output Voltage vs Current in LOW State; 2.5V Supply

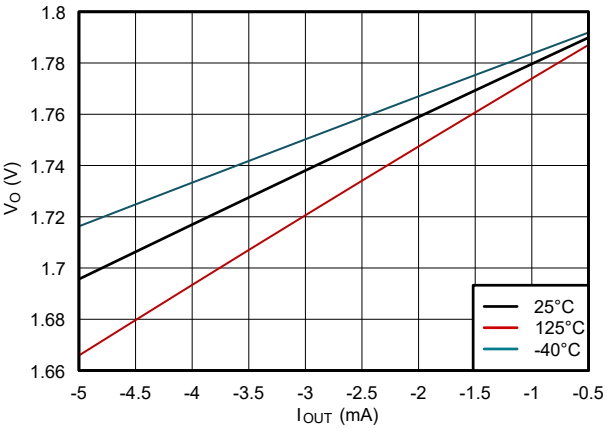


Figure 5-10. Output Voltage vs Current in HIGH State; 1.8V Supply

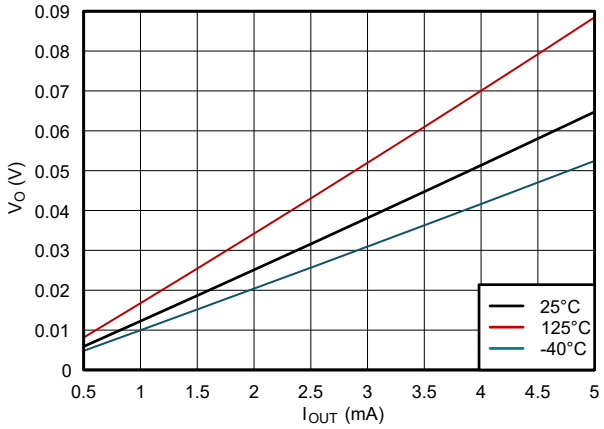


Figure 5-11. Output Voltage vs Current in LOW State; 1.8V Supply

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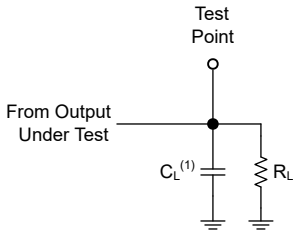
6 Parameter Measurement Information

Phase relationships between waveforms are chosen arbitrarily for the examples listed in the following table. Generators with the following characteristics supply all input pulses : PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

The outputs are measured individually with one input transition per measurement.

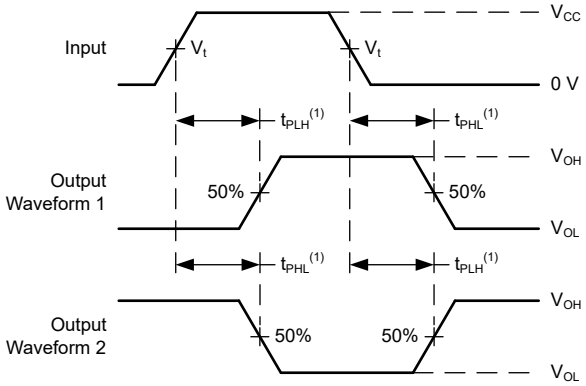
Table 6-1. Push-Pull Outputs

V_{CC}	V_t	R_L	C_L	ΔV
1.2V ± 0.1V	V_{CC}/2	2kΩ	15pF	0.1V
1.5V ± 0.12V	V_{CC}/2	2kΩ	15pF	0.1V
1.8V ± 0.15V	V_{CC}/2	1kΩ	15pF/30pF	0.15V
2.5V ± 0.2V	V_{CC}/2	500Ω	15pF/30pF	0.15V
3.3V ± 0.3V	1.5V	500Ω	15pF/50pF	0.3V
5.0V ± 0.5V	1.5V	500Ω	15pF/50pF	0.3V



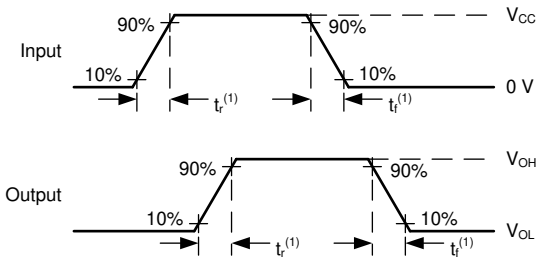
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

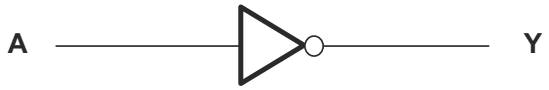
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7 Detailed Description

7.1 Overview

The SN74LVC1G04B-Q1 device contains inverter gate and performs the Boolean function Y = $\overline{A}$. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.3.4 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

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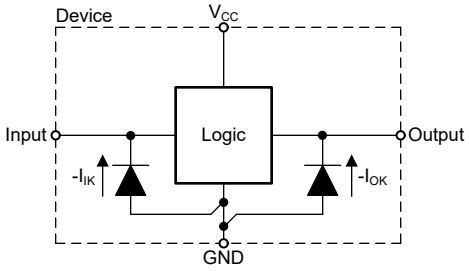


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.5 Over-Voltage Tolerant Inputs

The SN74LVC1G04B-Q1 includes over-voltage tolerant inputs. The input pins support high-state input voltages larger than the supply voltage by utilizing an input protection circuit that does not include a standard positive clamp diode. See *Recommended Operating Conditions* for the recommended input voltage.

CAUTION

Do not exceed the maximum input voltage range provided in *Absolute Maximum Ratings*. Exceeding the maximum input voltage range rating can cause immediate and permanent damage to the device.

7.4 Device Functional Modes

The Function Table lists the functional modes for SN74LVC1G04B-Q1.

Table 7-1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UVP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

8.2 Typical Application

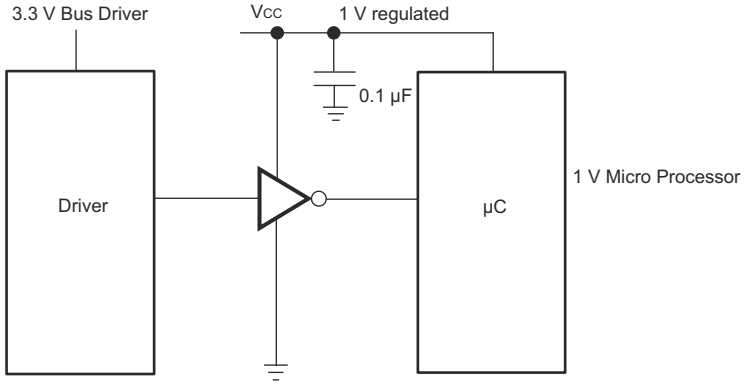


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention. Bus contention can drive currents that exceed maximum limits.

8.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specs. See (Δt/ΔV) in *Recommended Operating Conditions*
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*
   - Inputs are overvoltage tolerant allowing them to go as high as 3.6V at any valid V_{CC}
2. Recommend output conditions
   - Load currents must not exceed 20mA on the output and 50mA total for the part
   - Do not pull outputs above V_{CC}

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each V_{CC} terminal has a good bypass capacitor to prevent power disturbance. For the SN74LVC1G04B-Q1, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

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8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

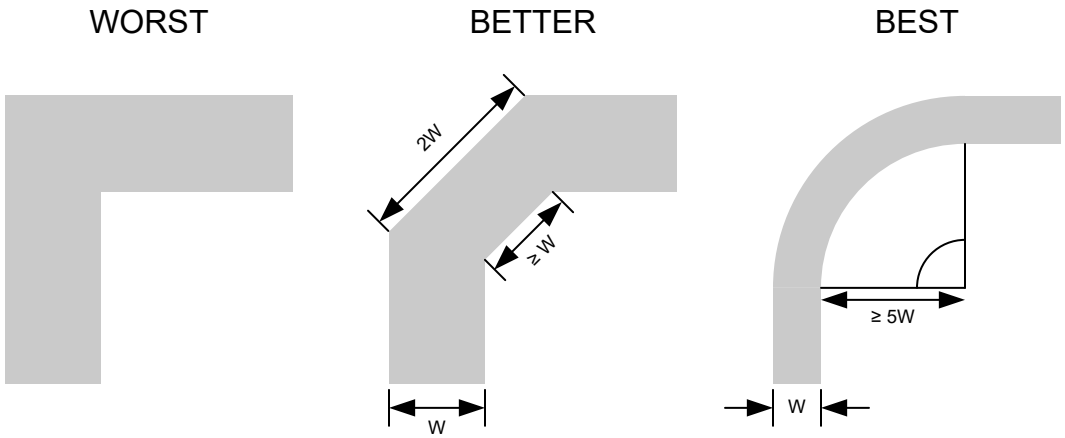


Figure 8-2. Example Trace Corners for Improved Signal Integrity

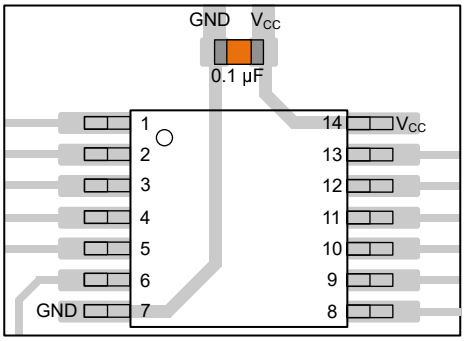


Figure 8-3. Example Bypass Capacitor Placement for TSSOP and Similar Packages

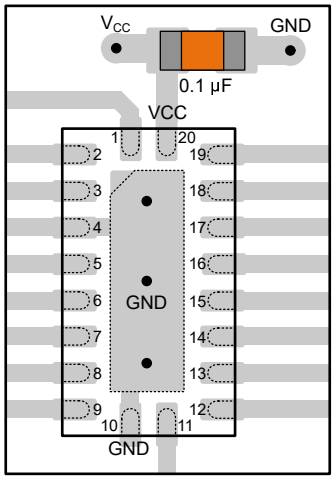


Figure 8-4. Example Bypass Capacitor Placement for WQFN and Similar Packages

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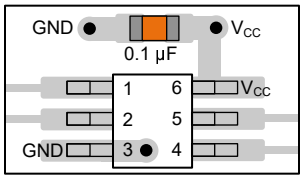


Figure 8-5. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

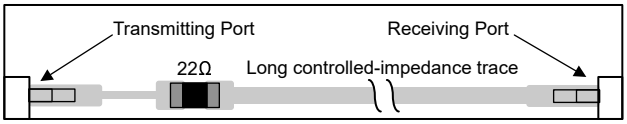


Figure 8-6. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application brief
- Texas Instruments, *Logic in Live-Insertion Applications With a Focus on GTLP* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Texas Instruments General Quality Guidelines*
- Texas Instruments, *Thermal Characteristics of SLL Packages and Devices* application note
- Texas Instruments, *Understanding Schmitt Triggers* application brief

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

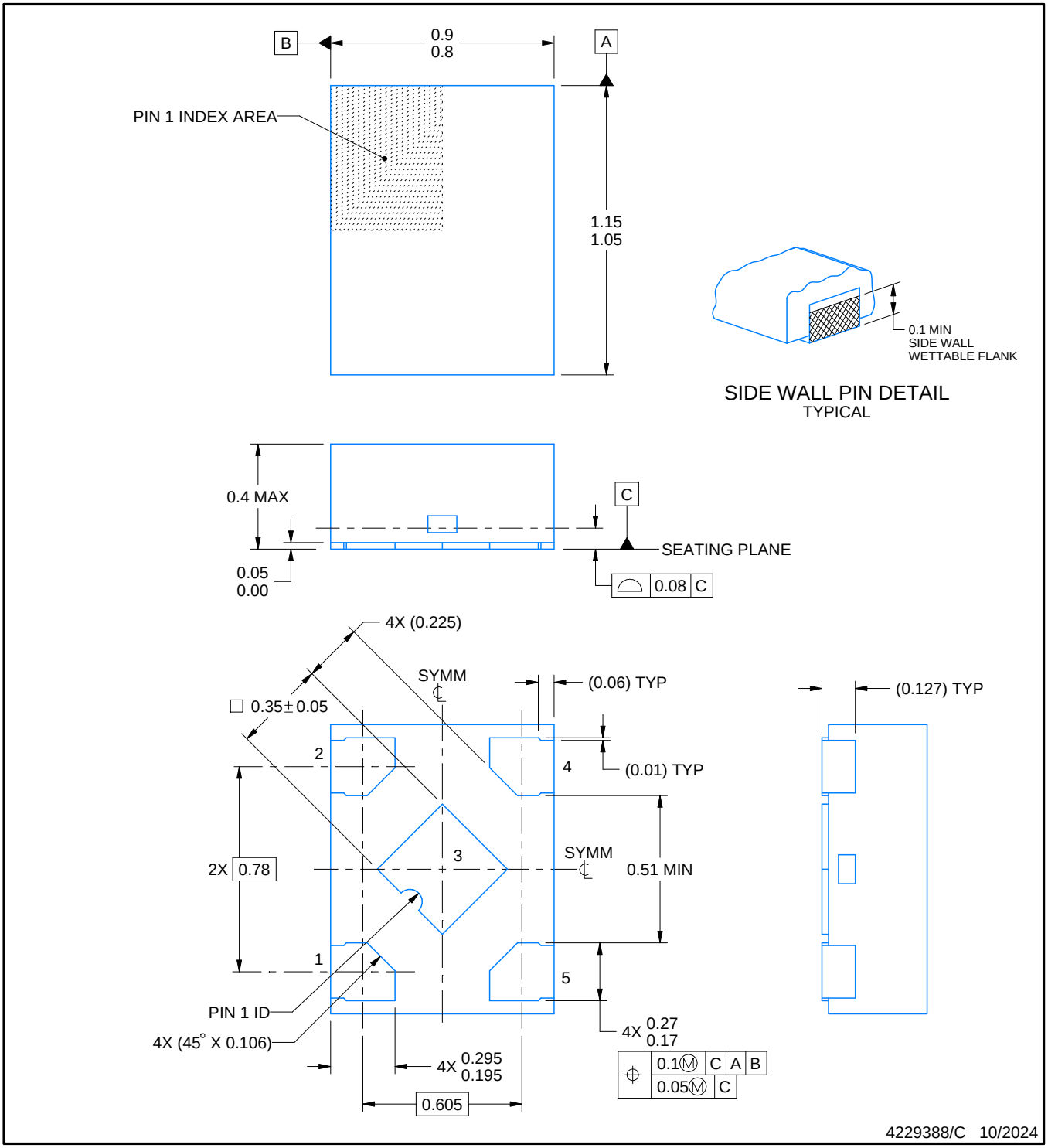
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PACKAGE OUTLINE

DTX0005A

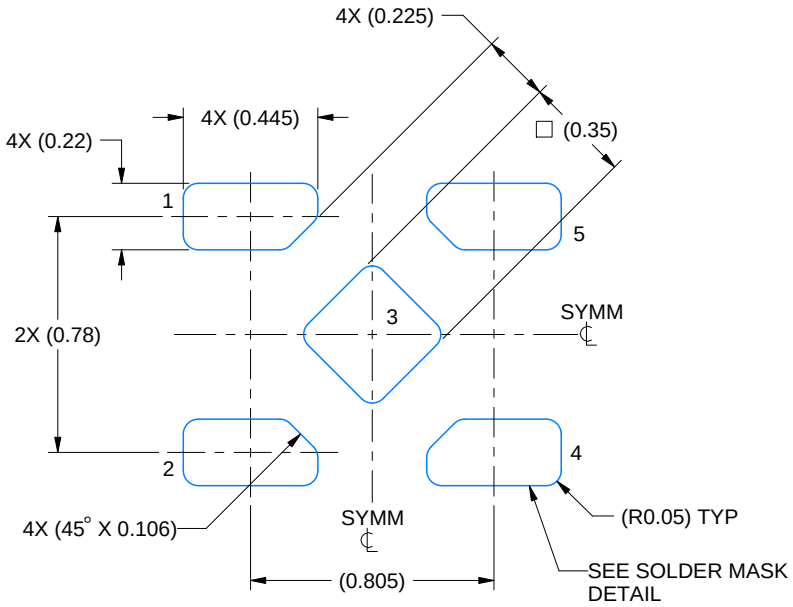
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

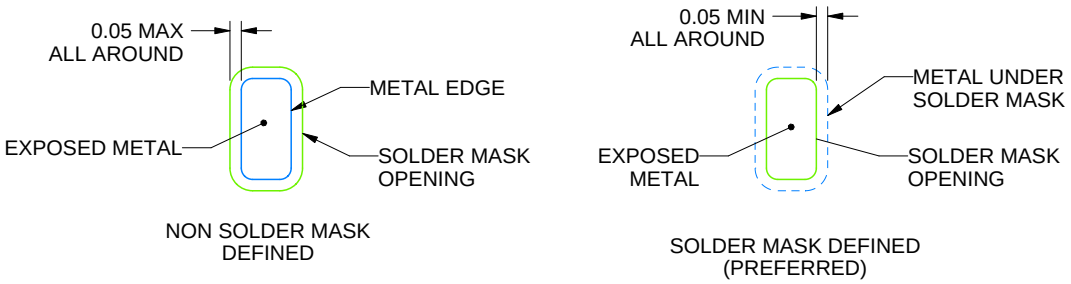


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

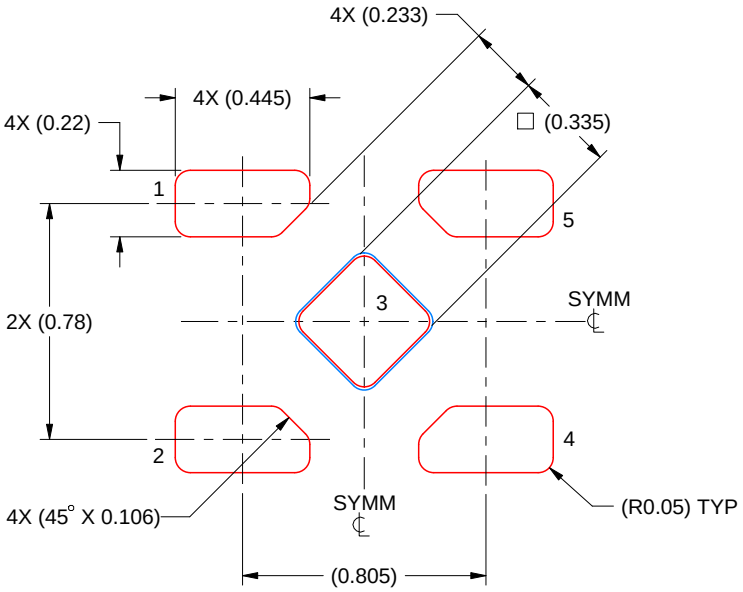


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

PRINTED SOLDER PASTE COVERAGE BY AREA UNDER PACKAGE
PAD 5: 92%

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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