# SN74LVC1G09B-Q1 Automotive Single 2–Input Positive-AND Gate with Open-Drain Output

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
- Operating range from 1.1V to 5.5V
- 5.5V tolerant input pins
- Supports standard pinouts
- Latch-up performance exceeds 100mA per JESD 78

## 2 Applications

- Combining power good signals
- Enable digital signals

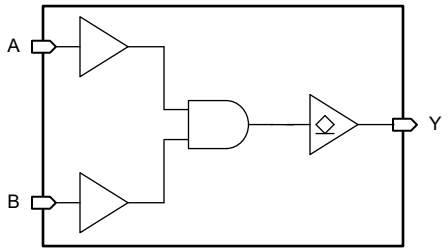
## 3 Description

The SN74LVC1G09B-Q1 device is a single 2-input positive-AND gate with an open-drain output.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN74LVC1G09B-Q1 | DTX (XSON, 5) | 1.1mm × 0.85mm | 1.1mm × 0.85mm |
| SN74LVC1G09B-Q1 | DBV (SOT-23, 5) | 2.9mm × 2.8mm | 2.9mm × 1.6mm |
| SN74LVC1G09B-Q1 | DCK (SOT-SC70, 5) | 2mm × 2.1mm | 2mm × 1.25mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram**

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# 4 Pin Configuration and Functions

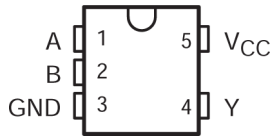



**Figure 4-1. DBV or DCK Package, 5-Pin SOT-23 or SOT-SC70 (Top View)**

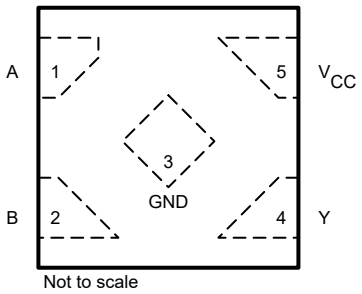



**Figure 4-2. DTX Package, 5-Pin X2SON (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A | 1 | I | Input A |
| B | 2 | I | Input B |
| GND | 3 | G | Ground Pin |
| Y | 4 | O | Output Y |
| $V_{CC}$ | 5 | P | Power Pin |

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | -0.5 | 6.5 | V |
| $V_O$ | Output voltage range (2) | | -0.5 | 6.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0V | | -50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0V | | -50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| $I_O$ | Continuous output current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | -65 | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B | ±1000 | |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Specifications | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.1 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | (High Impedance) | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65V to 1.95V | 0.65x Vcc | | V |
| | | $V_{CC}$ = 2.3V to 2.7V | 1.7 | | |
| | | $V_{CC}$ = 3.0V to 3.6V | 2 | | |
| | | $V_{CC}$ = 4.5V to 5.5V | 0.7x Vcc | | |
| $V_{IL}$ | Low-Level input voltage | $V_{CC}$ = 1.65V to 1.95V | | 0.35x Vcc | V |
| | | $V_{CC}$ = 2.3V to 2.7V | | 0.7 | |
| | | $V_{CC}$ = 3.0V to 3.6V | | 0.8 | |
| | | $V_{CC}$ = 4.5V to 5.5V | | 0.3x Vcc | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65V | | -4 | mA |
| | | $V_{CC}$ = 2.3V | | -8 | |
| | | $V_{CC}$ = 3.0V | | -16 | |
| | | | | -24 | |
| | | $V_{CC}$ = 4.5V | | -32 | |

over operating free-air temperature range (unless otherwise noted)

| Specifications | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65V | | 4 | mA |
| | | $V_{CC}$ = 2.3V | | 8 | |
| | | $V_{CC}$ = 3.0V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5V | | 32 | |
| Δt/Δv | Input transition rise or fall rate | $V_{cc}$ = 1.2V to 5.0V | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 125 | °C |

## 5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC(1) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $R_{\theta JA}$ | $R_{\theta JC(top)}$ | $R_{\theta JB}$ | $\Psi_{JT}$ | $\Psi_{JB}$ | $R_{\theta JC(bot)}$ | |
| DTX (XSON, 5) | 5 | 313.6 | 137.4 | 253.5 | 69.2 | 259 | 166.7 | °C/W |
| DBV (SOT-23, 5) | 5 | 357.1 | 263.7 | 264.4 | 195.6 | 262.2 | N/A | °C/W |
| DCK (SOT-SC70, 5) | 5 | 371.0 | 297.5 | 258.6 | 195.6 | 256.2 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$= –100µA | 1.1V to 5.5V | $V_{CC}$ - 0.1 | | | V |
| | $I_{OH}$= –4mA | 1.65V | 1.2 | | | |
| | $I_{OH}$= –8mA | 2.3V | 1.9 | | | |
| | $I_{OH}$= –12mA | 2.7V | 2.2 | | | |
| | $I_{OH}$= –16mA | 3V | 2.4 | | | |
| | $I_{OH}$= –24mA | 3V | 2.3 | | | |
| | $I_{OH}$= –32mA | 4.5V | 3.8 | | | |
| $V_{OL}$ | $I_{OL}$= 100µA | 1.1V to 5.5V | | | 0.15 | V |
| | $I_{OL}$= 4mA | 1.65V | | | 0.45 | |
| | $I_{OL}$= 8mA | 2.3V | | | 0.3 | |
| | $I_{OL}$= 12mA | 2.7V | | | 0.4 | |
| | $I_{OL}$= 16mA | 3V | | | 0.4 | |
| | $I_{OL}$= 24mA | 3V | | | 0.55 | |
| | $I_{OL}$= 32mA | 4.5V | | | 0.55 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | $V_{CC}$ = 0V to 5.5V | | | ±5 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = $V_{CC}$ | $V_{CC}$ = 0V | | | ±10 | µA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | 5.5V | | | ±15 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | $V_{CC}$ = 1.1V to 5.5V | | | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | 3.0V to 5.5V | | | 500 | µA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 3.3V | | 3.5 | | pF |
| $C_O$ | $V_O$ = $V_{CC}$ or GND | 3.3V | | | | pF |

## 5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See #i#Parameter Measurement Information

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $V_{CC}$ | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $t_{pd}$ | A or B | Y | $C_L$ = 15pF | 1.2V ± 0.1V | | 23 | 33 | ns |
| | | | | 1.5V ± 0.12V | | 7 | 8.5 | |
| | | | | 1.8V ± 0.15V | | 5 | 5.8 | |
| | | | | 2.5V ± 0.2V | | 3 | 3.8 | |
| | | | | 3.3V ± 0.3V | | 2.5 | 2.9 | |
| | | | | 5.0V ± 0.5V | | 2 | 2.4 | |
| | | | $C_L$ = 30pF | 1.8V ± 0.15V | 2.8 | 6 | 6.9 | ns |
| | | | | 2.5V ± 0.2V | 1.6 | 3.8 | 4.3 | |
| | | | $C_L$ = 50pF | 3.3V ± 0.3V | 1.4 | 3.2 | 3.9 | |
| | | | | 5.0V ± 0.5V | 1 | 2.5 | 3.2 | |
| $C_{pd}$ | | | f = 10MHz | 1.8V | | 3 | | pF |
| | | | | 2.5V | | 3 | | |
| | | | | 3.3V | | 4 | | |
| | | | | 5V | | 6 | | |

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O$ = 50Ω, $t_t$ ≤ 2.5ns.

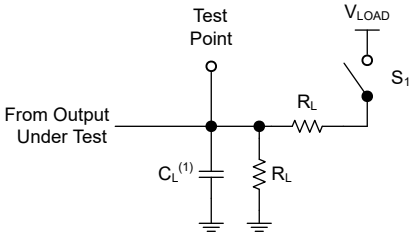
The outputs are measured individually with one input transition per measurement.

**Table 6-1. Open-Drain Outputs**

| TEST | S1 |
|---|---|
| $t_{PLZ}$, $t_{PZL}$ | CLOSED |

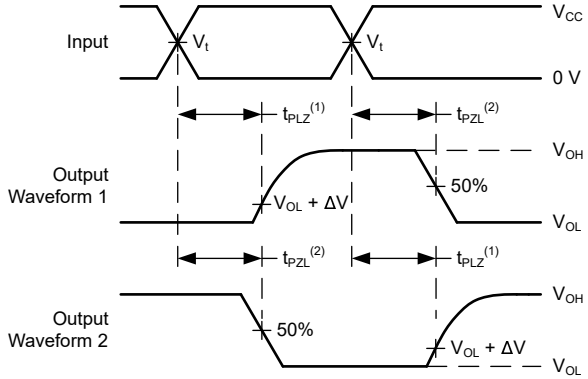
**Table 6-2. 3-State or Open-Drain Outputs**

| $V_{CC}$ | $V_t$ | $R_L$ | $C_L$ | ΔV | $V_{LOAD}$ |
|---|---|---|---|---|---|
| 1.2V ± 0.1V | $V_{CC}/2$ | 2kΩ | 15pF | 0.1V | $2×V_{CC}$ |
| 1.5V ± 0.12V | $V_{CC}/2$ | 2kΩ | 15pF | 0.1V | $2×V_{CC}$ |
| 1.8V ± 0.15V | $V_{CC}/2$ | 1kΩ | 15pF/30pF | 0.15V | $2×V_{CC}$ |
| 2.5V ± 0.2V | $V_{CC}/2$ | 500Ω | 15pF/30pF | 0.15V | $2×V_{CC}$ |
| 3.3V ± 0.3V | 1.5V | 500Ω | 15pF/50pF | 0.3V | 6V |
| 5.0V ± 0.5V | 1.5V | 500Ω | 15pF/50pF | 0.3V | 6V |




(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Open-Drain Outputs**




(1) $t_{PLZ}$ is the same as $t_{dis}$.
(2) $t_{PZL}$ is the same as $t_{en}$.

**Figure 6-2. Voltage Waveforms Propagation Delays**

# 7 Detailed Description

## 7.1 Overview

The SN74LVC1G09B-Q1 device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A + B}$ in positive logic.

## 7.2 Functional Block Diagram

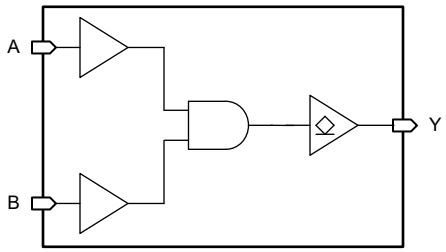



**Figure 7-1. Logic Diagram (Positive Logic)**

## 7.3 Feature Description

### *7.3.1 Open-Drain CMOS Outputs*

This device includes open-drain CMOS outputs. Open-drain outputs can only drive the output low. When in the high logical state, open-drain outputs are in a high-impedance state. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the device output power to avoid damage due to overcurrent. Follow the electrical and thermal limits defined in the *Absolute Maximum Ratings* at all times.

When placed into the high-impedance state, the output neither sources nor sinks current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, use a 10kΩ resistor to meet these requirements.

Leave unused open-drain CMOS outputs disconnected.

### *7.3.2 Partial Power Down ($I_{off}$)*

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the $I_{off}$ specification in the *Electrical Characteristics* table.

### *7.3.3 Standard CMOS Inputs*

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can

be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

### *7.3.4 Clamp Diode Structure*

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

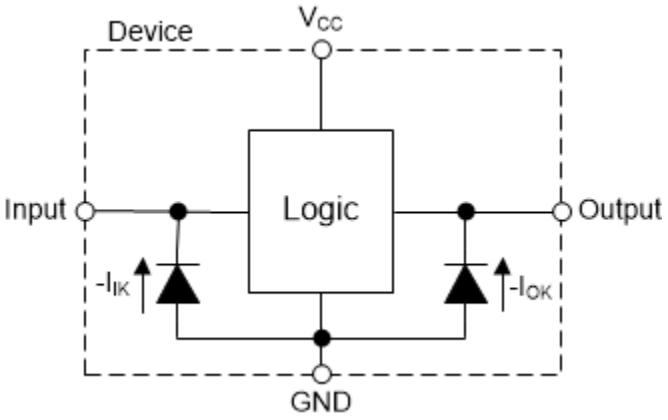



**Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output**

## 7.4 Device Functional Modes

Table 7-1 lists the functional modes for SN74LVC1G09B-Q1.

**Table 7-1. Function Table**

| INPUTS(1) | | OUTPUT (2) Y |
|---|---|---|
| A | B | |
| H | H | Z |
| L | X | L |
| X | L | L |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

In this application, two 2-input AND gates, SN74LVC1G09B-Q1, combine to produce a 4-input AND gate function as shown in the *Section 8.2* diagram.

The SN74LVC1G09B-Q1 directly controls the $\overline{\text{RESET}}$ pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled; disable in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

## 8.2 Typical Application

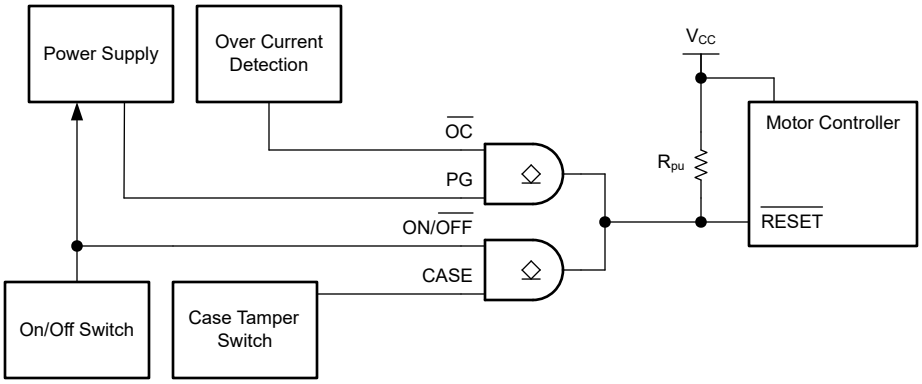



**Figure 8-1. Typical Application Block Diagram**

### 8.2.1 Design Requirements

The SN74LVC1G09B-Q1 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

The SN74LVC1G09B-Q1 allows switching control of analog and digital signals with a digital control signal. All input signals should remain as close to either 0V or $V_{CC}$ as possible for optimal operation.

#### 8.2.1.1 Power Considerations

Ensure that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics of the device, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G09B-Q1 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC1G09B-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC1G09B-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G09B-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC1G09B-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### *8.2.2 Detailed Design Procedure*

1. Recommended input conditions:
   - For rise time and fall time specifications, see Δt/Δv in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in the *Recommended Operating Conditions* table.
   - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5V at any valid $V_{CC}$.
2. Recommended output conditions:
   - Load currents not exceeding ±50mA.
3. Frequency selection criterion:
   - The effects of frequency upon the device's power consumption should be studied in the *CMOS Power Consumption and CPD Calculation* application note.
   - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the *Layout* section.

### *8.2.3 Application Curves*

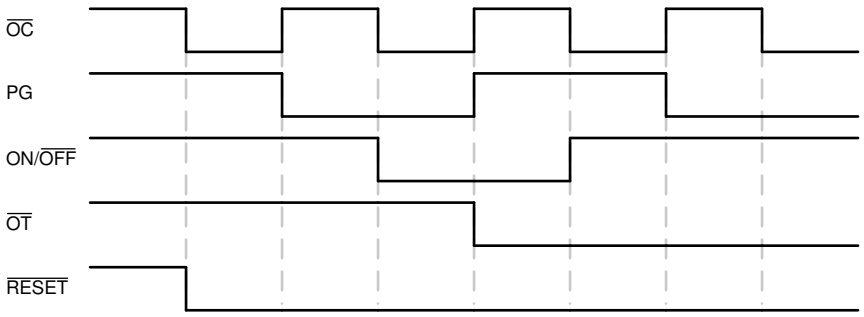



**Figure 8-2. Application Timing Diagram**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each $V_{CC}$ terminal has a good bypass capacitor to prevent power disturbance. For the SN74LVC1G09B-Q1, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

## 8.4 Layout

### *8.4.1 Layout Guidelines*

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width

- Lengths less than 12cm to minimize transmission line effects
- Avoid 90° corners for signal traces
- Use an unbroken ground plane below signal traces
- Flood fill areas around signal traces with ground
- Parallel traces must be separated by at least 3x dielectric thickness
- For traces longer than 12cm
  - Use impedance controlled traces
  - Source-terminate using a series damping resistor near the output
  - Avoid branches; buffer each signal that must branch separately

### *8.4.2 Layout Example*

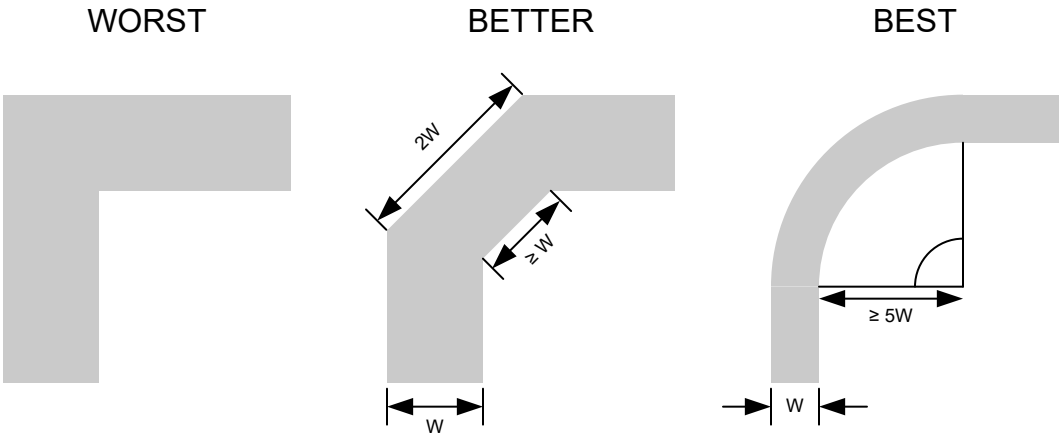



**Figure 8-3. Example Trace Corners for Improved Signal Integrity**

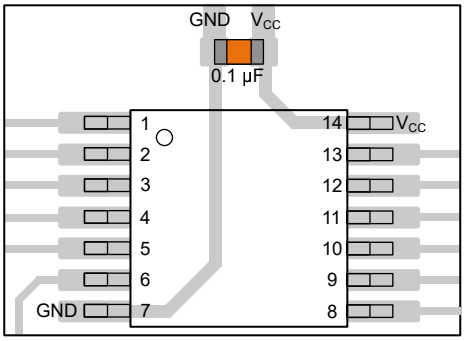



**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

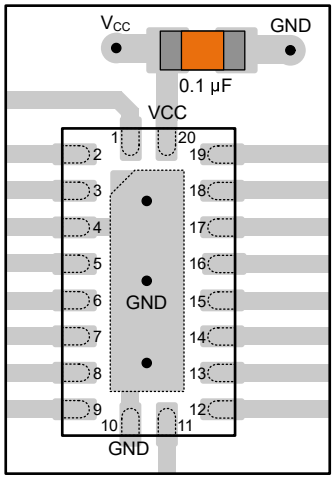



**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**

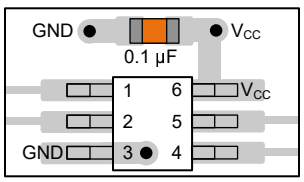



**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

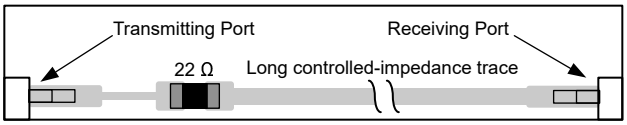



**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**

# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (October 2025) to Revision A (February 2026) | Page |
|---|---|
| • Changed the document status from *Advance Information* to *Production Data* | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PSN74LVC1G09DBVRQ1 | Active | Preproduction | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | - | Call TI | Call TI | - | |
| PSN74LVC1G09DCKRQ1 | Active | Preproduction | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | - | Call TI | Call TI | - | |
| PSN74LVC1G09DTXRQ1 | Active | Preproduction | X2SON (DTX) \| 5 | 3000 \| LARGE T&R | - | Call TI | Call TI | - | |
| SN74LVC1G09BDBVRQ1 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | - | 3S8H |
| SN74LVC1G09BDTXRQ1 | Active | Production | X2SON (DTX) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | - | X |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**OTHER QUALIFIED VERSIONS OF SN74LVC1G09B-Q1 :**

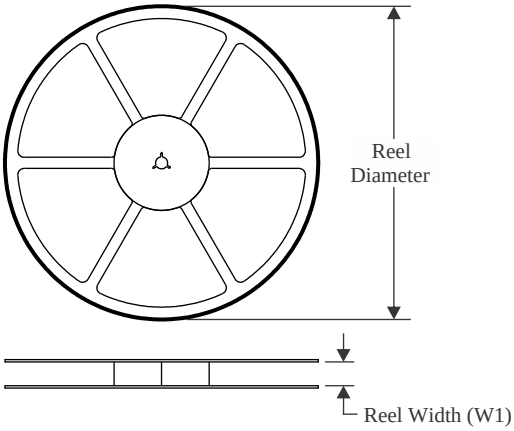
- Catalog : SN74LVC1G09B

NOTE: Qualified Version Definitions:

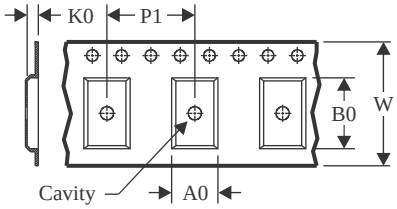
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

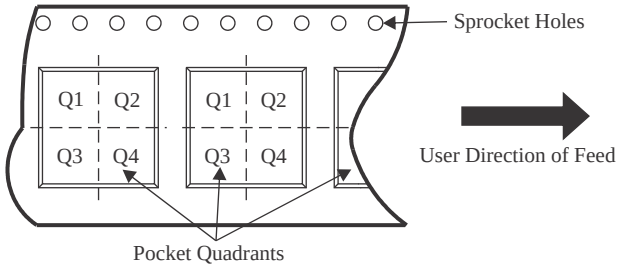



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

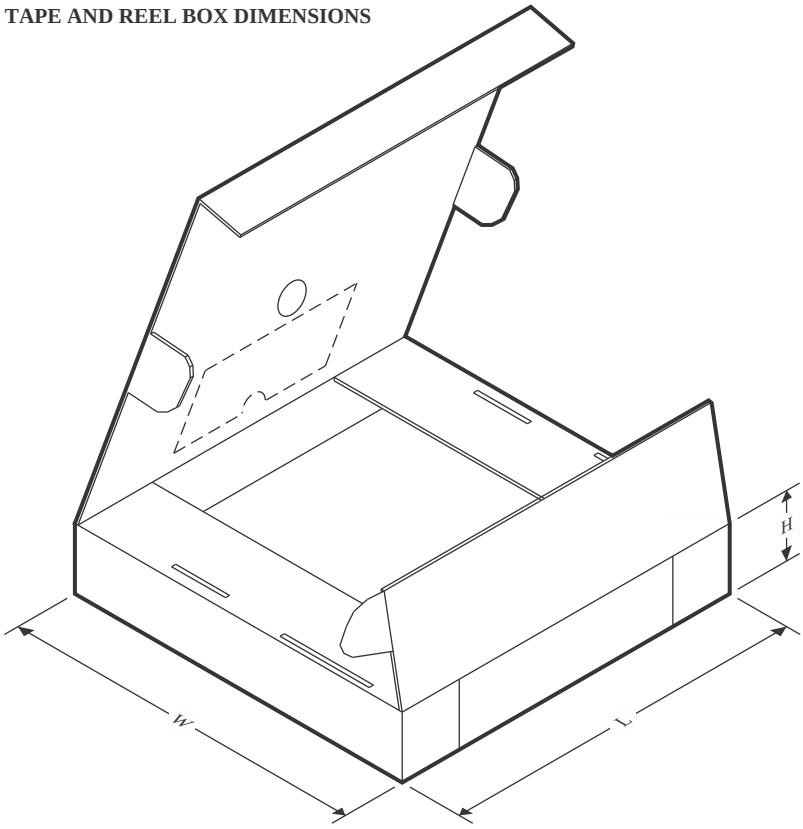
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1G09BDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

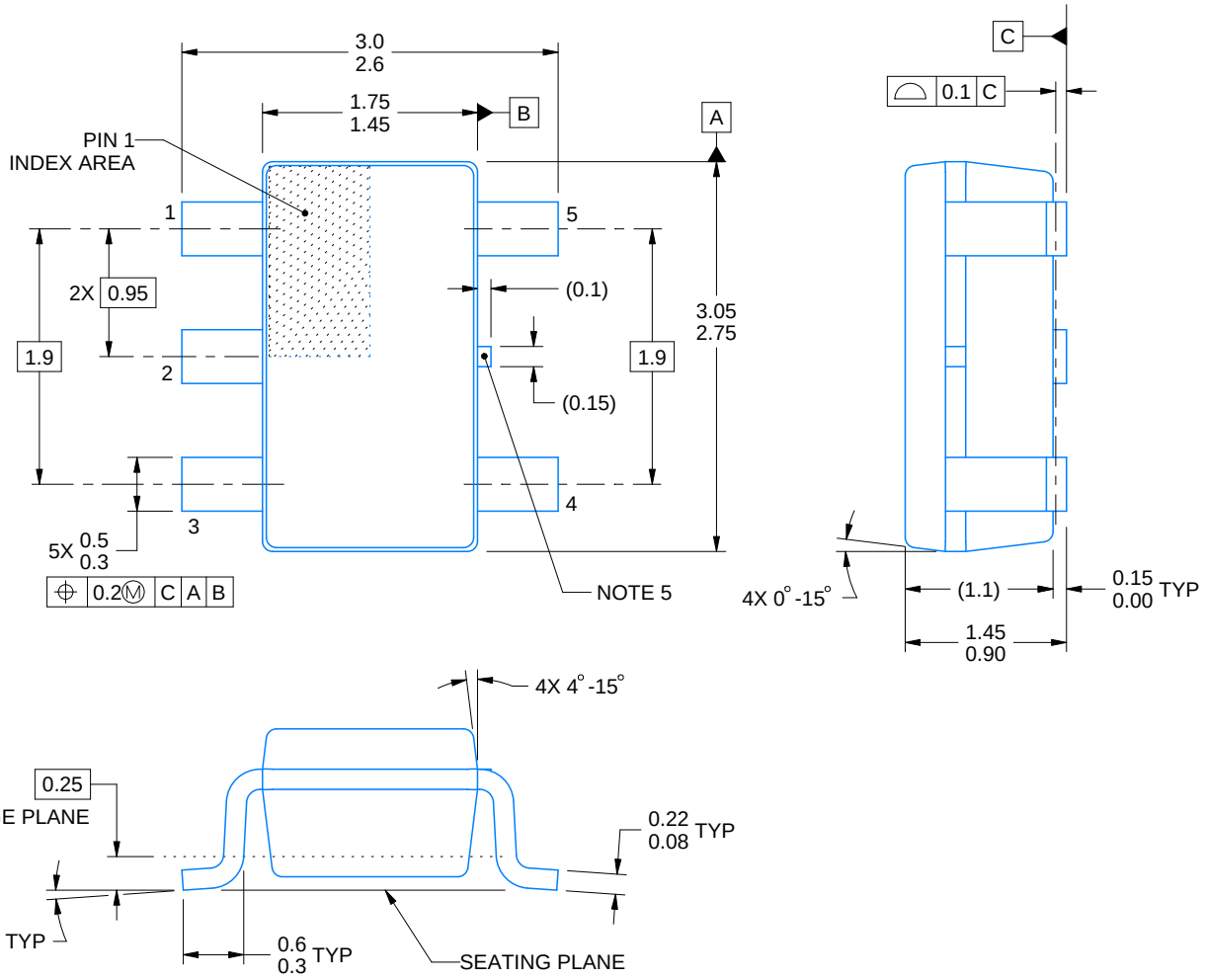
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1G09BDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

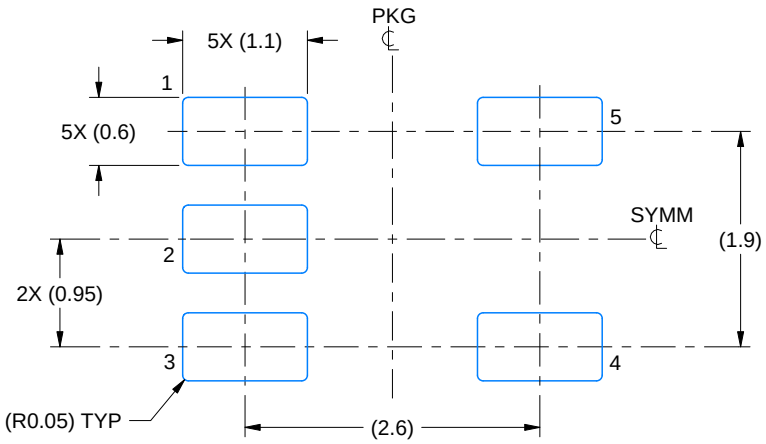
SMALL OUTLINE TRANSISTOR



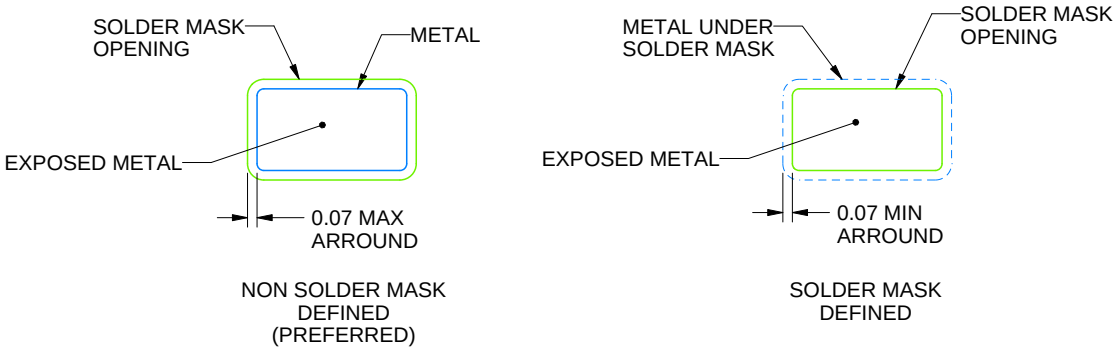

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

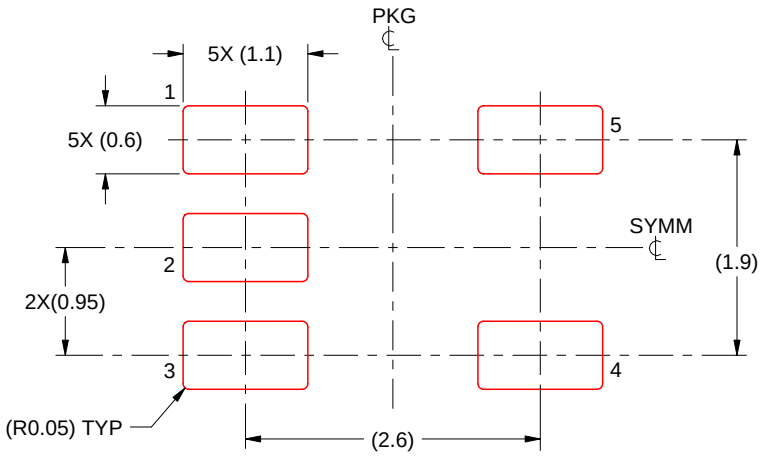



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

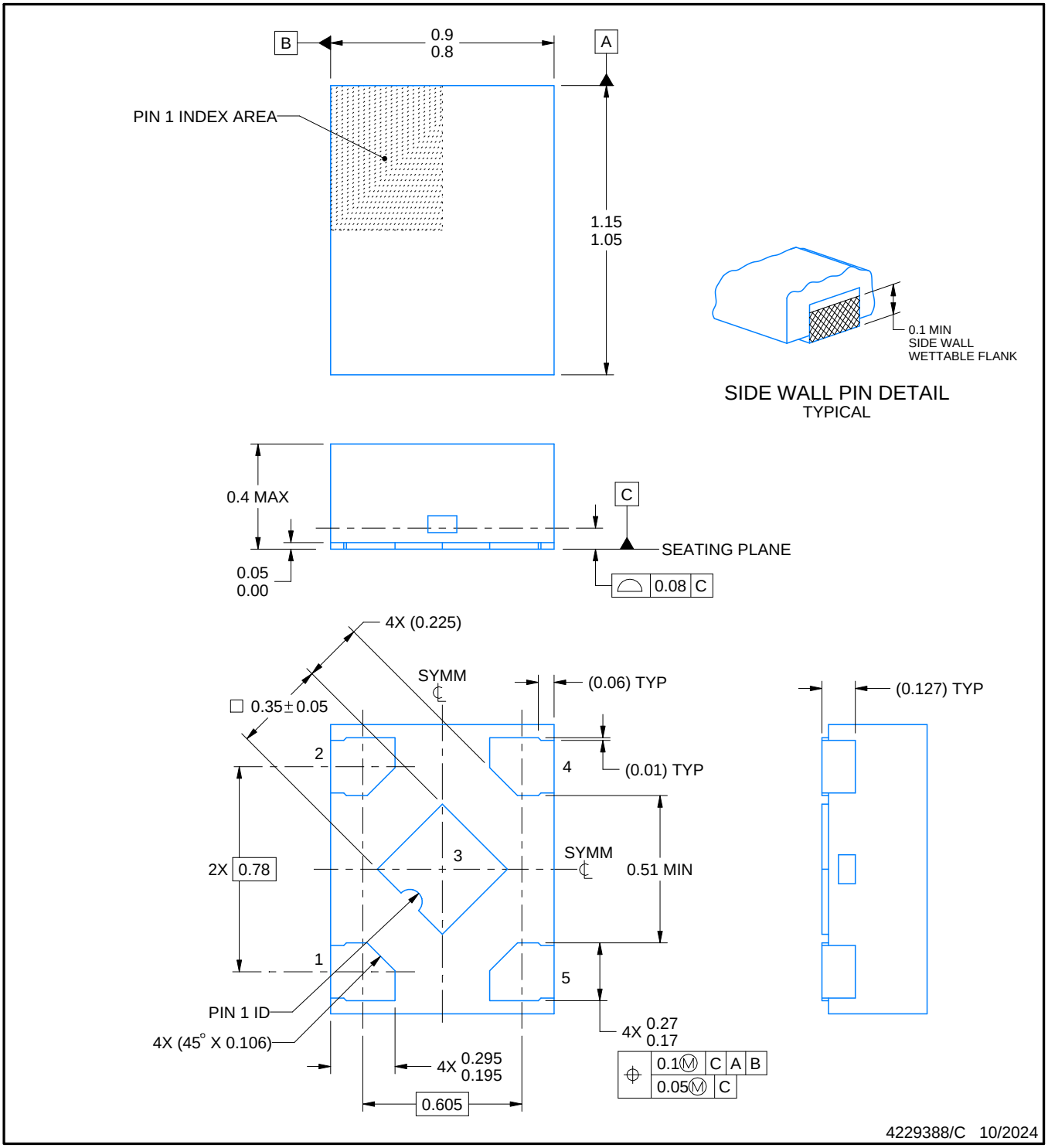
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DTX0005A

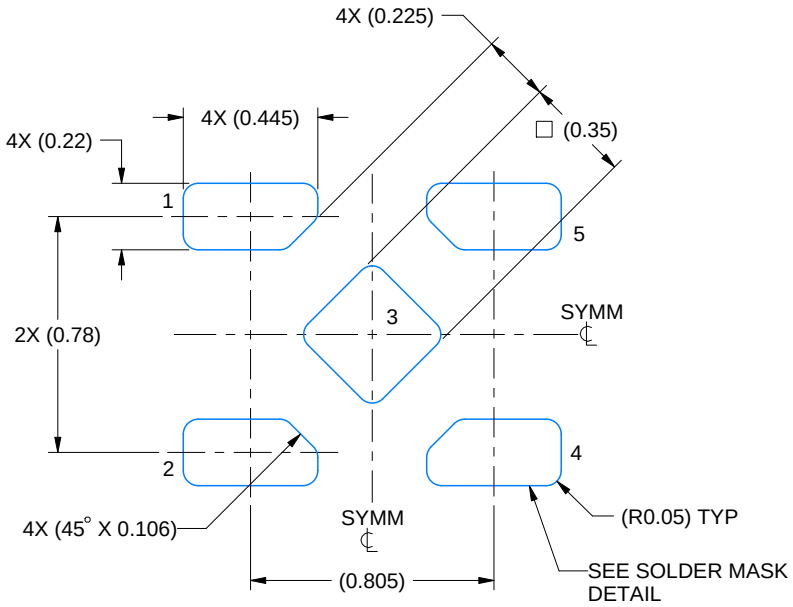
## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

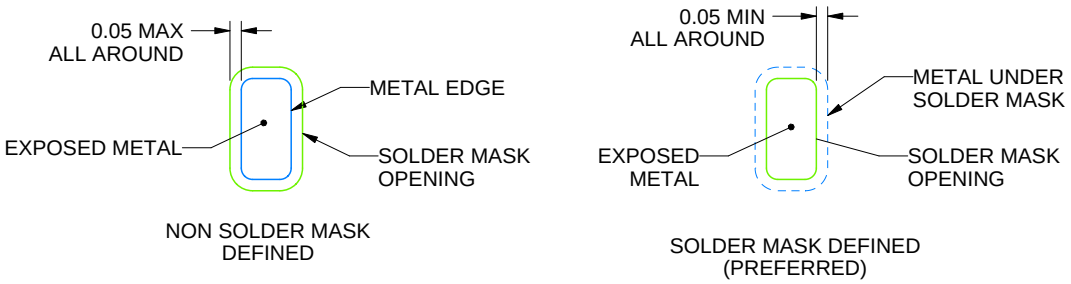



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

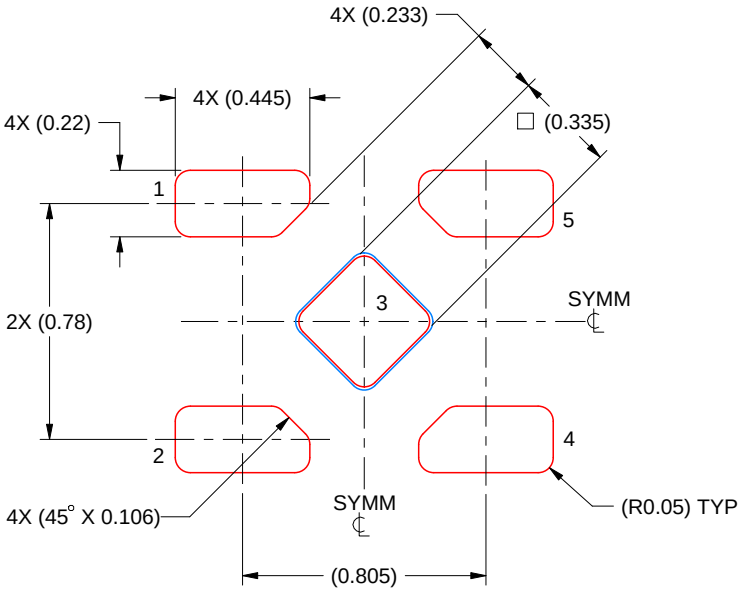



SOLDER MASK DETAILS

4229388/C 10/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

PRINTED SOLDER PASTE COVERAGE BY AREA UNDER PACKAGE
PAD 5: 92%

4229388/C 10/2024

NOTES: (continued)

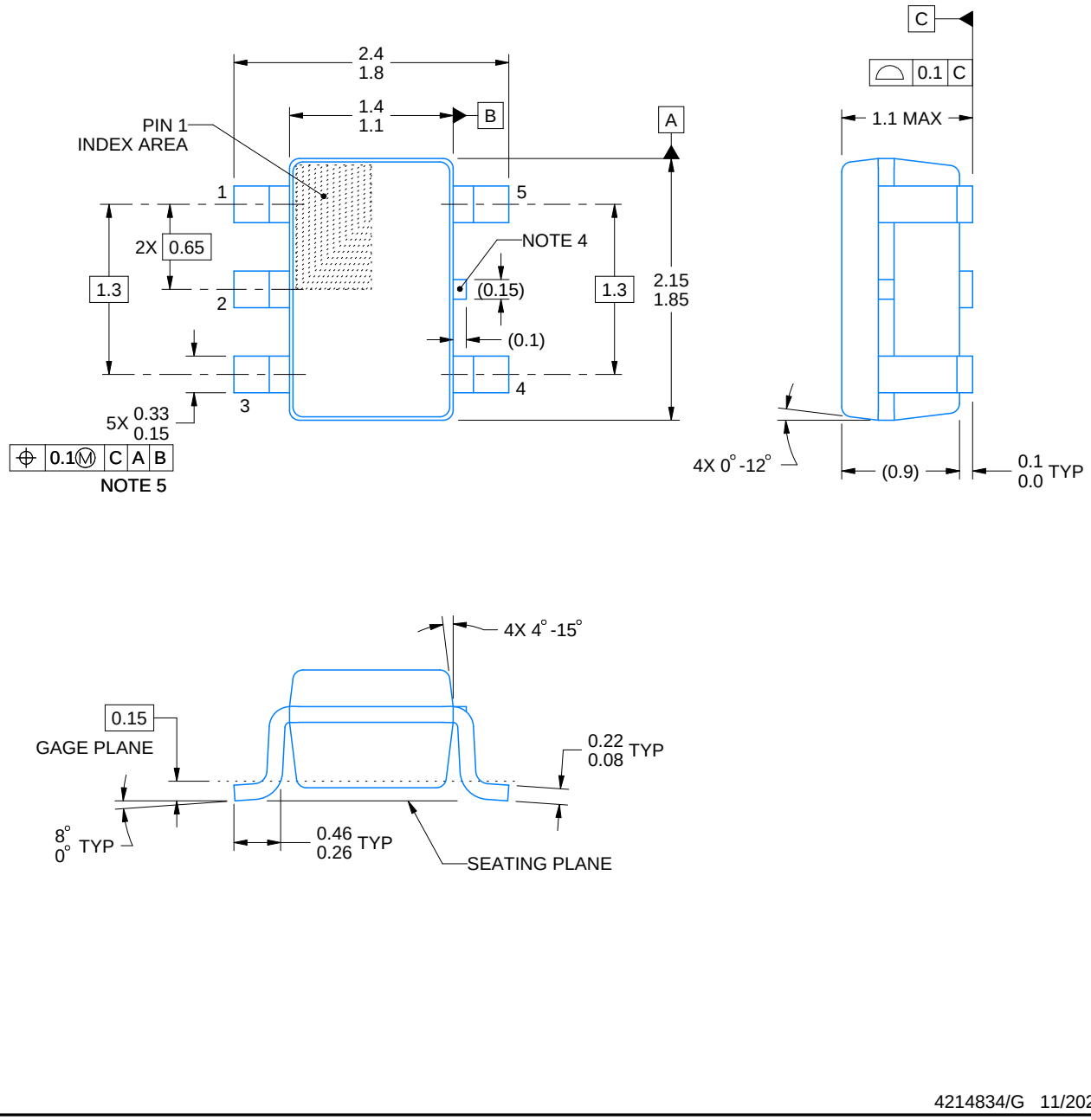
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

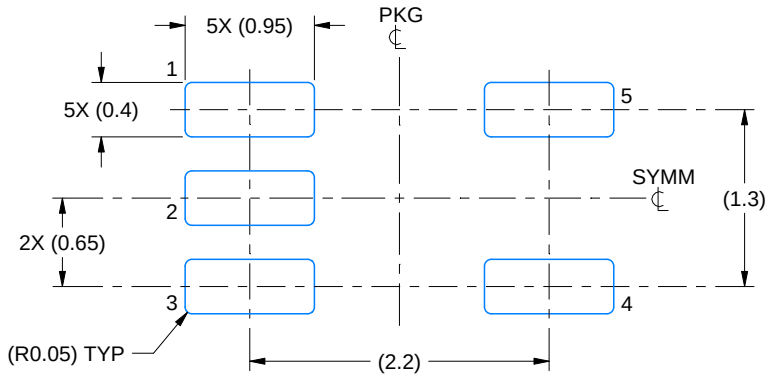
SMALL OUTLINE TRANSISTOR



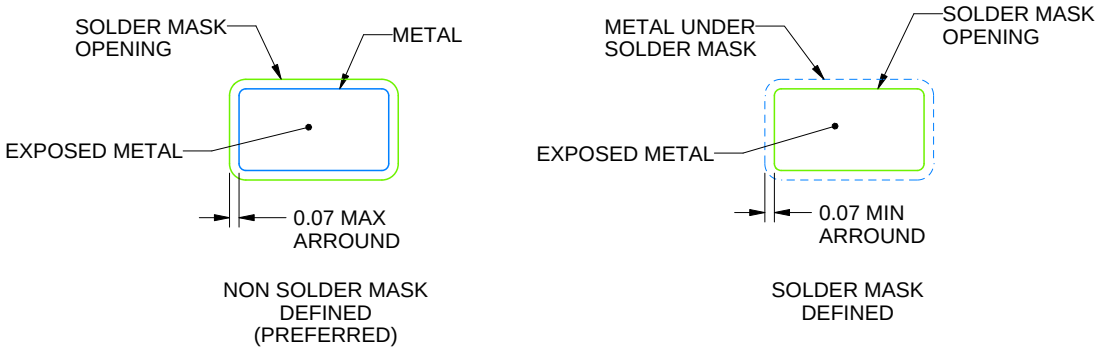

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

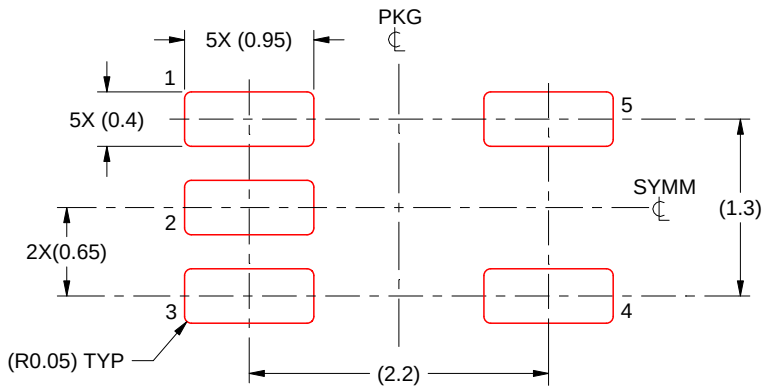



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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