SN74LVC1G126-Q1 Single Bus Buffer Gate With 3-State Output

1 Features

- Qualified for automotive applications
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Provides down translation to V_{CC}
- Low power consumption, 10µA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports live insertion, partial-power-down mode, and back drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- Cable modem termination systems
- High-speed data acquisition and generation
- Motor controls: high-voltage
- Power line communication modems
- SSDs: internal or external
- Video broadcasting and infrastructure: scalable platforms
- Video broadcasting: IP-based multi-format transcoders
- Video communication systems

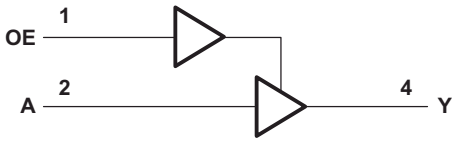
3 Description

The SN74LVC1G126-Q1 device is a single line driver with 3-state output. The output is disabled when the output-enable input is low.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
1P1G126QDBVRQ1	SOT-23 (5)	2.90mm × 1.60mm
1P1G126QDRYRQ1	SON (6)	1.00mm × 1.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

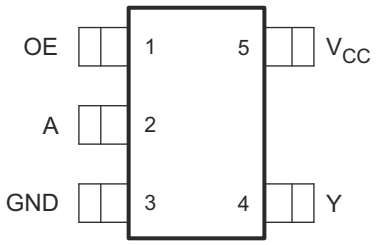
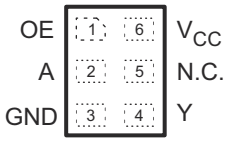


Figure 4-1. DBV Package 5-Pin SOT-23 Top View



N.C. is no connection

See all mechanical drawings at the end of this data sheet for package dimensions.

Figure 4-2. DRY Package 6-Pin SON Transparent Top View

Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	DBV (SOT-23)	DRY (SON)		
A	2	2	I	A Input
GND	3	3	—	Ground Pin
NC	—	5	—	No connection
OE	1	1	I	OE Enable/Input
V_{CC}	5	6	—	Power Pin
Y	4	4	O	Y Output

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

PARAMETER		DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 1.95V	0.65 × V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3V to 3.6V	2		
		V_{CC} = 4.5V to 5.5V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65V to 1.95V		0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3V to 3.6V		0.8	
		V_{CC} = 4.5V to 5.5V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		–4	mA
		V_{CC} = 2.3V		–8	
		V_{CC} = 3V		–16	
				–24	
		V_{CC} = 4.5V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		24	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		5	
T_A	Operating free-air temperature		–40	125	°C

(1) Hold all unused inputs of the device at V_{CC} or GND for proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G126-Q1		UNIT
		DBV	DRY	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	357.1	279.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	263.7	182.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	264.4	154.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	195.6	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	262.2	153.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100µA		1.65V to 5.5V	V_{CC} – 0.1			V
		I_{OH} = –4mA		1.65V	1.2			
		I_{OH} = –8mA		2.3V	1.9			
		I_{OH} = –16mA		3V	2.4			
		I_{OH} = –24mA		3V	2.3			
				4.5V	3.8			
V_{OL}		I_{OL} = 100µA		1.65V to 5.5V			0.1	V
		I_{OL} = 4mA		1.65V			0.45	
		I_{OL} = 8mA		2.3V			0.3	
		I_{OL} = 16mA		3V			0.4	
		I_{OL} = 24mA		3V			0.55	
				4.5V			0.55	
I_I	A or OE inputs	V_I = 5.5V or GND		0 to 5.5V			±5	µA
I_{off}		V_I or V_O = 5.5V		0			±10	µA
I_{OZ}		V_O = 0 to 5.5V		3.6V			10	µA
I_{CC}		V_I = 5.5V or GND	I_O = 0	1.65V to 5.5V			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6V, Other inputs at V_{CC} or GND		3V to 5.5V			500	µA
C_i		V_I = V_{CC} or GND		3.3V		4		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

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5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1	5.8	1	4.5	ns
t_{en}	OE	Y	1.2	5.8	1	5	ns
t_{dis}	OE	Y	1	6	1	4.2	ns

5.7 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10MHz	19	21	pF
		Outputs disabled		3	4	

5.8 Typical Characteristics

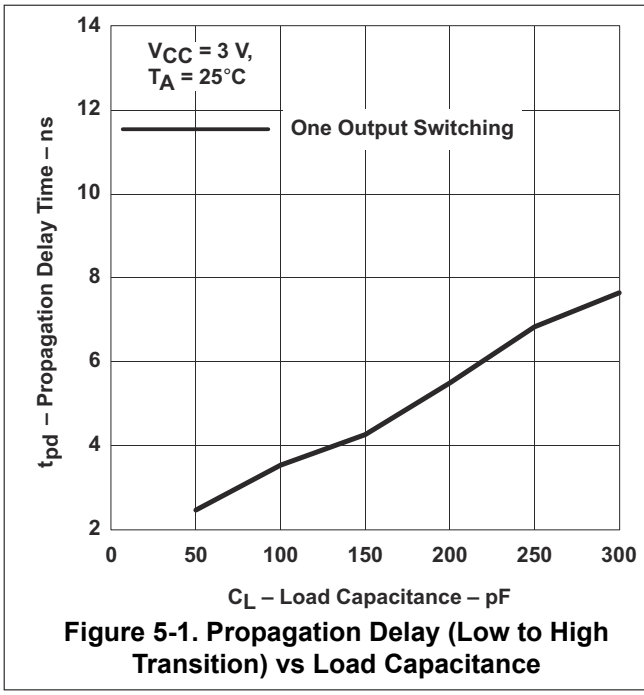

Figure 5-1. Propagation Delay (Low to High Transition) vs Load Capacitance

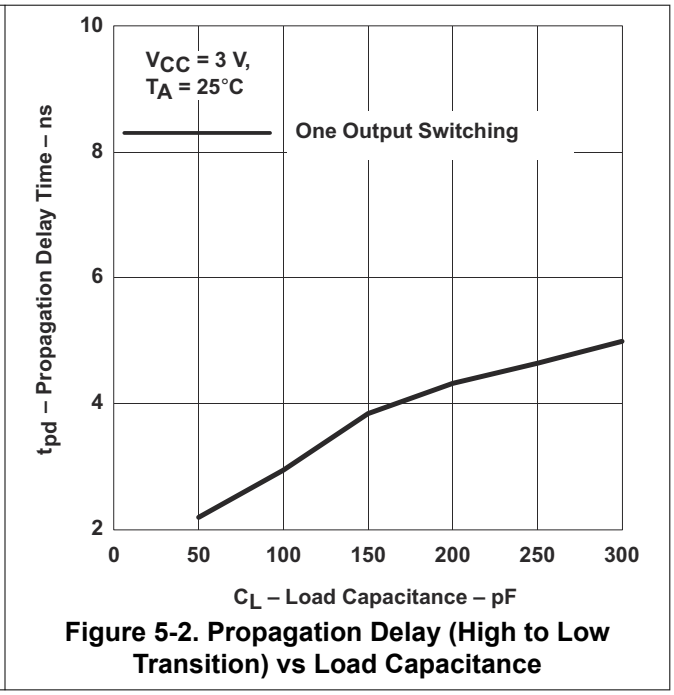

Figure 5-2. Propagation Delay (High to Low Transition) vs Load Capacitance

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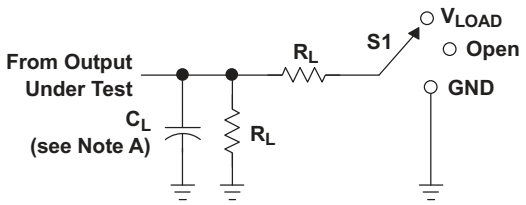
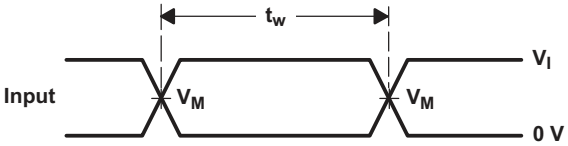
6 Parameter Measurement Information



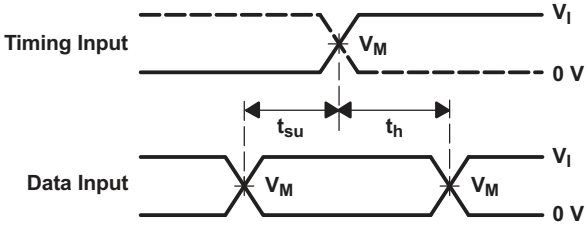
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

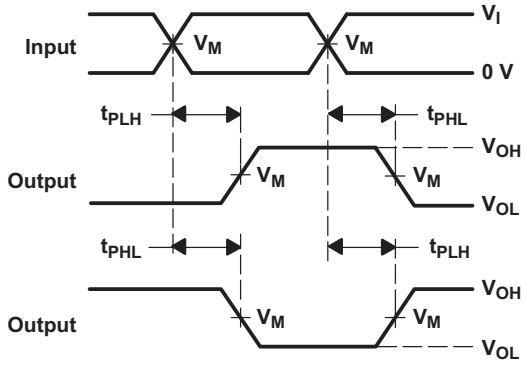
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



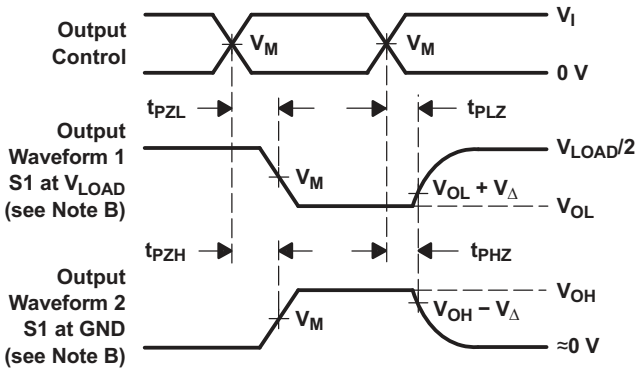
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

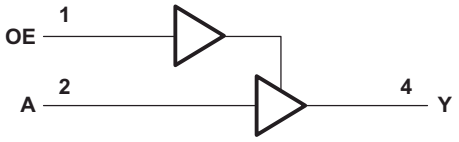
7.1 Overview

The SN74LVC1G126-Q1 device contains a dual buffer gate with output enable control and performs the Boolean function Y = A.

This device is specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the powered-down device.

To establish the high-impedance state during power up or power down, tie OE to GND through a pull-down resistor; the current-sourcing capability of the driver determines the minimum value of the resistor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

7.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a

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valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.3.4 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

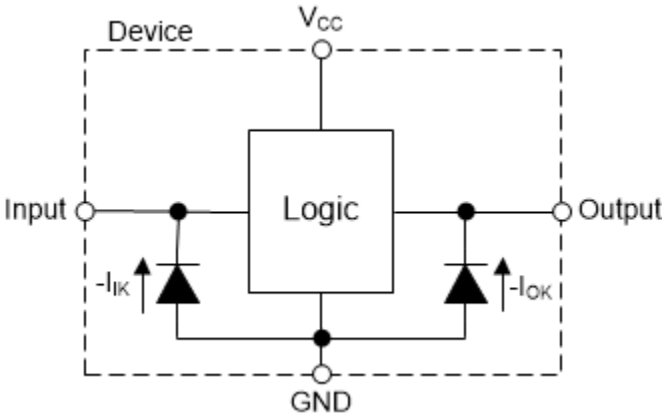

Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

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8 Application and Implementation

8.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.2 Application Information

The SN74LVC1G126-Q1 device is a high-drive CMOS device that can be used as an output enabled buffer with a high output drive, such as an LED application. The device can produce 24mA of drive current at 3.3V, which is designed for driving multiple outputs and good for high speed applications up to 100MHz. The inputs are 5.5V tolerant allowing the SN74LVC1G126-Q1 device to translate down to V_{CC}.

8.3 Typical Application

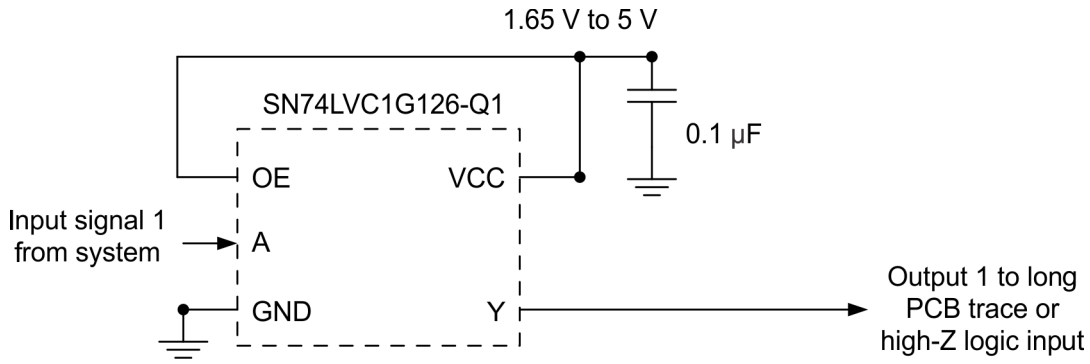

Figure 8-1. Application Schematic

8.3.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention to prevent currents that exceed the maximum limits. Combine outputs to produce higher drive, but remember that the high drive also creates faster edges into light loads. Consider routing and load conditions to prevent ringing.

8.3.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommend Output Conditions:
   - Load currents must not exceed 50mA per output and 100mA total for the part.

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8.3.3 Application Curves

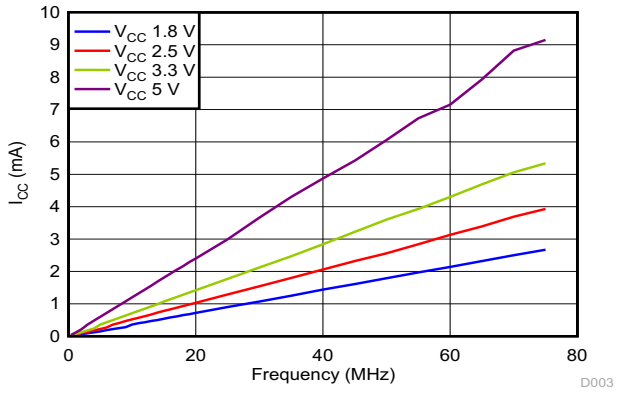

Figure 8-2. I_{CC} vs Frequency

8.4 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} terminal needs a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF capacitor is recommended. If there are multiple V_{CC} terminals, then 0.01µF or 0.022µF capacitors are recommended for each power terminal. Parallel multiple bypass capacitors to reject different frequencies of noise. For best results, install the bypass capacitor as close to the power terminal as possible.

8.5 Layout

8.5.1 Layout Guidelines

When using multiple bit logic devices, verify that the inputs are not floating. In many cases, functions or parts of functions of digital logic devices are unused. Some examples show one unused input on a triple-input AND gate or one unused gate on a 4-buffer gate. Do not leave input pins unconnected because the undefined voltages at the outside connections result in undefined operational states.

To read the rules that must be observed under all circumstances, see Recommended Operating Conditions. Connect all unused inputs of digital logic devices to a high or low bias to prevent them from floating. The function of the device determines what logic level to apply to which unused input. Generally, the logic level is tied to GND or V_{CC}, whichever makes more sense or is more convenient. Floating outputs are acceptable unless the part is a transceiver. If the transceiver has an output enable pin, the pin disables the outputs section of the part when asserted. The transceiver does not disable the input section of the I/Os, so the I/Os also cannot float when disabled.

8.5.2 Layout Example

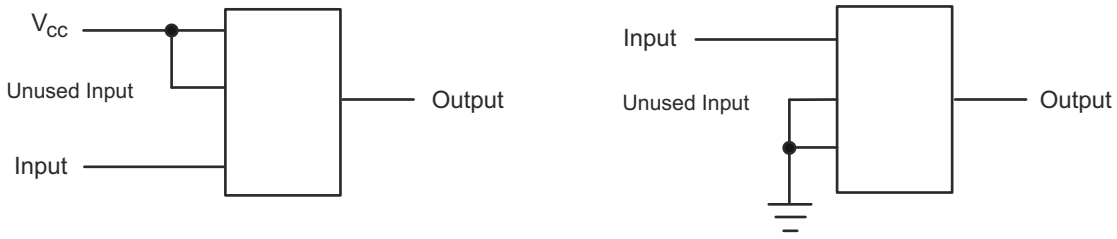

Figure 8-3. Layout Diagram

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9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 10, 2025 to August 14, 2026 (from Revision D (August 2020) to Revision E (August 2026)) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document..... 1
- Changed Junction-to-ambient thermal resistance value for DBV package from: 240.9°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 165.8°C/W to: 263.7°C/W.. 5
- Changed Junction-to-board characterization value for DBV package from: 143.2°C/W to: 264.4°C/W..... 5
- Changed Junction-to-top characterization value for DBV package from: 84.4°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 142.5°C/W to: 262.2°C/W..... 5

Changes from Revision C (April 2019) to Revision D (August 2020) **Page**

- Corrected values in features list..... 1
- Updated the numbering format for tables, figures and cross-references throughout the document..... 1
- Updated *Description* and *Device Information* table..... 1
- Changed ESD ratings table to automotive format..... 4
- Corrected I_{OH} and I_{OL} MAX values in *Recommended Operating Conditions* table 5
- Corrected *Electrical Characteristics* table..... 6
- Removed *Switching Characteristics, CL = 15pF* and *Switching Characteristics, –40°C to 85°C* tables..... 7
- Corrected MAX *Switching Characteristics* values..... 7
- Removed unneeded columns in *Operating Characteristics* table..... 7
- Removed first image and unused rows in table in *Parameter Measurement Information* section..... 8
- Updated *Feature Description* section 9
- Fixed cross references in *Detailed Design Procedure* section..... 11
- Deleted incorrect history tags from revision C: Changed 1.65V to 3.6V VCC to 1.65V to 5V VCC operation and Changed MAX operating temperature to 125°C in Recommended Operating Conditions table..... 0

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
1P1G126QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34Q5, C26O)
1P1G126QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34Q5, C26O)
1P1G126QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34Q5, C26O)
1P1G126QDRYRQ1	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HN
1P1G126QDRYRQ1.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G126-Q1 :

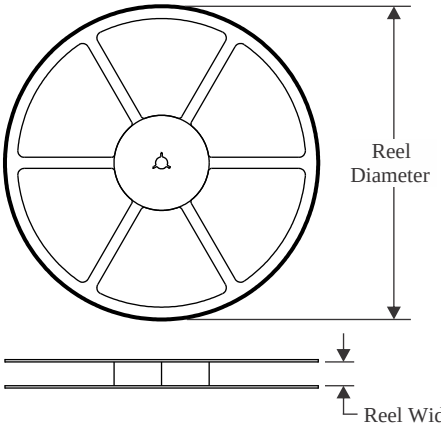
- Catalog : SN74LVC1G126
- Enhanced Product : SN74LVC1G126-EP

NOTE: Qualified Version Definitions:

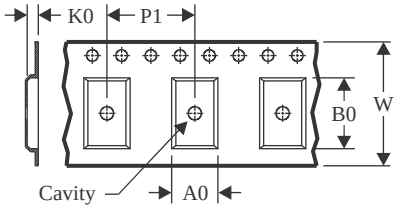
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

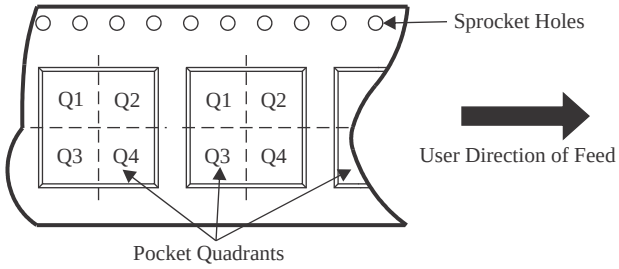


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

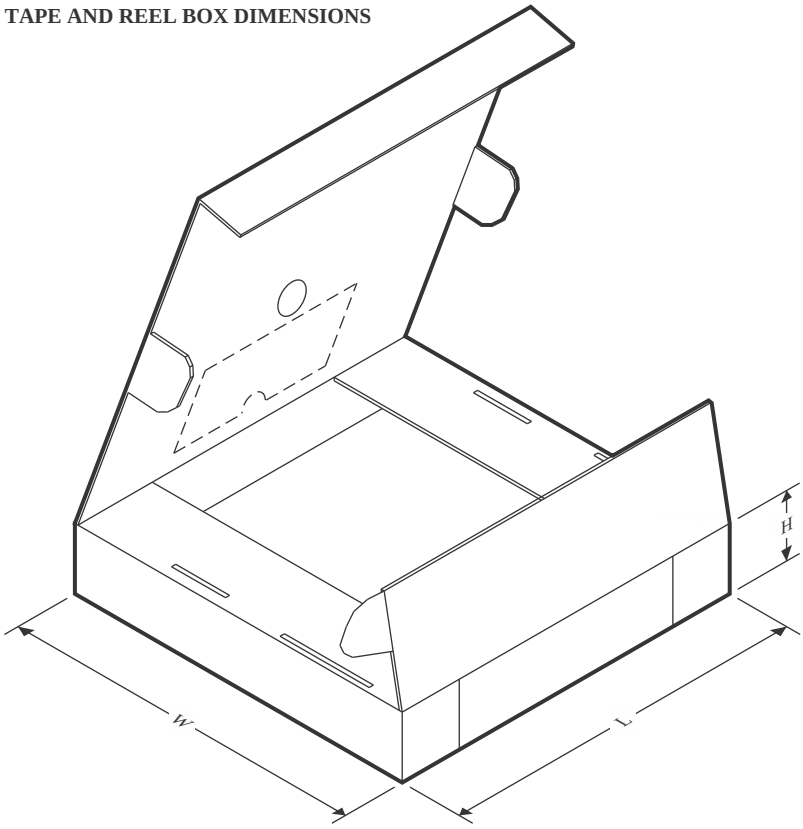
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1P1G126QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
1P1G126QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

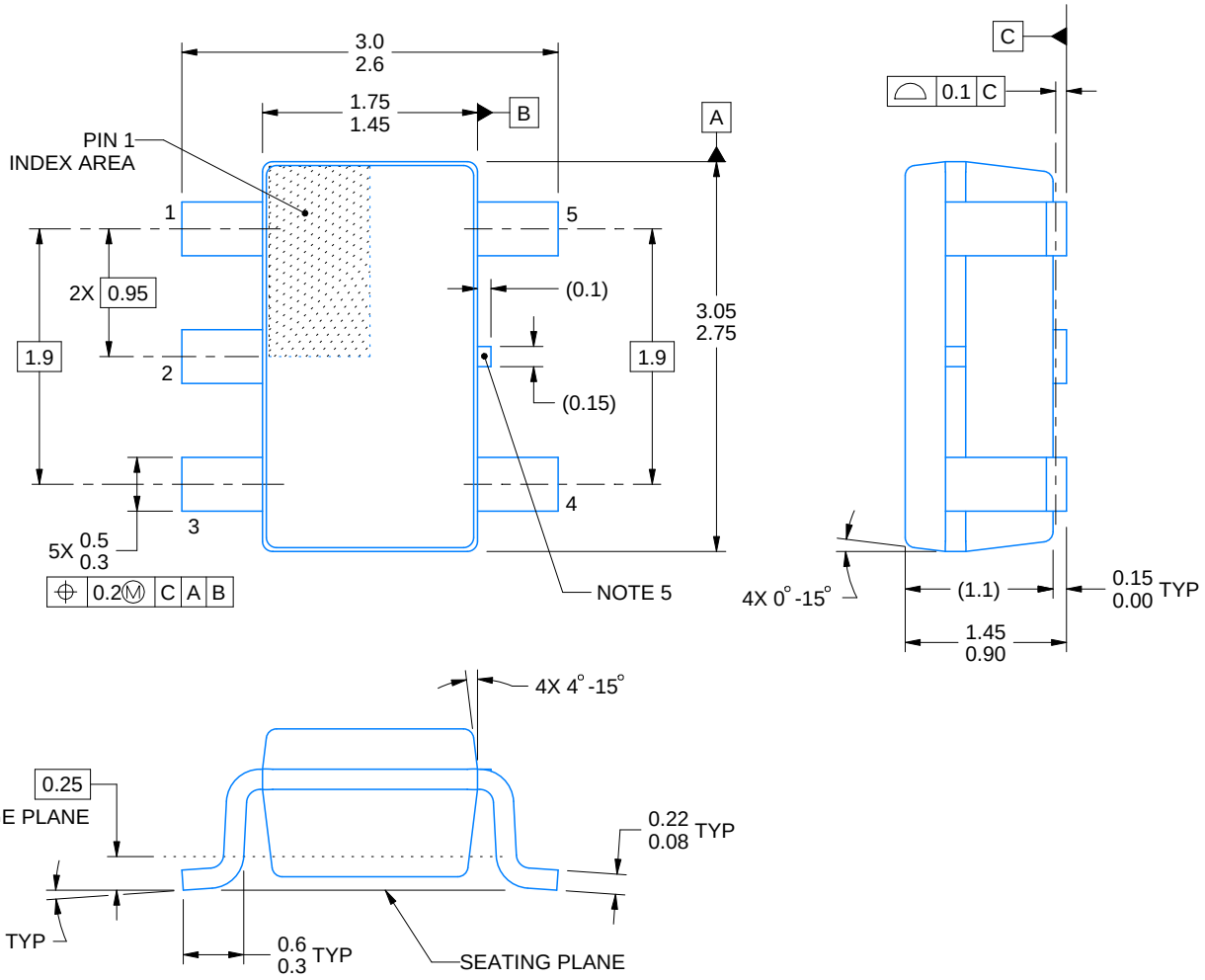
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1P1G126QDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0
1P1G126QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

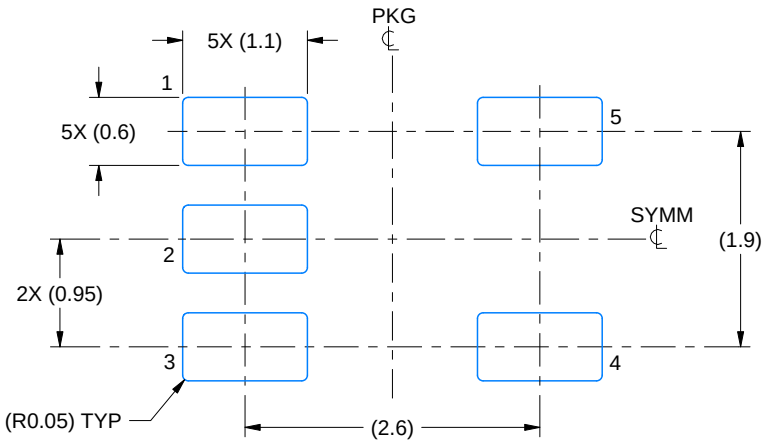
SMALL OUTLINE TRANSISTOR



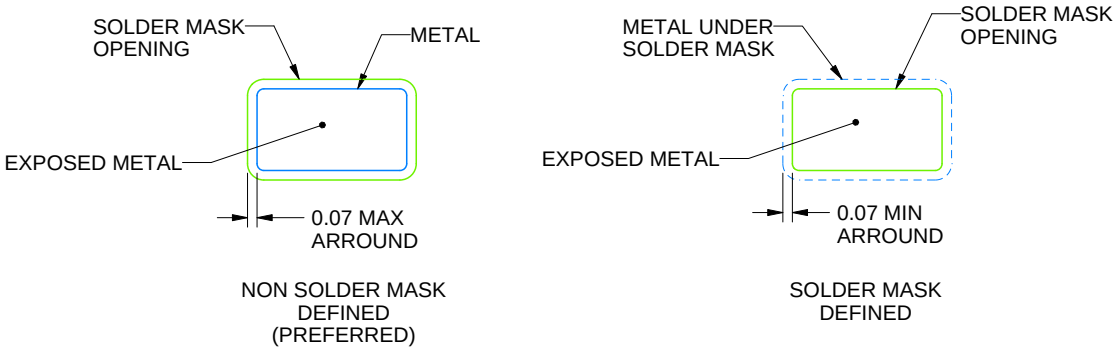
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

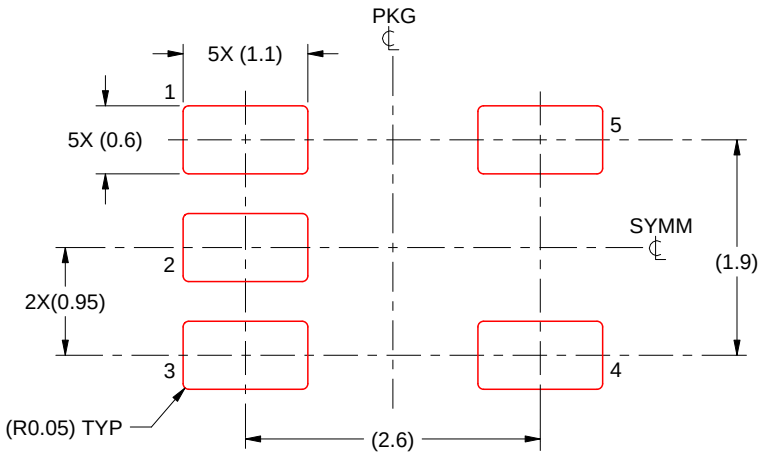


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

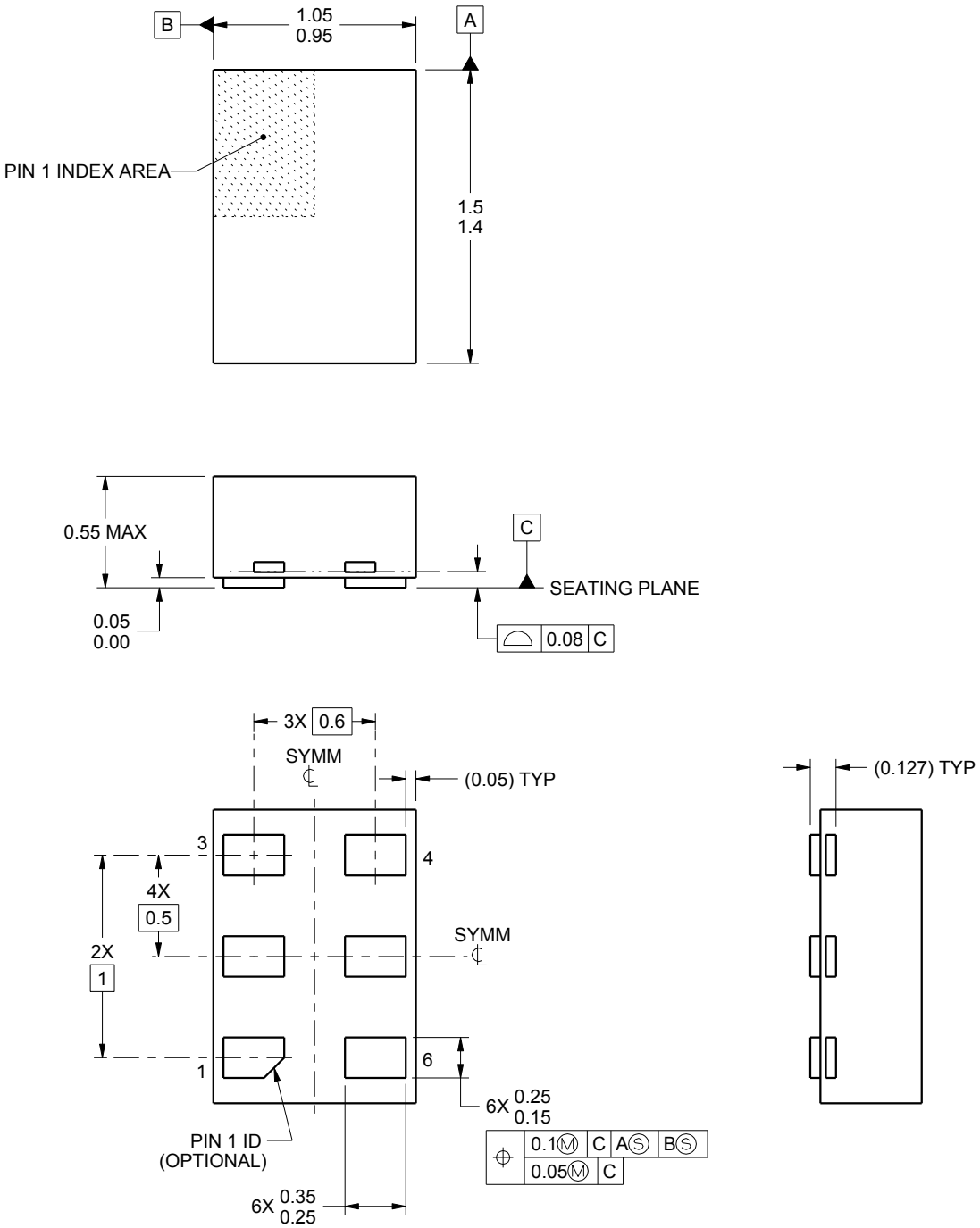
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRY0006B

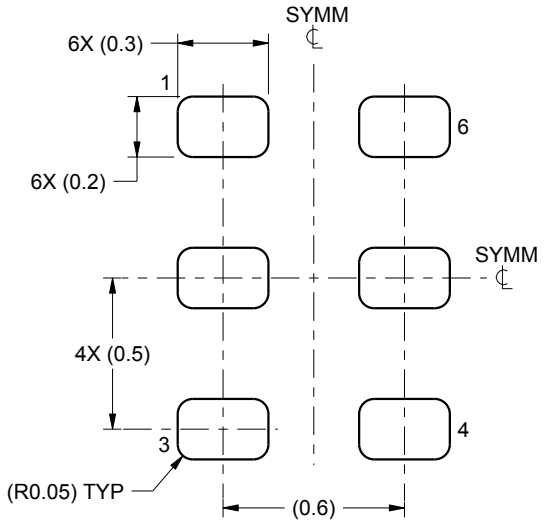
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

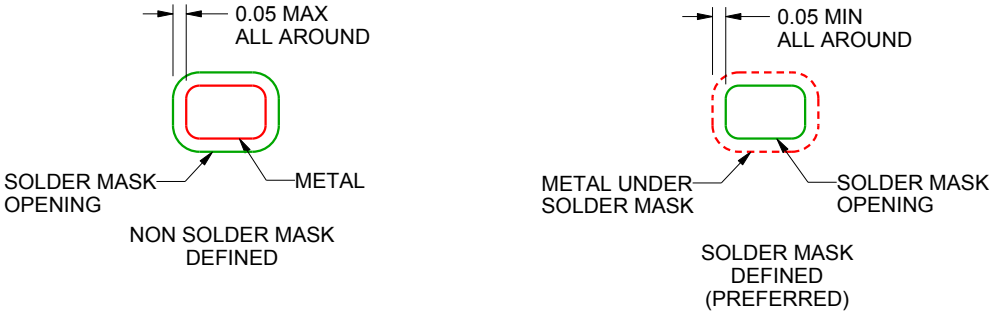


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

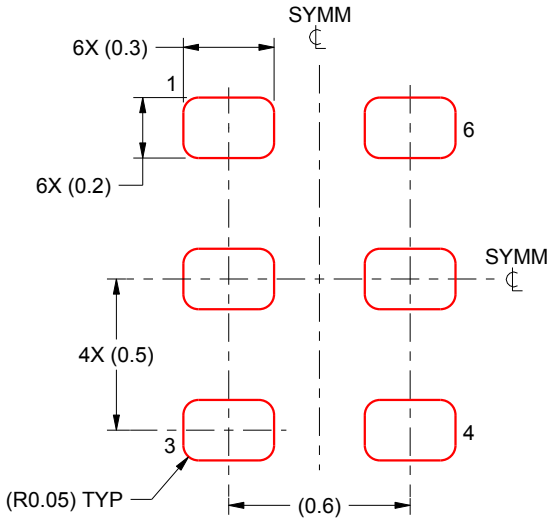
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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