SN74LVC1G17 Single Schmitt-Trigger Buffer

1 Features

- Available in ultra small 0.64mm^2 package (DPW) with 0.5mm pitch
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Maximum t_{pd} of 4.6ns at 3.3V
- Low power consumption, 10µA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000V human-body model (A114A)
  - 200V machine model (A115A)
  - 1000V charged-device model (C101)

2 Applications

- AV receiver
- Audio dock: portable
- Blu-ray player and home theater
- MP3 player/recorder
- Personal Digital Assistant (PDA)
- Power: telecom/server AC/DC supply: single controller: analog and digital
- Solid State Drive (SSD): client and enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: enterprise
- Video analytics: server
- Wireless headset, keyboard, and mouse

3 Description

This single Schmitt-trigger buffer is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G17 device contains one buffer and performs the Boolean function Y = A.

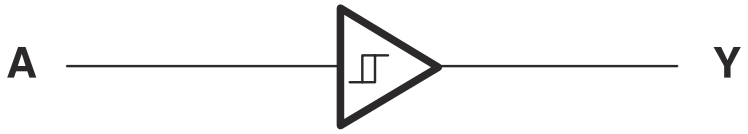
The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G17 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8mm × 0.8mm.

Package Information

DEVICE NAME	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC1G17	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DRL (SOT-5X3, 5)	1.6mm × 1.6mm	1.6mm × 1.2mm
	DCK (SC70, 5)	2.0mm × 2.1mm	2.0mm × 1.25mm
	DPW (X2SON, 5)	0.8mm × 0.8mm	0.8mm × 0.8mm
	DRY (USON, 6)	1.45mm × 1mm	1.45mm × 1.0mm
	DSF (X2SON, 6)	1.0mm × 1.0mm	1.0mm × 1.0mm
	YZP (DSBGA, 5)	1.75mm × 1.25mm	1.75mm × 1.25mm
	YZV (DSBGA, 4)	1.25mm × 1.25mm	1.25mm × 1.25mm

(1) For all available packages, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

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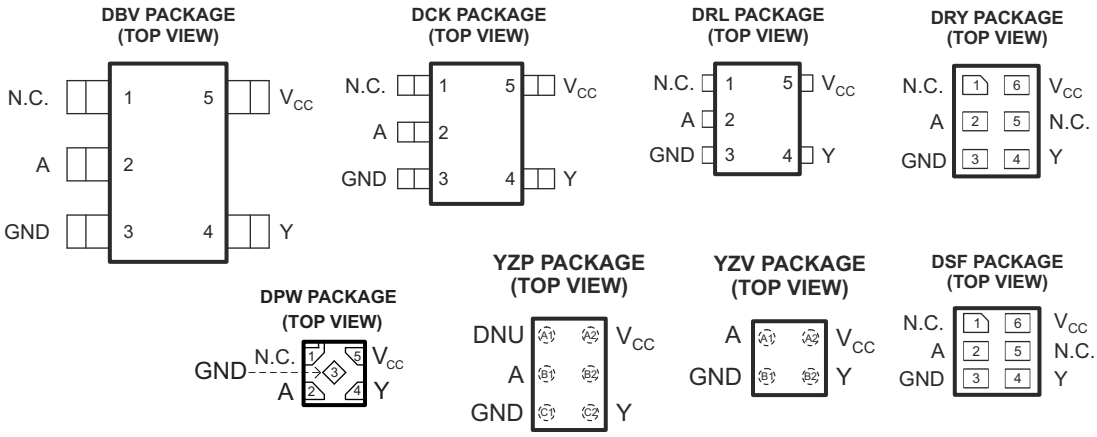
4 Pin Configuration and Functions



N.C. – No internal connection
See mechanical drawings for dimensions.
DNU – Do not use

Pin Functions

PIN					DESCRIPTION
NAME	DBV, DCK, DRL, DPW	DRY, DSF	YZP	YZV	
NC	1	1, 5	A1, B2	–	Not connected
A	2	2	B1	A1	Input
GND	3	3	C1	B1	Ground
Y	4	4	C2	B2	Output
V_{CC}	5	6	A2	A2	Power terminal

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

5.3 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		–4	mA
		V_{CC} = 2.3V		–8	
		V_{CC} = 3V		–16	
				–24	
		V_{CC} = 4.5V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the *Implications of Slow or Floating CMOS Inputs* application note.

5.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G17							UNIT
		DBV	DCK	DRL	DRY	YZP	DPW	YZV	
		5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	357.1	371.0	350	608	130	340	181	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	263.7	297.5	121	432	54	215	1	
$R_{\theta JB}$	Junction-to-board thermal resistance	264.4	258.6	171	446	51	294	39	
ψ_{JT}	Junction-to-top characterization parameter	195.6	195.6	11	191	1	41	8	
ψ_{JB}	Junction-to-board characterization parameter	262.2	256.2	169	442	50	294	38	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	–	198	–	250	–	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics—DC Limit Changes

Table 5-1. DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	25°C			–40°C TO 85°C			–40°C TO 125°C			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP	MAX	
V_{T+} (Positive-going input threshold voltage)		1.65V				0.76		1.13	0.76		1.13	V
		2.3V				1.08		1.56	1.08		1.56	
		3V				1.48		1.92	1.48		1.92	
		4.5V				2.19		2.74	2.19		2.74	
		5.5V				2.65		3.33	2.65		3.33	
V_{T-} (Negative-going input threshold voltage)		1.65V				0.35		0.59	0.35		0.59	V
		2.3V				0.56		0.88	0.56		0.88	
		3V				0.89		1.2	0.89		1.2	
		4.5V				1.51		1.97	1.51		1.97	
		5.5V				1.88		2.4	1.88		2.4	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		1.65V				0.36		0.64	0.36		0.64	V
		2.3V				0.45		0.78	0.45		0.78	
		3V				0.51		0.83	0.51		0.83	
		4.5V				0.58		0.93	0.58		0.93	
		5.5V				0.69		1.04	0.69		1.04	
V_{OH}	I_{OH} = –100µA	1.65V to 5.5V				V_{CC} – 0.1			V_{CC} – 0.1			V
	I_{OH} = –4mA	1.65V				1.2			1.2			
	I_{OH} = –8mA	2.3V				1.9			1.9			
	I_{OH} = –16mA	3V				2.4			2.4			
	I_{OH} = –24mA					2.3			2.3			
	I_{OH} = –32mA	4.5V				3.8			3.8			
V_{OL}	I_{OL} = 100µA	1.65V to 5.5V						0.1			0.1	V
	I_{OL} = 4mA	1.65V						0.45			0.45	
	I_{OL} = 8mA	2.3V						0.3			0.3	
	I_{OL} = 16mA	3V						0.4			0.4	
	I_{OL} = 24mA							0.55			0.55	
	I_{OL} = 32mA	4.5V						0.55			0.55	
I_I A input	V_I = 5.5V or GND	0 to 5.5V						±5			±5	µA
I_{off}	V_I or V_O = 5.5V	0						±10			±10	µA
I_{CC}	V_I = 5.5V or GND, I_O = 0	1.65V to 5.5V						10			10	µA
	V_I = 3.6V or GND, I_O = 0	3V to 3.6V		0.5	1.5							
ΔI_{CC}	One input at V_{CC} – 0.6V, Other inputs at $V_{C\ C}$ or GND	3V to 5.5V						500			500	µA
C_I	V_I = V_{CC} or GND	3.3V		4.5								pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Switching Characteristics, C_L = 15pF

Table 5-2. C_L = 15pF

over recommended operating free-air temperature range, C_L = 15pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C								UNIT
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2.8	9.9	1.6	5.5	1.5	4.6	0.9	4.4	ns

5.7 Switching Characteristics AC Limit, –40°C to 85°C

Table 5-3. AC Limit, –40°C to 85°C

over recommended operating free-air temperature range, C_L = 30pF or 50pF (unless otherwise noted) (see Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C								UNIT
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.8	11	2	6.5	1.8	5.5	1.2	5	ns

5.8 Switching Characteristics AC Limit, –40°C to 125°C

Table 5-4. AC Limit –40°C to 125°C

over recommended operating free-air temperature range, C_L = 30pF or 50pF (unless otherwise noted) (see Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 125°C								UNIT
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.8	13	2	8	1.8	6.5	1.2	6	ns

5.9 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10MHz	20	21	22	26	pF

5.10 Typical Characteristics

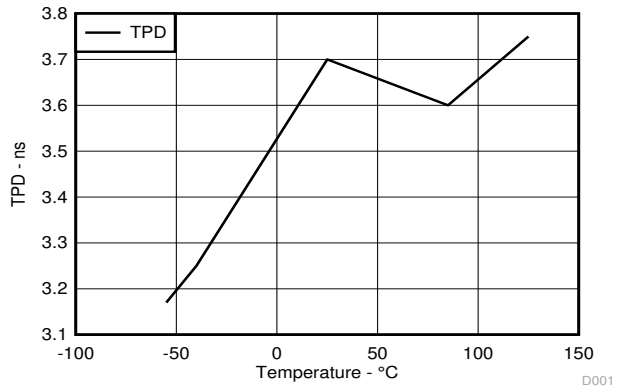


Figure 5-1. Across Temperature at 3.3V Vcc

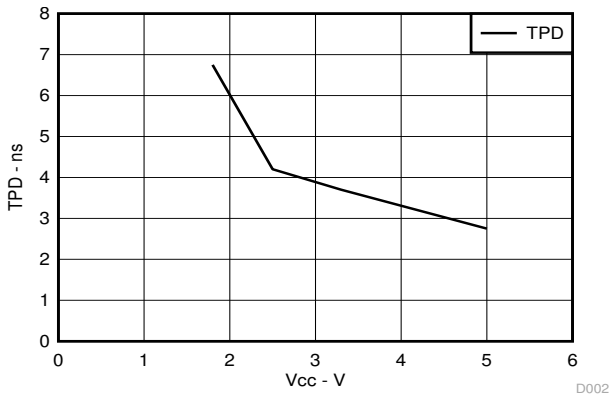
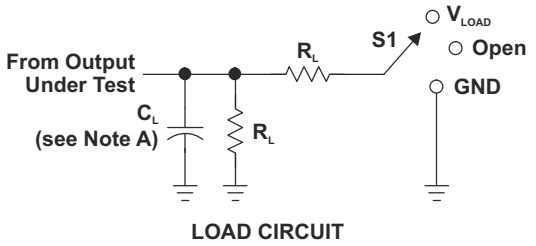


Figure 5-2. Across Vcc at 25°C

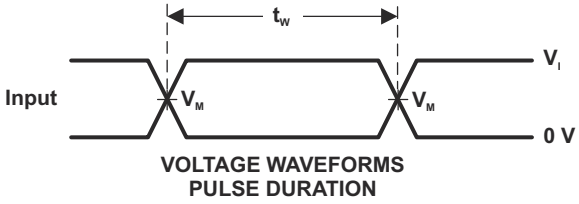
6 Parameter Measurement Information



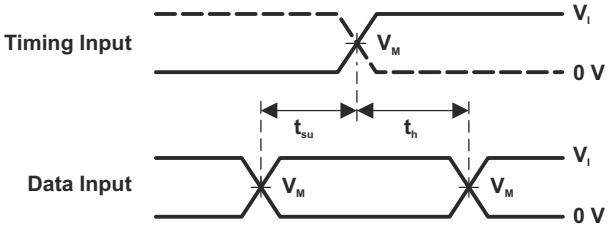
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

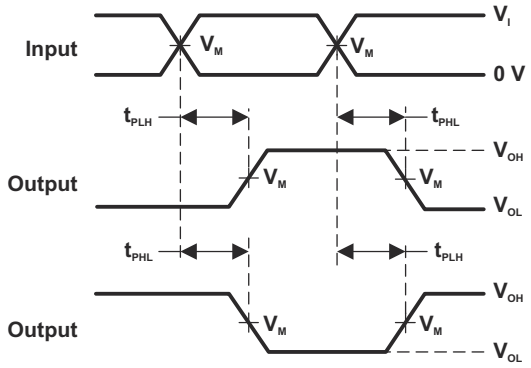
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



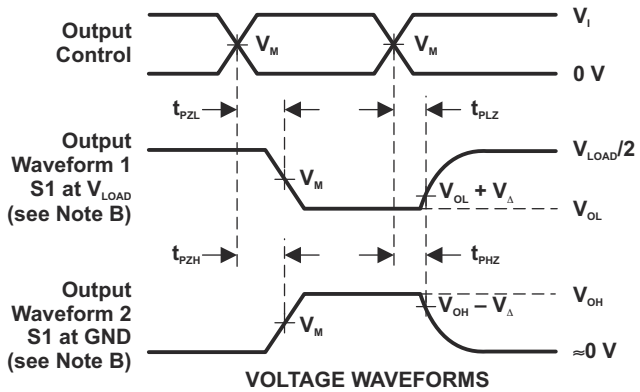
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



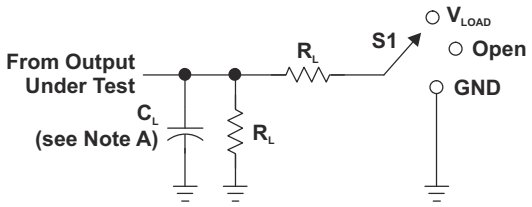
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

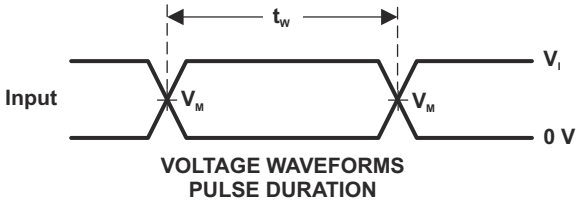
Figure 6-1. Load Circuit and Voltage Waveforms



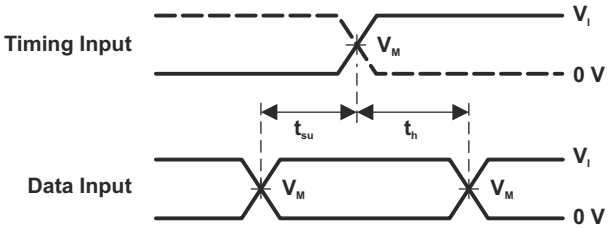
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

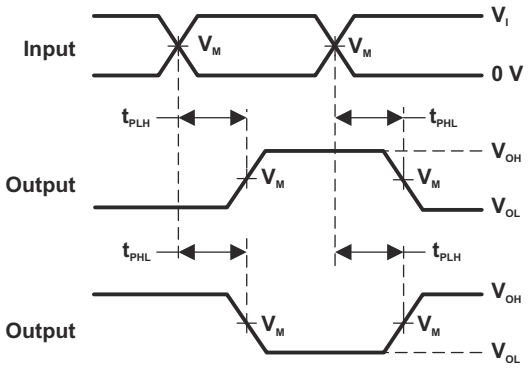
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



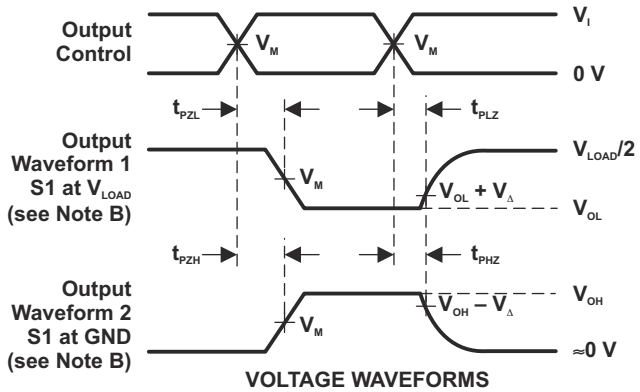
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
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NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
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F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

7 Detailed Description

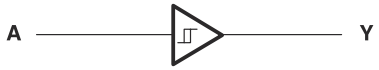
7.1 Overview

The SN74LVC1G17 device contains one Schmitt trigger buffer and performs the Boolean function Y = A. The device functions as an independent buffer, but because of the Schmitt action, the device has different input threshold levels for positive-going (VT+) and negative-going signals.

The DPW package technology is a major breakthrough in IC packaging. The DPW package is 0.64mm square footprint that saves board space over other package options while still retaining the traditional and manufacturing-friendly lead pitch of 0.5mm.

The SN74LVC1G17 is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when the device is powered down.

7.2 Functional Block Diagram



7.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65V to 5.5V
- Allows down voltage translation
- Inputs accept voltages to 5.5V
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0V

7.4 Device Functional Modes

Table 7-1. Function Table

INPUT A	OUTPUT Y
H	H
L	L

8 Applications and Implementation

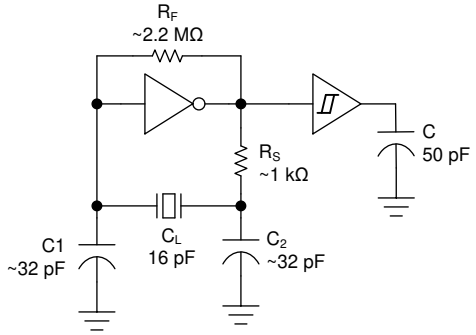
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G17 is a high drive CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. SN74LVC1G17 can produce 24mA of drive current at 3.3V; engineers can use it for driving multiple outputs and good for high speed applications up to 100MHz. The inputs are 5.5V tolerant allowing SN74LVC1G17 to translate down to V_{CC}.

8.2 Typical Application



8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention, because bus contention can drive currents to exceed maximum limits. Consider routing and load conditions to prevent ringing because the high drive also creates fast edges into light loads.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating Conditions table at any valid V_{CC}.
2. Recommend Output Conditions
   - Do not exceed load currents (I_O max) per output or (continuous current through V_{CC} or GND) total current for the part. These limits are located in the Absolute Max Ratings table.
   - Do not pull outputs above V_{CC}.

8.2.3 Application Curves

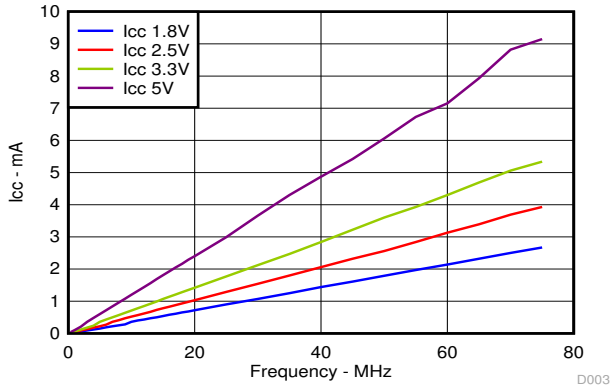


Figure 8-1. ICC vs Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

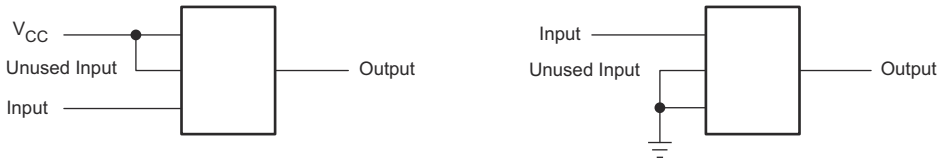
Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF capacitor is recommended. If there are multiple Vcc pins, then a 0.01µF or 0.022µF capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. For best results, install the bypass capacitor as close to the power pin as possible.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, verify that inputs do not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Do no leave such input terminals unconnected because the undefined voltages at the outside connections result in undefined operational states. In all circumstances, observe the rules specified below. Connect all unused inputs of digital logic devices to a high or low bias to prevent them from floating. The logic level that applies to any particular unused input depends on the function of the device. Generally the logic level is tied to the Gnd or Vcc, whichever is the better choice.

8.4.2 Layout Example



9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision X (June 2025) to Revision Y (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 280°C/W to: 371.0°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 66°C/W to: 297.5°C/W	5
• Changed Junction-to-board thermal resistance value for DCK package from: 67°C/W to: 258.6°C/W	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DCK package from: 66°C/W to: 256.2°C/W	5

Changes from Revision W (September 2020) to Revision X (June 2025)	Page
• Updated the document to reflect TI writing standards	1
• Changed *Device Information* table to *Package Information*	1
• Moved T_{stg} to *Absolute Maximum Ratings* table	4
• Changed *Handling Ratings* to *ESD Ratings*	4
• Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W	5
• Changed Junction-to-board thermal resistance value for DBV package from: 62°C/W to: 264.4°C/W	5
• Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W	5
• Removed rise time and fall time information from the recommended input conditions in the *Detailed Design Procedure*	11

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G17DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C175, C17F, C17J, C17K, C17R) (C17H, C17P, C17S)
SN74LVC1G17DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C175, C17F, C17J, C17K, C17R) (C17H, C17P, C17S)
SN74LVC1G17DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C175, C17F, C17J, C17K, C17R) (C17H, C17P, C17S)
SN74LVC1G17DBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F
SN74LVC1G17DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F
SN74LVC1G17DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F
SN74LVC1G17DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F
SN74LVC1G17DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C175, C17F, C17J, C17K, C17R) (C17H, C17P, C17S)
SN74LVC1G17DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C175, C17F, C17J, C17K, C17R) (C17H, C17P, C17S)
SN74LVC1G17DBVTE4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F
SN74LVC1G17DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F
SN74LVC1G17DBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F
SN74LVC1G17DCK3	Last Time Buy	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	(C7F, C7Z)
SN74LVC1G17DCK3.B	Last Time Buy	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SNBI	Level-1-260C-UNLIM	-40 to 85	(C7F, C7Z)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G17DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(1X8, C75, C7F, C7J, C7K, C7R, C7T) (C7H, C7P, C7S)
SN74LVC1G17DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1X8, C75, C7F, C7J, C7K, C7R, C7T) (C7H, C7P, C7S)
SN74LVC1G17DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(1X8, C75, C7F, C7J, C7K, C7R, C7T) (C7H, C7P, C7S)
SN74LVC1G17DCKRE4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S
SN74LVC1G17DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S
SN74LVC1G17DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S
SN74LVC1G17DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S
SN74LVC1G17DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C75, C7F, C7J, C7K, C7R, C7T) (C7H, C7P, C7S)
SN74LVC1G17DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C75, C7F, C7J, C7K, C7R, C7T) (C7H, C7P, C7S)
SN74LVC1G17DCKTE4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S
SN74LVC1G17DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S
SN74LVC1G17DCKTG4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S
SN74LVC1G17DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S4
SN74LVC1G17DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S4
SN74LVC1G17DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C77, C7R)
SN74LVC1G17DRLR.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C77, C7R)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G17DRLRG4	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C77, C7R)
SN74LVC1G17DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7
SN74LVC1G17DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7
SN74LVC1G17DRYRG4	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7
SN74LVC1G17DRYRG4.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7
SN74LVC1G17DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C7
SN74LVC1G17DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C7
SN74LVC1G17DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7
SN74LVC1G17DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7
SN74LVC1G17YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C7N
SN74LVC1G17YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C7N
SN74LVC1G17YZTR.B	Active	Production	DSBGA (YZT) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C7
SN74LVC1G17YZVR	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C7 (7, N)
SN74LVC1G17YZVR.B	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C7 (7, N)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC1G17 :

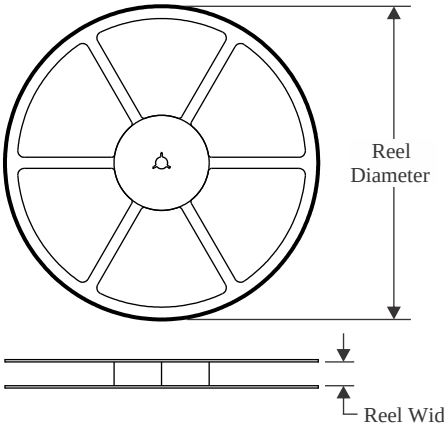
- Automotive : SN74LVC1G17-Q1
- Enhanced Product : SN74LVC1G17-EP

NOTE: Qualified Version Definitions:

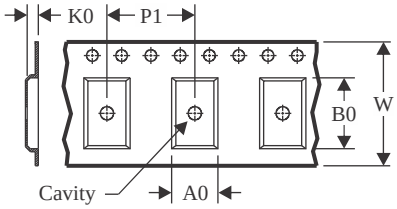
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

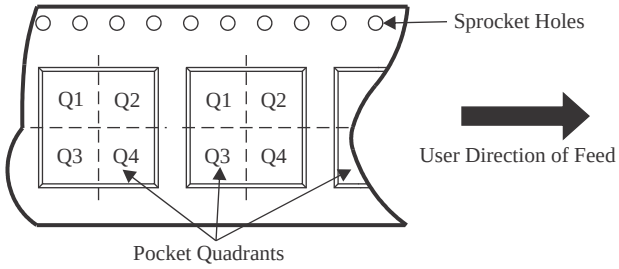


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

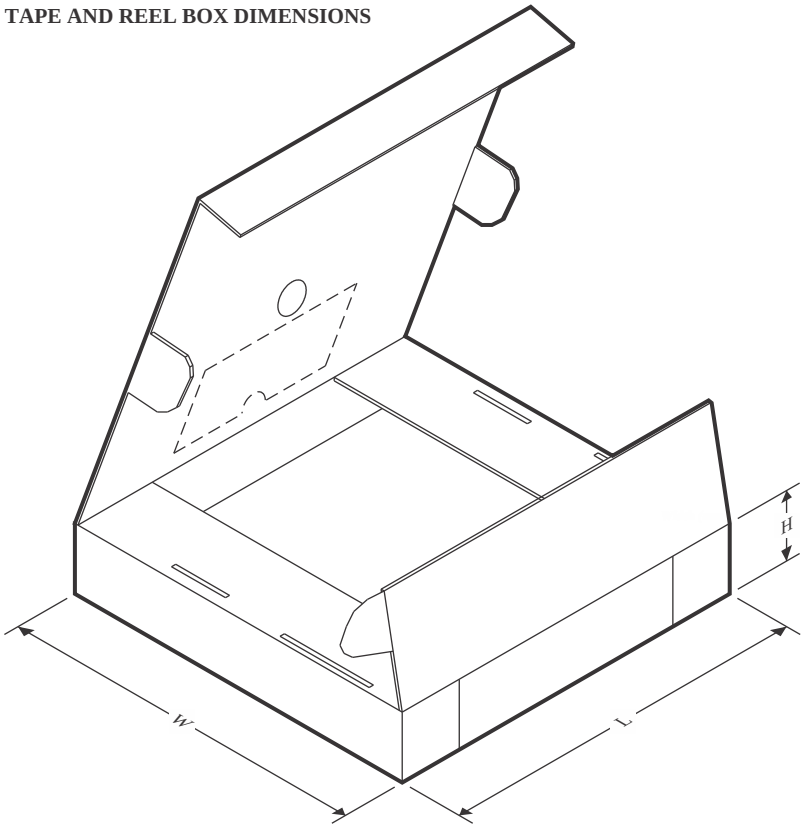


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G17DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G17DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G17DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G17DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G17DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G17DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G17DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G17DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G17DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G17DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G17DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G17DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G17DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G17YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G17YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G17DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G17DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G17DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G17DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G17DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G17DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G17DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G17DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G17DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G17DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G17DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G17DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G17DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G17DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G17DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G17YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

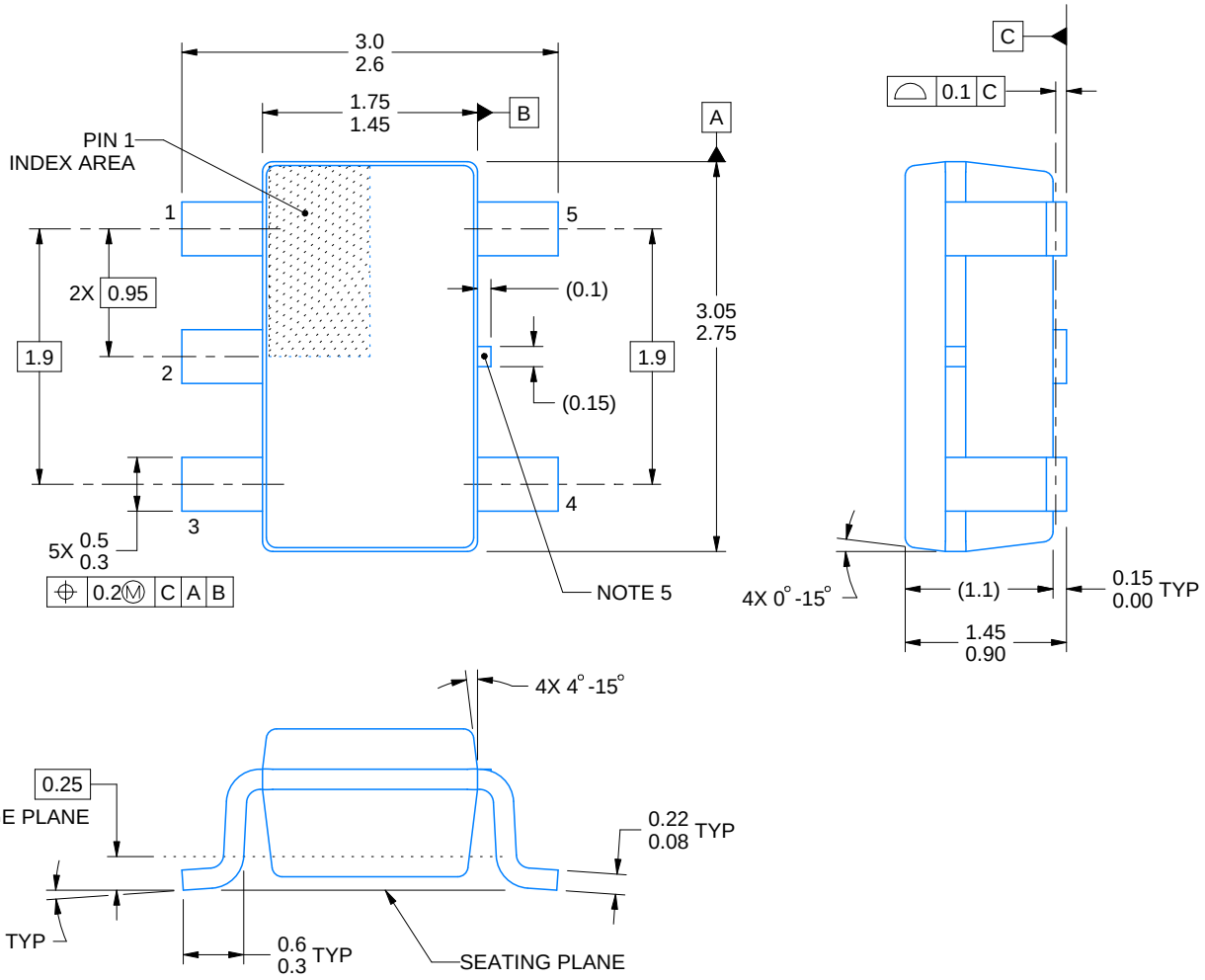
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G17YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

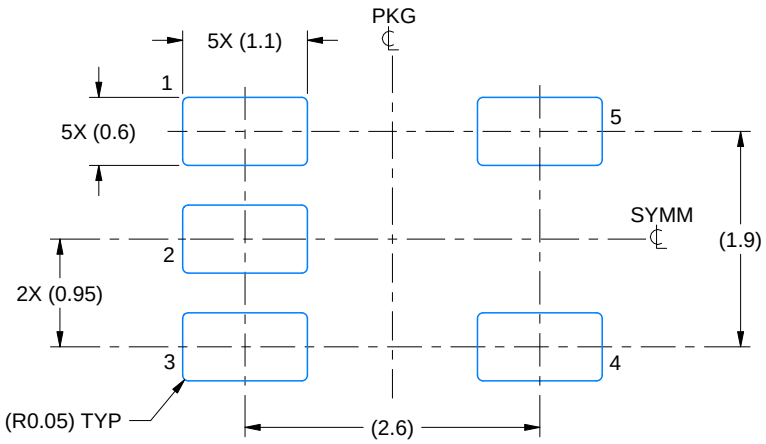
SMALL OUTLINE TRANSISTOR



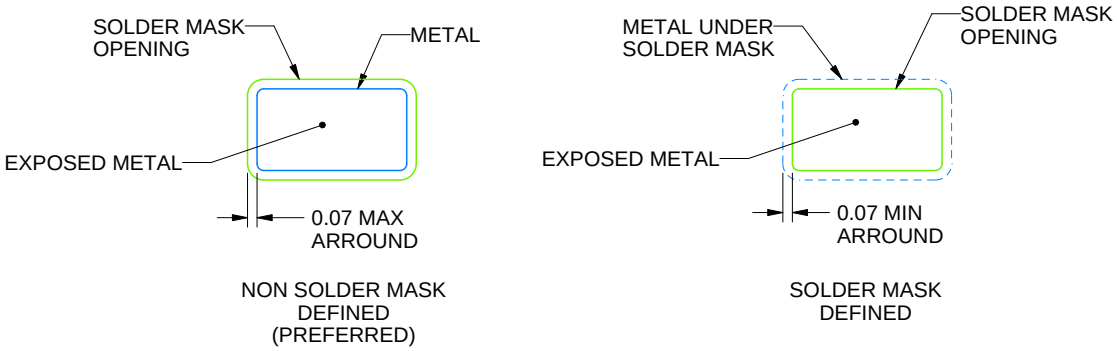
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

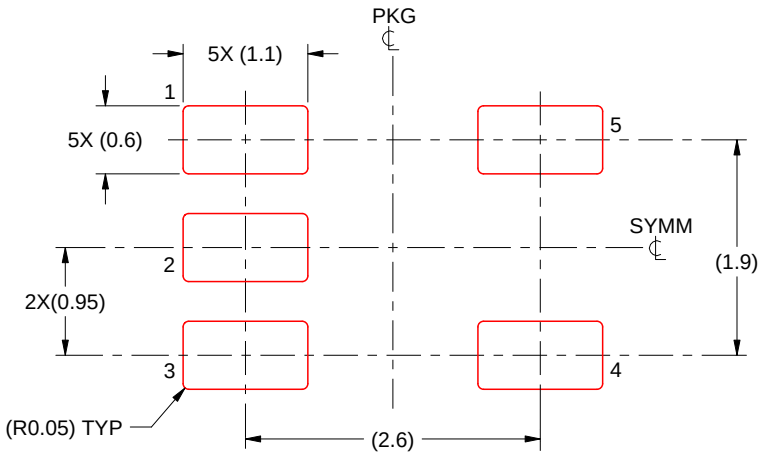


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

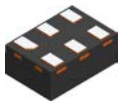
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

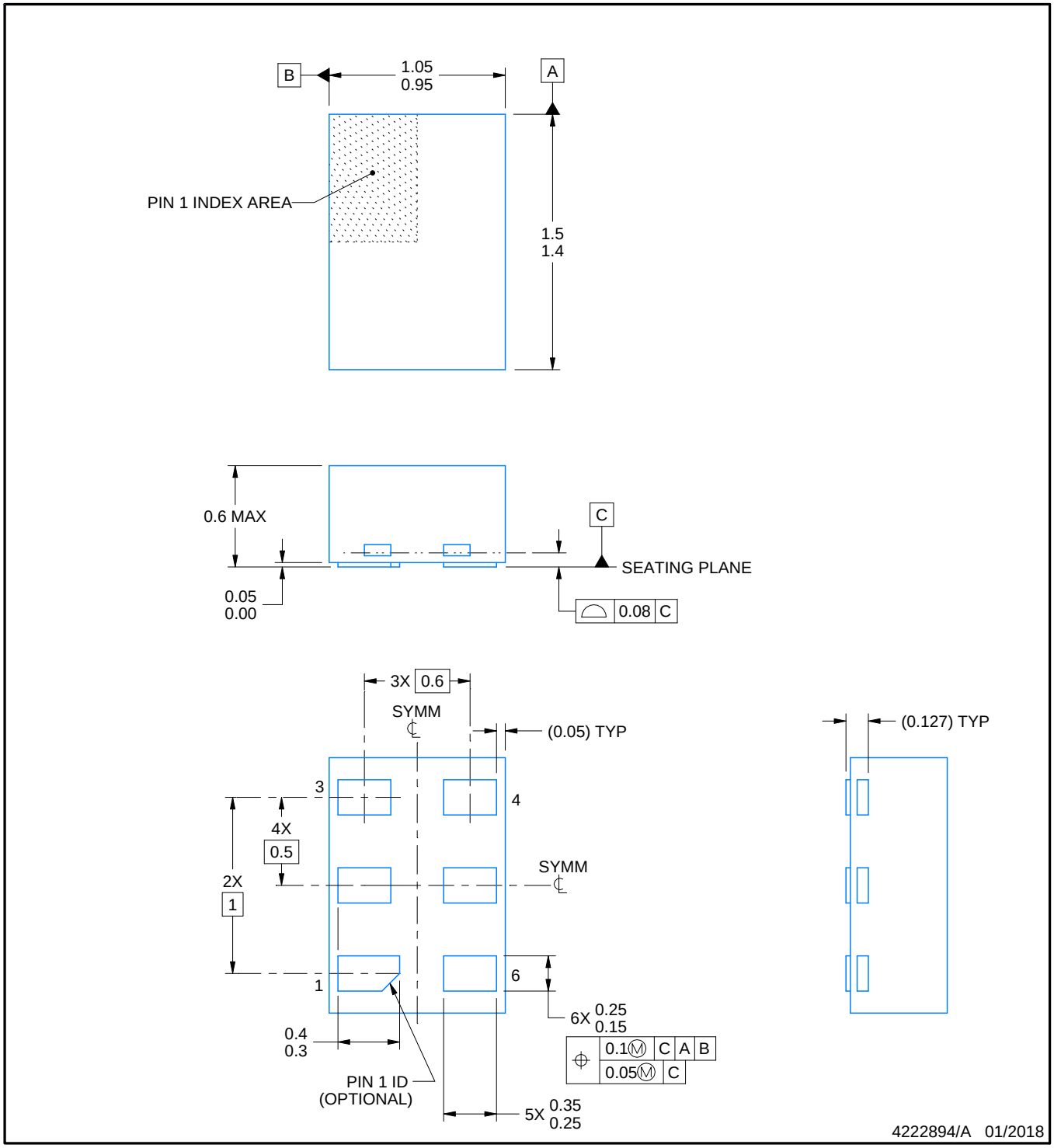
DRY0006A



PACKAGE OUTLINE

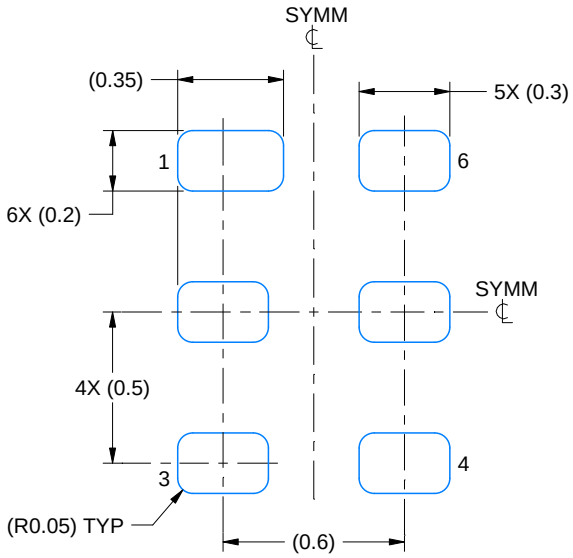
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

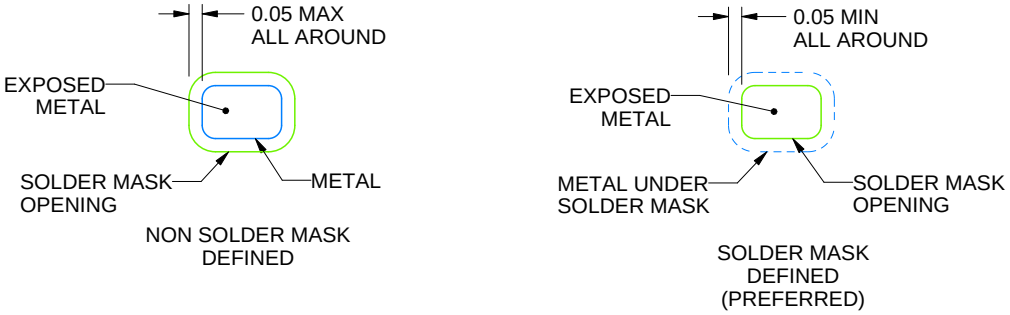


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

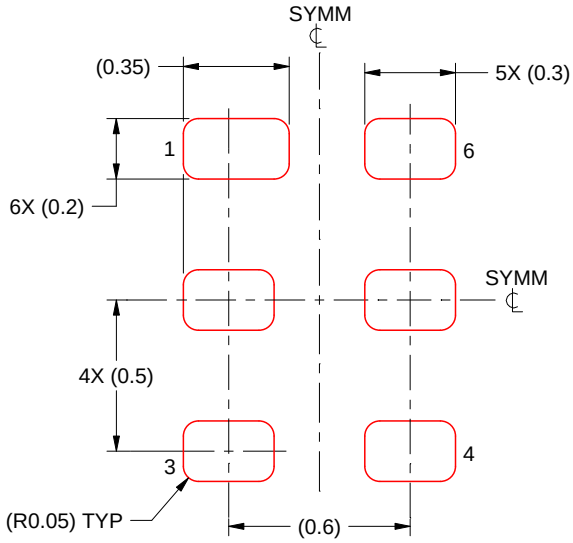
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

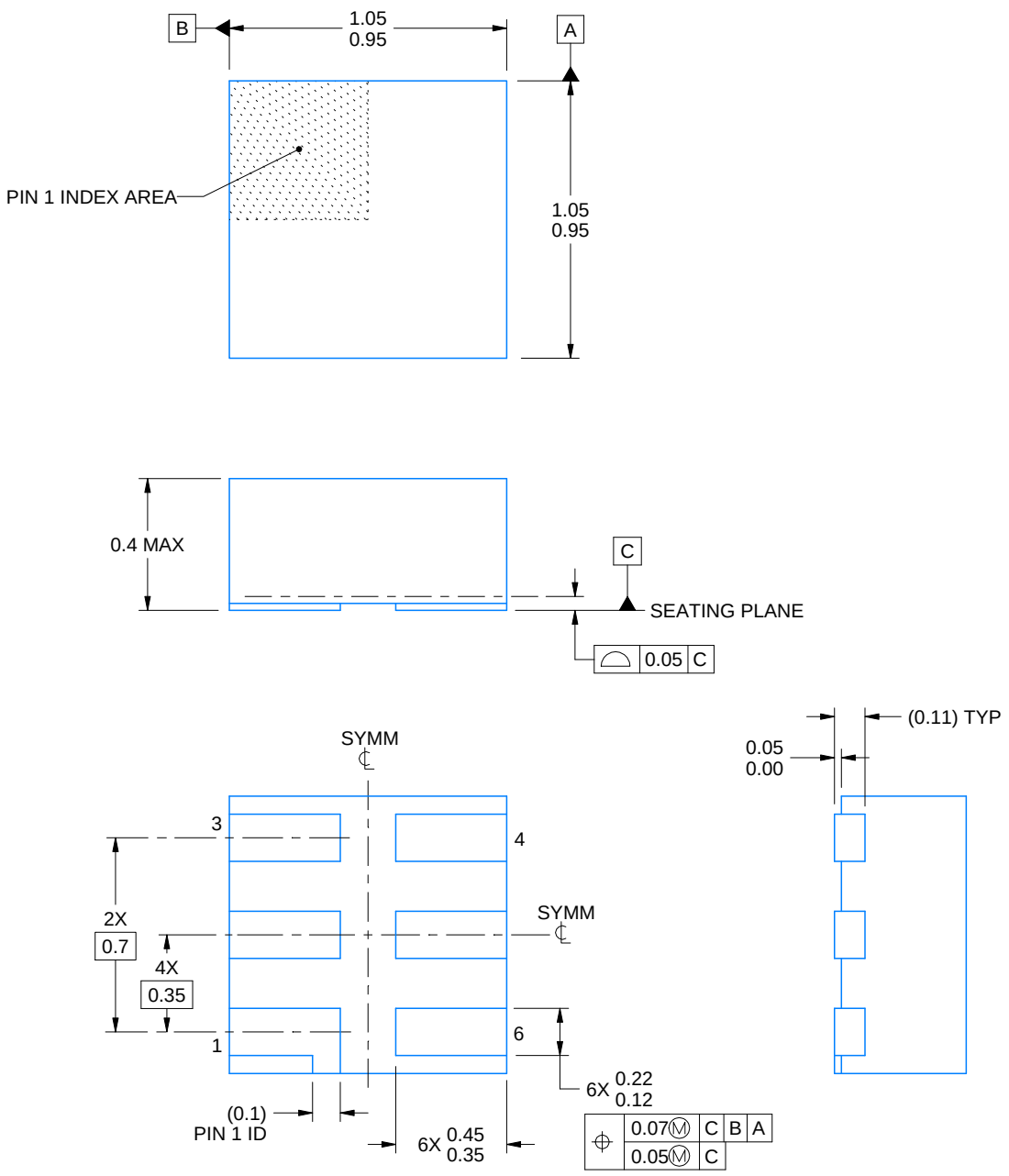
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

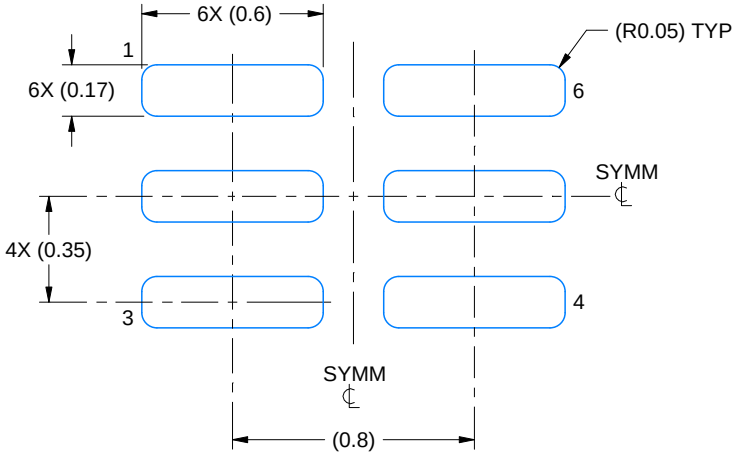
PLASTIC SMALL OUTLINE - NO LEAD



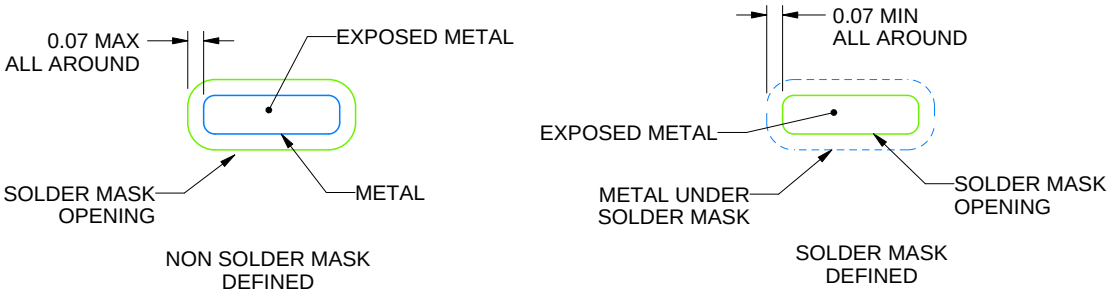
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

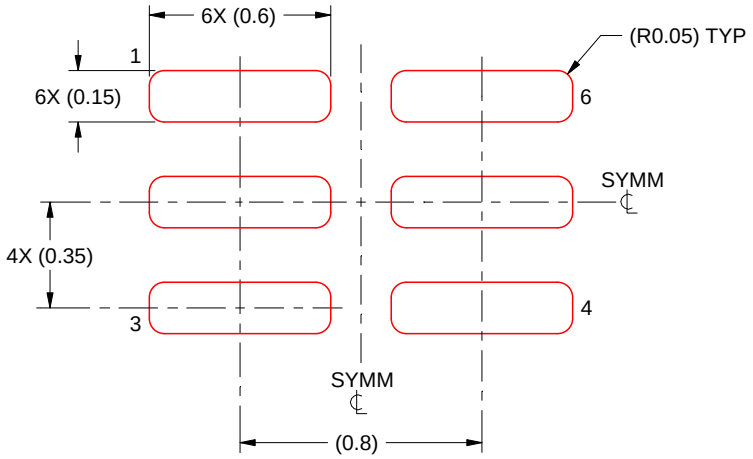
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

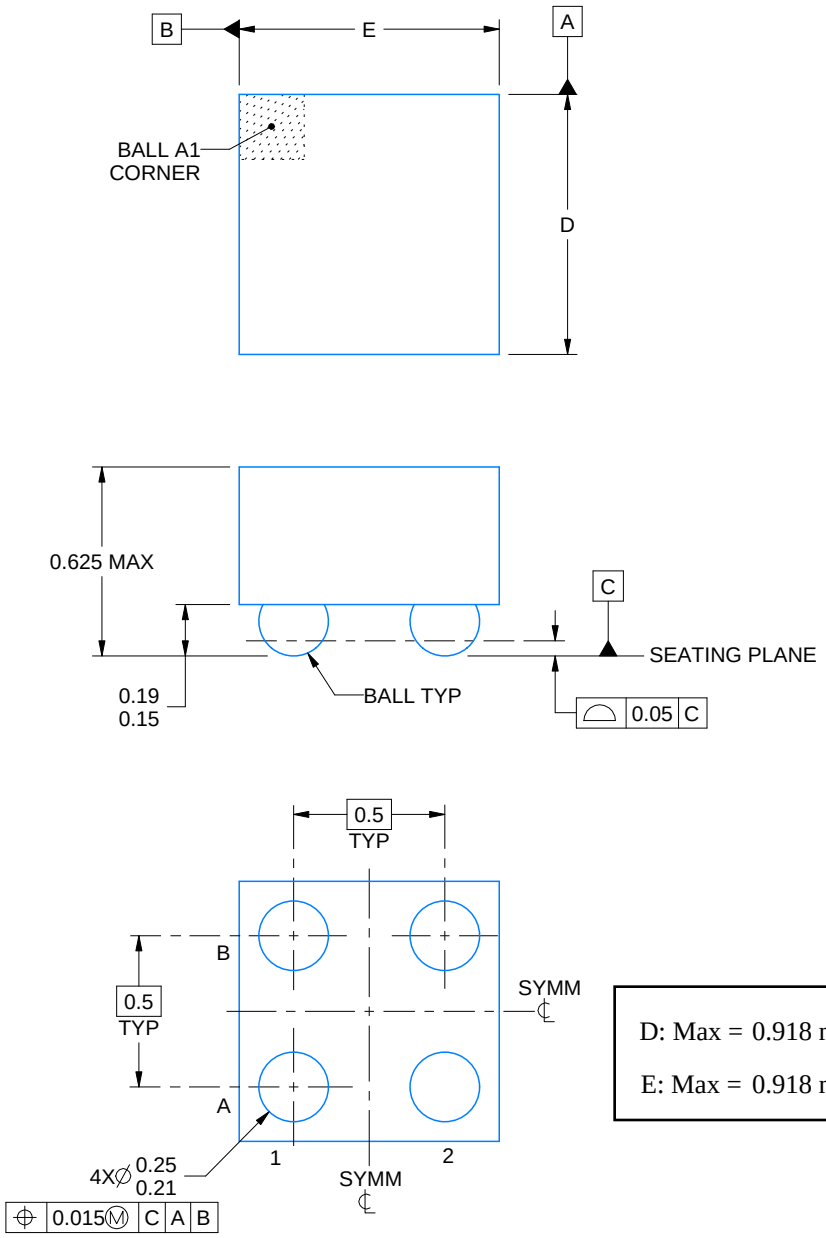
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZT0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



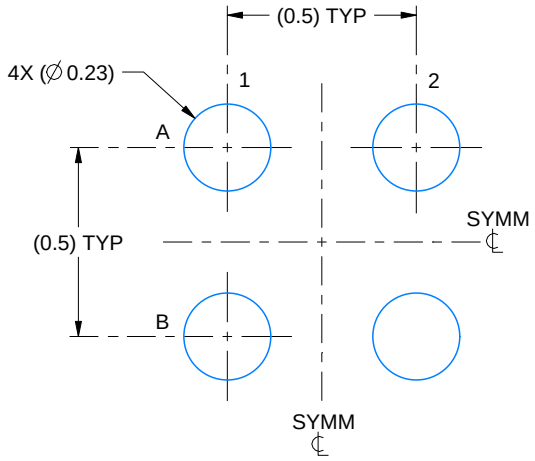
D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

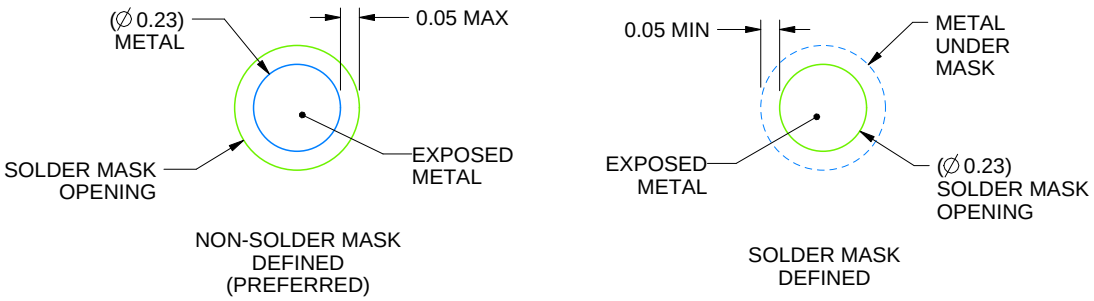
4219477/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X

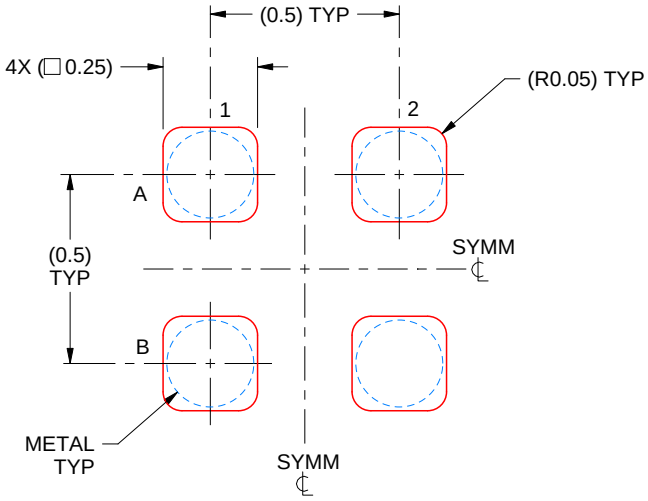


SOLDER MASK DETAILS
NOT TO SCALE

4219477/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4219477/A 05/2017

NOTES: (continued)

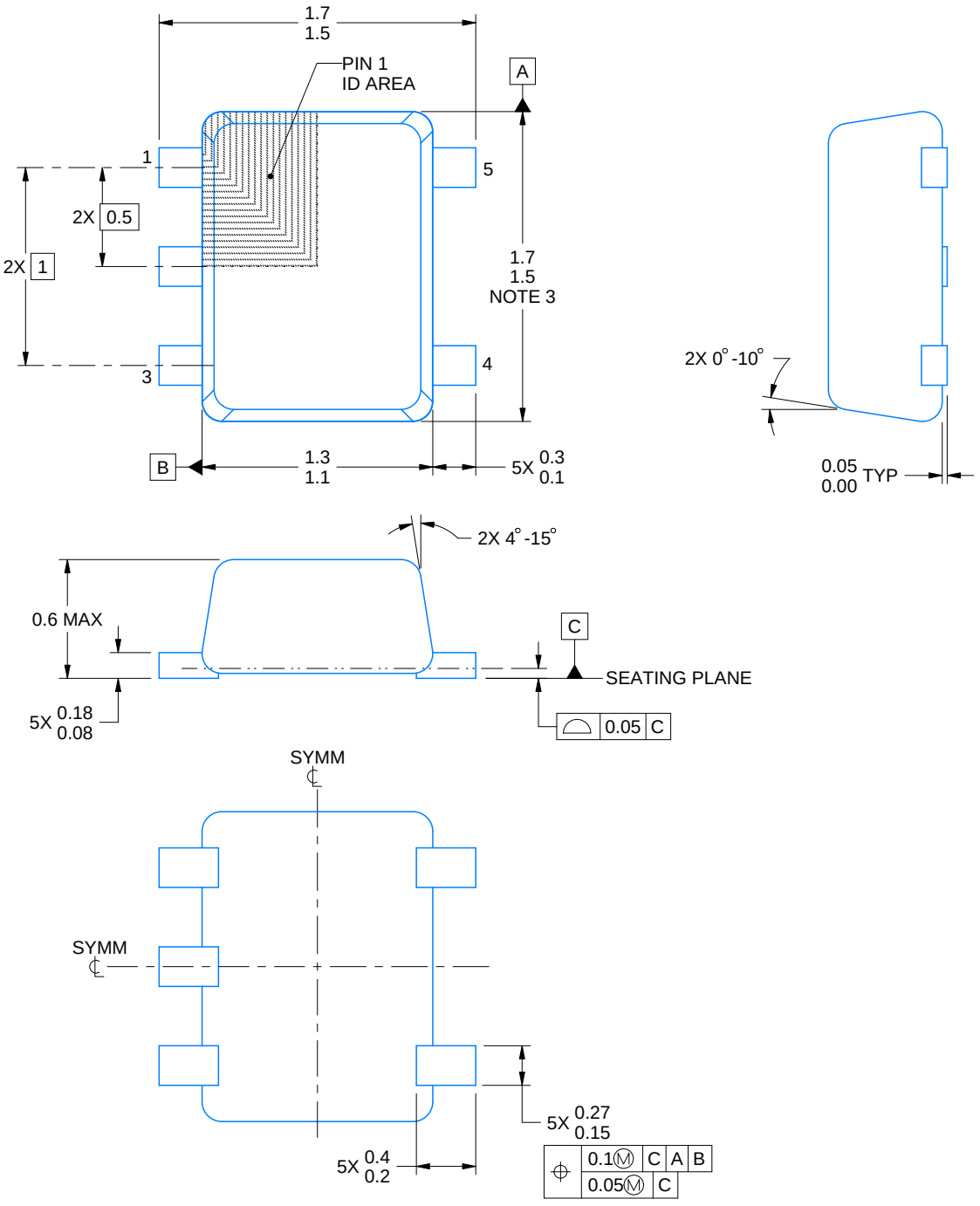
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DRL0005A

SOT - 0.6 mm max height

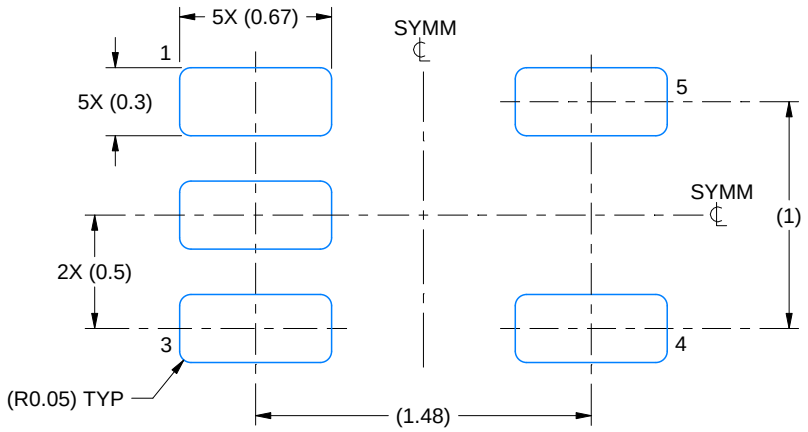
PLASTIC SMALL OUTLINE



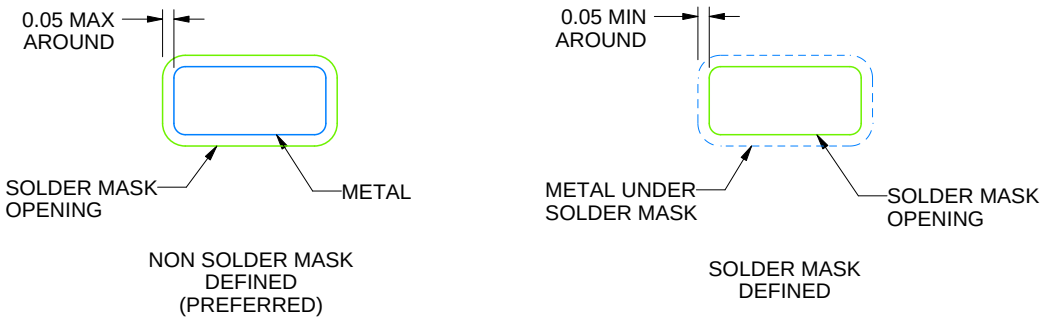
4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X

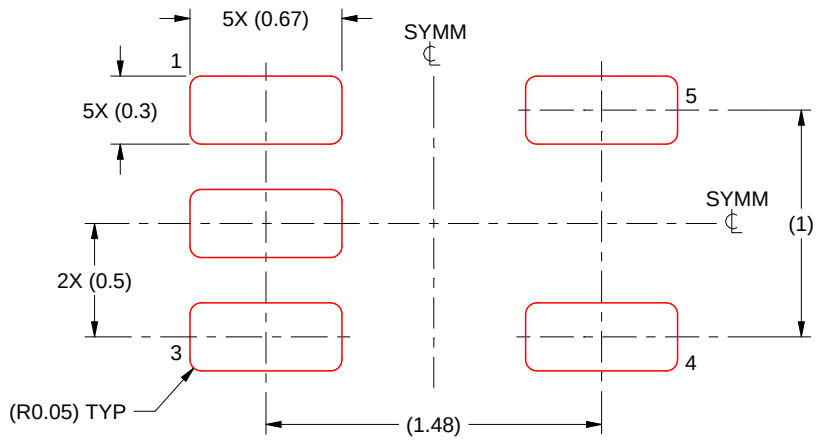


SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

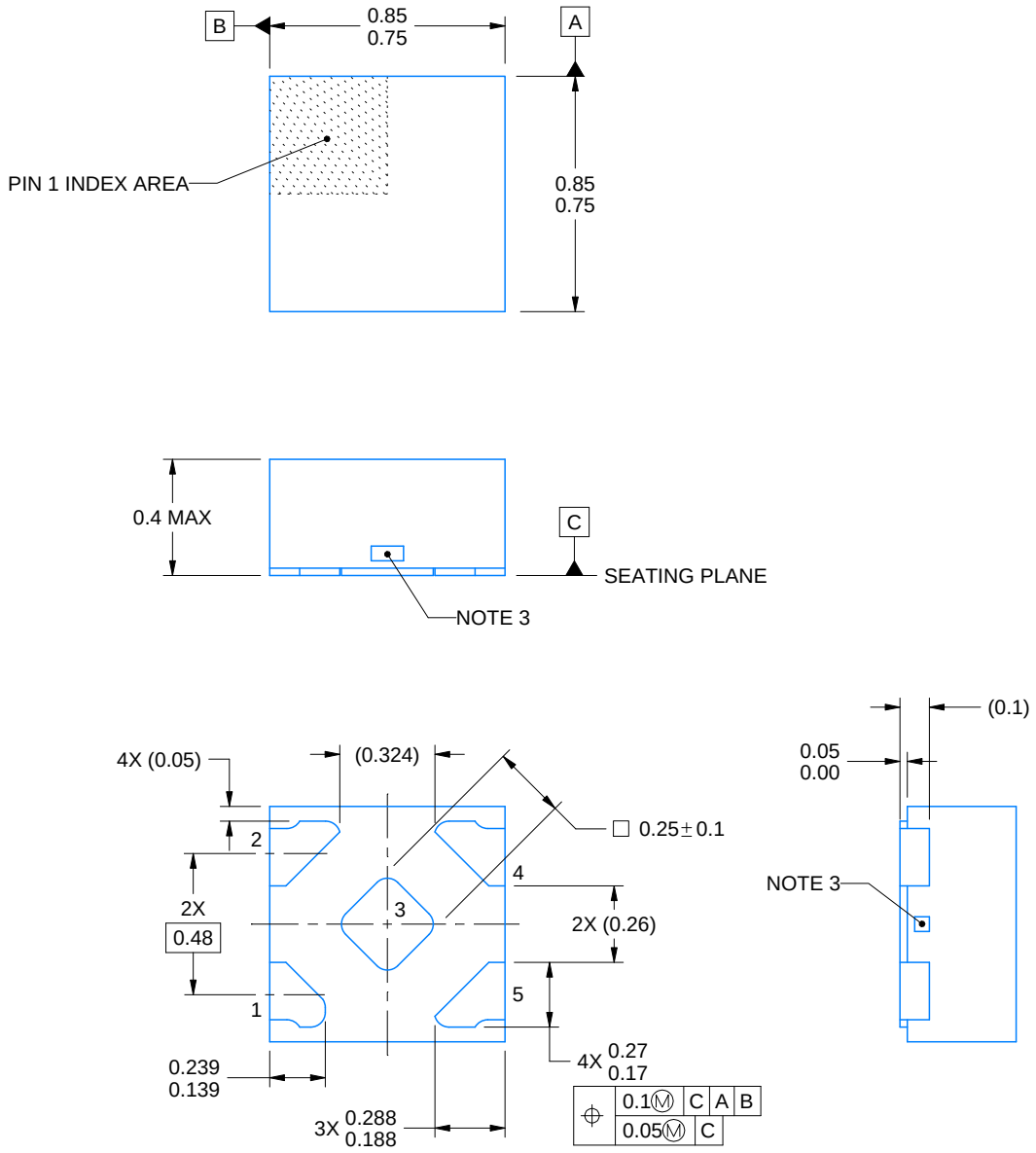
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

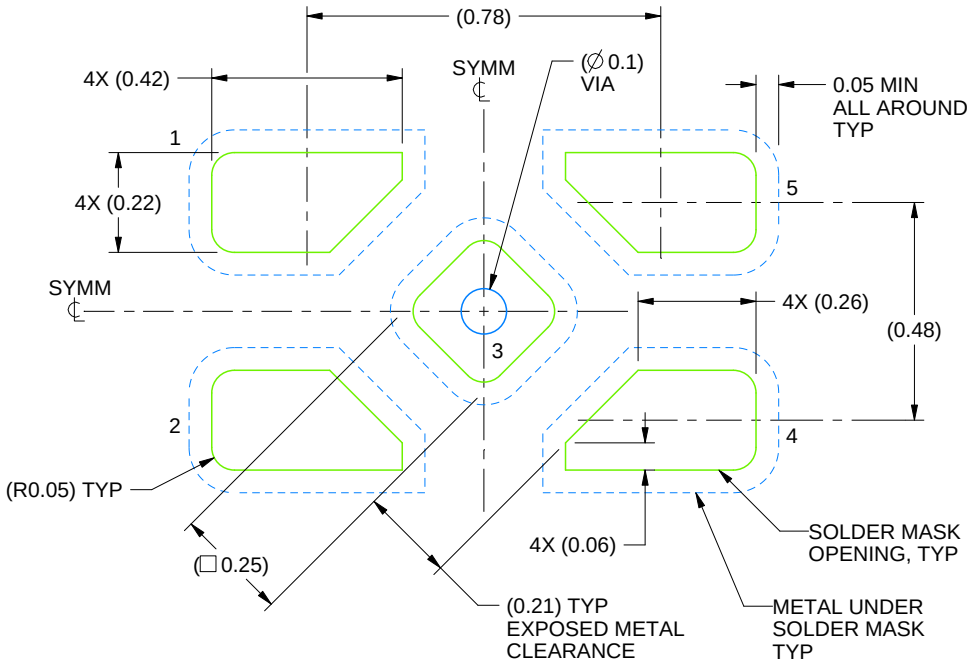
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

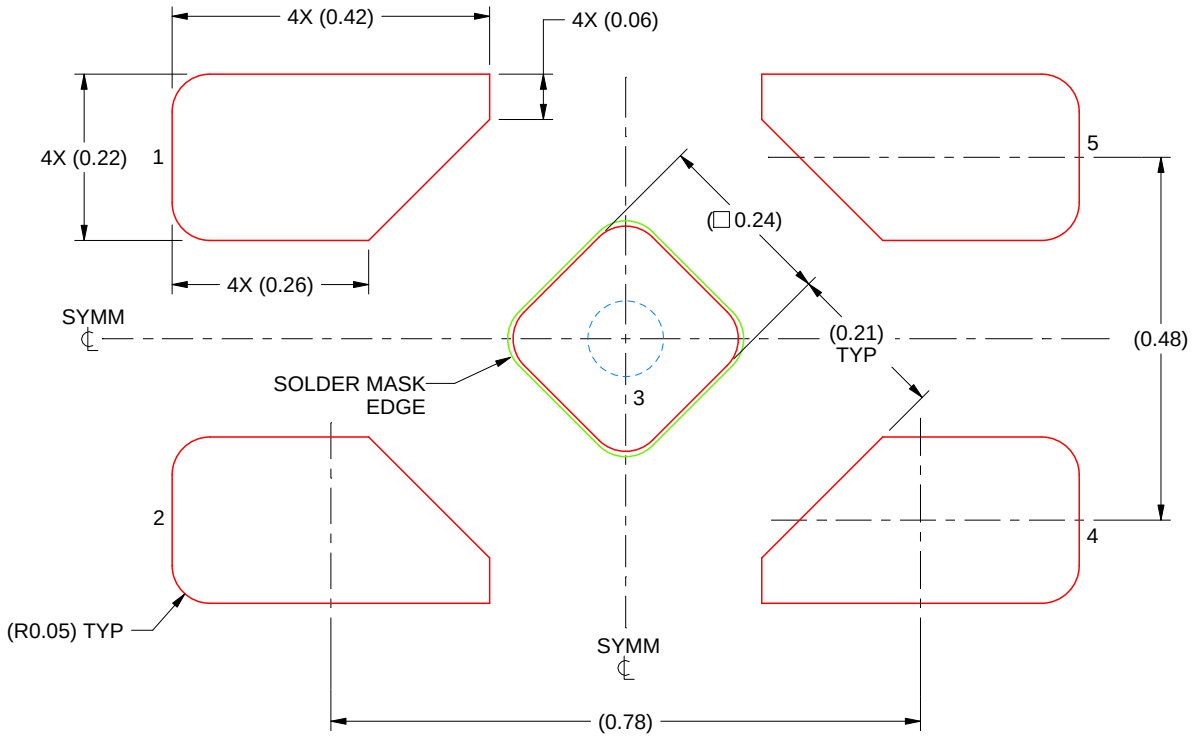
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

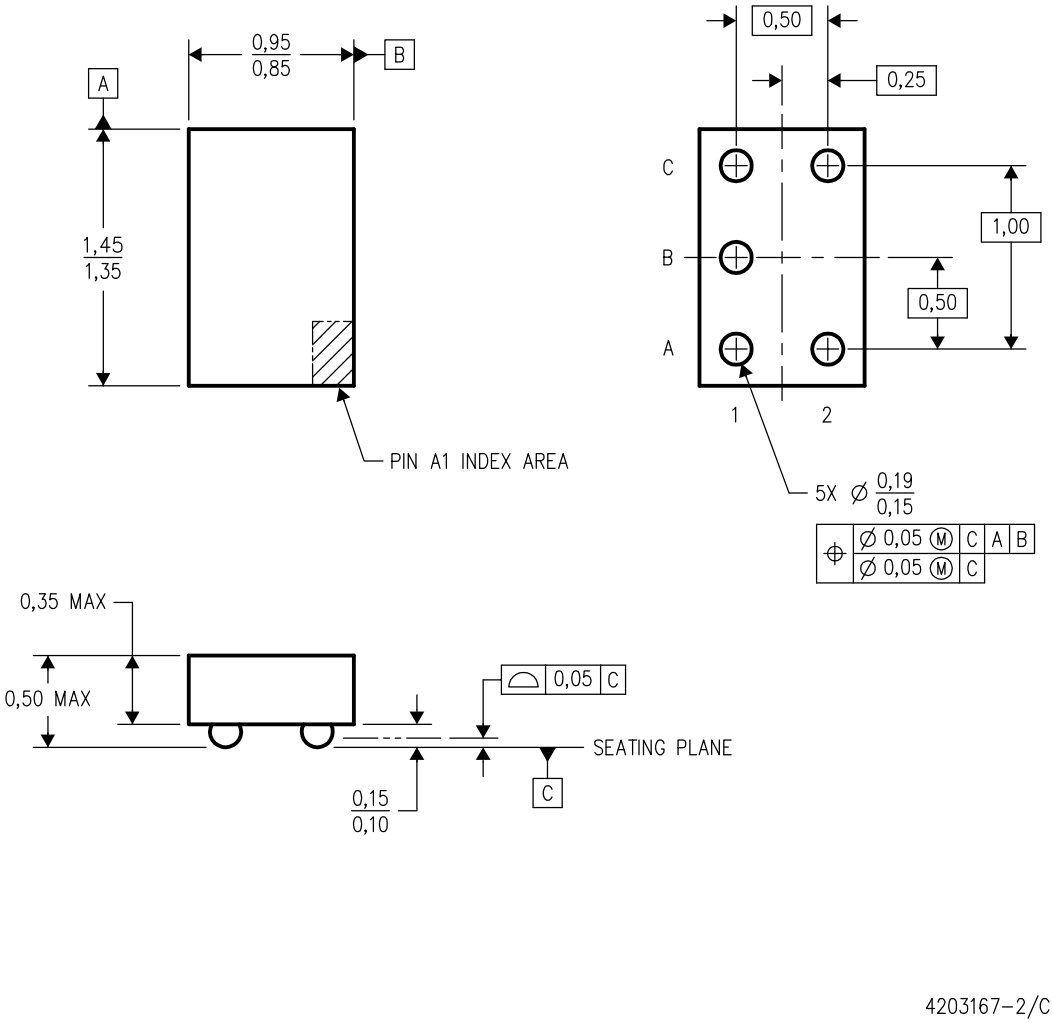
EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YEA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is tin–lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead–free.

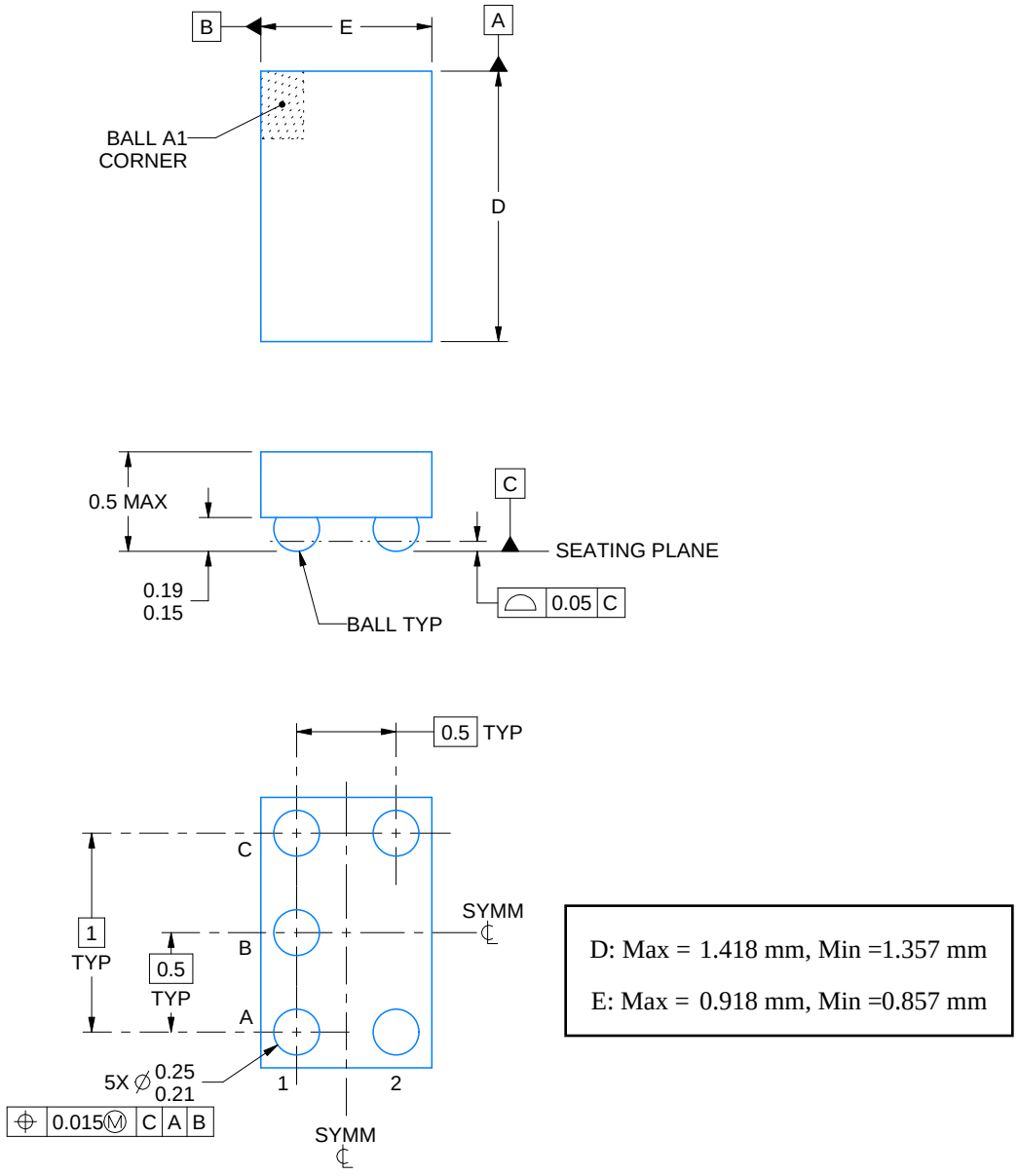
NanoStar is a trademark of Texas Instruments.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



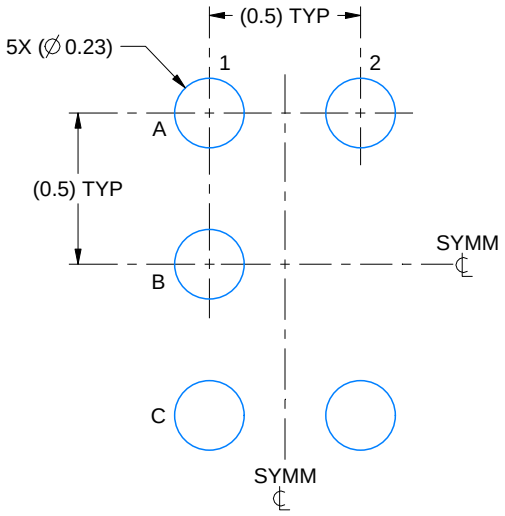
D: Max = 1.418 mm, Min =1.357 mm

E: Max = 0.918 mm, Min =0.857 mm

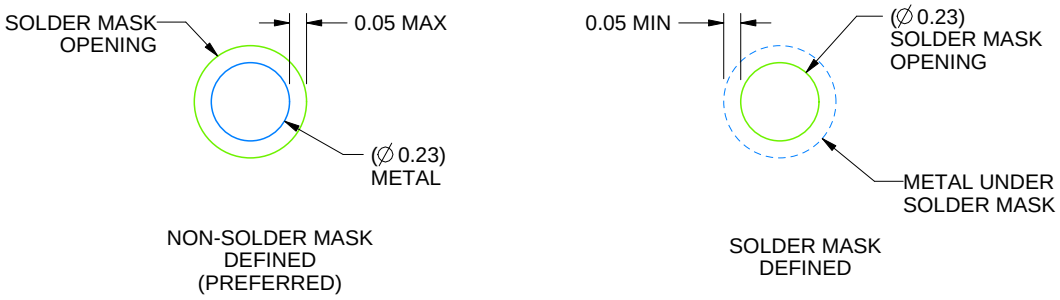
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

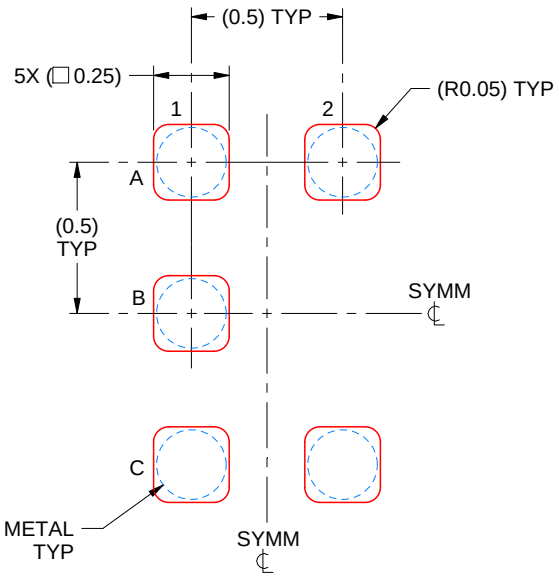


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



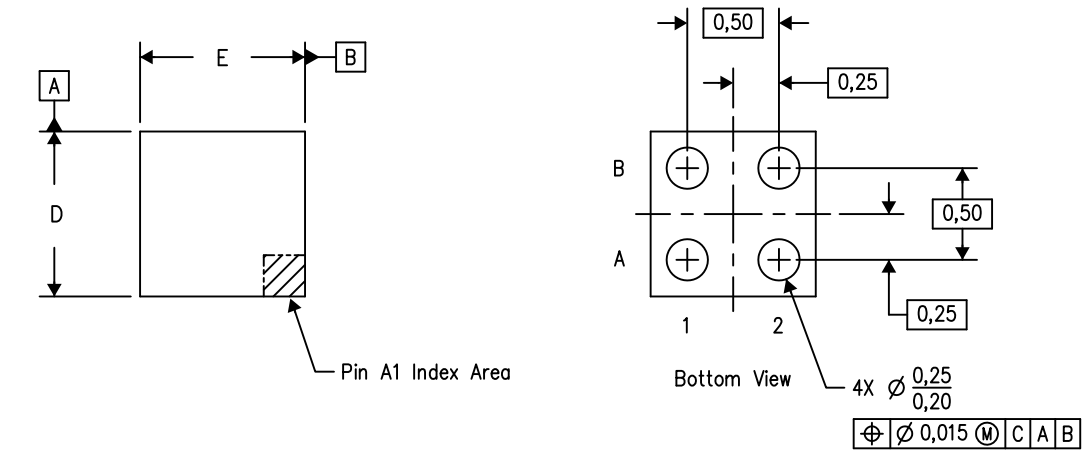
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

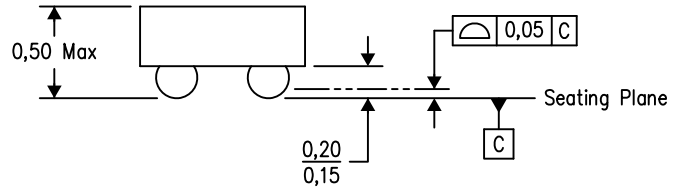
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY





D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

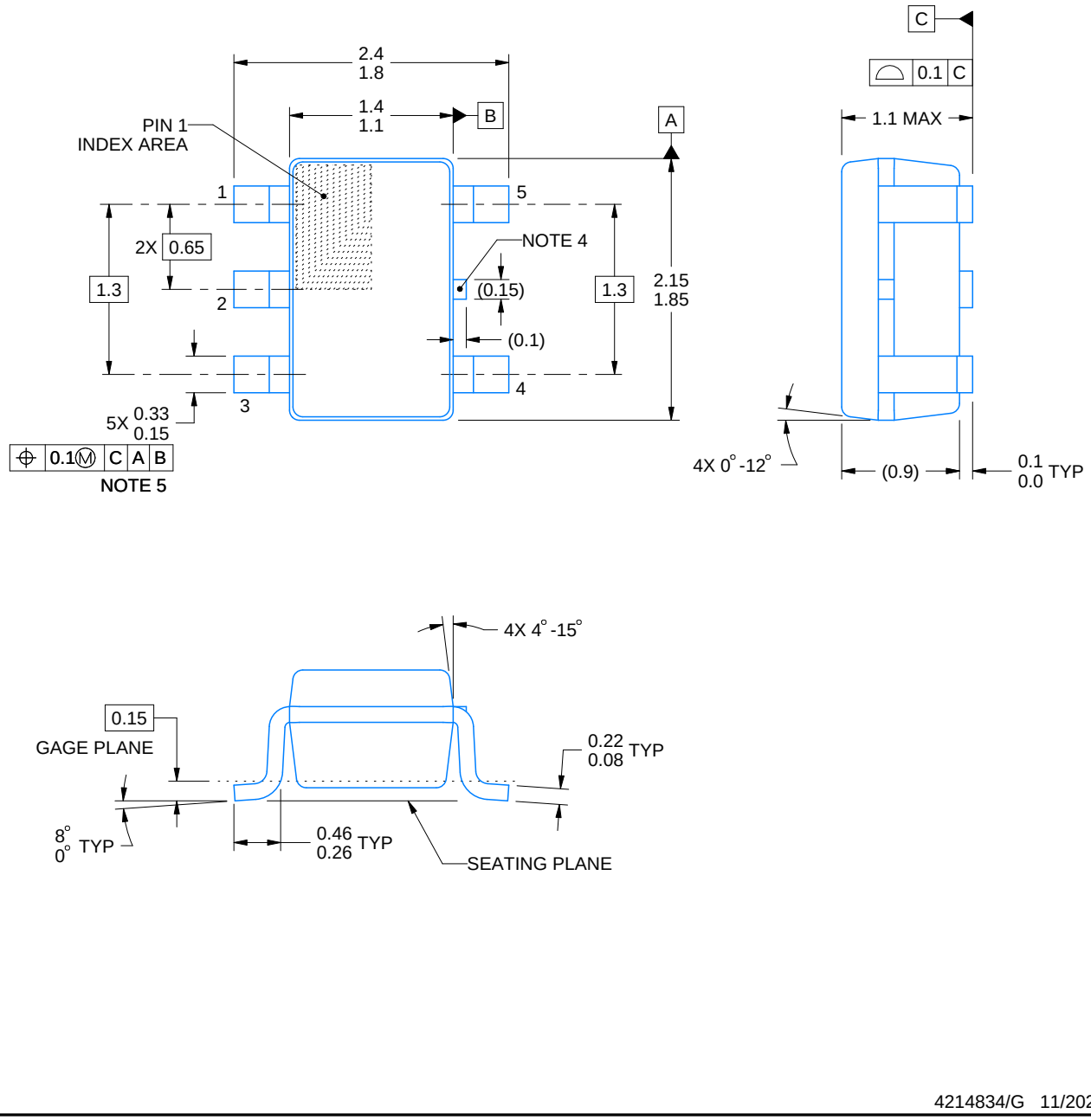
NanoFree is a trademark of Texas Instruments.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

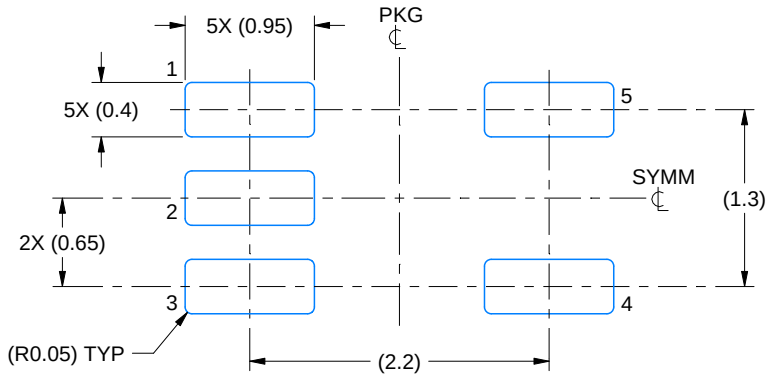
SMALL OUTLINE TRANSISTOR



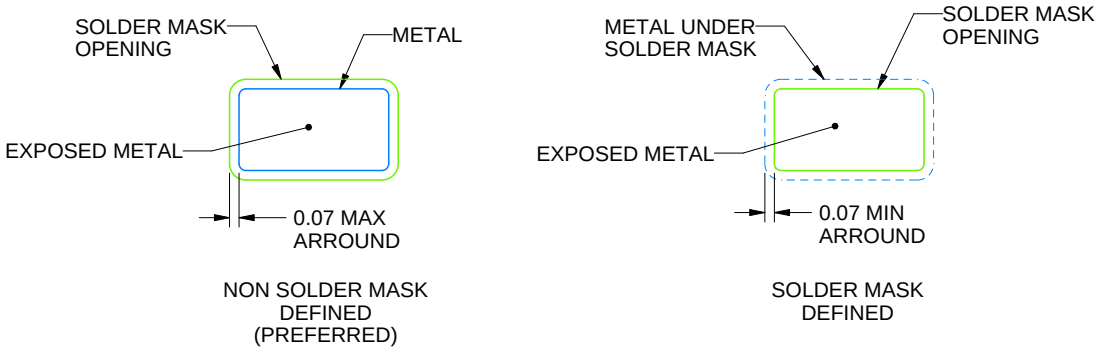
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

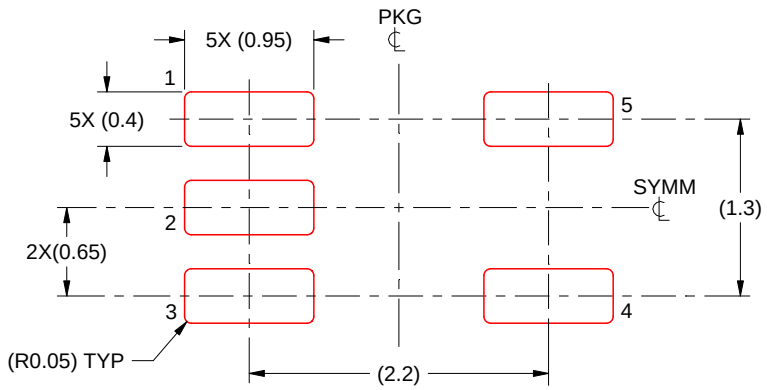


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



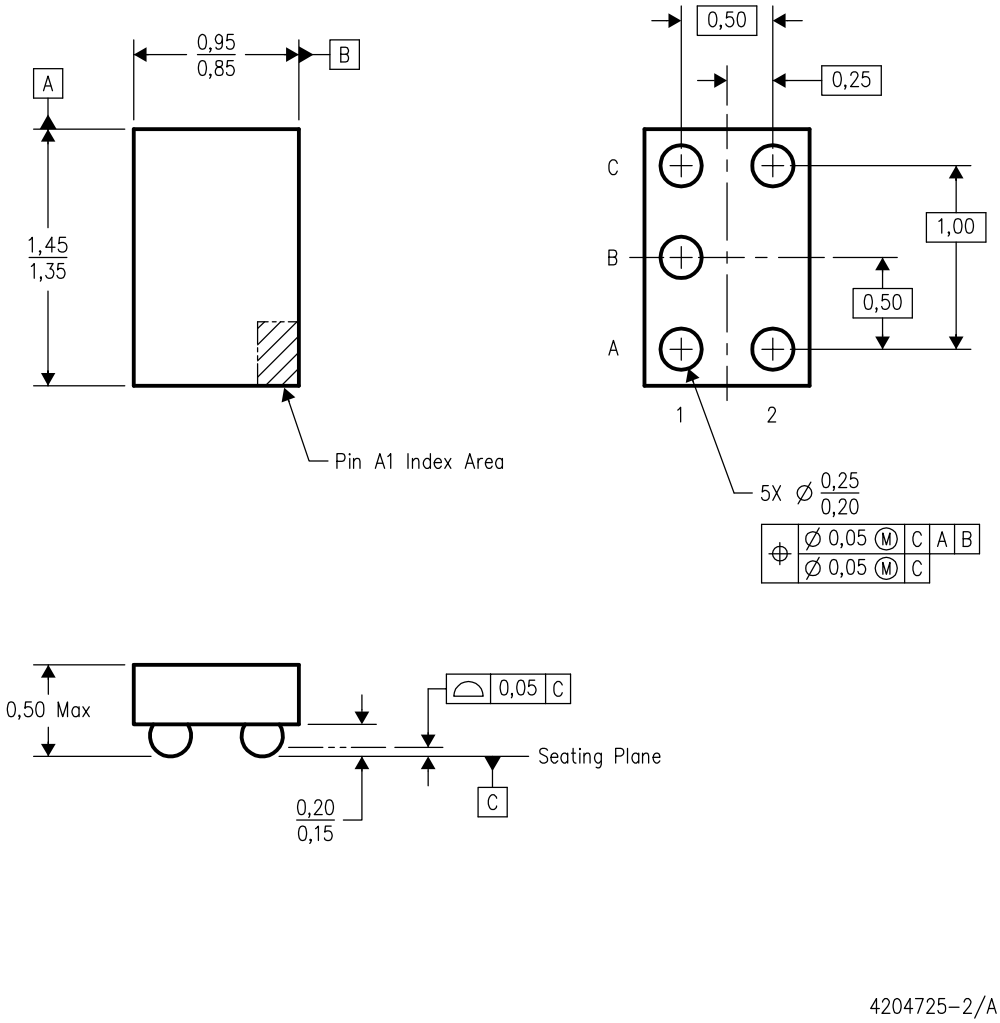
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

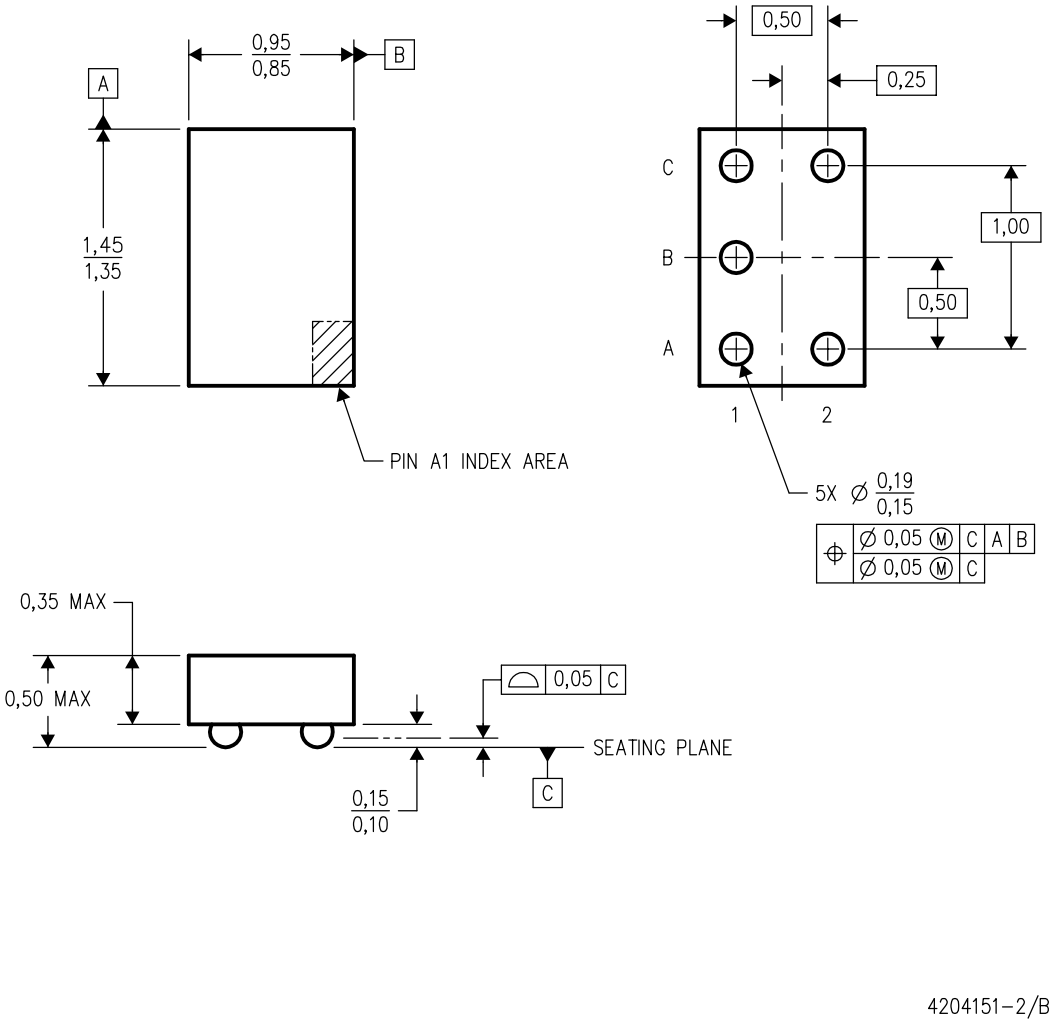
YEP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead–free.

NanoStar is a trademark of Texas Instruments.

YZA (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Package complies to JEDEC MO–211 variation EA.
E. This package is lead–free. Refer to the 5 YEA package (drawing 4203167) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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