SN74LVC1G17-Q1 Single Schmitt-Trigger Buffer

1 Features

- Qualified for automotive applications
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Maximum t_{pd} of 8ns at 3.3V
- Low power consumption, 20µA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- ESD protection exceeds JEDEC JS-001
  - 2000V human-body model
  - 1000V charged-device model

2 Applications

- AV receiver
- Audio dock: portable
- Blu-ray player and home theater
- MP3 player/recorder
- Personal Digital Assistant (PDA)
- Power: telecom/server AC/DC supply: single controller: analog and digital
- Solid State Drive (SSD): client and enterprise
- TV: LCD/digital and high-definition (HDTV)
- Tablet: enterprise
- Video analytics: server
- Wireless headset, keyboard, and mouse

3 Description

This single Schmitt-trigger buffer is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G17-Q1 device contains one buffer and performs the Boolean function Y = A.

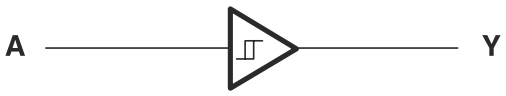
The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The SN74LVC1G17-Q1 is available in a variety of packages.

Package Information

DEVICE NAME	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN74LVC1G17-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC-70, 5)	2.0mm × 2.1mm	2.0mm × 1.25mm
	DRY (USON, 6)	1.45mm × 1.0mm	1.45mm × 1.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

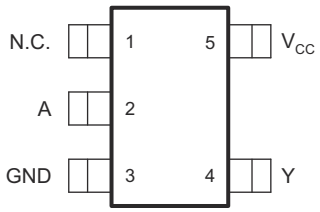


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

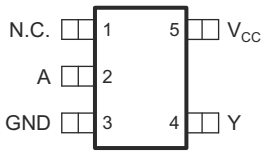
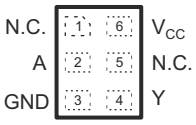


Figure 4-2. DCK Package 5-Pin SC-70 Top View



1. N.C. - No internal connection

See mechanical drawings for at the end of the data sheet for dimensions

Figure 4-3. DRY Package 6-Pin SON Transparent Top View

Table 4-1. Pin Functions

PIN			DESCRIPTION
NAME	DBV, DCK	DRY	
NC	1	1, 5	Not connected
A	2	2	Input
GND	3	3	Ground
Y	4	4	Output
V_{CC}	5	6	Power terminal

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

See (1).

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		–4	mA
		V_{CC} = 2.3V		–8	
		V_{CC} = 3V		–16	
				–24	
		V_{CC} = 4.5V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI *Implications of Slow or Floating CMOS Inputs* application note.

5.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G17-Q1			UNIT
		DBV	DCK	DRY	
		5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	357.1	371.0	608	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	263.7	297.5	432	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	264.4	258.6	446	°C/W
ψ_{JT}	Junction-to-top characterization parameter	195.6	195.6	191	°C/W
ψ_{JB}	Junction-to-board characterization parameter	262.2	256.2	442	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	198	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+} (Positive-going input threshold voltage)		1.65V	0.64		1.25	V
		2.3V	1		1.68	
		3V	1.36		2.04	
		4.5V	2.07		2.86	
		5.5V	2.53		3.43	
V_{T-} (Negative-going input threshold voltage)		1.65V	0.23		0.71	V
		2.3V	0.44		1.05	
		3V	0.77		1.35	
		4.5V	1.22		2.09	
		5.5V	1.73		2.52	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		1.65V	0.26		0.74	V
		2.3V	0.33		0.92	
		3V	0.4		0.99	
		4.5V	0.45		1.28	
		5.5V	0.56		1.32	
V_{OH}	I_{OH} = –100µA	1.65V to 5.5V	V_{CC} – 0.1			V
	I_{OH} = –4mA	1.65V	1.2			
	I_{OH} = –8mA	2.3V	1.9			
	I_{OH} = –16mA	3V	2.4			
	I_{OH} = –24mA		2.3			
	I_{OH} = –32mA	4.5V	3.8			
V_{OL}	I_{OL} = 100µA	1.65V to 5.5V			0.1	V
	I_{OL} = 4mA	1.65V			0.45	
	I_{OL} = 8mA	2.3V			0.4	
	I_{OL} = 16mA	3V			0.5	
	I_{OL} = 24mA				0.7	
	I_{OL} = 32mA	4.5V			0.7	
I_I A input	V_I = 5.5V or GND	0 to 5.5V			±10	µA
I_{off}	V_I or V_O = 5.5V	0			±25	µA
I_{CC}	V_I = 5.5V or GND, I_O = 0	1.65V to 5.5V			20	µA
ΔI_{CC}	One input at V_{CC} – 0.6V, Other inputs at $V_{C\,C}$ or GND	3V to 5.5V			500	µA
C_I	V_I = V_{CC} or GND	3.3V		4.5		pF

5.6 Switching Characteristics AC Limit

over recommended operating free-air temperature range, C_L = 30pF or 50pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 125°C								UNIT
			V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2.8	14	1	9	1.5	8	0.7	7	ns

5.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10MHz	20	21	22	26	pF

5.8 Typical Characteristics

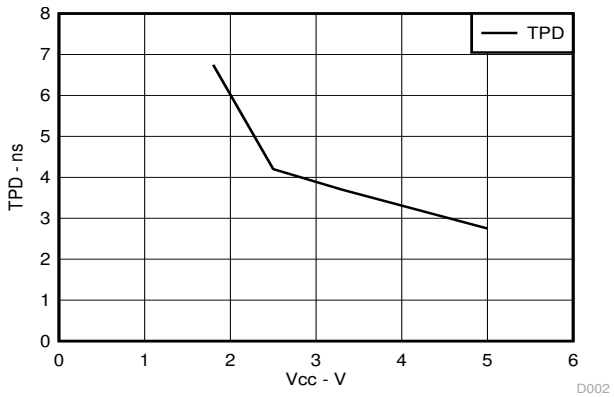
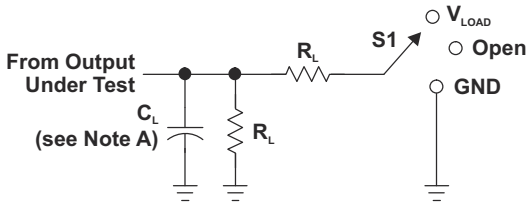


Figure 5-1. Across Vcc at 25°C

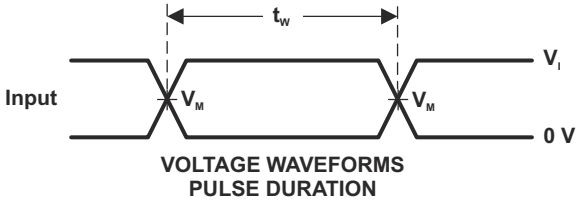
6 Parameter Measurement Information



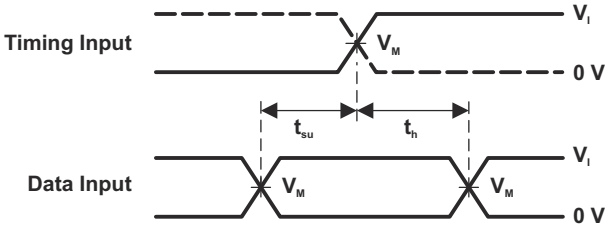
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

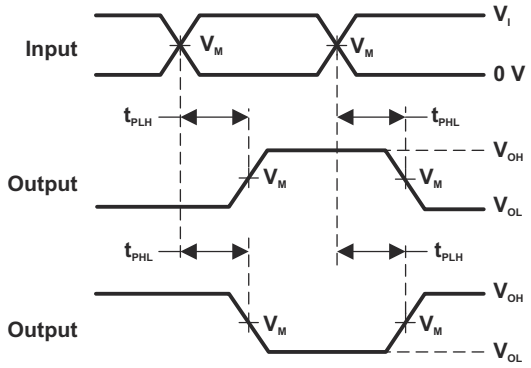
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



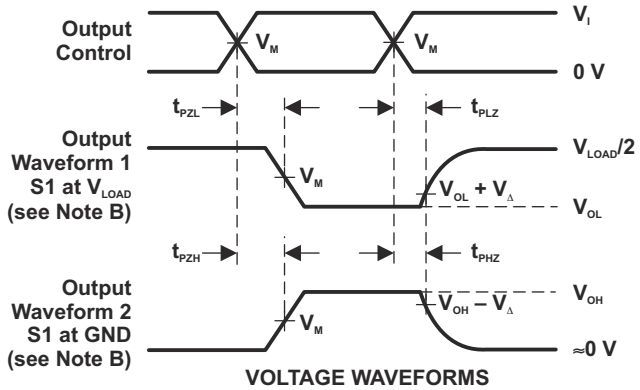
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

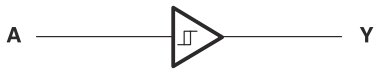
7 Detailed Description

7.1 Overview

The SN74LVC1G17-Q1 device contains one Schmitt trigger buffer and performs the Boolean function Y = A. The device functions as an independent buffer, but because of Schmitt action, it will have different input threshold levels for a positive-going (V_{T+}) and negative-going (V_{T-}) signals .

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram



7.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65V to 5.5V
- Allows down-voltage translation
- Inputs accept voltages to 5.5V
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0V

7.4 Device Functional Modes

Table 7-1. Function Table

INPUT A	OUTPUT Y
H	H
L	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G17-Q1 is a high-drive CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. It can produce 24mA of drive current at 3.3V making it Ideal for driving multiple outputs and good for high speed applications up to 100MHz. The inputs are 5.5V tolerant allowing it to translate down to V_{CC}.

8.2 Typical Application

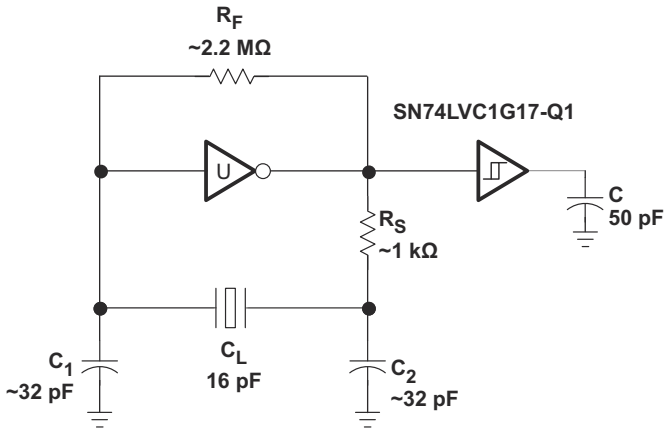


Figure 8-1. SN74LVC1G17-Q1 Typical Application

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See (Δt/ΔV) in the
   - *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the
   - *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the
   - *Recommended Operating Conditions* table at any valid V_{CC} .
2. Recommend Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed (continuous current through V_{CC} or GND) total current for the part. These limits are located in the
   - *Absolute Max Ratings* table.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

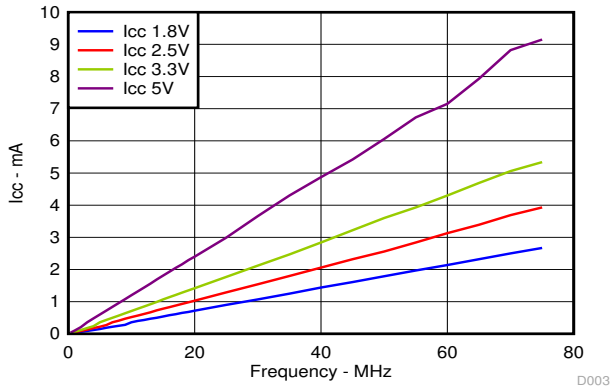


Figure 8-2. ICC vs Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

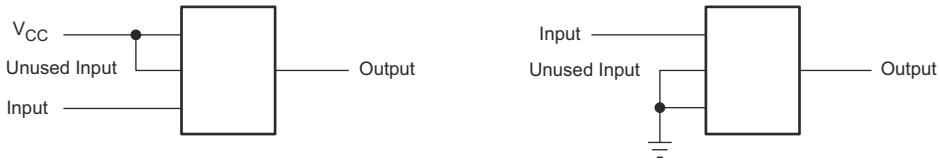
To prevent power disturbance, verify that each Vcc pin has a good bypass capacitor. For devices with a single supply a 0.1µF capacitor is recommended and if there are multiple Vcc pins then a 0.01µF or 0.022µF capacitor is recommended for each power pin. Parallel multiple bypass caps to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for the best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input terminals should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or Vcc whichever make more sense or is more convenient.

8.4.2 Layout Example



9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2025) to Revision E (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 280°C/W to: 371.0°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 66°C/W to: 297.5°C/W	5
• Changed Junction-to-board thermal resistance value for DCK package from: 67°C/W to: 258.6°C/W	5
• Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DCK package from: 66°C/W to: 256.2°C/W	5

Changes from Revision C (January 2020) to Revision D (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *Device Information* table to *Package Information*	1
• Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W	5
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W	5
• Changed Junction-to-board thermal resistance value for DBV package from: 62°C/W to: 264.4°C/W	5
• Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W	5
• Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC1G17QDBVRQ1G4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34W5, C17O)
74LVC1G17QDBVRQ1G4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34W5, C17O)
74LVC1G17QDBVRQ1G4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34W5, C17O)
SN74LVC1G17QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34W5, C17O)
SN74LVC1G17QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34W5, C17O)
SN74LVC1G17QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(34W5, C17O)
SN74LVC1G17QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C7J, C7O)
SN74LVC1G17QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C7J, C7O)
SN74LVC1G17QDCKRQ1.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C7J, C7O)
SN74LVC1G17QDRYRQ1	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HM
SN74LVC1G17QDRYRQ1.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC1G17-Q1 :

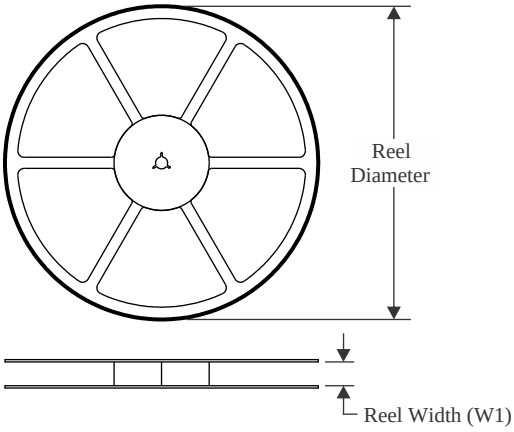
- Catalog : SN74LVC1G17
- Enhanced Product : SN74LVC1G17-EP

NOTE: Qualified Version Definitions:

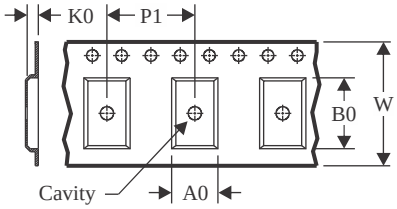
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

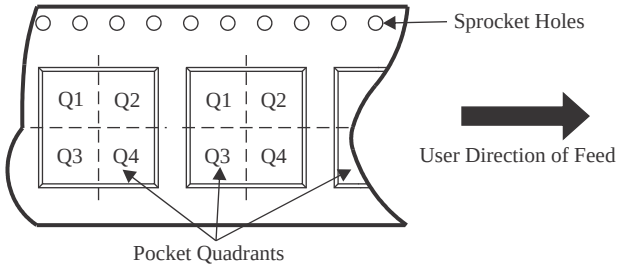


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

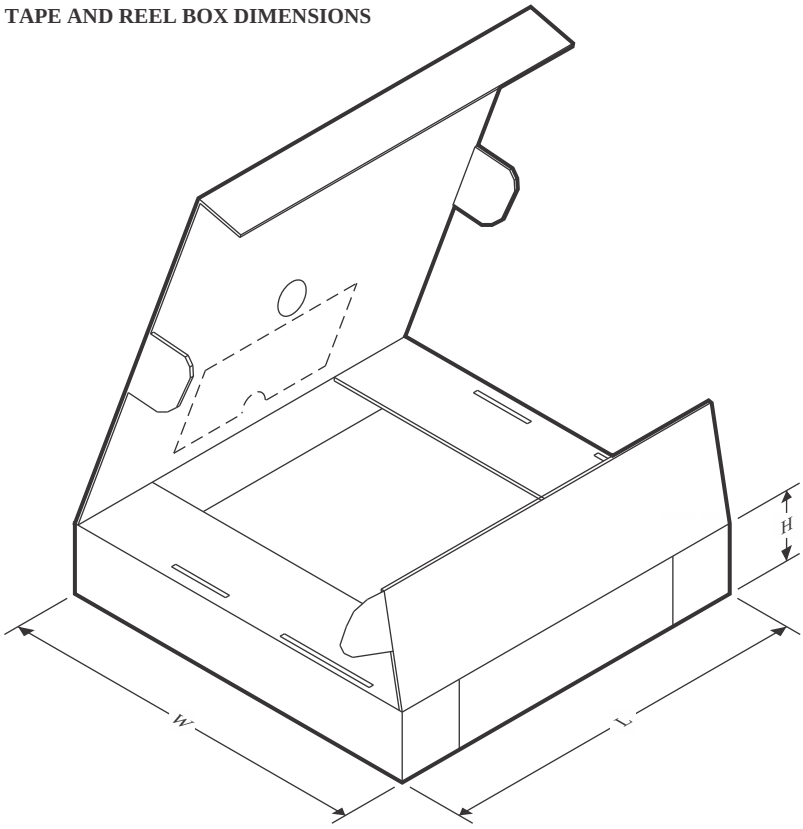
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G17QDBVRQ1G4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
74LVC1G17QDBVRQ1G4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G17QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

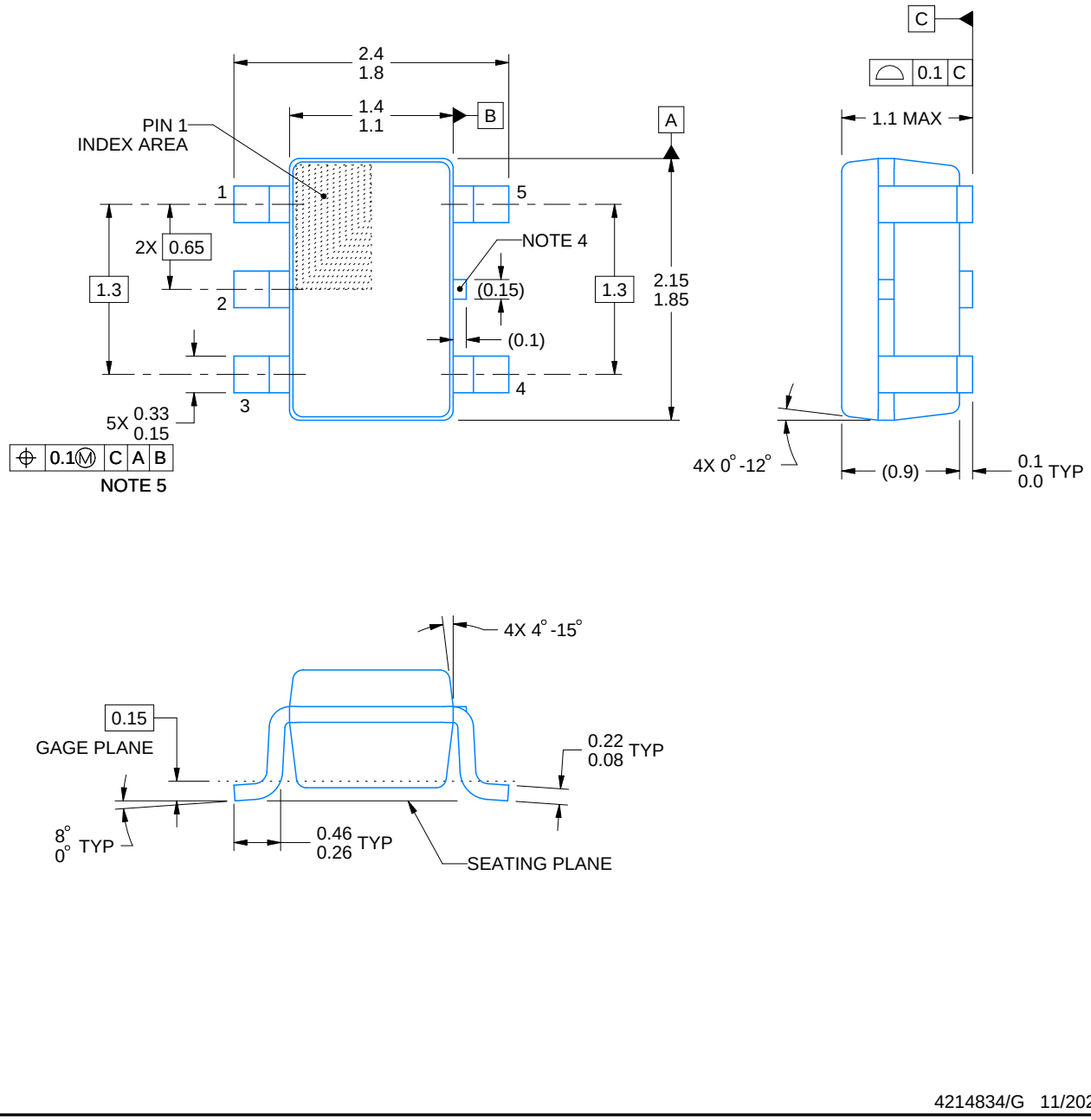
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G17QDBVRQ1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
74LVC1G17QDBVRQ1G4	SOT-23	DBV	5	3000	200.0	183.0	25.0
SN74LVC1G17QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G17QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
SN74LVC1G17QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

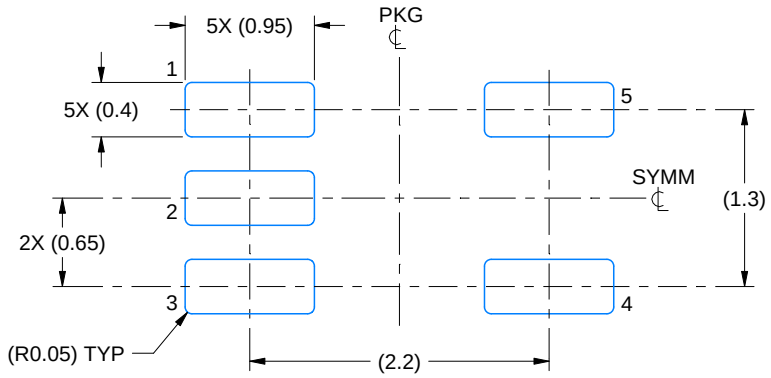
SMALL OUTLINE TRANSISTOR



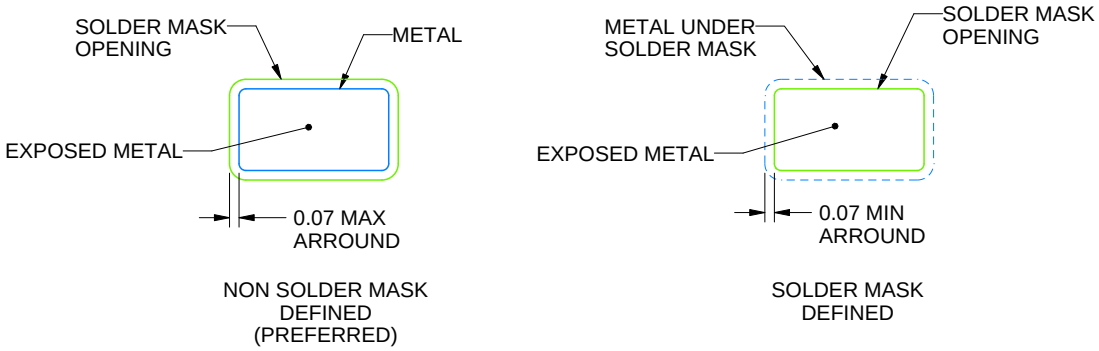
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

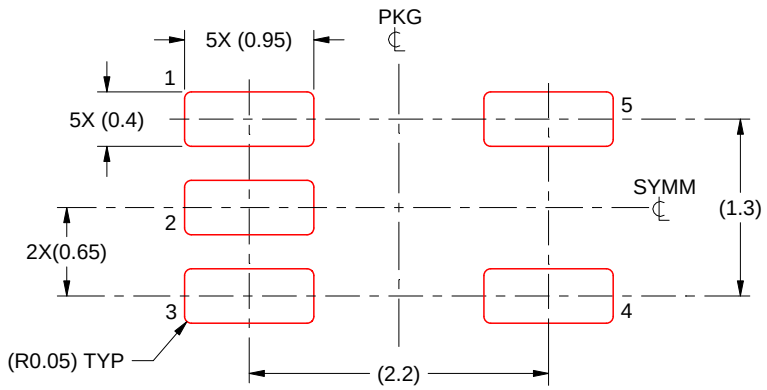


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

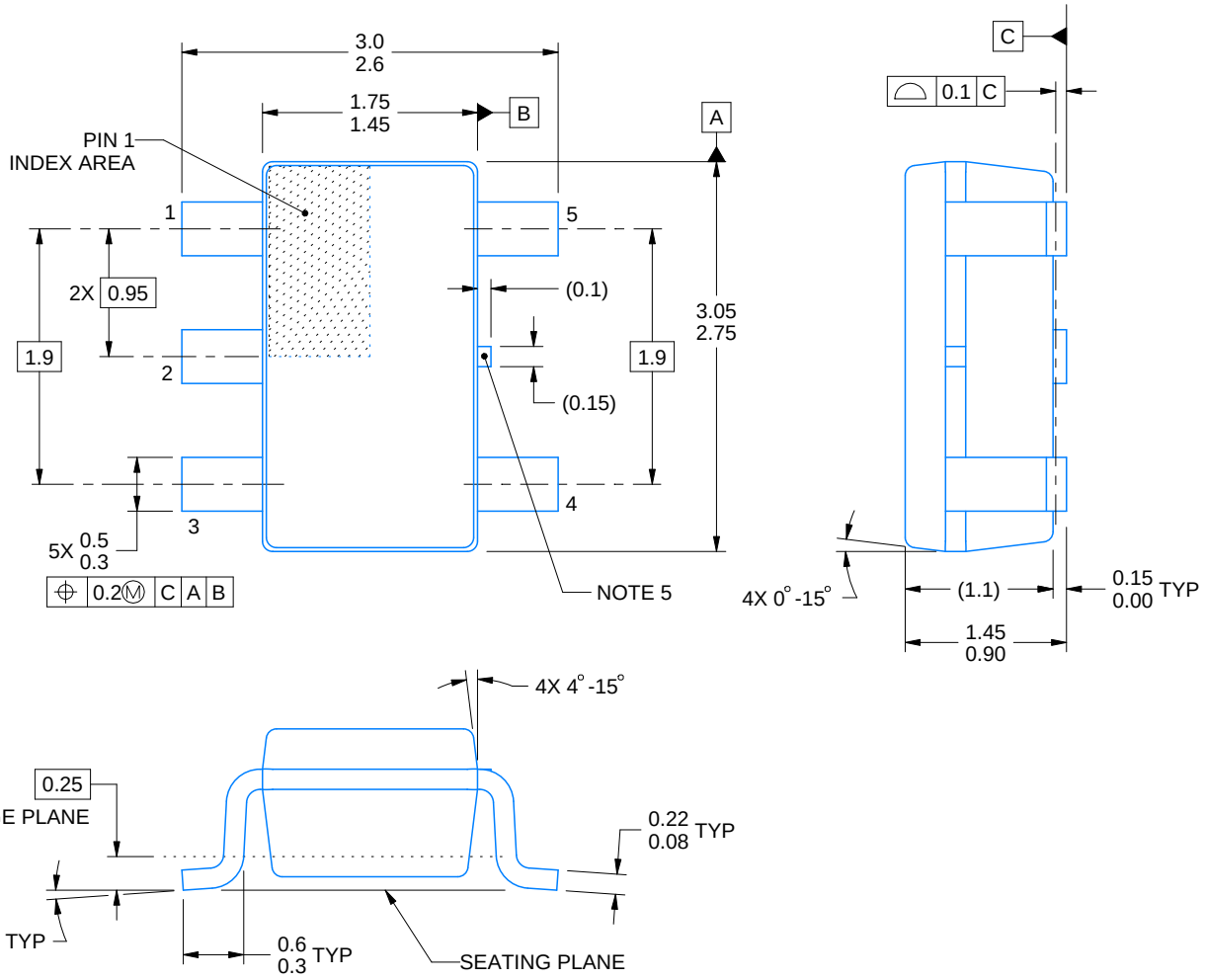
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

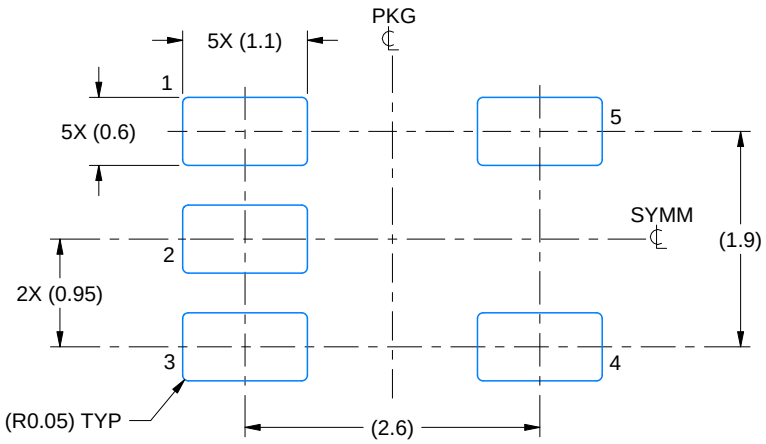
SMALL OUTLINE TRANSISTOR



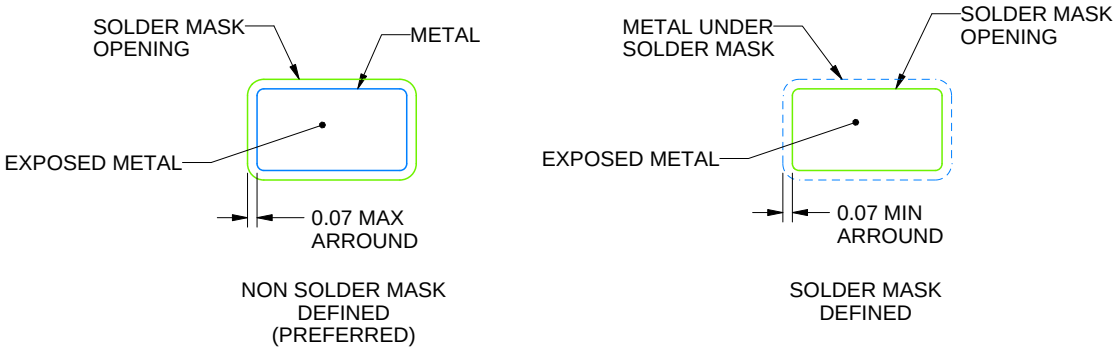
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

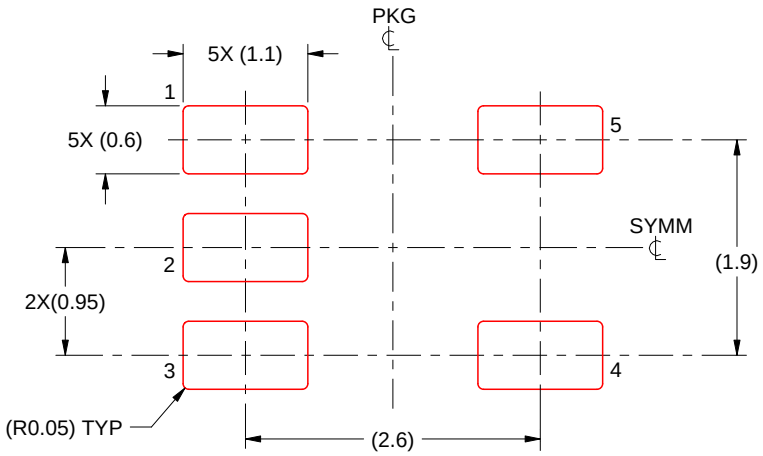


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

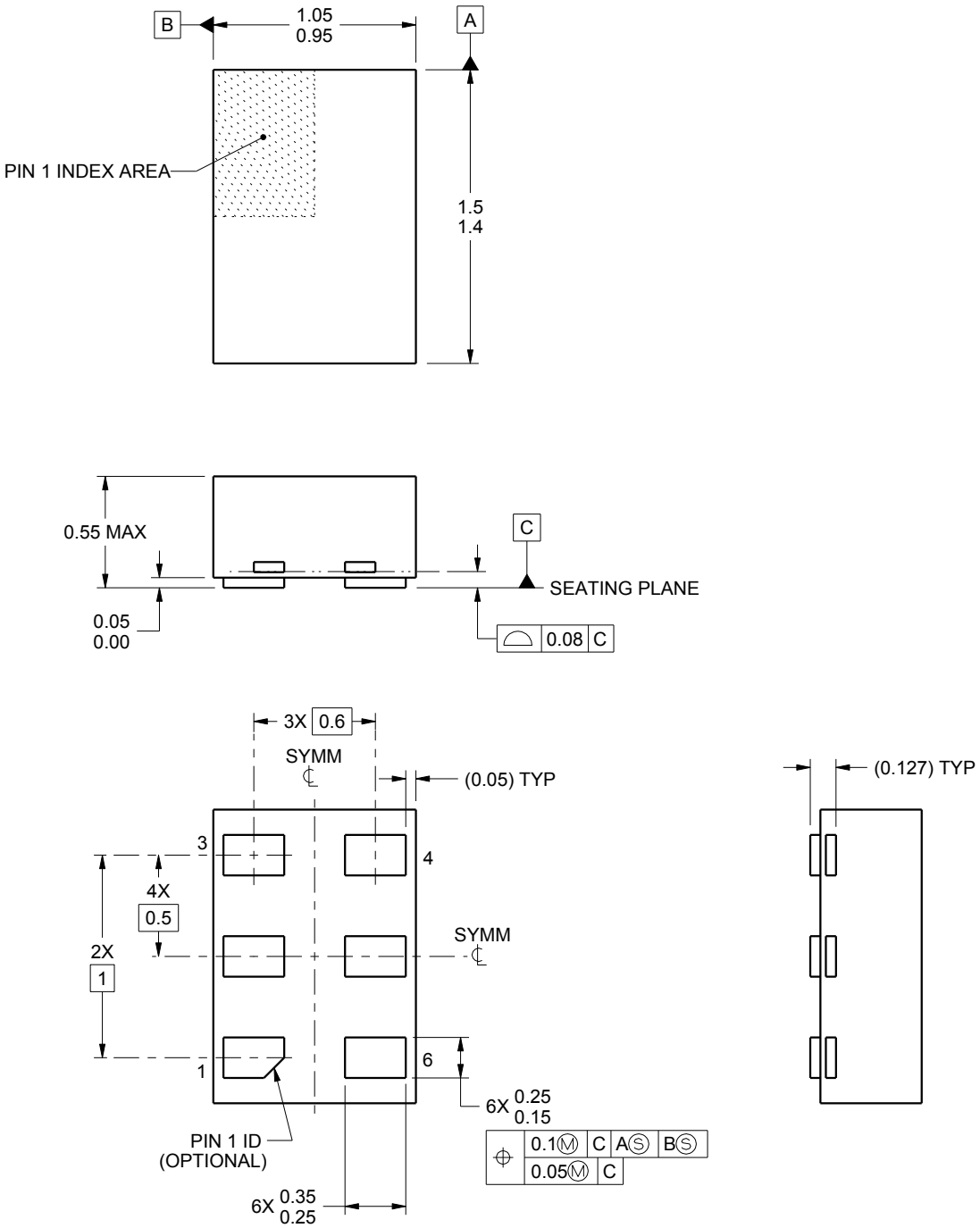
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRY0006B

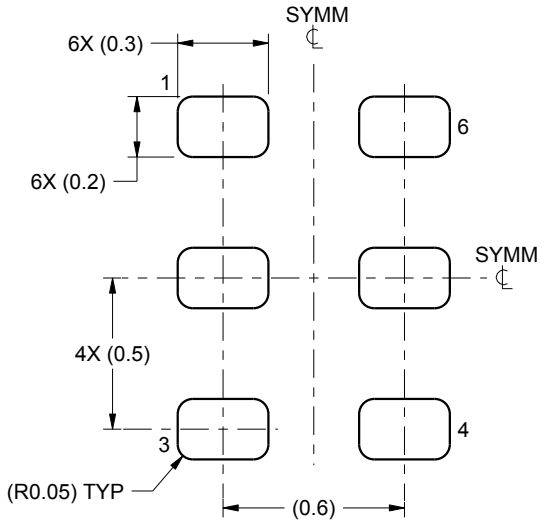
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

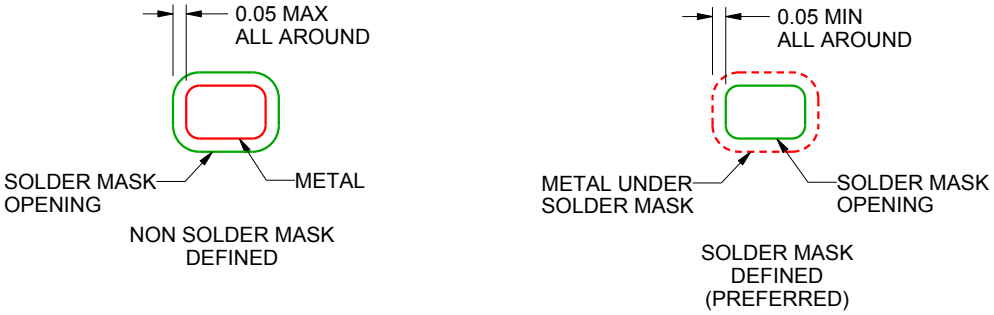


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

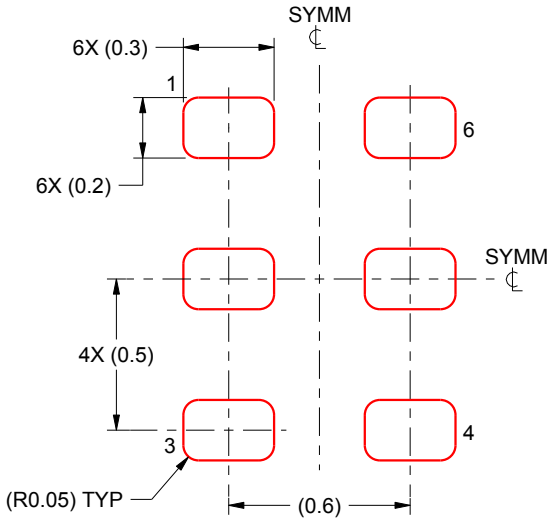
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025