SN74LVC1G19 1-of-2 Decoder and Demultiplexer

1 Features

- Available in the Texas Instruments NanoFree™ package
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Supports down translation to V_{CC}
- Maximum t_{pd} of 4ns at 3.3V
- Low power consumption, 10µA maximum I_{CC}
- ±24mA output drive at 3.3V
- V_{OLP} (output ground bounce) <0.8V typical at V_{CC} = 3.3V, T_A = 25°C
- V_{OHV} (output V_{OH} undershoot) >2V typical at V_{CC} = 3.3V, T_A = 25°C
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- AV receivers
- Audio docks: portable
- Blu-ray® players and home theater
- MP3 players/recorders
- Personal digital assistants (PDAs)
- Power: telecom/server AC/DC supply: single controller: analog and digital
- Solid state drives (SSDs): client and enterprise
- TVs: LCD/digital and high-definition (HDTVs)
- Tablets: enterprise
- Video analytics: server
- Wireless headsets, keyboards, and mice

3 Description

This decoder and demultiplexer is designed for 1.65V to 5.5V V_{CC} operation.

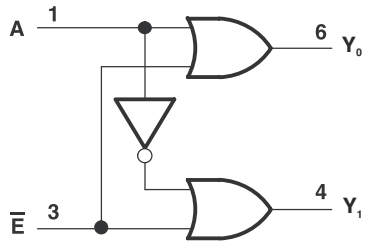
The SN74LVC1G19 device is a 1-of-2 decoder and demultiplexer. When $\overline{E}$ input is high, the decoder is disabled and both outputs are high. When $\overline{E}$ input is low, the A input selects which output is low.

This device is designed for partial-power-down applications using I_{off}.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74LVC1G19DBV	SOT-23 (6)	2.9mm × 1.6mm
SN74LVC1G19DCK	SC70 (6)	2.0mm × 1.25mm
SN74LVC1G19DRL	SOT (6)	1.6mm × 1.2mm
SN74LVC1G19DRY	SON (6)	1.45mm × 1.0mm
SN74LVC1G19YZP	DSBGA (6)	1.41mm × 0.91mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

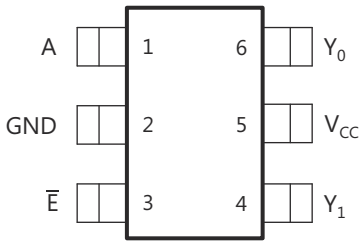


Figure 4-1. DBV Package 6-Pin SOT-23 Top View

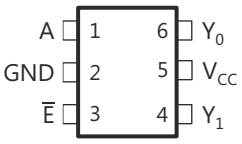


Figure 4-2. DRL Package 6-Pin SOT Top View

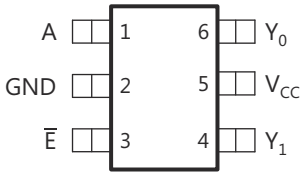


Figure 4-3. DCK Package 6-Pin SC70 Top View

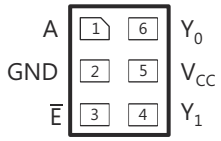


Figure 4-4. DRY Package 6-Pin SON Top View

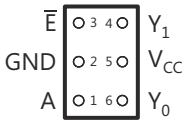


Figure 4-5. YZP Package 6-Pin DSBGA Bottom View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Address input, selects which output goes low.
$\overline{E}$	3	I	Enable input, active low
GND	2	—	Ground
V_{CC}	5	—	Power pin
Y_0	6	O	Output 0, low when selected by A low and $\overline{E}$ low
Y_1	4	O	Output 1, low when selected by A high and $\overline{E}$ low

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 1.95V	0.65 × V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3V to 3.6V	2		
		V_{CC} = 4.5V to 5.5V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65V to 1.95V		0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3V to 3.6V		0.8	
		V_{CC} = 4.5V to 5.5V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		–4	mA
		V_{CC} = 2.3V		–8	
		V_{CC} = 3V		–16	
				–24	
		V_{CC} = 4.5V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		5	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23, 6)	6	225.5	155.0	138.2	84.2	137.9	-	°C/W
DCK (SOT-SC70, 6)	6	254.1	191.3	158.1	92.5	158.0	-	°C/W
YZP (DSBGA, 6)	6	123	-	-	-	-	-	°C/W
DRY (SON, 6)	6	234	-	-	-	-	-	°C/W
DRL (SOT, 6)	6	142	-	-	-	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	I_{OH} = –100 µA	1.65V to 5.5V	V_{CC} – 0.1			V
	I_{OH} = –4mA	1.65V	1.2			
	I_{OH} = –8mA	2.3V	1.9			
	I_{OH} = –16mA	3V	2.4			
	I_{OH} = –24mA		2.3			
	I_{OH} = –32mA	4.5V	3.8			
V_{OL}	I_{OL} = 100 µA	1.65V to 5.5V			0.1	V
	I_{OL} = 4mA	1.65V			0.45	
	I_{OL} = 8mA	2.3V			0.3	
	I_{OL} = 16mA	3V			0.4	
	I_{OL} = 24mA				0.55	
	I_{OL} = 32mA	4.5V			0.55	
I_I	V_I = 5.5V or GND	0 to 5.5V			±1	µA
I_{off}	V_I or V_O = 5.5V	0			±10	µA
I_{CC}	V_I = 5.5V or GND, I_O = 0	1.65V to 5.5V			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6V, Other inputs at V_{CC} or GND	3V to 5.5V			500	µA
C_I	V_I = V_{CC} or GND	3.3V		3.5		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Switching Characteristics, C_L = 15pF

over recommended operating free-air temperature range, C_L = 15pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or $\overline{E}$	Y	2.5	16.1	1.5	5.9	1	4	0.5	2.8	ns

5.7 Switching Characteristics, C_L = 30pF or 50pF

over recommended operating free-air temperature range, C_L = 30pF or 50pF (unless otherwise noted) (see Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8V ± 0.15V		V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or $\overline{E}$	Y	3.2	16.1	1.5	6.5	1.1	5.2	0.5	3.9	ns

5.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10MHz	15.5	16	16	18	pF

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5.9 Typical Characteristics

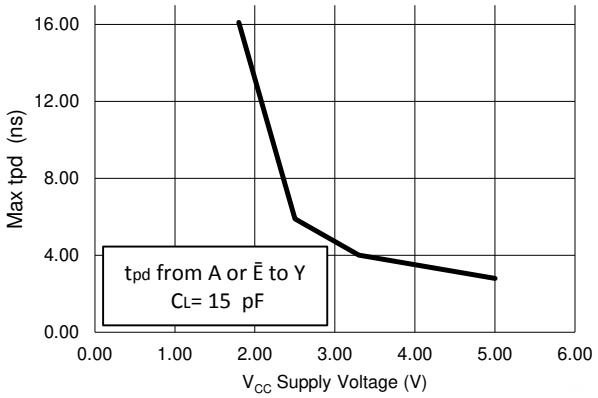


Figure 5-1. Time Propagation Delay vs V_{CC}, C_L= 15pF

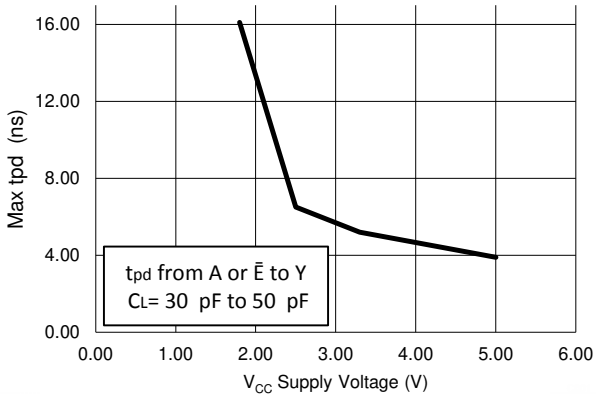
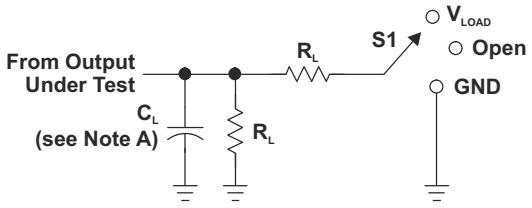


Figure 5-2. Time Propagation Delay vs V_{CC}, C_L= 30pF or 50pF

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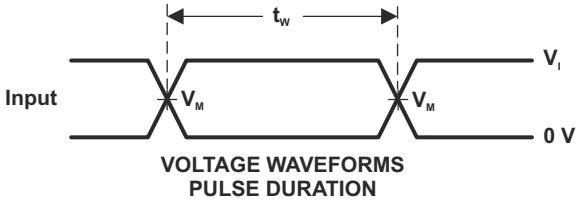
6 Parameter Measurement Information



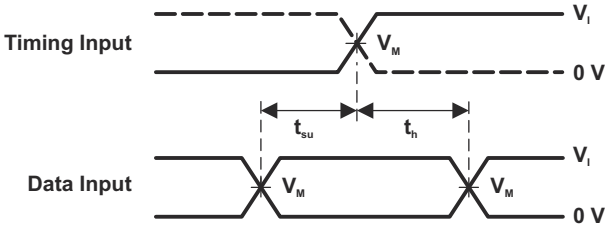
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

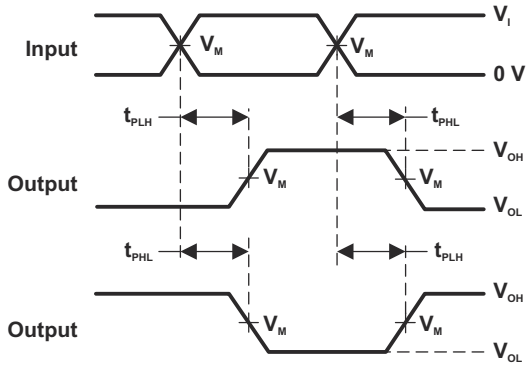
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



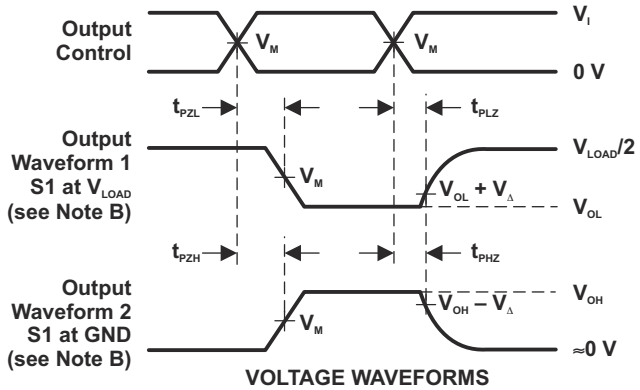
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

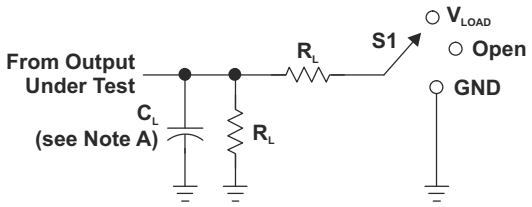


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

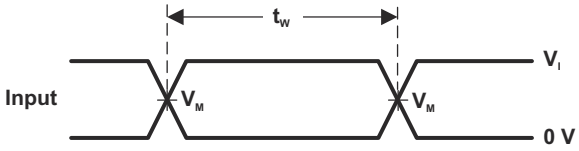
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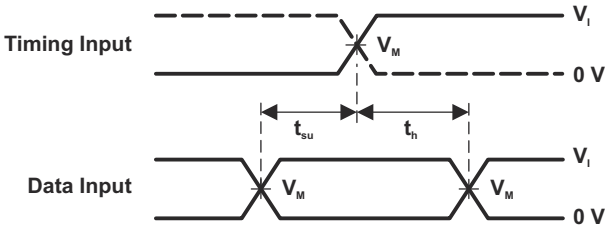
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

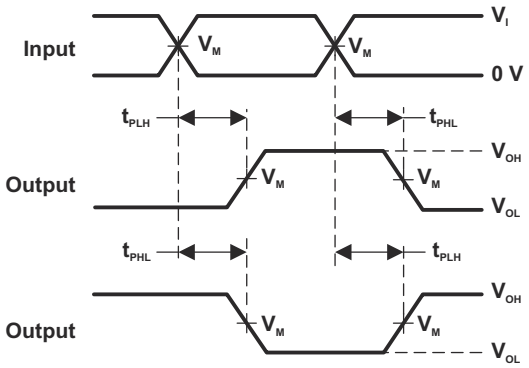
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



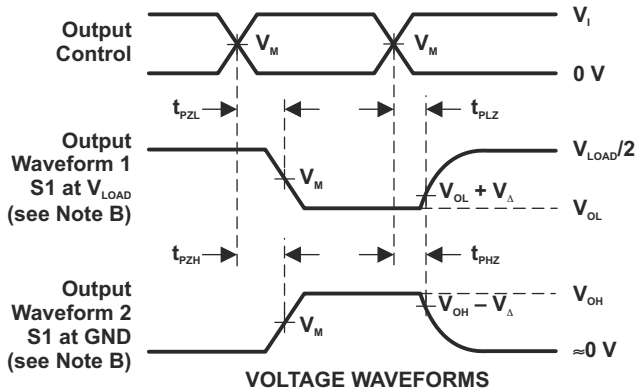
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
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NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

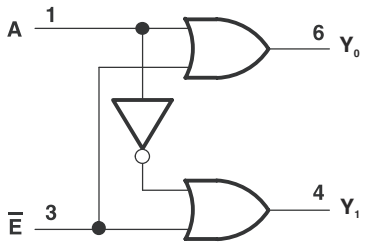
This decoder and demultiplexer is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G19 device is a 1-of-2 decoder and demultiplexer. This device decodes the 1-bit address on input A and places a logic low on the matching address output, Y_0 or Y_1, when the enable ($\overline{E}$) input signal is low.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

7.2 Functional Block Diagram



7.3 Feature Description

SN74LVC1G19 is available in NanoFree package. NanoFree is a major breakthrough in IC packaging concepts, it is a bare die package developed for applications that require the smallest possible package. The device supports 5V V_{CC} operation. All inputs accept voltages up to 5.5V. ±24mA output drive at 3.3V. The maximum time propagation delay (t_{pd}) is 5.4ns at 3.3V. The device has low-power consumption, with a 10µA maximum I_{CC}. There is typical output ground bounce (V_{OLP}) and output V_{OH} undershoot (V_{OHV}). This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature confirms that damaging current does not back flow through the device when the device is powered down. The SN74LVC1G19 device has isolation during power off. I_{off} supports live insertion, partial-power-down mode, and back drive protection.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVC1G19.

Table 7-1. Function Table

INPUTS		OUTPUTS	
$\overline{E}$	A	Y_0	Y_1
L	L	L	H
L	H	H	L
H	X	H	H

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G19 device is a 1-of-2 decoder and demultiplexer. This device decodes the 1 bit address on input A and places a logic low on the matching address output, Y_0 or Y_1, when the enable ($\overline{E}$) input signal is low. The device can produce 24mA of drive current at 3.3V making it appropriate for driving multiple outputs.

8.2 Typical Application

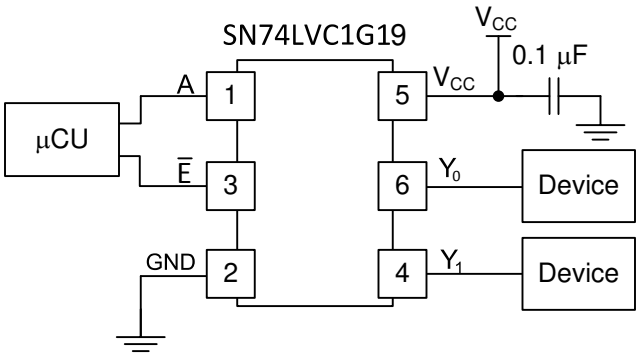


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that exceed maximum limits. Outputs can be combined to produce higher drive but the high drive also creates faster edges into light loads so routing and load conditions must be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see (Δt/ΔV) in *Recommended Operating Conditions* table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommend Output Conditions:
   - Load currents must not exceed 50mA per output and 100mA total for the part.
   - Series resistors on the output can be used if the user desires to slow the output edge signal or limit the output current.

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8.2.3 Application Curve

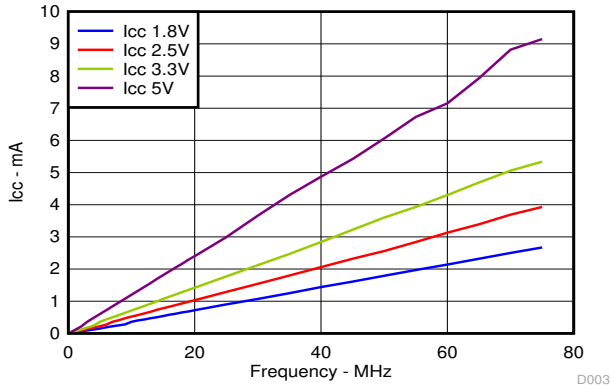


Figure 8-2. I_{CC} vs Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Absolute Maximum Ratings* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01µF or 0.022µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally the unused inputs are tied to GND or V_{CC}, whichever makes more sense or is more convenient.

8.4.2 Layout Example

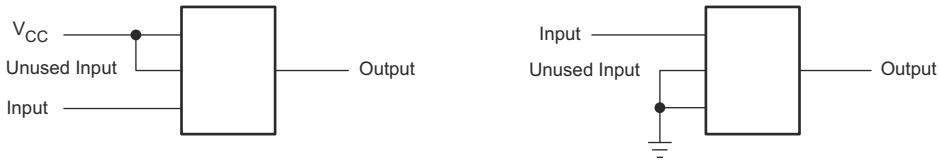


Figure 8-3. Layout Diagram

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9 Device and Documentation Support

9.1 Third-Party Products Disclaimer

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9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2014 to November 1, 2026 (from Revision G (February 2014) to Revision H (November 2026)) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Updated format for *Thermal Information* table.....5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 165°C/W to: 225.5°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 259°C/W to: 254.1°C/W.....5

Changes from Revision F (July 2012) to Revision G (February 2014) — **Page**

- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... 1
- Deleted *Ordering Information* table..... 1
- Updated I_{off} in *Features*..... 1

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G19DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(C195, C19R)
SN74LVC1G19DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(C195, C19R)
SN74LVC1G19DBVRE4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(C195, C19R)
SN74LVC1G19DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195, C19R)
SN74LVC1G19DBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195, C19R)
SN74LVC1G19DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(CY5, CYF, CYK, CYR)
SN74LVC1G19DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(CY5, CYF, CYK, CYR)
SN74LVC1G19DCKRE4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY5
SN74LVC1G19DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY5
SN74LVC1G19DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY5
SN74LVC1G19DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(1JZ, CY7, CYR)
SN74LVC1G19DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1JZ, CY7, CYR)
SN74LVC1G19DRLRG4	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1JZ, CY7, CYR)
SN74LVC1G19DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 85	CY
SN74LVC1G19DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY
SN74LVC1G19DRYRG4	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY
SN74LVC1G19DRYRG4.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY
SN74LVC1G19YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CY7, CYN)
SN74LVC1G19YZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CY7, CYN)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

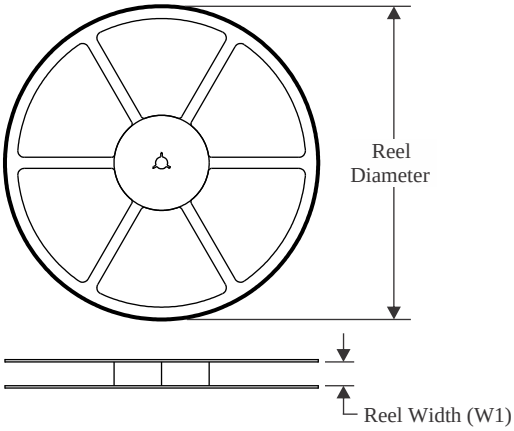
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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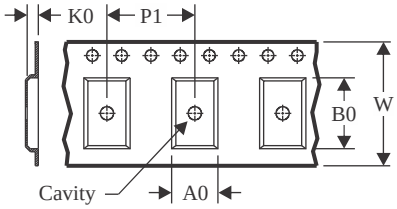
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

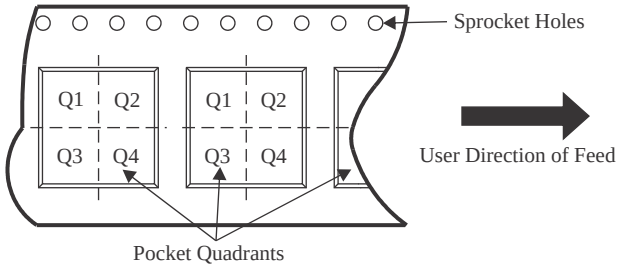


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

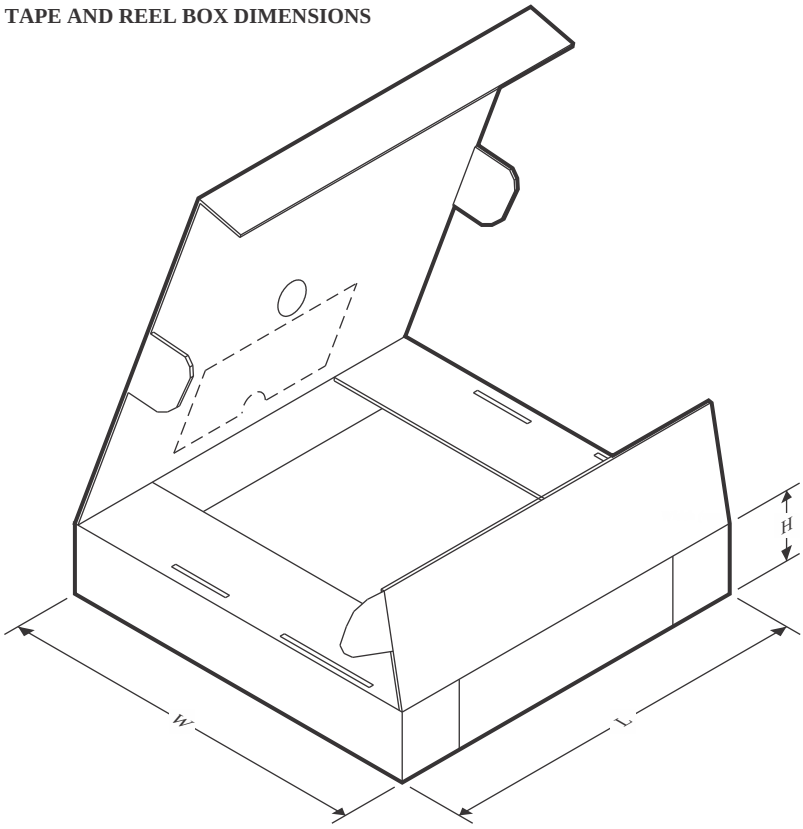


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G19DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G19DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G19DCKRG4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G19DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G19DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G19DRYR	SON	DRY	6	5000	180.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
SN74LVC1G19DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G19DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G19YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

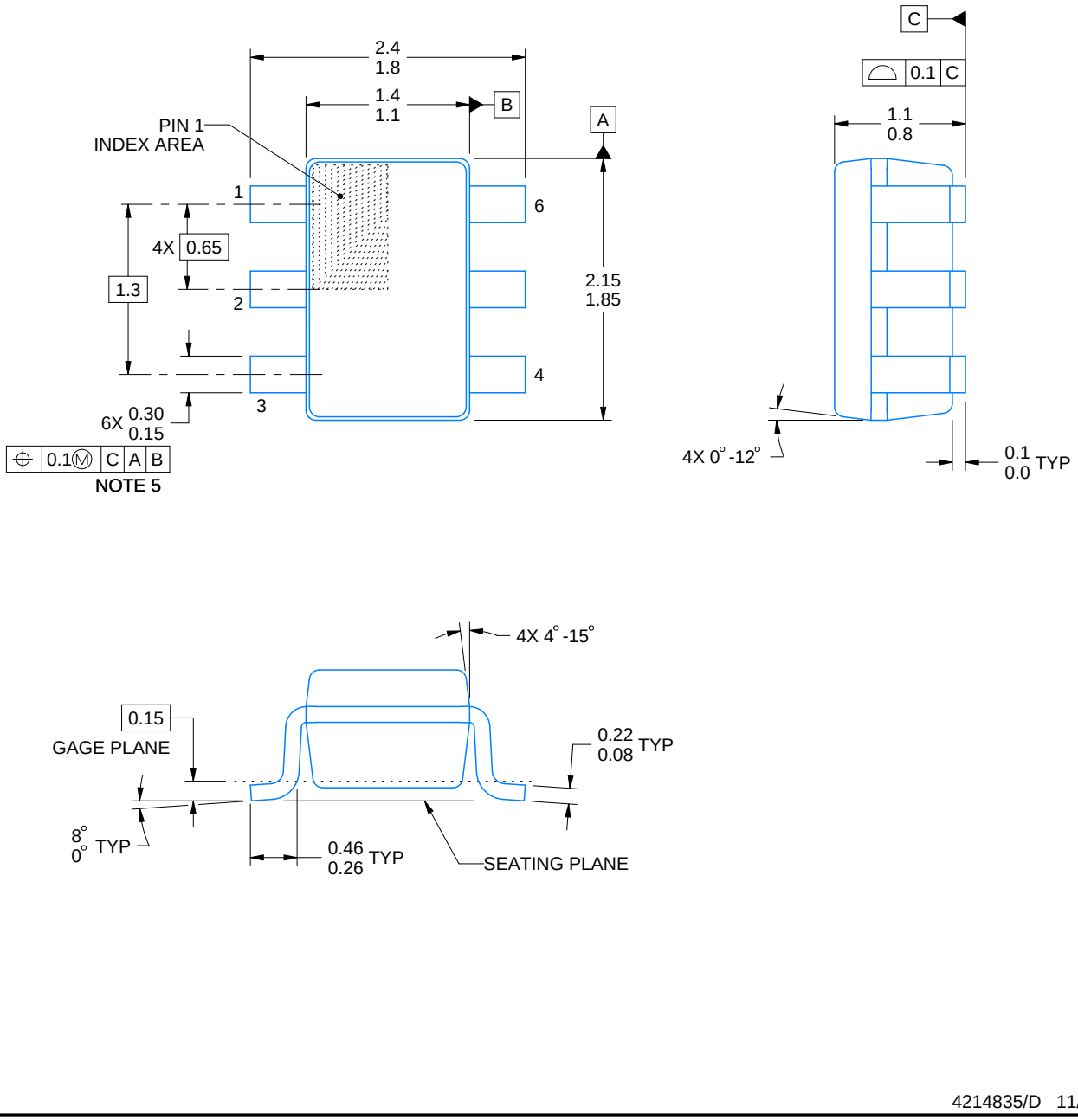
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G19DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC1G19DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G19DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G19DRYR	SON	DRY	6	5000	200.0	183.0	25.0
SN74LVC1G19DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G19DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G19YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

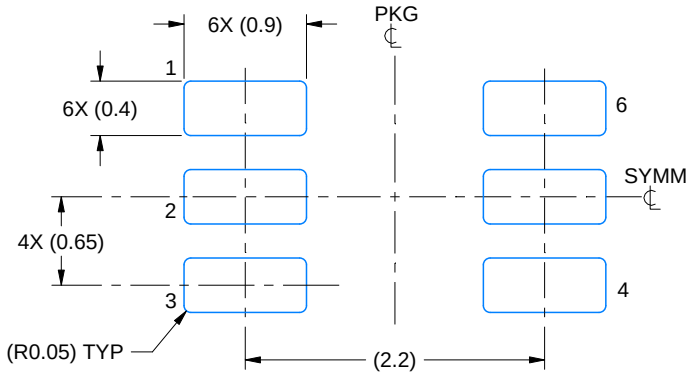
SMALL OUTLINE TRANSISTOR



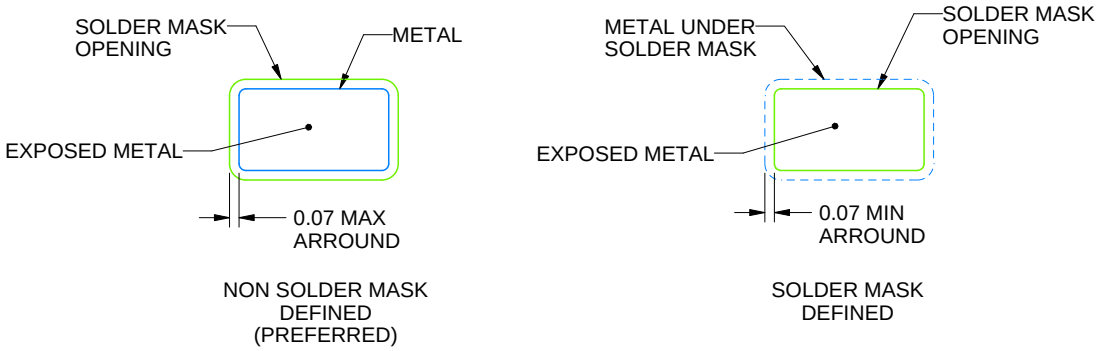
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

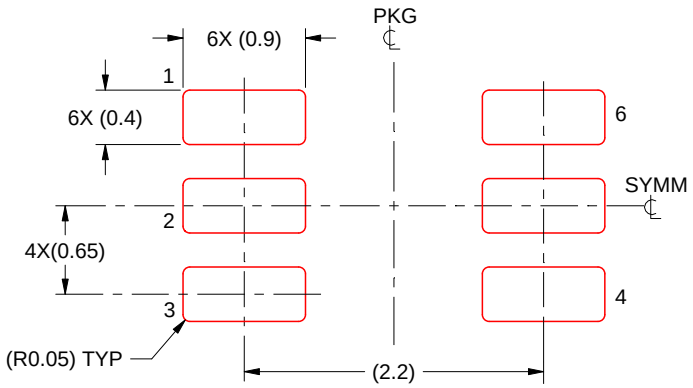


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

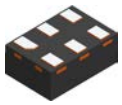
DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

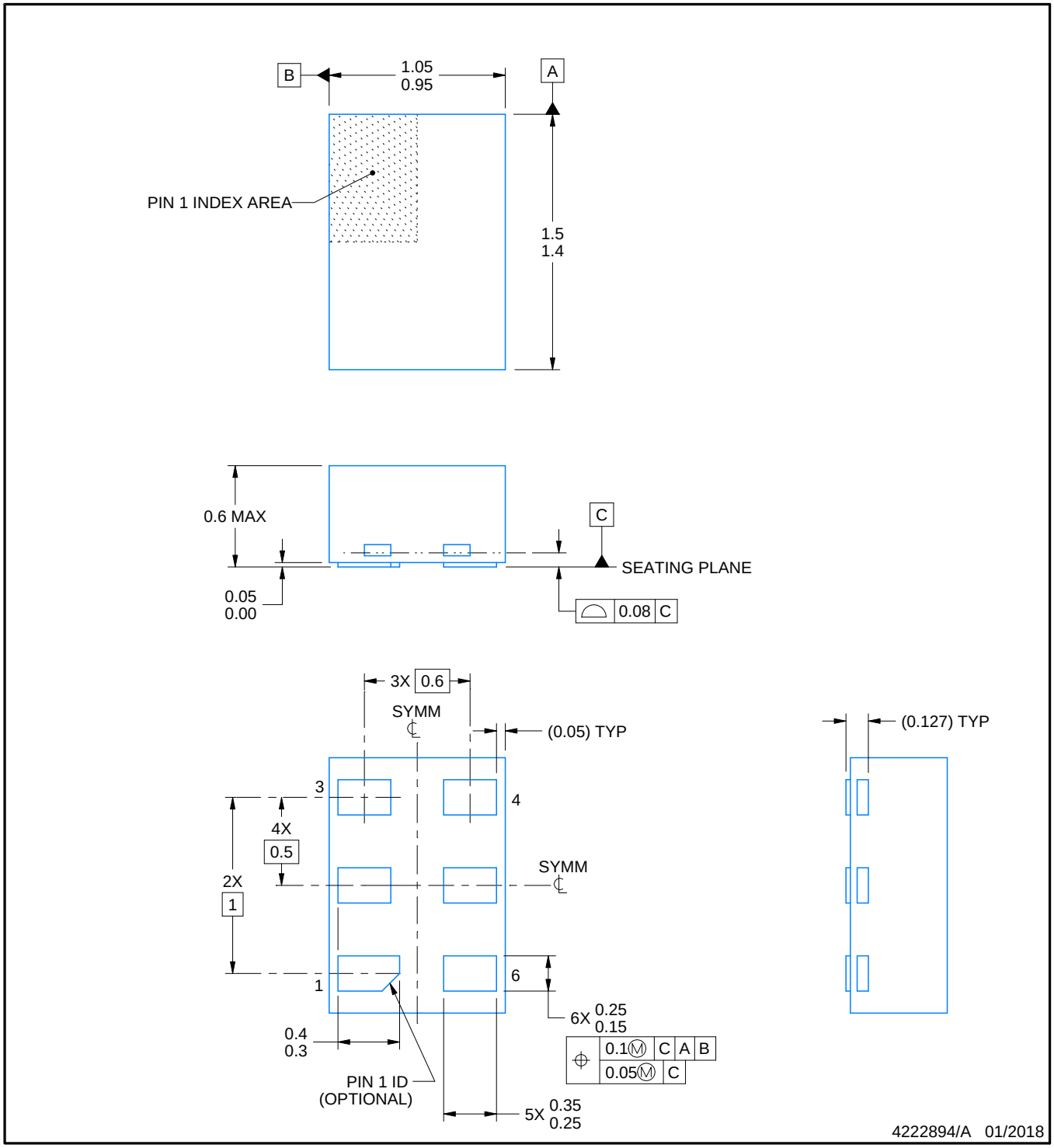
DRY0006A



PACKAGE OUTLINE

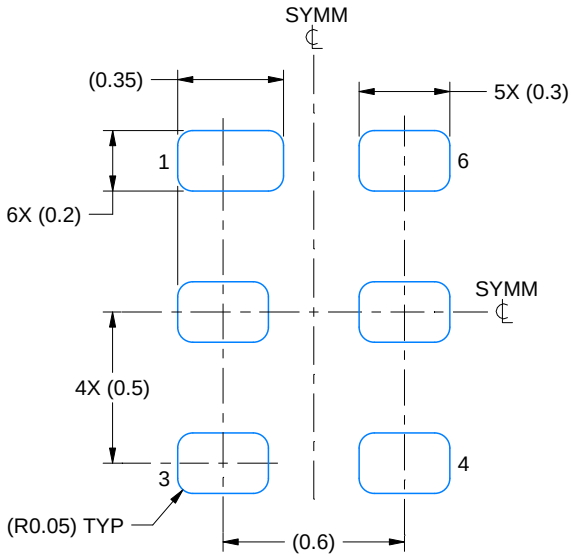
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

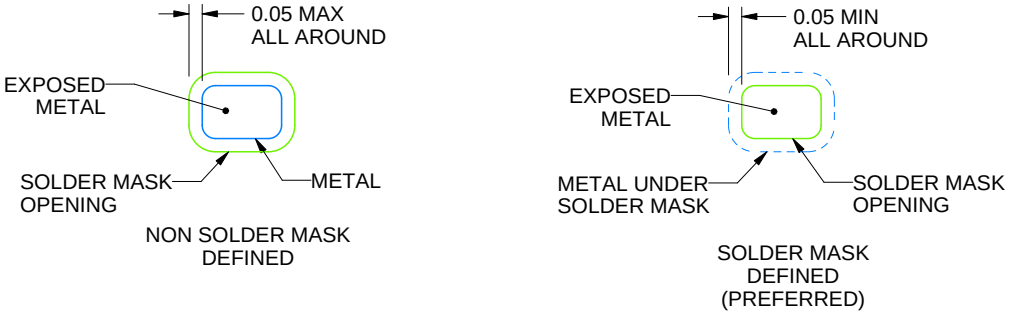


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

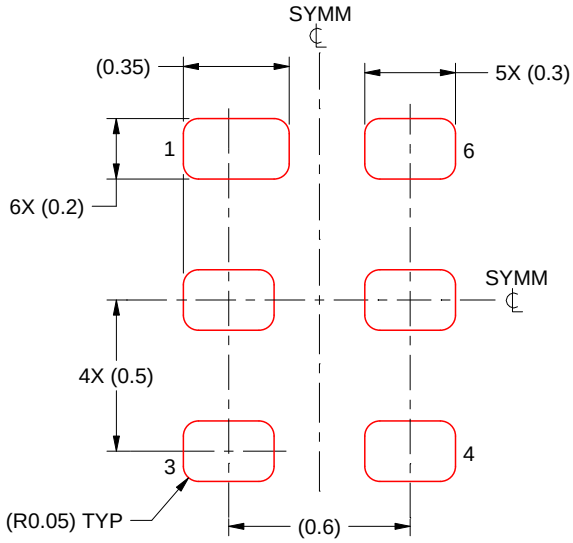
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

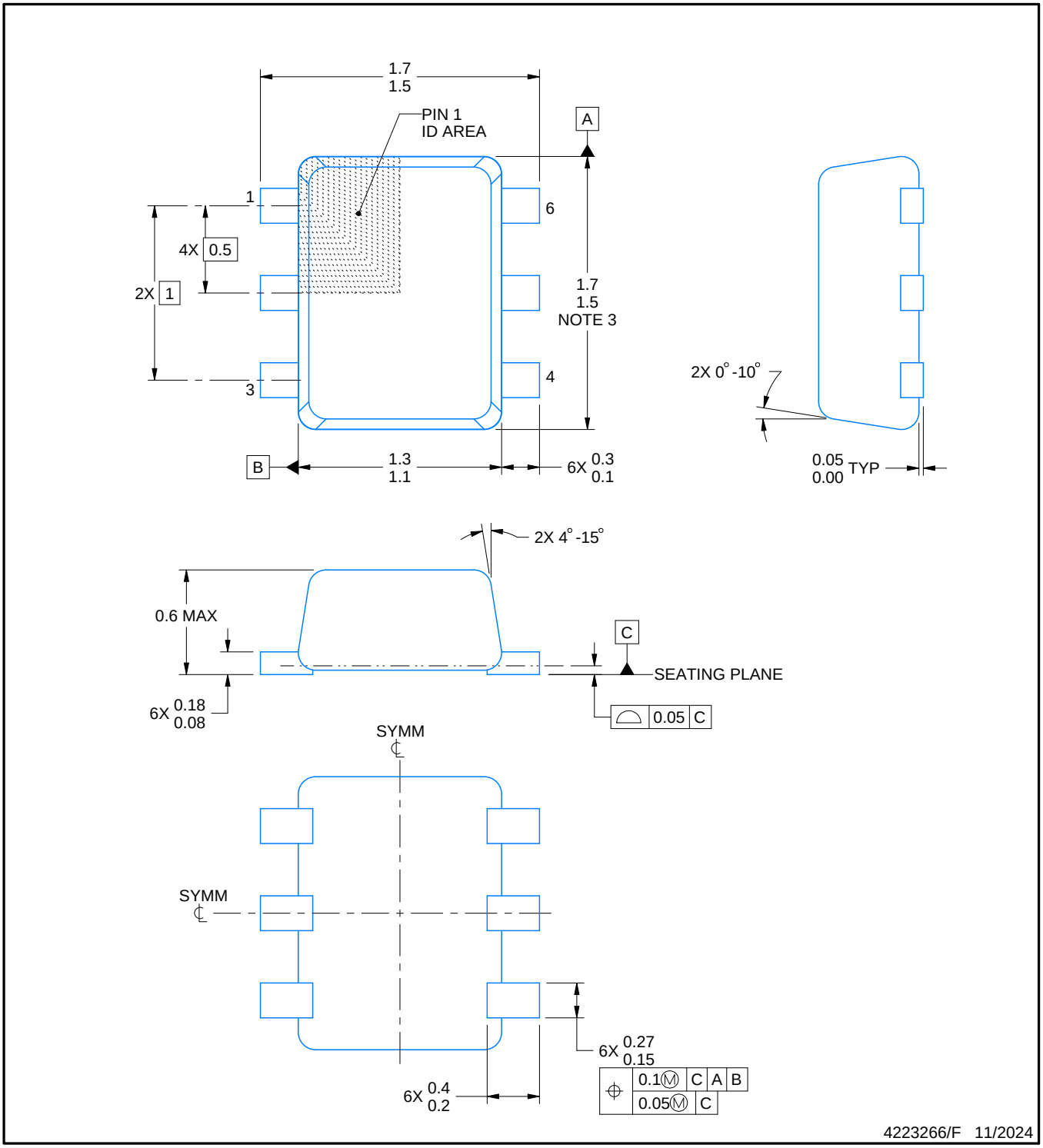


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

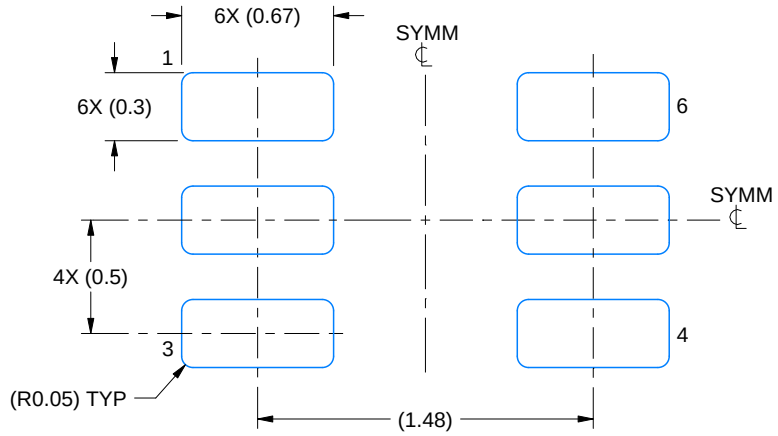
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

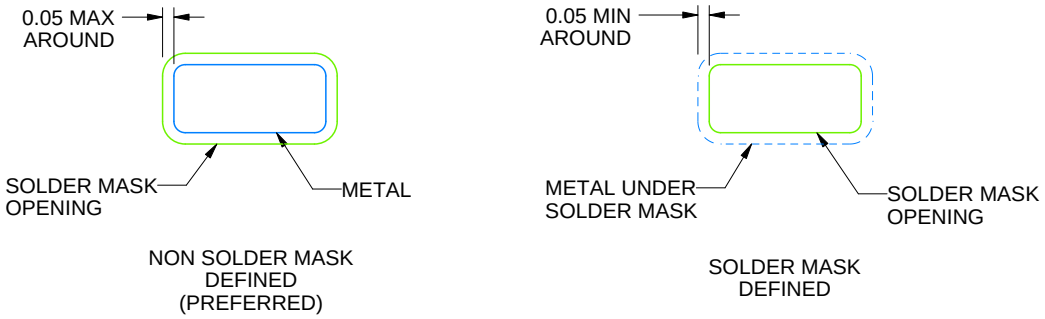
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

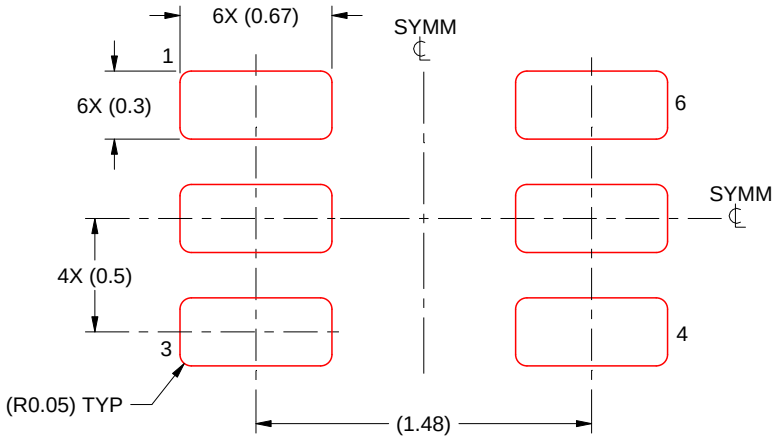
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

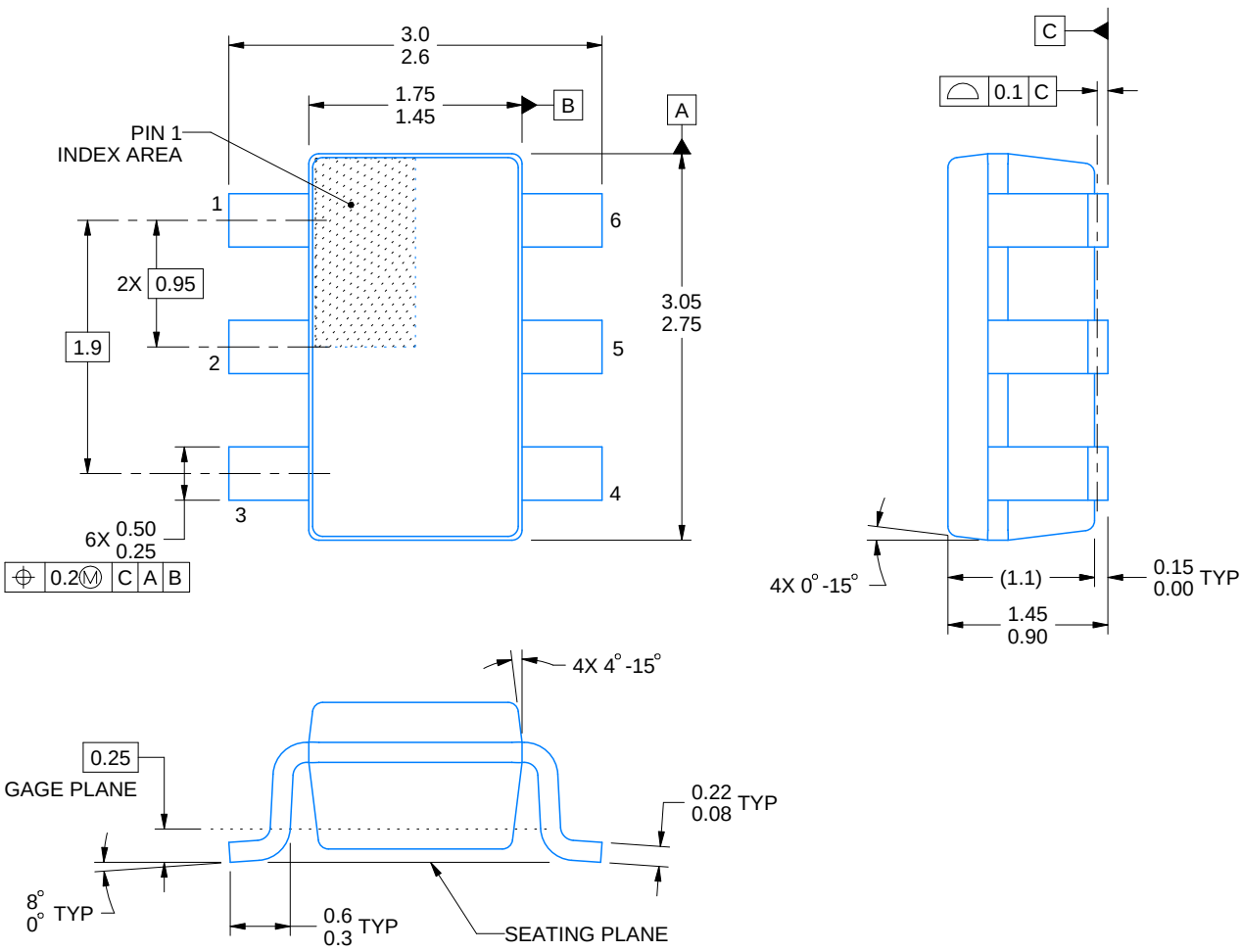
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

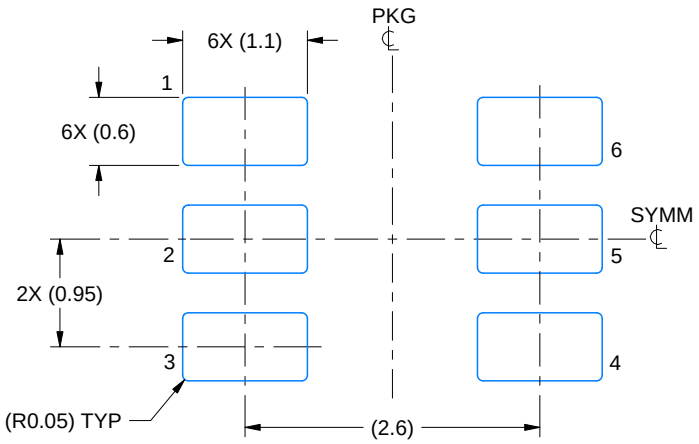
SMALL OUTLINE TRANSISTOR



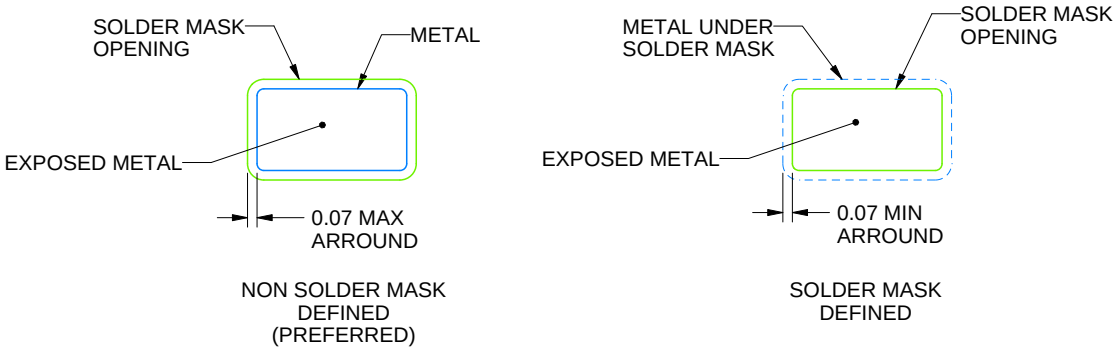
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

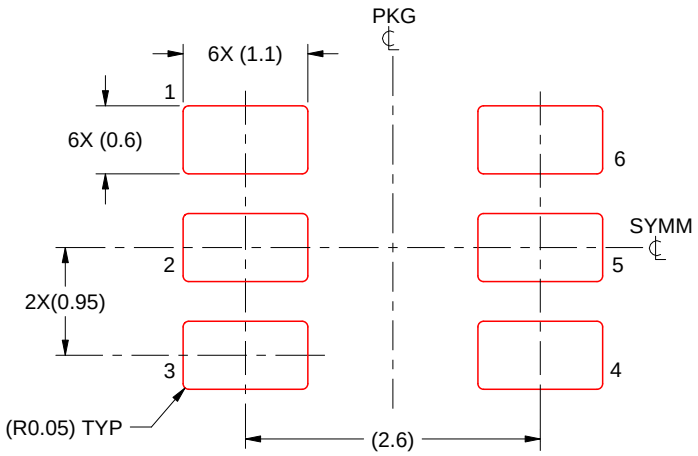


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

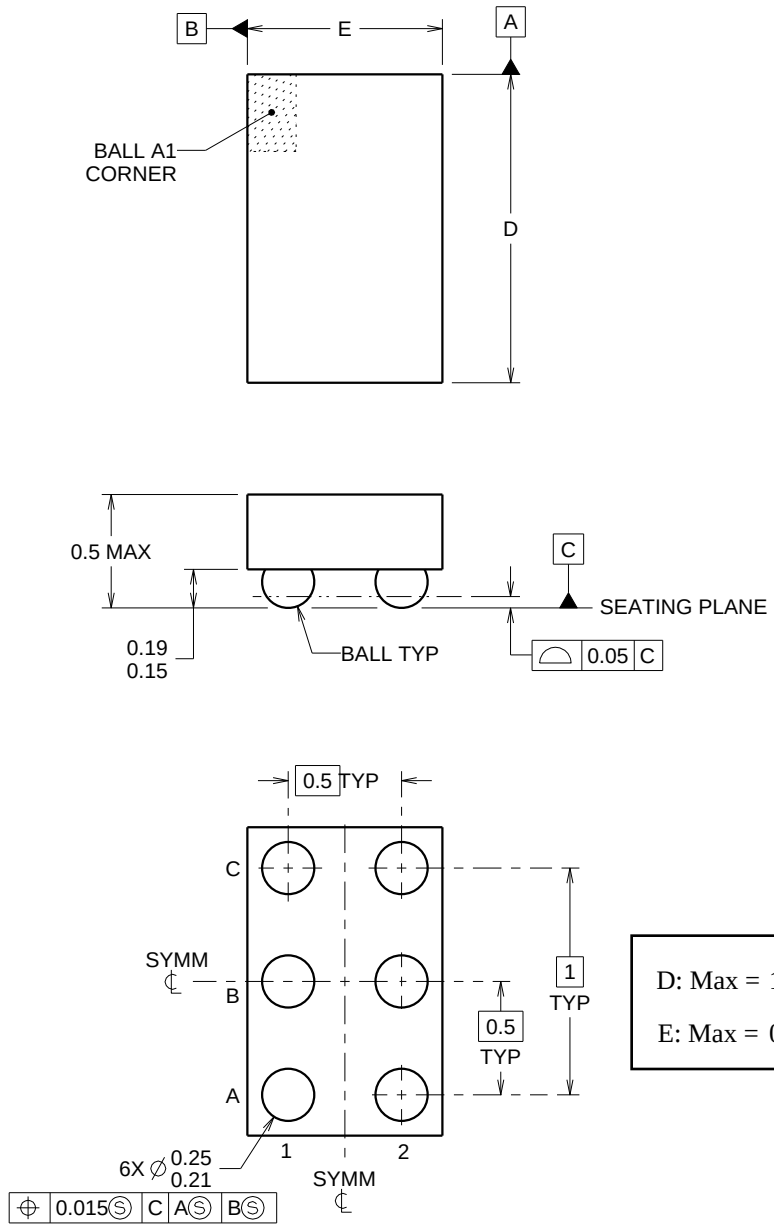
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.357 mm

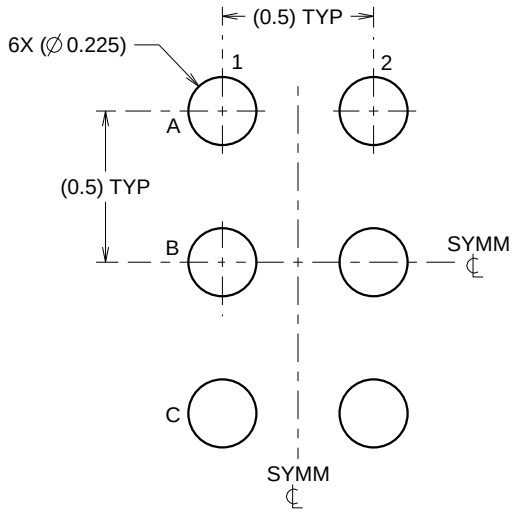
E: Max = 0.918 mm, Min =0.857 mm

4219524/A 06/2014

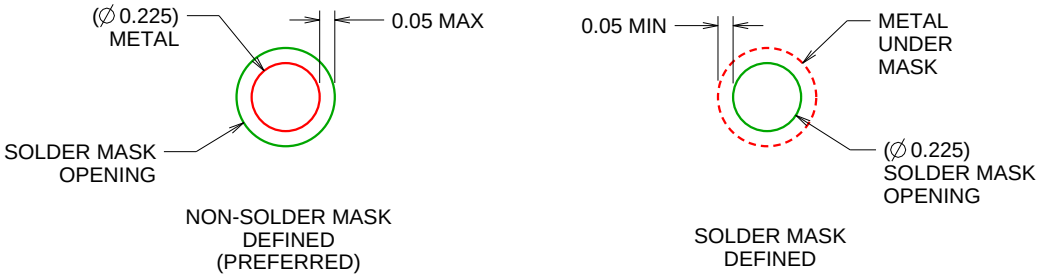
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

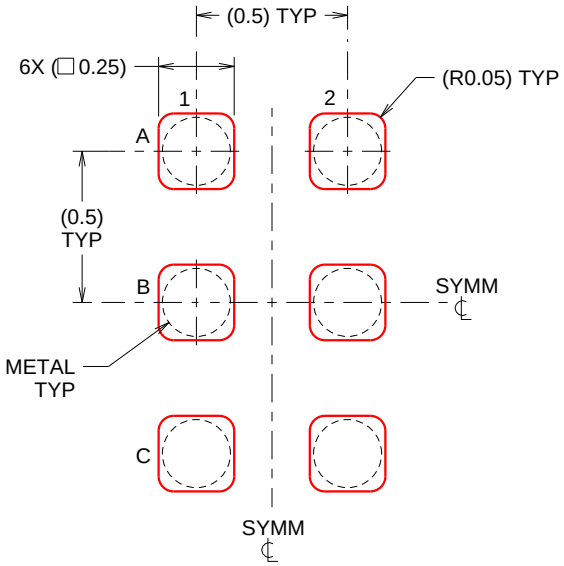


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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