SN74LVC1G373B-Q1 Automotive Single D-Type Latch With 3-State Output

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
- Operating range from 1.1V to 5.5V
- 5.5V tolerant input pins
- Supports standard pinouts
- Latch-up performance exceeds 100mA per JESD 78

2 Applications

- Braking systems
- Hospital patient care
- Retail automation
- Printers

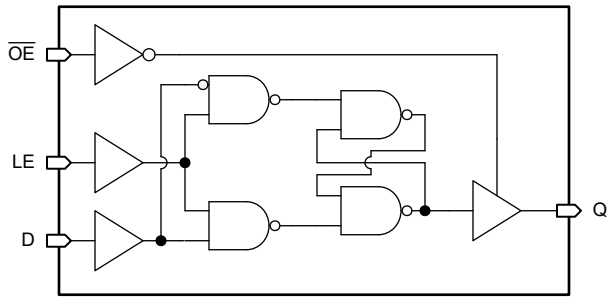
3 Description

The SN74LVC1G373B-Q1 contains one D-type latch with 3-state output . While the latch-enable (LE) input is high, the Q output follows the data (D) input. When LE is low, the Q output is latched at the logic level set up at the D input. The output enable ($\overline{OE}$) does not affect the internal operations of the latch. Old data can be retained or new data can be written while the output is in the high-impedance state.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC1G373B-Q1	DCK (SC70, 6)	2.1mm × 2mm	2mm × 1.25mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

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4 Pin Configuration and Functions

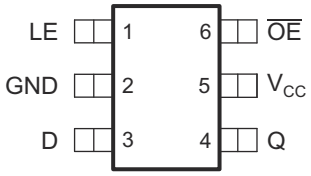


Figure 4-1. DCK Package 5-Pin SC70 Top View

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
LE	1	I	Latch enable
GND	2	G	Ground
D	3	I	Data input
Q	4	O	Output
V_{CC}	5	P	Positive supply
$\overline{OE}$	6	I	Output enable input, active low

(1) I= input, O = output, P = power, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range - High Impedance(2)		-0.5	6.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	(High or low state)	0	V_{CC}	V
V_O	Output voltage	(High Impedance)	0	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 1.1V to 1.95V	0.65x Vcc		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3.0V to 3.6V	2		
		V_{CC} = 4.5V to 5.5V	0.7x Vcc		
V_{IL}	Low-Level input voltage	V_{CC} = 1.1V to 1.95V		0.35x Vcc	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3.0V to 3.6V		0.8	
		V_{CC} = 4.5V to 5.5V		0.3x Vcc	

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I_{OH}	High-level output current	V_{CC} = 1.65V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 3.0V		-16	
				-24	
		V_{CC} = 4.5V		-32	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3.0V		16	
				24	
		V_{CC} = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{cc} = 1.2V to 2.5V		20	ns/V
		V_{cc} = 3.3V ± 0.3V		10	
		V_{cc} = 5.0V ± 0.5V		5	
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DCK (SOT-SC70, 6)	6	371.0	297.5	258.6	195.6	256.2	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH}= –100µA	1.1V to 5.5V	V_{CC} - 0.1			V_{CC} - 0.1			V
	I_{OH}= –4mA	1.65V	1.2			1.2			V
	I_{OH}= –8mA	2.3V	1.9			1.9			V
	I_{OH}= –12mA	2.7V	2.2			2.2			V
	I_{OH}= –16mA	3V	2.4			2.4			V
	I_{OH}= –24mA	3V	2.3			2.3			V
	I_{OH}= –32mA	4.5V	3.8			3.8			V
V_{OL}	I_{OL}= 100µA	1.1V to 5.5V			0.1			0.15	V
	I_{OL}= 4mA	1.65V			0.24			0.45	V
	I_{OL}= 8mA	2.3V			0.3			0.3	V
	I_{OL}= 12mA	2.7V			0.4			0.4	V
	I_{OL}= 16mA	3V			0.4			0.4	V
	I_{OL}= 24mA	3V			0.55			0.55	V
	I_{OL}= 32mA	4.5V			0.55			0.55	V
I_I	V_I = V_{CC} or GND	V_{CC} = 0V to 5.5V			±1			±5	µA
I_{OFF}	V_I or V_O = V_{CC}	V_{CC} = 0V			±1			±10	µA
I_{OZ}	V_O = V_{CC} or GND	5.5V			±1			±15	µA

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 1.1V to 5.5V			1			10	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	3.0V to 5.5V			500			500	µA
C_I	V_I = V_{CC} or GND	3.3V		3.5			3.5		pF
C_O	V_O = V_{CC} or GND	3.3V		6.3					pF

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
f_{clock}	Clock frequency		1.2V ± 0.1V			32	MHz
			1.5V ± 0.12			75	
f_{clock}	Clock frequency		1.8V ± 0.15V			115	MHz
			2.5V ± 0.2V			202	
			3.3V ± 0.3V			280	
			5V ± 0.5V			395	
t_W	Pulse duration	LE high	1.2V ± 0.1V	7			ns
			1.5V ± 0.12V	3			
t_W	Pulse duration	LE high	1.8V ± 0.15V	2			ns
			2.5V ± 0.2V	2			
			3.3V ± 0.3V	2			
			5V ± 0.5V	2			
t_{SU}	Setup time	Data before LE low	1.2V ± 0.1V	10			ns
			1.5V ± 0.12V	4			
t_{SU}	Setup time	Data before LE low	1.8V ± 0.15V	3			ns
			2.5V ± 0.2V	2			
			3.3V ± 0.3V	2			
			5V ± 0.5V	1			
t_H	Hold time	Data after LE low	1.2V ± 0.1V	0			ns
			1.5V ± 0.12V	0			
t_H	Hold time	Data after LE low	1.8V ± 0.15V	0			ns
			2.5V ± 0.2V	0			
			3.3V ± 0.3V	0			
			5V ± 0.5V	0			

5.7 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	D	Q	C_L = 15pF	1.2V ± 0.1V			55.1	ns
t_{pd}	D	Q	C_L = 15pF	1.5V ± 0.12V			14.2	ns
t_{pd}	D	Q	C_L = 15pF	1.8V ± 0.15V			9.5	ns

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	D	Q	C_L = 15pF	2.5V ± 0.2V			5.7	ns
t_{pd}	D	Q	C_L = 15pF	3.3V ± 0.3V			4.2	ns
t_{pd}	D	Q	C_L = 15pF	5V ± 0.5V			3.3	ns
t_{pd}	D	Q	C_L = 50pF	1.2V ± 0.1V			57.7	ns
t_{pd}	D	Q	C_L = 50pF	1.5V ± 0.12V			15.3	ns
t_{pd}	D	Q	C_L = 50pF	1.8V ± 0.15V	2		10.2	ns
t_{pd}	D	Q	C_L = 50pF	2.5V ± 0.2V	1.5		6.1	ns
t_{pd}	D	Q	C_L = 50pF	3.3V ± 0.3V	1		5.1	ns
t_{pd}	D	Q	C_L = 50pF	5V ± 0.5V	1		4	ns
t_{pd}	LE	Q	C_L = 15pF	1.2V ± 0.1V			54.8	ns
t_{pd}	LE	Q	C_L = 15pF	1.5V ± 0.12V			13.5	ns
t_{pd}	LE	Q	C_L = 15pF	1.8V ± 0.15V			9	ns
t_{pd}	LE	Q	C_L = 15pF	2.5V ± 0.2V			5.3	ns
t_{pd}	LE	Q	C_L = 15pF	3.3V ± 0.3V			4	ns
t_{pd}	LE	Q	C_L = 15pF	5V ± 0.5V			3.3	ns
t_{pd}	LE	Q	C_L = 50pF	1.2V ± 0.1V			57.5	ns
t_{pd}	LE	Q	C_L = 50pF	1.5V ± 0.12V			14.5	ns
t_{pd}	LE	Q	C_L = 50pF	1.8V ± 0.15V	2		9.7	ns
t_{pd}	LE	Q	C_L = 50pF	2.5V ± 0.2V	1.5		5.8	ns
t_{pd}	LE	Q	C_L = 50pF	3.3V ± 0.3V	1		4.8	ns
t_{pd}	LE	Q	C_L = 50pF	5V ± 0.5V	1		4	ns
t_{en}	$\overline{OE}$	Q	C_L = 15pF	1.2V ± 0.1V			61.7	ns
t_{en}	$\overline{OE}$	Q	C_L = 15pF	1.5V ± 0.12V			12	ns
t_{en}	$\overline{OE}$	Q	C_L = 15pF	1.8V ± 0.15V			8.1	ns
t_{en}	$\overline{OE}$	Q	C_L = 15pF	2.5V ± 0.2V			4.8	ns
t_{en}	$\overline{OE}$	Q	C_L = 15pF	3.3V ± 0.3V			3.5	ns
t_{en}	$\overline{OE}$	Q	C_L = 15pF	5V ± 0.5V			2	ns
t_{en}	$\overline{OE}$	Q	C_L = 50pF	1.2V ± 0.1V			75.4	ns
t_{en}	$\overline{OE}$	Q	C_L = 50pF	1.5V ± 0.12V			13.7	ns
t_{en}	$\overline{OE}$	Q	C_L = 50pF	1.8V ± 0.15V	2		9.2	ns
t_{en}	$\overline{OE}$	Q	C_L = 50pF	2.5V ± 0.2V	1.5		5.4	ns
t_{en}	$\overline{OE}$	Q	C_L = 50pF	3.3V ± 0.3V	0.9		4.6	ns
t_{en}	$\overline{OE}$	Q	C_L = 50pF	5V ± 0.5V	0.7		2.6	ns
t_{dis}	$\overline{OE}$	Q	C_L = 15pF	1.2V ± 0.1V			38.3	ns
t_{dis}	$\overline{OE}$	Q	C_L = 15pF	1.5V ± 0.12V			11.8	ns
t_{dis}	$\overline{OE}$	Q	C_L = 15pF	1.8V ± 0.15V			7.7	ns
t_{dis}	$\overline{OE}$	Q	C_L = 15pF	2.5V ± 0.2V			4.7	ns
t_{dis}	$\overline{OE}$	Q	C_L = 15pF	3.3V ± 0.3V			4.1	ns
t_{dis}	$\overline{OE}$	Q	C_L = 15pF	5V ± 0.5V			3.6	ns
t_{dis}	$\overline{OE}$	Q	C_L = 50pF	1.2V ± 0.1V			40.6	ns
t_{dis}	$\overline{OE}$	Q	C_L = 50pF	1.5V ± 0.12V			13.5	ns
t_{dis}	$\overline{OE}$	Q	C_L = 50pF	1.8V ± 0.15V	2		8.4	ns
t_{dis}	$\overline{OE}$	Q	C_L = 50pF	2.5V ± 0.2V	1		5	ns

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{dis}	$\overline{OE}$	Q	C_L = 50pF	3.3V ± 0.3V	1		5	ns
t_{dis}	$\overline{OE}$	Q	C_L = 50pF	5V ± 0.5V	0.8		4	ns
C_{pd}		Outputs Enabled	f = 10MHz	1.8V		15		pf
C_{pd}		Outputs Enabled	f = 10MHz	2.5V		17		pf
C_{pd}		Outputs Enabled	f = 10MHz	3.3V		19		pf
C_{pd}		Outputs Enabled	f = 10MHz	5V		22		pf
C_{pd}		Outputs Disabled	f = 10MHz	1.8V		3		pf
C_{pd}		Outputs Disabled	f = 10MHz	2.5V		3		pf
C_{pd}		Outputs Disabled	f = 10MHz	3.3V		3		pf
C_{pd}		Outputs Disabled	f = 10MHz	5V		4		pf

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

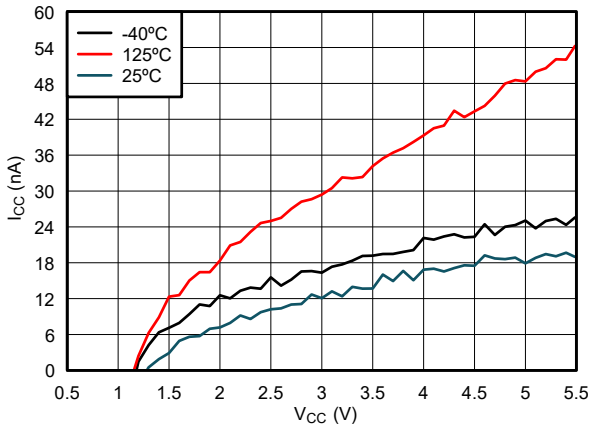


Figure 5-1. Supply Current Across Supply Voltage and Temperature

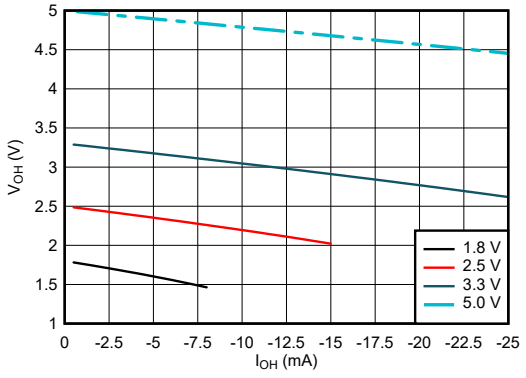


Figure 5-2. Output Voltage vs Current in HIGH State

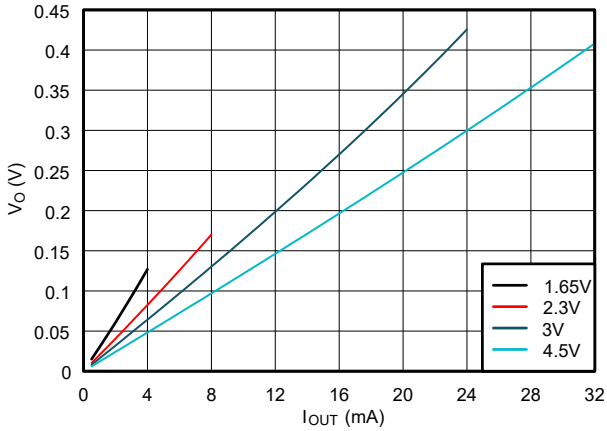


Figure 5-3. Output Voltage vs Current in LOW State

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

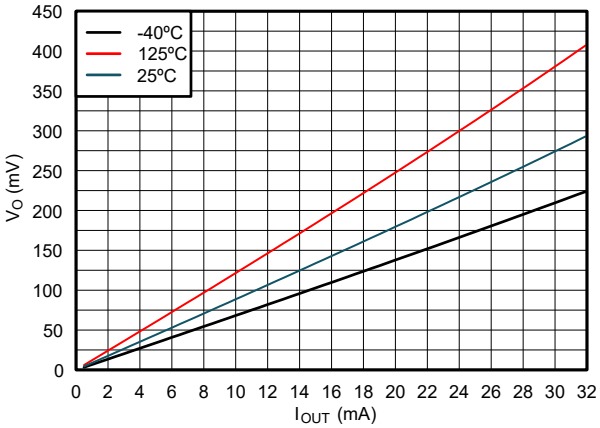


Figure 5-4. Output Voltage vs Current in LOW State; 4.5V Supply

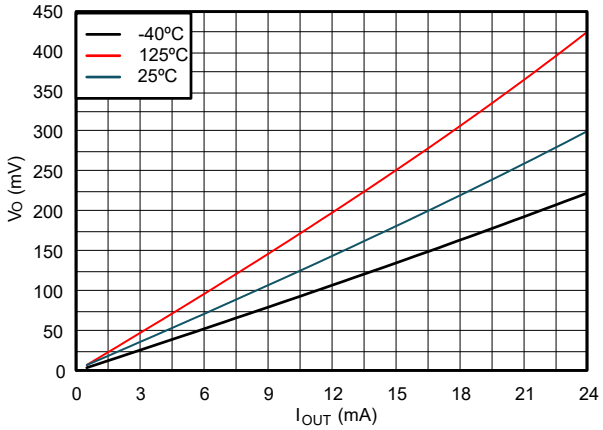


Figure 5-5. Output Voltage vs Current in LOW State; 3V Supply

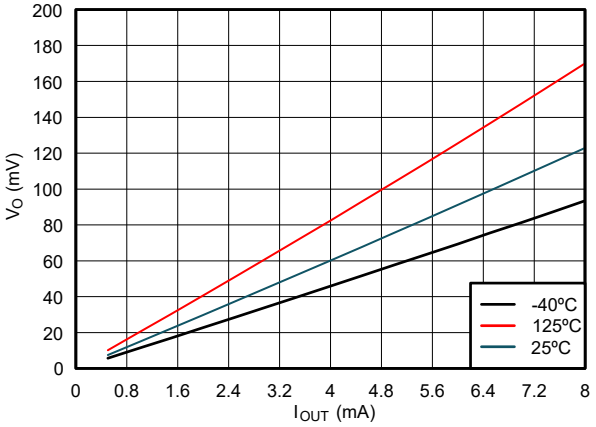


Figure 5-6. Output Voltage vs Current in LOW State; 2.3V Supply

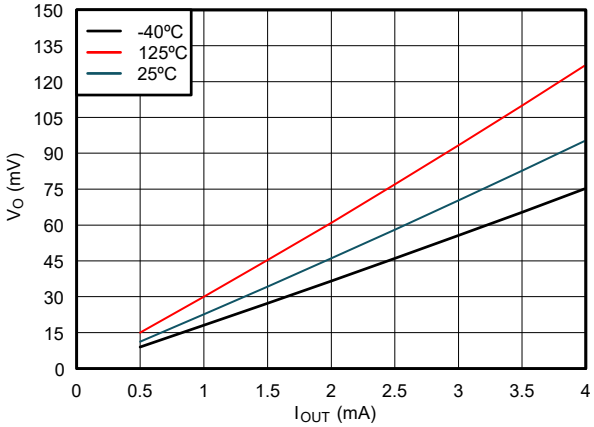


Figure 5-7. Output Voltage vs Current in LOW State; 1.65V Supply

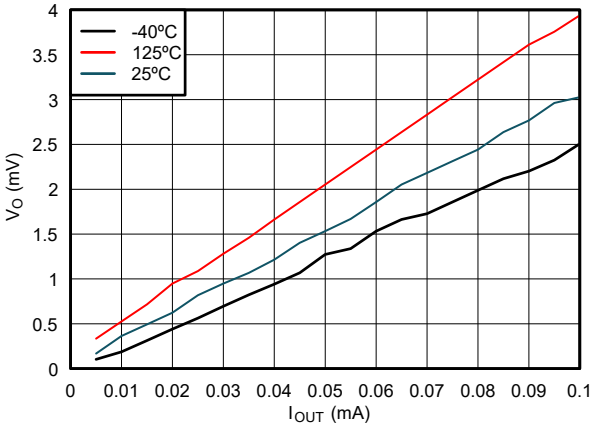


Figure 5-8. Output Voltage vs Current in LOW State; 1.38V Supply

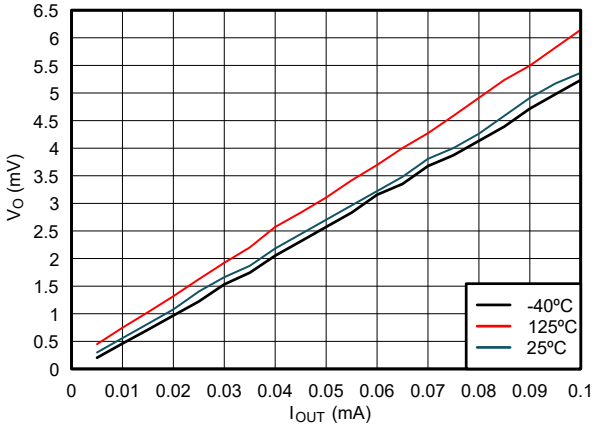


Figure 5-9. Output Voltage vs Current in LOW State; 1.1V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

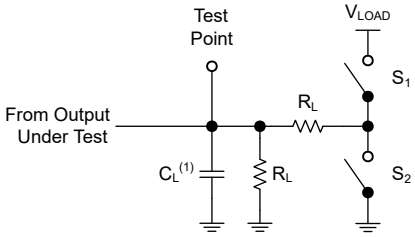
The outputs are measured individually with one input transition per measurement.

Table 6-1. 3-State Outputs

TEST	S1	S2
t_{PLH}, t_{PHL}	OPEN	OPEN
t_{PLZ}, t_{PZL}	CLOSED	OPEN
t_{PHZ}, t_{PZH}	OPEN	CLOSED

Table 6-2. 3-State or Open-Drain Outputs

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
1.2V ± 0.1V	V_{CC}/2	2kΩ	15pF	0.1V	2×V_{CC}
1.5V ± 0.12V	V_{CC}/2	2kΩ	15pF	0.1V	2×V_{CC}
1.8V ± 0.15V	V_{CC}/2	1kΩ	15pF/30pF	0.15V	2×V_{CC}
2.5V ± 0.2V	V_{CC}/2	500Ω	15pF/30pF	0.15V	2×V_{CC}
3.3V ± 0.3V	1.5V	500Ω	15pF/50pF	0.3V	6V
5.0V ± 0.5V	1.5V	500Ω	15pF/50pF	0.3V	6V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs

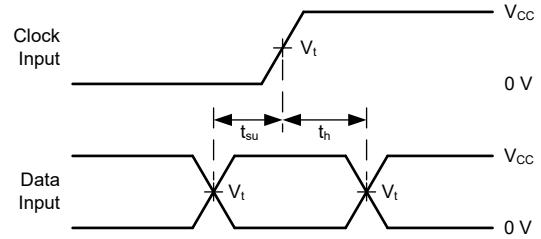


Figure 6-3. Voltage Waveforms, Setup and Hold Times

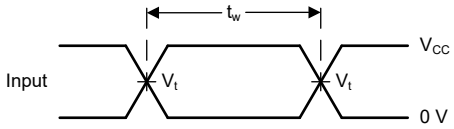
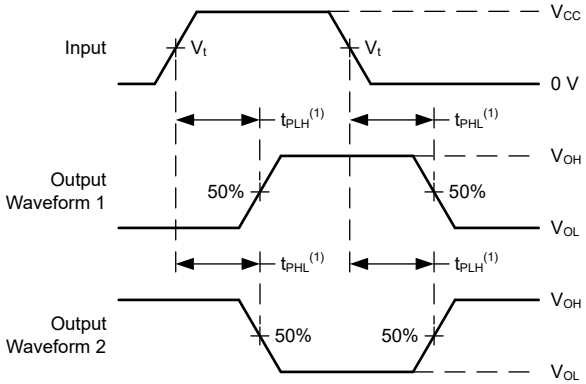
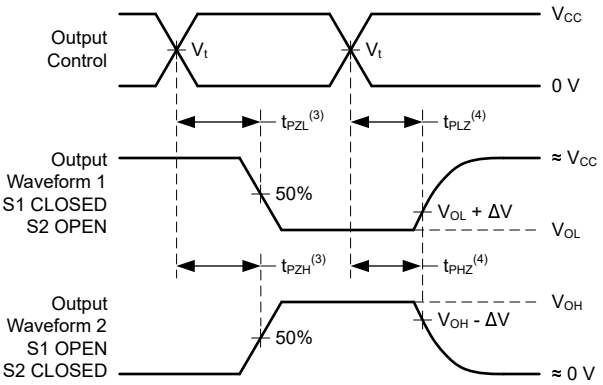


Figure 6-2. Voltage Waveforms, Pulse Duration



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

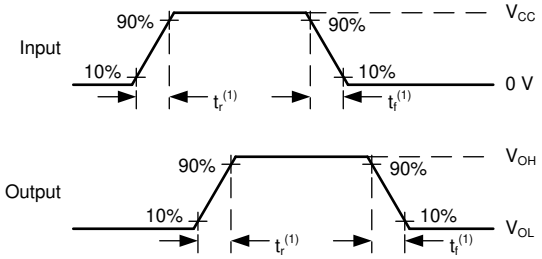
Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-5. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-6. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74LVC1G373B-Q1 is a D-type latch.

When the latch is enabled (LE is high), data is allowed to pass through from the D input to the Q output.

When the latch is disabled (LE is low), the Q output holds the last state regardless of changes at the D input.

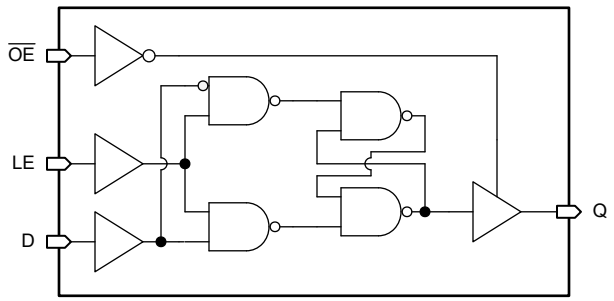
If the latch enable (LE) input is held low during startup, the output state is unknown until the latch enable (LE) input is driven high with valid a input signals at the data (D) input.

When the output is enabled ($\overline{OE}$ is low), the output is actively driving low or high.

When the output is disabled ($\overline{OE}$ is high), the output is set into the high-impedance state.

The active low output enable ($\overline{OE}$) does not have any impact on the stored state in the latch.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

7.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.4 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.3.5 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

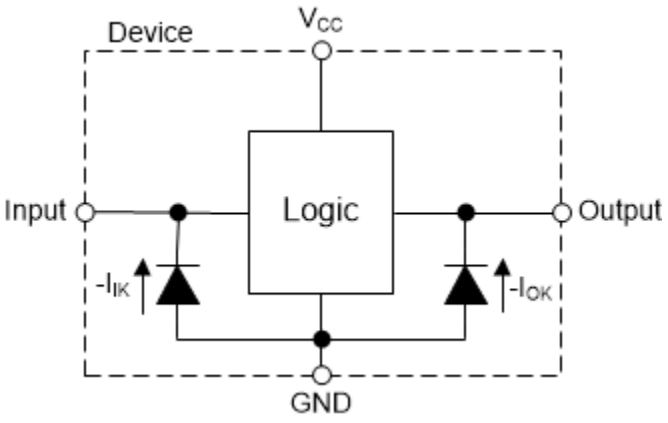


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.6 Over-Voltage Tolerant Inputs

The SN74LVC1G373B-Q1 includes over-voltage tolerant inputs. The input pins support high-state input voltages larger than the supply voltage by utilizing an input protection circuit that does not include a standard positive clamp diode. See *Recommended Operating Conditions* for the recommended input voltage.

CAUTION

Do not exceed the maximum input voltage range provided in *Absolute Maximum Ratings*. Exceeding the maximum input voltage range rating can cause immediate and permanent damage to the device.

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS(1)			OUTPUT(2)
$\overline{OE}$	LE	D	Q
L	H	L	L
L	H	H	H
L	L	X	Q_0 (3)
H	X	X	Z

(1) L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = don't care
(2) L = output low, H = output high, Q_0 = previous state, Z = high impedance
(3) At startup, Q_0 is unknown

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74LVC1G373B-Q1 is used to store one bit of data controlled by the LE and D1 input signals.

The output enable ($\overline{OE}$) is permanently tied low in the application to keep the output active at all times.

8.2 Typical Application

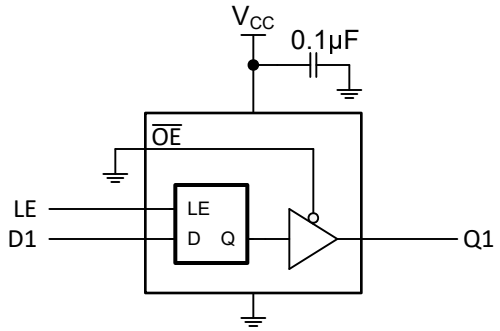


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC1G373B-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G373B-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC1G373B-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74LVC1G373B-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G373B-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC1G373B-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74LVC1G373B-Q1 to the receiving device.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curves

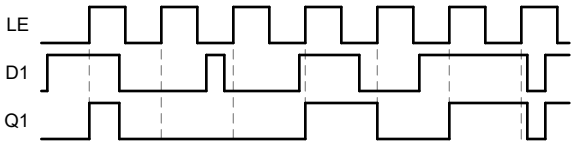


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

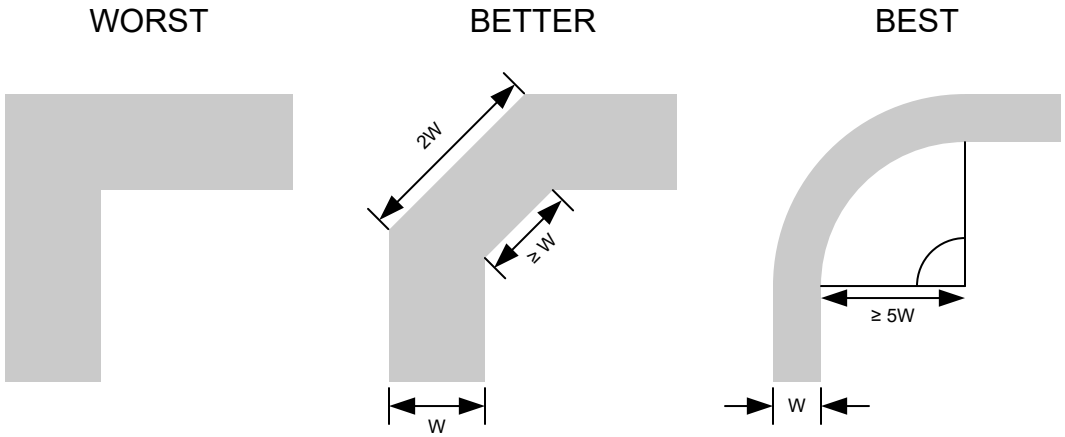


Figure 8-3. Example Trace Corners for Improved Signal Integrity

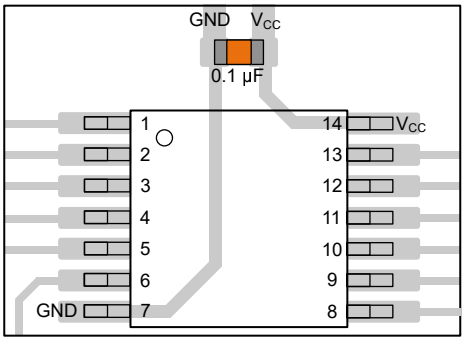


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

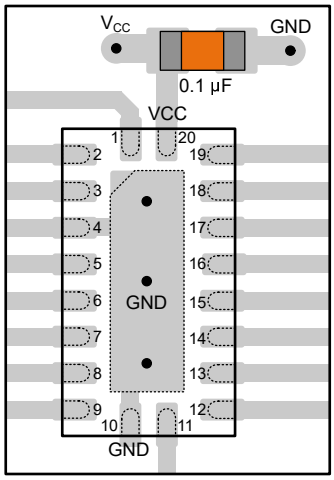


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

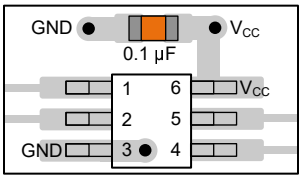


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

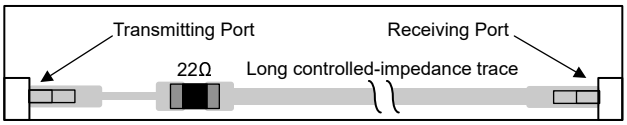


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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