SN74LVC1G57 Configurable Multiple-Function Gate

1 Features

- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
  - Supports down translation to V_{CC}
- Maximum t_{pd} of 6.3ns at 3.3V
- Schmitt-Triggered inputs
- Low power consumption, 10µA maximum I_{CC}
- ±24mA Output Drive at 3.3V
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II
- Available in the Texas Instruments NanoFree™ Package

2 Applications

- Active noise cancellation (ANC)
- Barcode scanners
- Blood pressure monitors
- CPAP machines
- Cable solutions
- Embedded PCs
- Field transmitter: temperature or pressure sensors
- HVAC: heating, ventilating, and air conditioning
- TVs: high-definition (HDTV), LCD, and digital
- Video communications systems

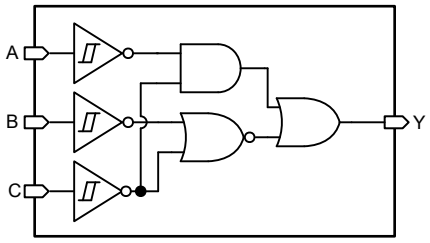
3 Description

The SN74LVC1G57 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can select the logic functions AND, OR, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND. SN74LVC1G57 functions as two independent buffers, but because of Schmitt action, the device can have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC1G57	DBV (SOT-23, 6)	2.90mm × 2.80mm	2.90mm × 1.60mm
	DCK (SC70, 6)	2.00mm × 2.10mm	2.00mm × 1.25mm
	DRY (SON, 6)	1.45mm × 1.00mm	1.45mm × 1.00mm
	DRL (SOT, 6)	1.60mm × 1.20mm	1.60mm × 1.60mm
	DSF (SON, 6)	1.00mm × 1.00mm	1.00mm × 1.00mm
	YZP (DSBGA)	1.41mm × 0.91mm	1.41mm × 0.91mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

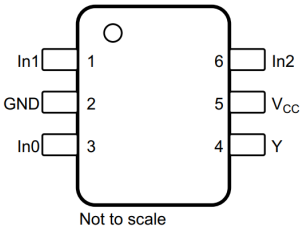

Figure 4-1. DBV, DCK, or DRL Package 6-Pin SOT-23, SC70, or SOT Top View

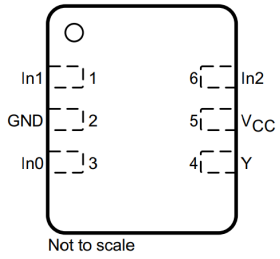

Figure 4-2. DRY or DSF Package 6-Pin SON Top View

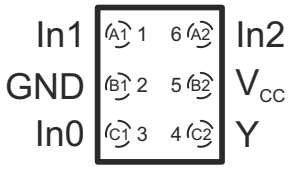

Figure 4-3. YZP Package 6-Pin DSBGA Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	In1	I	Logic input 1
2	GND	—	Ground
3	In0	I	Logic input 0
4	Y	O	Logic output
5	V_{CC}	—	Power
6	In2	I	Logic input 2

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}		–0.5	6.5	V
Input voltage, V_I(2)		–0.5	6.5	V
Voltage range (applied to any output), V_O	High-impedance or power-off state(2)	–0.5	6.5	V
	High or low state(2)(3)	–0.5	V_{CC} + 0.5	
Input clamp current, I_{IK} (V_I < 0)			–50	mA
Output clamp current, I_{OK} (V_O < 0)			–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		–4	mA
		V_{CC} = 2.3V		–8	
		V_{CC} = 3V		–16	
				–24	
		V_{CC} = 4.5V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
T_A	Operating free-air temperature	BGA package	–40	85	°C
		All other packages	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to verify proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

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5.4 Thermal Information

THERMAL METRIC[1]		SN74LVC1G57						UNIT
		DBV (SOT)	DCK (SOT)	DRL (SOT)	YZP (DSGBA)	DSF (SON)	DRY (SON)	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.5	254.1	252.5	124	360.1	332.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	155.0	191.3	111.6	1.4	158.8	198.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	138.2	158.1	118.5	29.7	213.5	189	°C/W
ψ_{JT}	Junction-to-top characterization parameter	84.2	92.5	11.8	0.5	20.4	44.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	137.9	158	118.8	30.1	213.2	189.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	V_{CC} = 1.65V		0.79		1.16	V
		V_{CC} = 2.3V		1.11		1.56	
		V_{CC} = 3V		1.5		1.87	
		V_{CC} = 4.5V		2.16		2.74	
		V_{CC} = 5.5V		2.61		3.33	
V_{T-}	Negative-going input threshold voltage	V_{CC} = 1.65V		0.35		0.62	V
		V_{CC} = 2.3V		0.58		0.87	
		V_{CC} = 3V		0.84		1.19	
		V_{CC} = 4.5V		1.41		1.9	
		V_{CC} = 5.5V		1.87		2.29	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 1.65V		0.3		0.62	V
		V_{CC} = 2.3V		0.4		0.8	
		V_{CC} = 3V		0.53		0.87	
		V_{CC} = 4.5V		0.71		1.04	
		V_{CC} = 5.5V		0.71		1.11	
V_{OH}		V_{CC} = 1.65V to 5.5V, I_{OH} = –100 µA		V_{CC} – 0.1			V
		V_{CC} = 1.65V, I_{OH} = –4mA		1.2			
		V_{CC} = 2.3V, I_{OH} = –8mA		1.9			
		V_{CC} = 3V, I_{OH} = –16mA		2.4			
		V_{CC} = 3V, I_{OH} = –24mA		2.3			
		V_{CC} = 4.5V, I_{OH} = –32mA		3.8			
V_{OL}		V_{CC} = 1.65V to 5.5V, I_{OL} = 100 µA				0.1	V
		V_{CC} = 1.65V, I_{OL} = 4mA				0.45	
		V_{CC} = 2.3V, I_{OL} = 8mA				0.3	
		V_{CC} = 3V, I_{OL} = 16mA	T_A = –40°C to 85°C			0.4	
			T_A = –40°C to 125°C			0.45	
		V_{CC} = 3V, I_{OL} = 24mA				0.55	
		V_{CC} = 4.5V, I_{OL} = 32mA	T_A = –40°C to 85°C			0.55	
			T_A = –40°C to 125°C			0.58	
I_I		V_{CC} = 0V to 5.5V, V_I = 5.5V or GND				±1	µA
I_{off}		V_{CC} = 0V, V_I or V_O = 5.5V				±10	µA
I_{CC}		V_{CC} = 1.65V to 5.5V, V_I = 5.5V or GND, I_O = 0				10	µA
ΔI_{CC}		V_{CC} = 3V to 5.5V, one input at V_{CC} – 0.6V, other inputs at V_{CC} or GND				500	µA

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5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
C_i		V_{CC} = 3.3V, V_I = V_{CC} or GND			3.5		pF
C_{pd}	Power dissipation capacitance	f = 10MHz, T_A = 25°C	V_{CC} = 1.8V		20		pF
			V_{CC} = 2.5V		20		
			V_{CC} = 3.3V		21		
			V_{CC} = 5V		22		

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted; see Figure 6-1)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	Any input to Y (output)	T_A = –40°C to 85°C	V_{CC} = 1.8V ± 0.15V	3.2		14.4	ns
			V_{CC} = 2.5V ± 0.2V	2		8.3	
			V_{CC} = 3.3V ± 0.3V	1.5		6.3	
			V_{CC} = 5V ± 0.5V	1.1		5.1	
		T_A = –40°C to 125°C	V_{CC} = 1.8V ± 0.15V	3.2		16.4	
			V_{CC} = 2.5V ± 0.2V	2		9.3	
			V_{CC} = 3.3V ± 0.3V	1.5		7.3	
			V_{CC} = 5V ± 0.5V	1.1		6.1	

5.7 Typical Characteristics

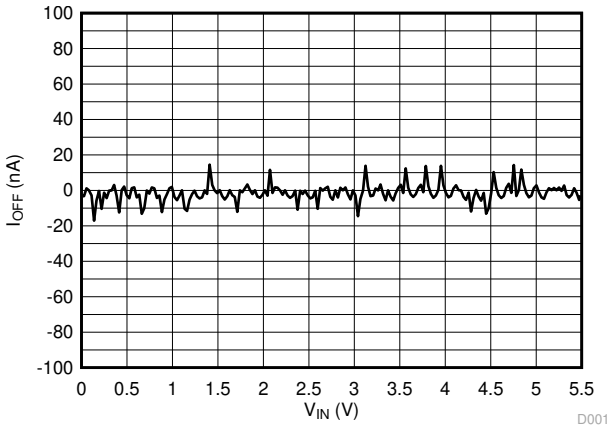

Figure 5-1. Partial-Power-Down Mode I_{OFF} Across V_{IN}

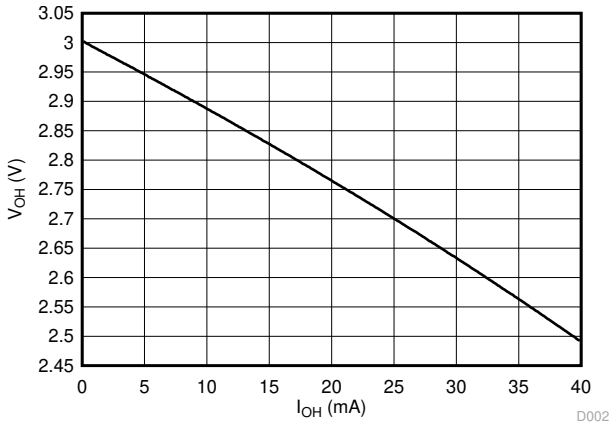

Figure 5-2. Output Voltage (V_{OH}) vs Current (I_{OH})

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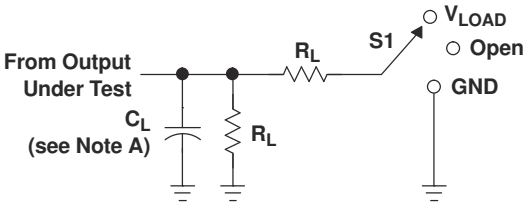
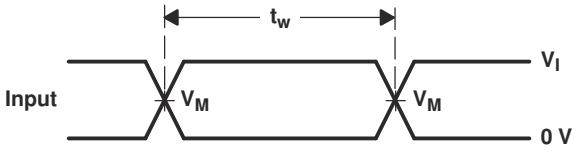
6 Parameter Measurement Information



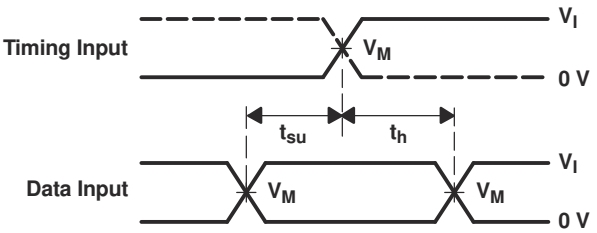
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

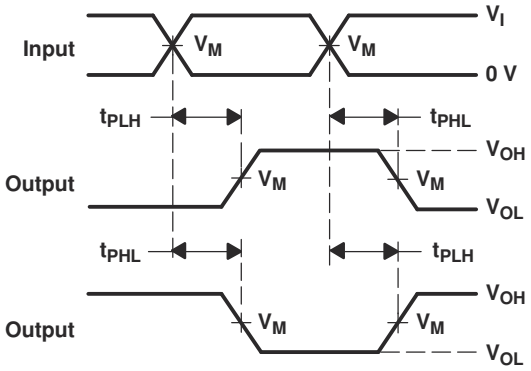
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



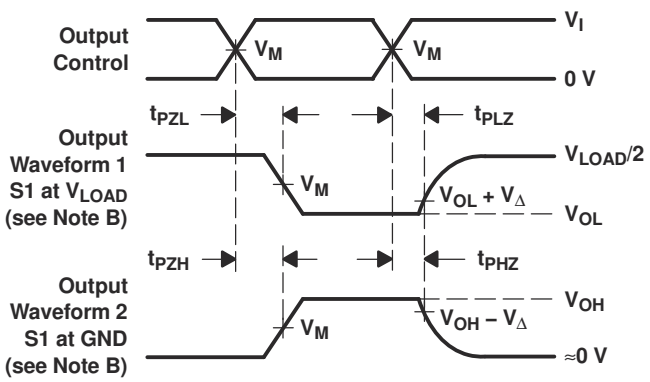
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

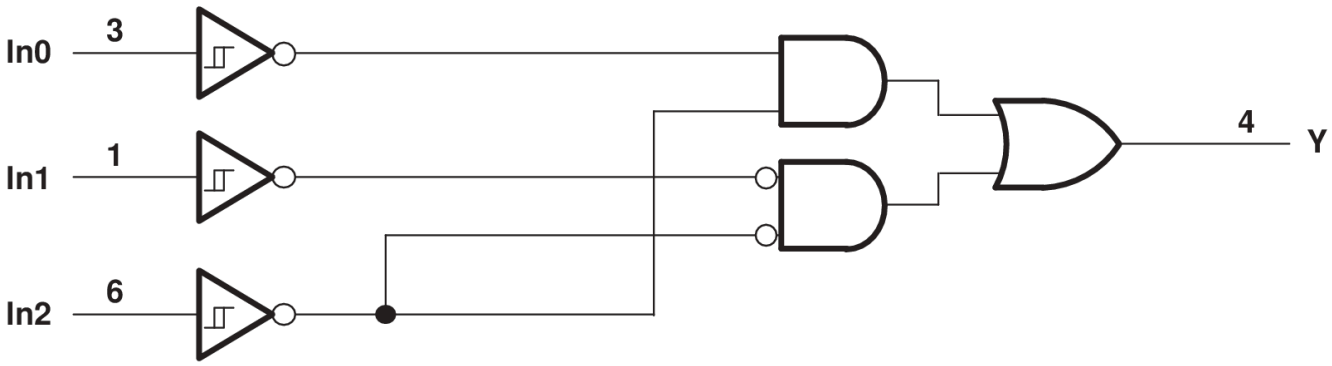
7.1 Overview

The SN74LVC1G57 device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can select the logic functions AND, OR, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

This configurable multiple-function gate is designed for 1.65V to 5.5V V_{CC} operation.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Schmitt-Trigger Inputs

Schmitt-trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs

7.3.2 Inputs Accept Voltages to 5.5V

The SN74LVC1G57 is a configurable multiple-function gate is designed for 1.65V to 5.5V V_{CC} operation. Inputs are over-voltage tolerant up to 5.5V. This feature allows the use of this device as a translator in a mixed 1.8V, 3.3V, and 5V system environment.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVC1G57 and Table 7-2 lists the logic configuration images.

Table 7-1. Function Table

INPUTS			OUTPUT
In2	In1	In0	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

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Table 7-2. Logic Configurations

LOGIC FUNCTION	FIGURE NO.
2-Input AND	Figure 7-1
2-Input AND with both inputs inverted	Figure 7-4
2-Input NAND with inverted input	Figure 7-2 and Figure 7-3
2-Input OR with inverted input	Figure 7-2 and Figure 7-3
2-Input NOR	Figure 7-4
2-Input NOR with both inputs inverted	Figure 7-1
2-Input XNOR	Figure 7-5

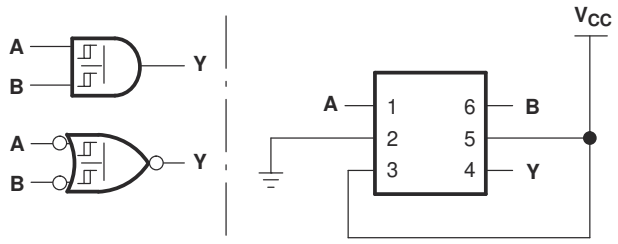

Figure 7-1. 2-Input AND Gate

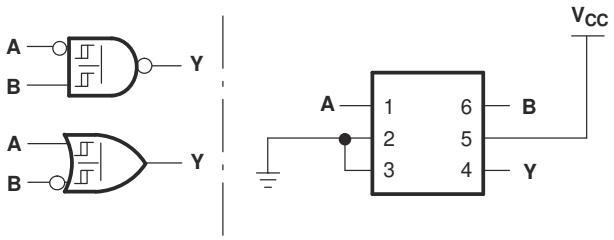

Figure 7-2. 2-Input NAND Gate With Inverted A Input

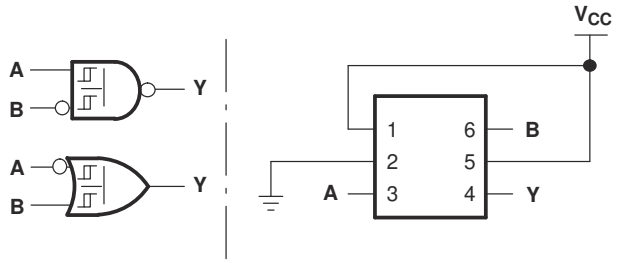

Figure 7-3. 2-Input NAND Gate With Inverted B Input

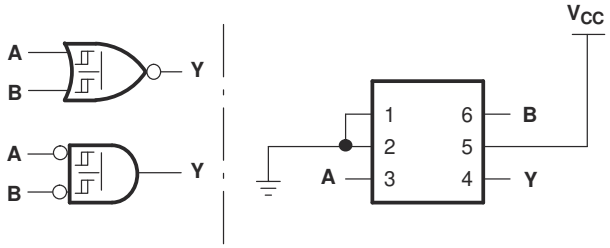

Figure 7-4. 2-Input NOR Gate

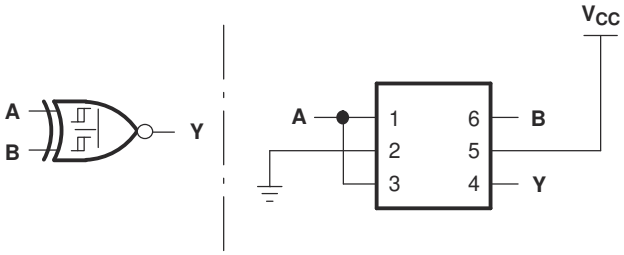

Figure 7-5. 2-Input XNOR Gate

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G57 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can select the logic functions AND, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

8.2 Typical Application

This application shows the SN74LVC1G57 configured as an OR gate with an inverted input. This particular configuration is helpful for dual sensor or switch applications where one of the inputs is normally closed or a logic high *1*. Normally this application would require two external gates, but because the SN74LVC1G57 can be configured to meet this function the application can be implemented with a single chip design.

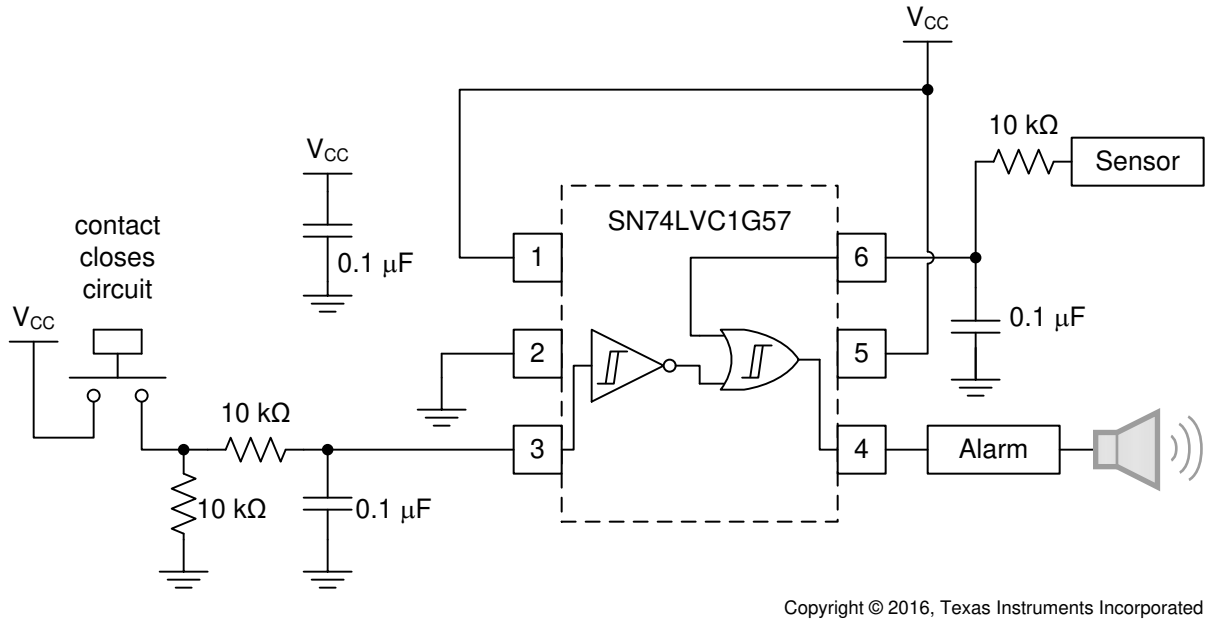

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Figure 8-1. Dual-Sensor Alarm Trigger

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8.2.1 Design Requirements

8.2.1.1 Application Truth Table

Because we are working with two independent alarm triggers, we need to ensure that the alarm signal is only sent whenever either condition is met. Therefore our resulting truth table will look very much like a logic OR function. However, since we are also assuming one of the conditions to always be true, i.e. a door that should remain closed, we make use of the inverted input in Table 8-1.

Table 8-1. Dual-Sensor Truth Table

INPUTS		OUTPUT
TRIGGER OR SWITCH	SENSOR	ALARM
L	X	H
H	L	L
X	H	H

8.2.1.2 Schmitt-Trigger Inputs

On a normal (non-Schmitt-Trigger) input the part switches at the same point on the rising edge and falling edge. With a slow rising edge the part switches at the threshold. When the switch occurs it requires current from V_{CC}. When current is forced from V_{CC}, the V_{CC} level can drop causing the threshold to shift. When the threshold shifts it crosses the input again causing the part to switch again. This can go on and on causing oscillation which can cause excessive current. The same thing can happen if there is noise on the input. The noise can cross the threshold multiple times and cause oscillation or multiple clocking. To address these problems, use a Schmitt-Trigger type device to translate the slow or noisy edges into something faster that meets the input rise and fall specs of the following device. A true Schmitt-Trigger input does not have rise and fall time limitations.

8.2.2 Detailed Design Procedure

1. Recommended Input conditions:
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommended output conditions:
   - Load currents must not exceed 20mA on the output and 50mA total for the part.
   - Outputs must not be pulled above V_{CC}.

8.2.3 Application Curves

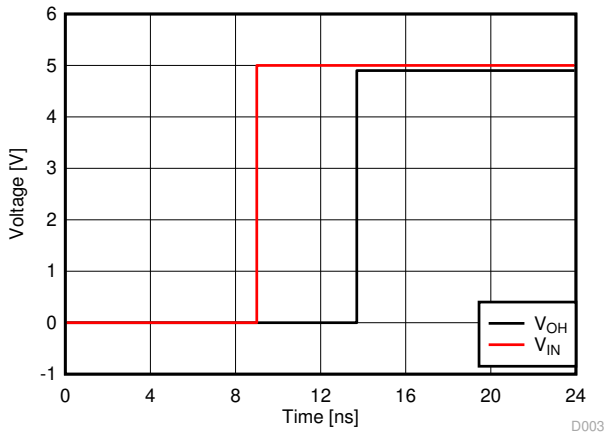

Figure 8-2. Simulated Output V_{OH} at 5V and 25°C

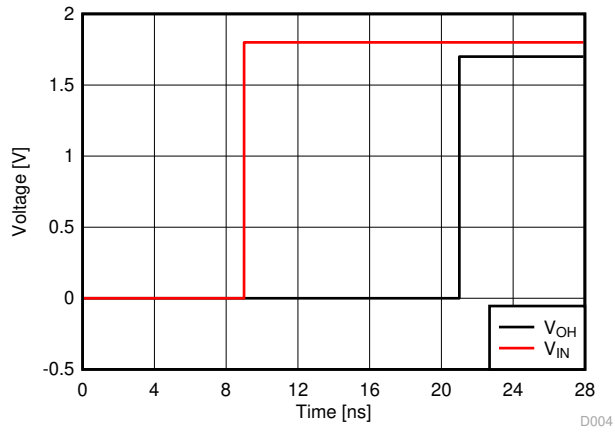

Figure 8-3. Simulated Output V_{OH} at 1.8V and 25°C

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1µF bypass capacitor is recommended for each supply pin. An acceptable design is to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

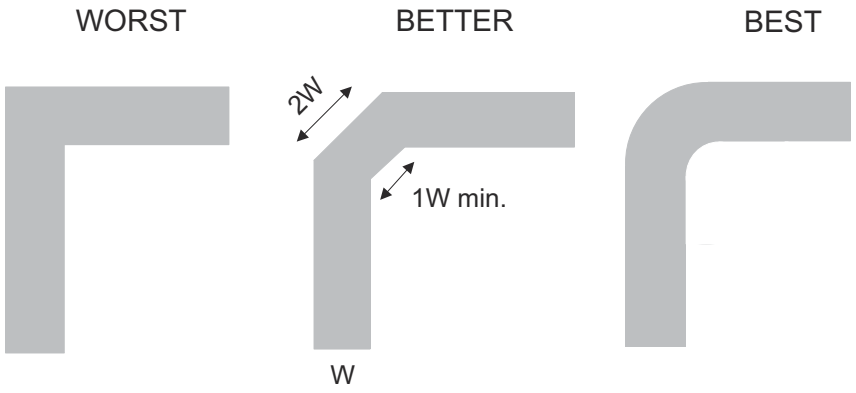

Figure 8-4. Trace Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 1, 2016 to November 17, 2026 (from Revision P (November 2016) to Revision Q (November 2026)) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Changed Junction-to-ambient thermal resistance value for DBV package from: 223°C/W to: 225.5°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 174.4°C/W to: 155.0°C/W.. 5
- Changed Junction-to-board thermal resistance value for DBV package from: 71°C/W to: 138.2°C/W.....5
- Changed Junction-to-top characterization parameter value for DBV package from: 57.1°C/W to: 84.2°C/W....5
- Changed Junction-to-board characterization parameter value for DBV package from: 70.3°C/W to: 137.9°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 271.7°C/W to: 254.1°C/W.....5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 129.8°C/W to: 191.3°C/W..5
- Changed Junction-to-board thermal resistance value for DCK package from: 73.1°C/W to: 158.1°C/W..... 5
- Changed Junction-to-top characterization parameter value for DCK package from: 8.3°C/W to: 92.5°C/W..... 5
- Changed Junction-to-board characterization parameter value for DCK package from: 72.4°C/W to: 158.0°C/W..... 5

Changes from Revision O (December 2013) to Revision P (November 2016) **Page**

- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... 1
- Changed Package thermal impedance, $R_{\theta JA}$, values From: 165°C/W To: 223°C/W (DBV), From: 259°C/W To: 271.7°C/W (DCK), From: 142°C/W To: 252.5°C/W (DRL), and From: 123°C/W To: 124°C/W (YZP)..... 5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G57DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CA7O, CA7R)
SN74LVC1G57DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CA7O, CA7R)
SN74LVC1G57DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA7R
SN74LVC1G57DBVRG4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CA7R
SN74LVC1G57DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CL5, CLF, CLJ, CL K, CLR)
SN74LVC1G57DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CL5, CLF, CLJ, CL K, CLR)
SN74LVC1G57DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CLF
SN74LVC1G57DCKRG4.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CLF
SN74LVC1G57DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(1K2, CL7, CLR)
SN74LVC1G57DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(1K2, CL7, CLR)
SN74LVC1G57DRLRG4	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1K2
SN74LVC1G57DRLRG4.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1K2
SN74LVC1G57DRY2	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRY2.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRYRG4	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DRYRG4.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL
SN74LVC1G57YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CLN
SN74LVC1G57YZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CLN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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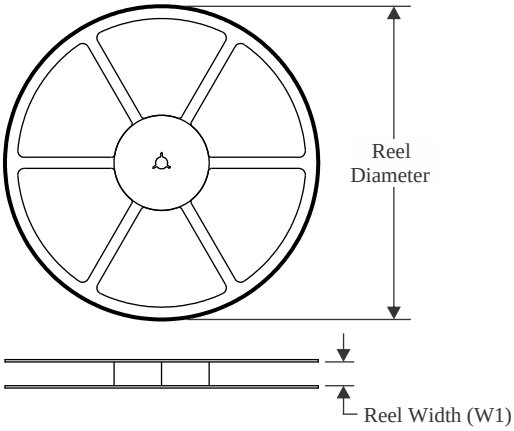
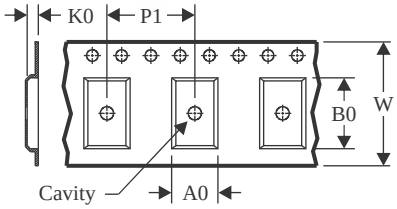
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

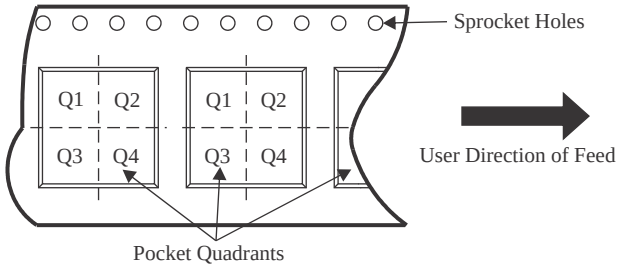


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

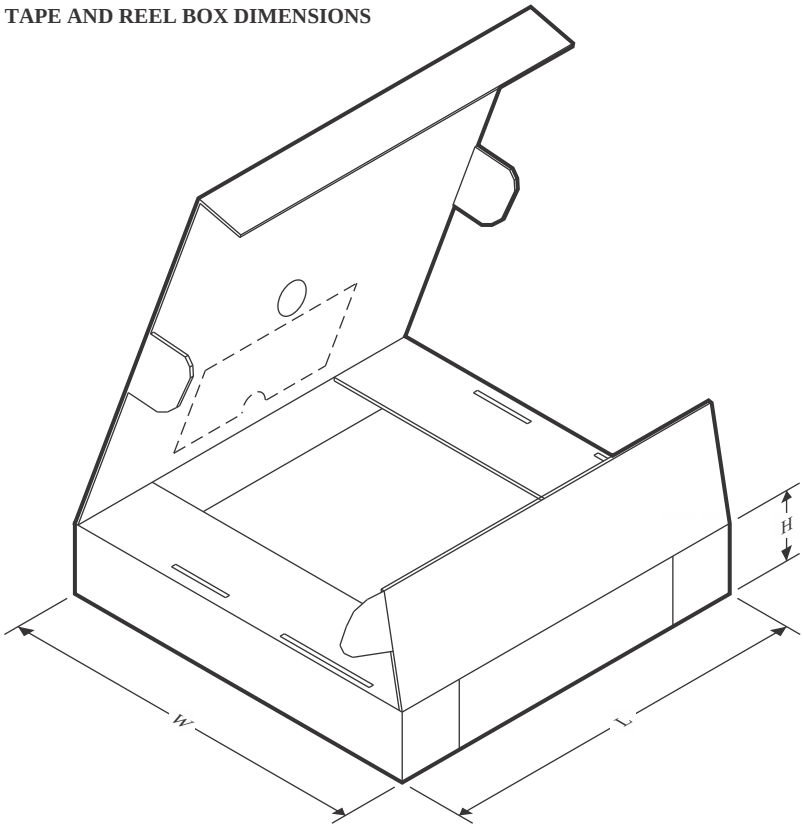


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G57DBVRG4	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G57DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G57DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G57DRLRG4	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G57DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G57DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G57DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G57DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

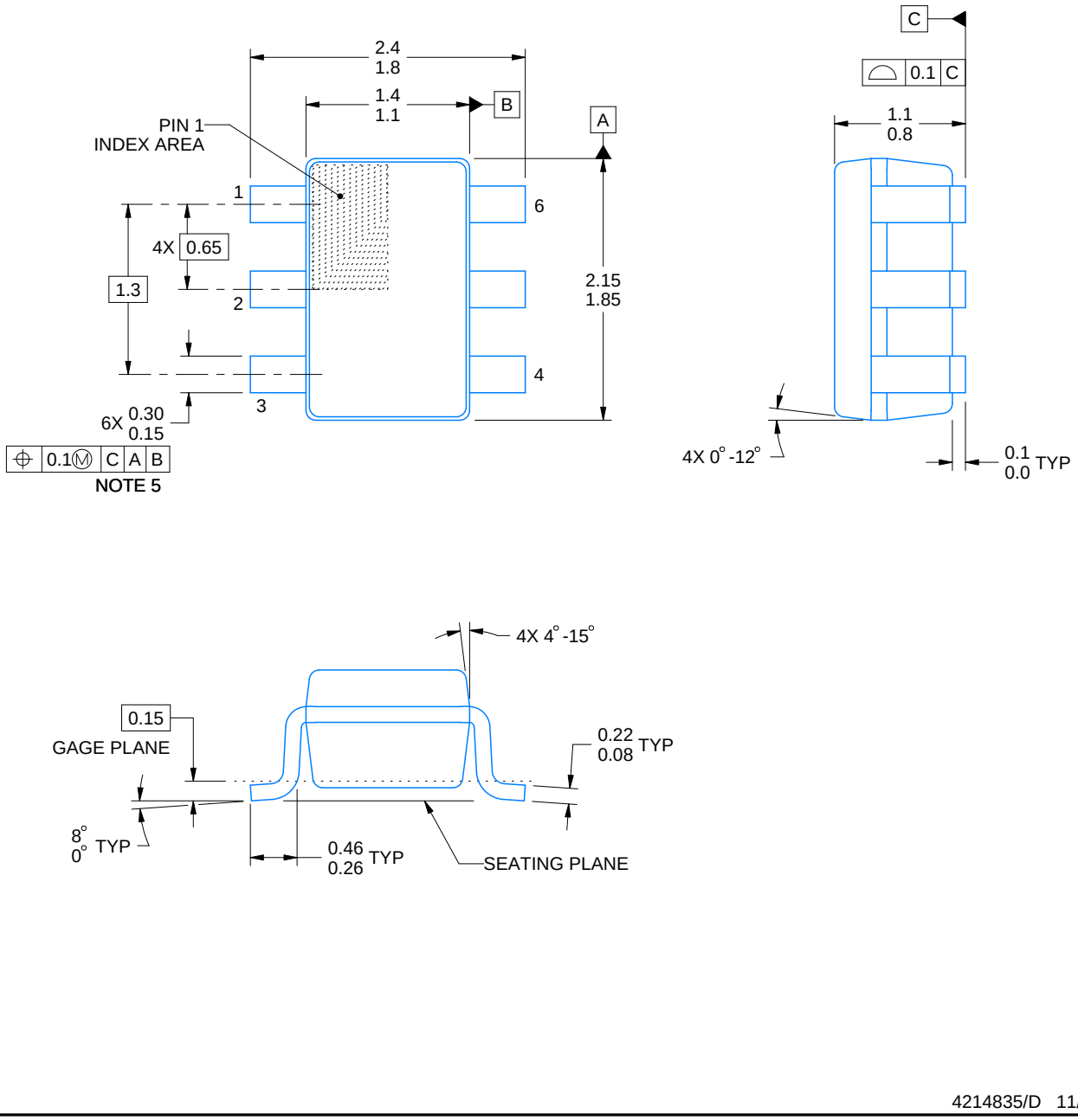
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
SN74LVC1G57DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G57DBVRG4	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC1G57DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74LVC1G57DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G57DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G57DRLRG4	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G57DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G57DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G57DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G57DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G57YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

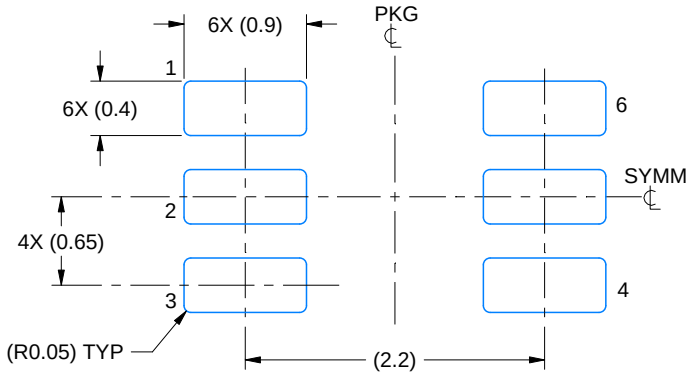
SMALL OUTLINE TRANSISTOR



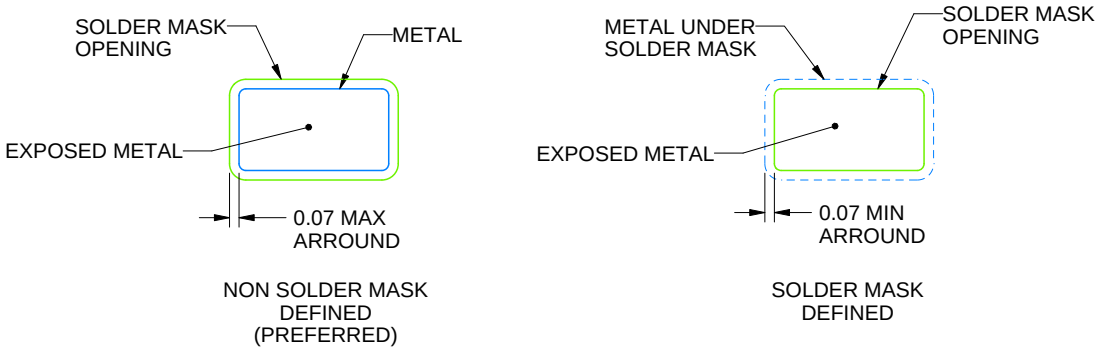
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

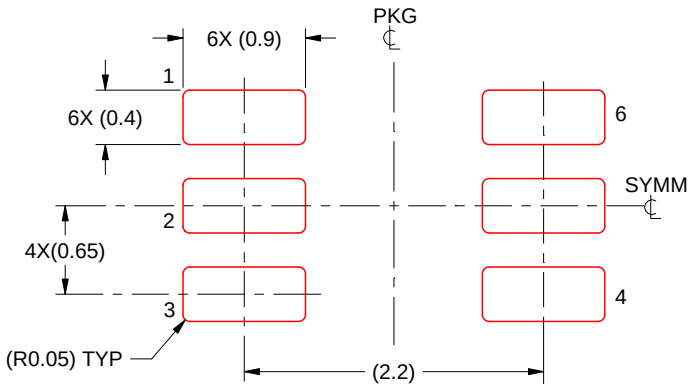


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

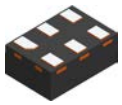
DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

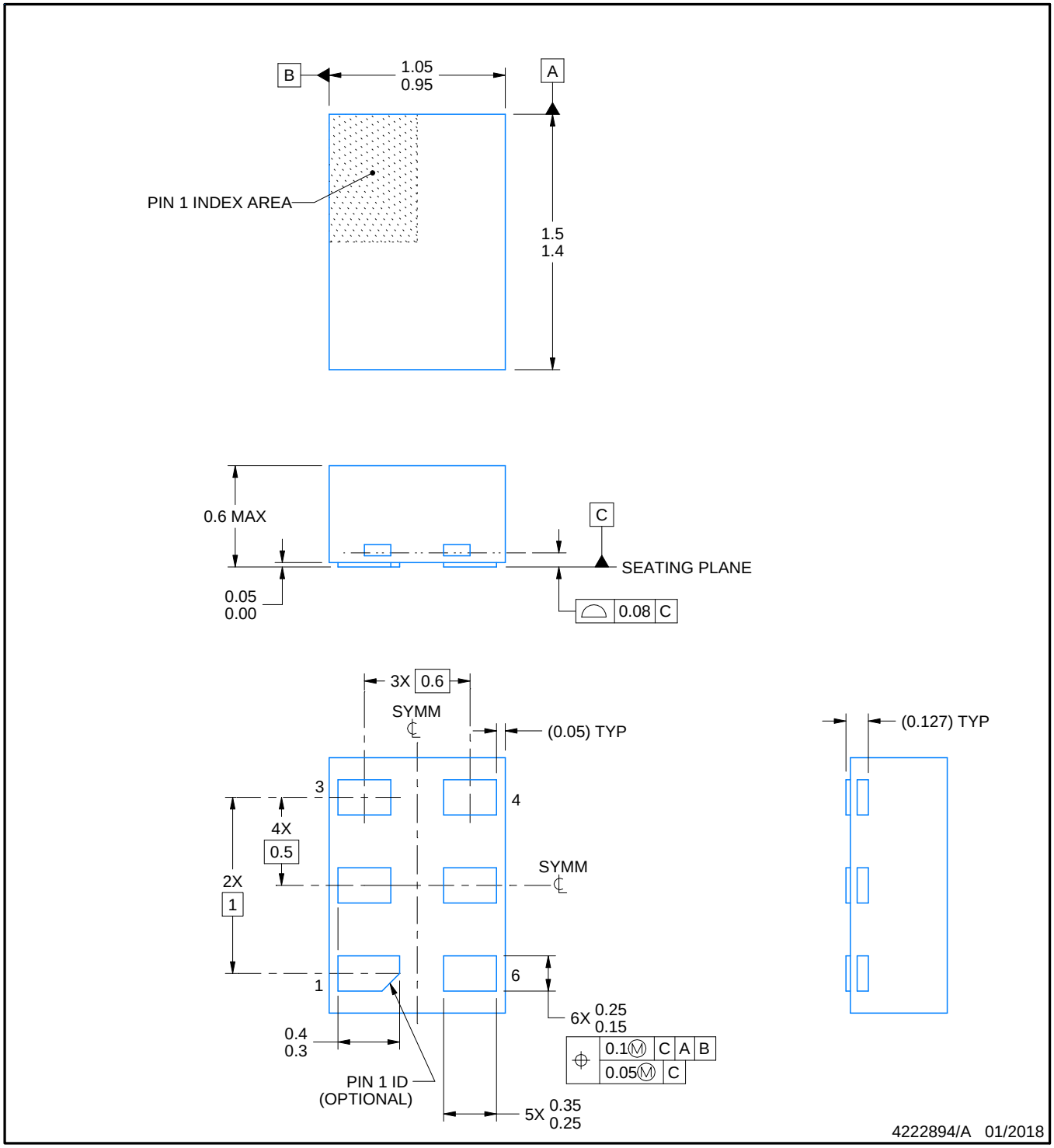
DRY0006A



PACKAGE OUTLINE

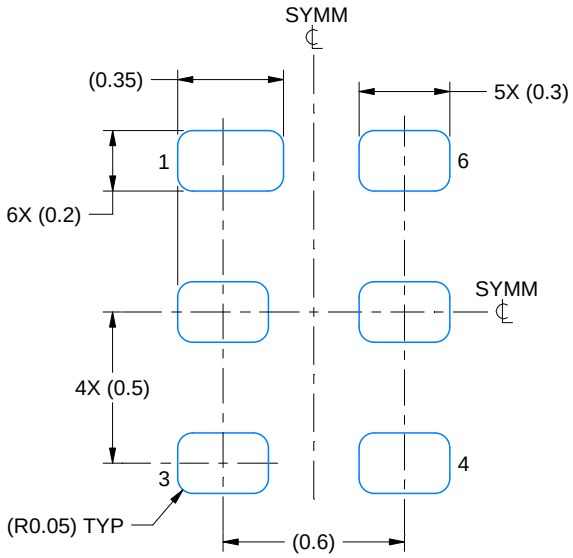
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

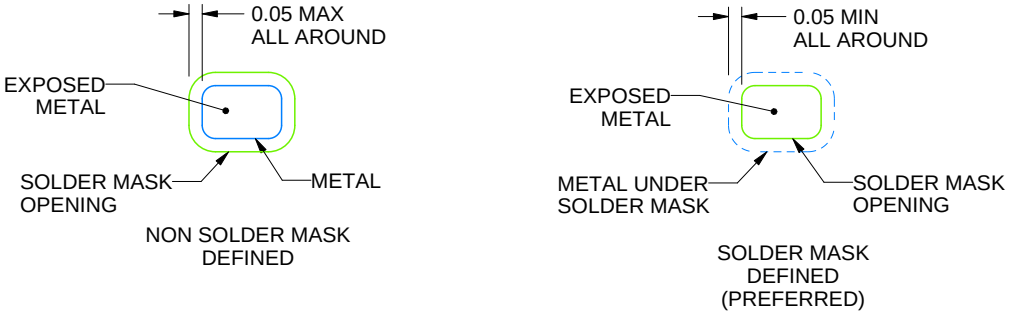


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

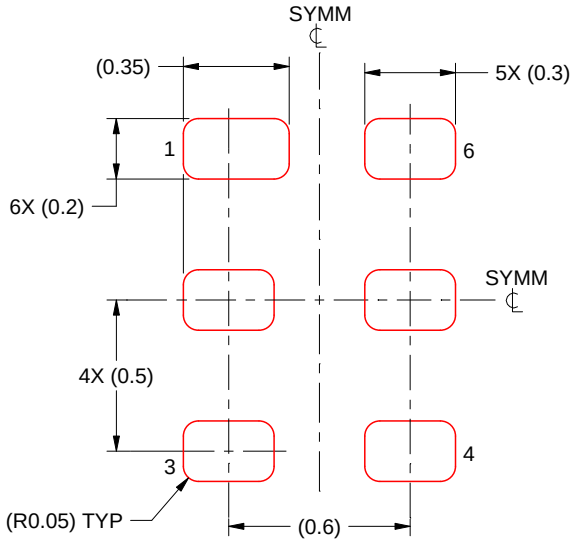
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

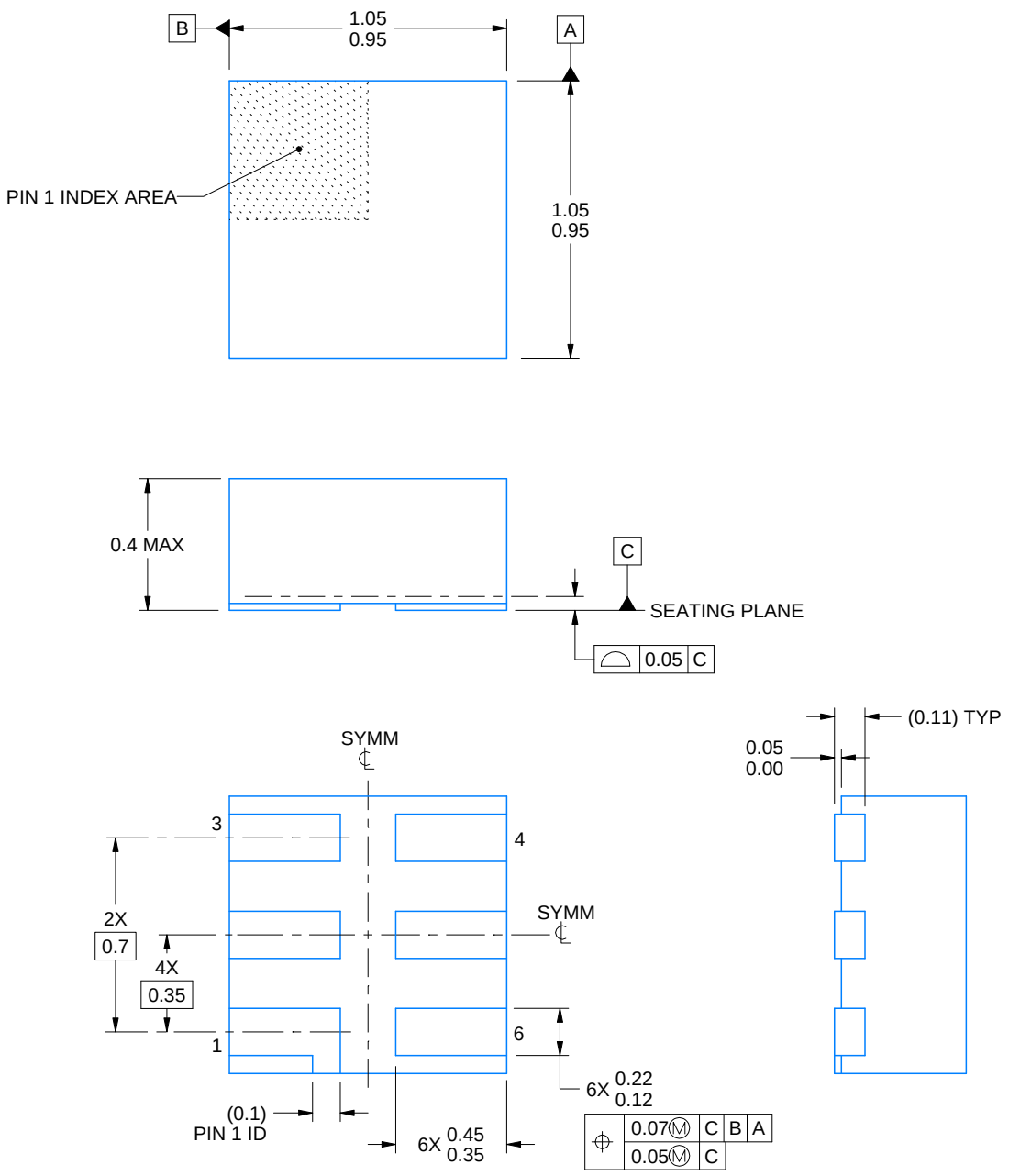
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

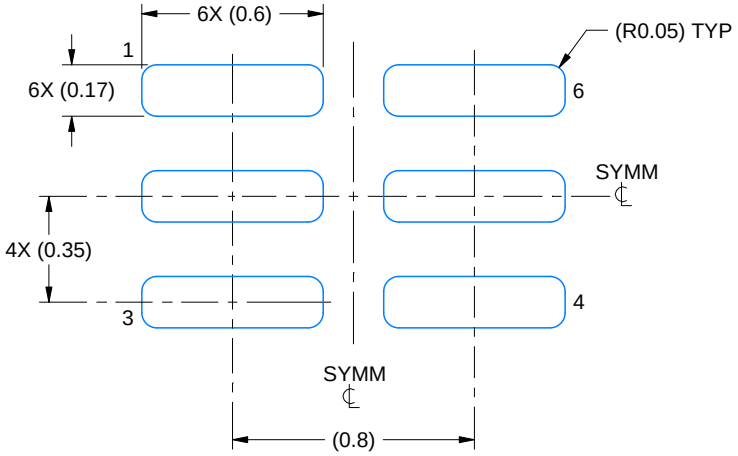
PLASTIC SMALL OUTLINE - NO LEAD



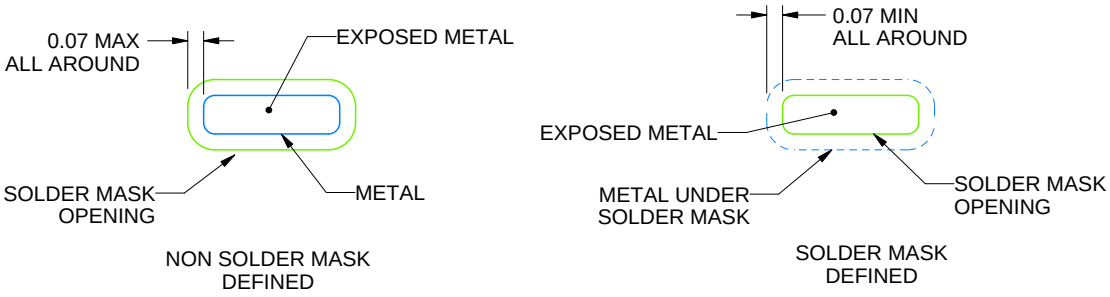
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

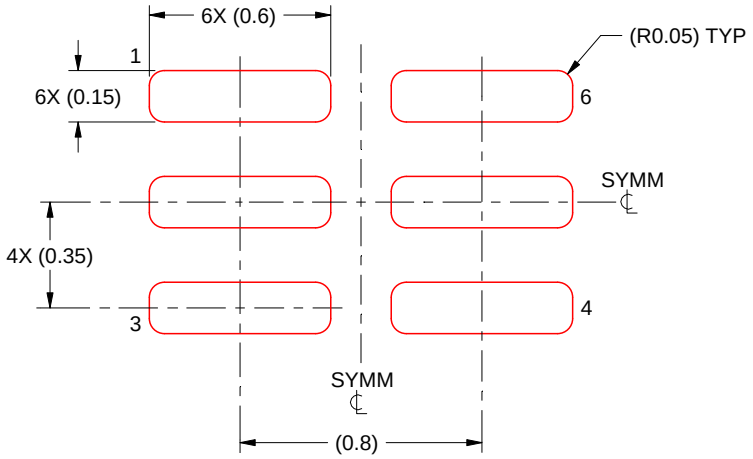
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

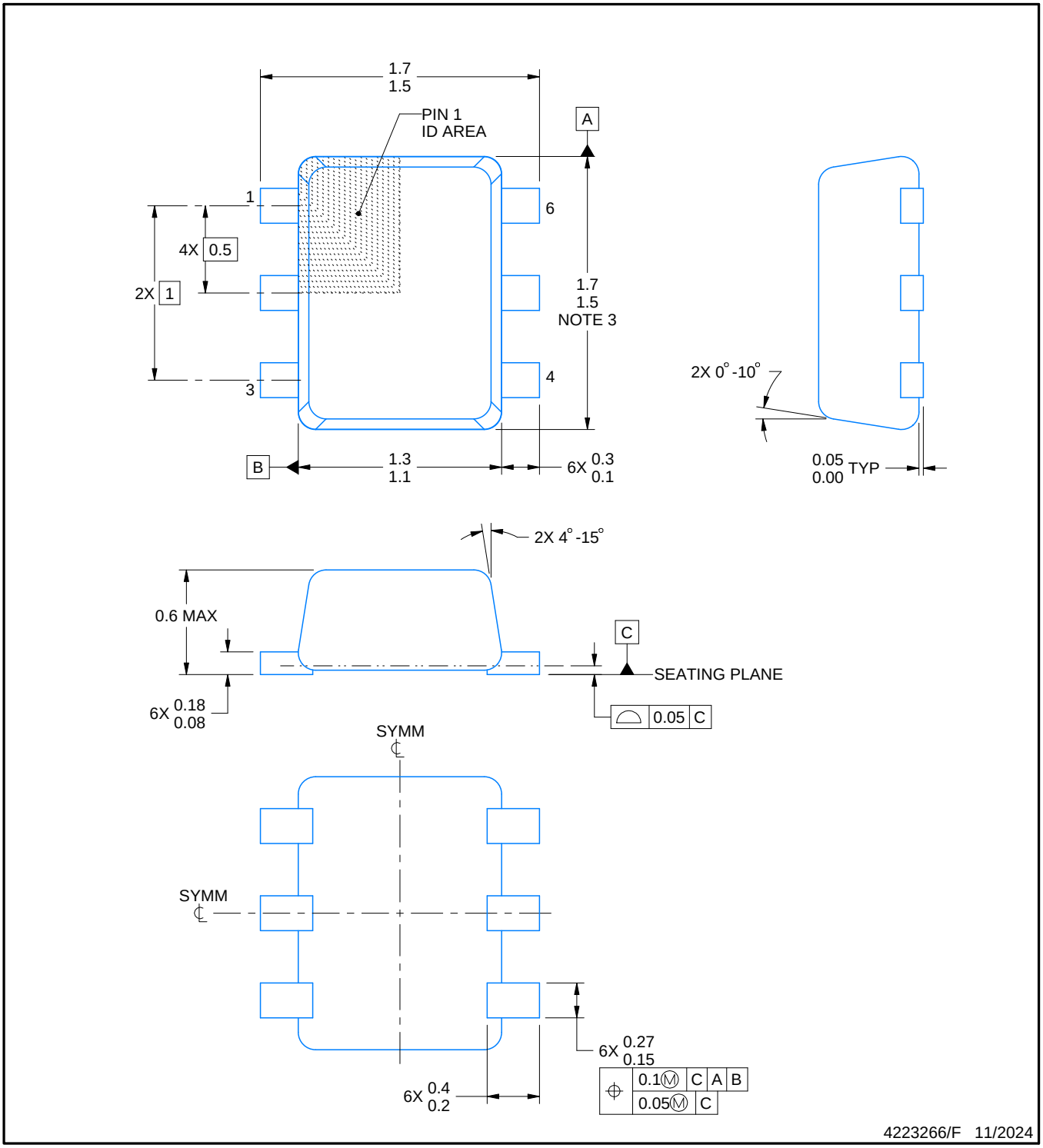


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

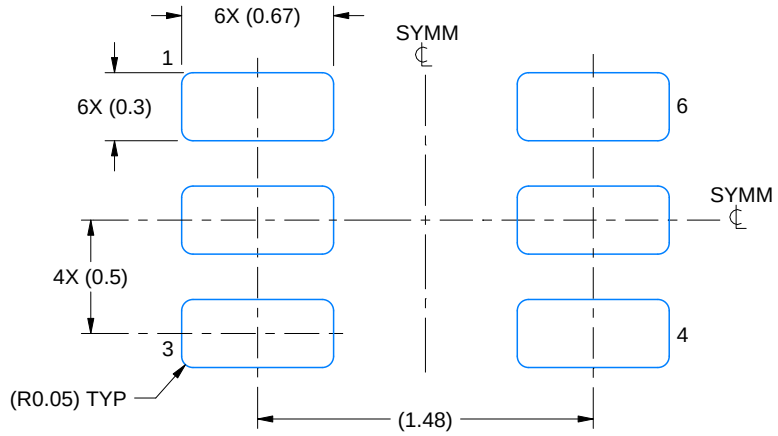
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

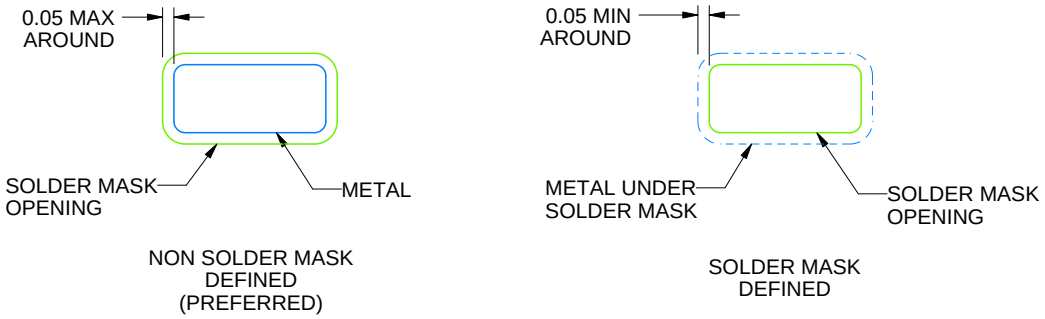
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

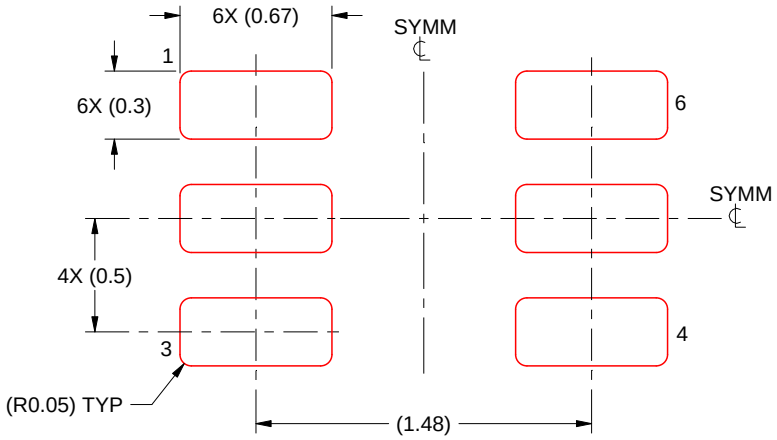
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

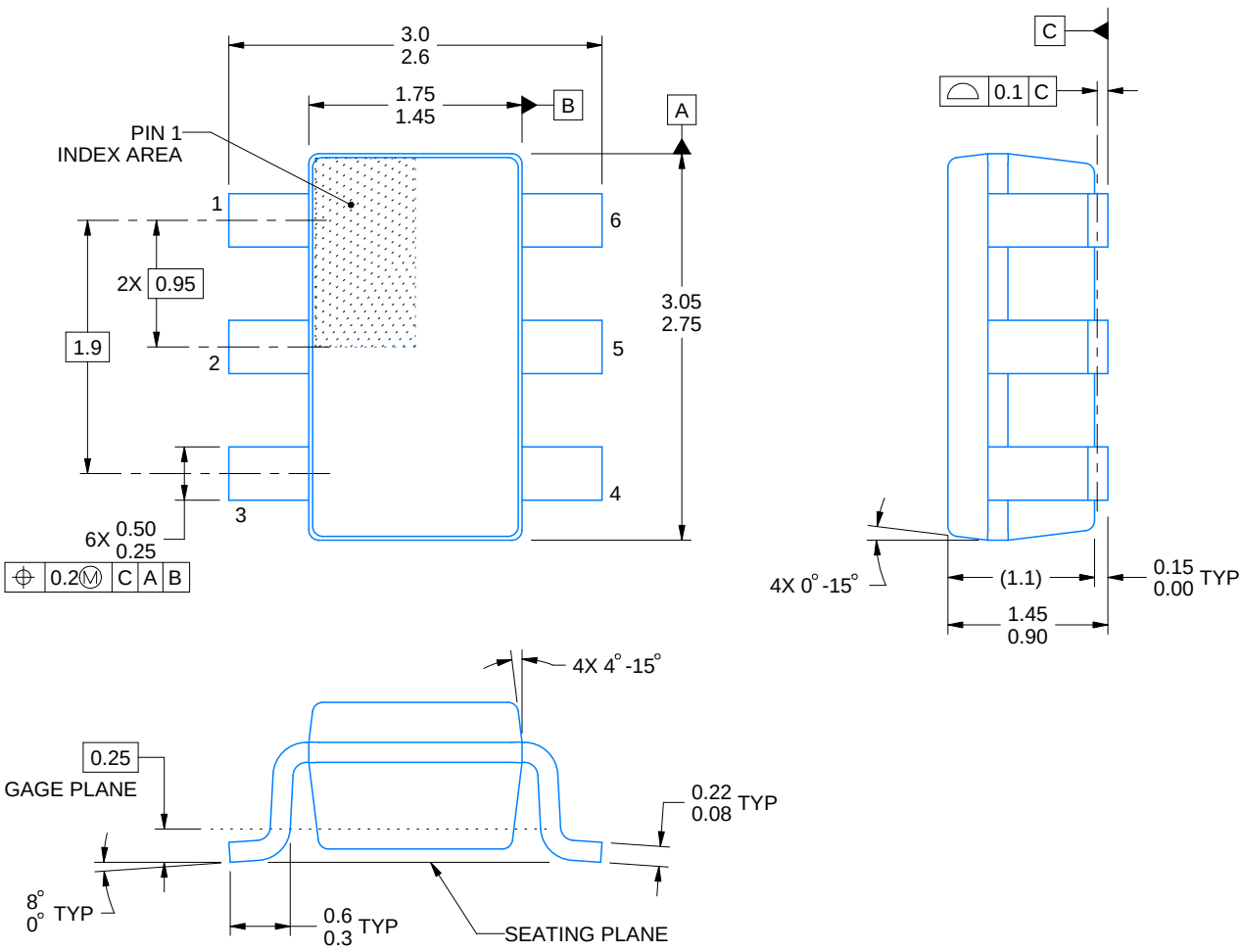
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

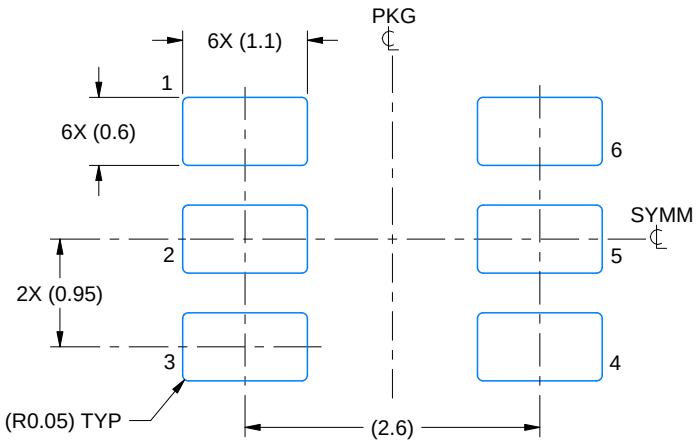
SMALL OUTLINE TRANSISTOR



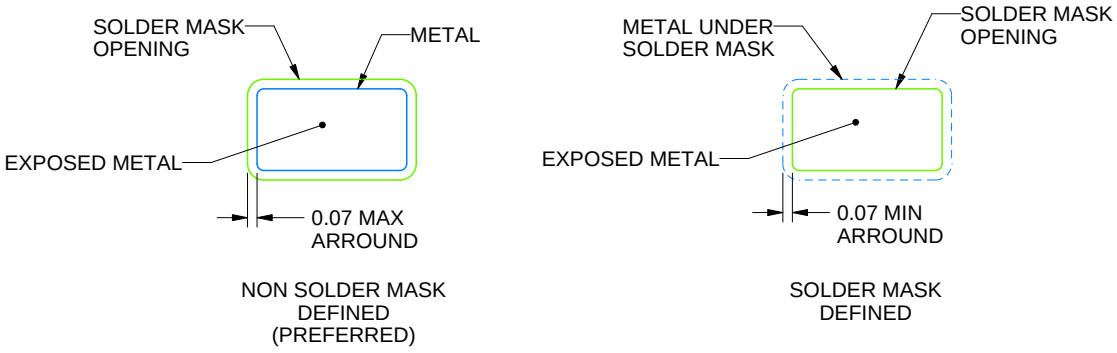
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

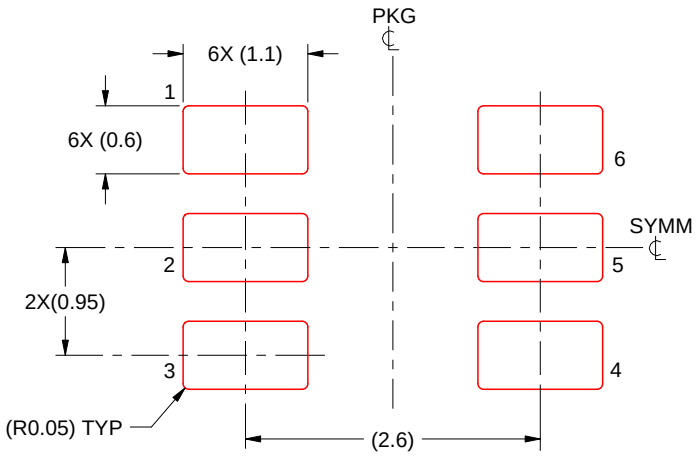


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

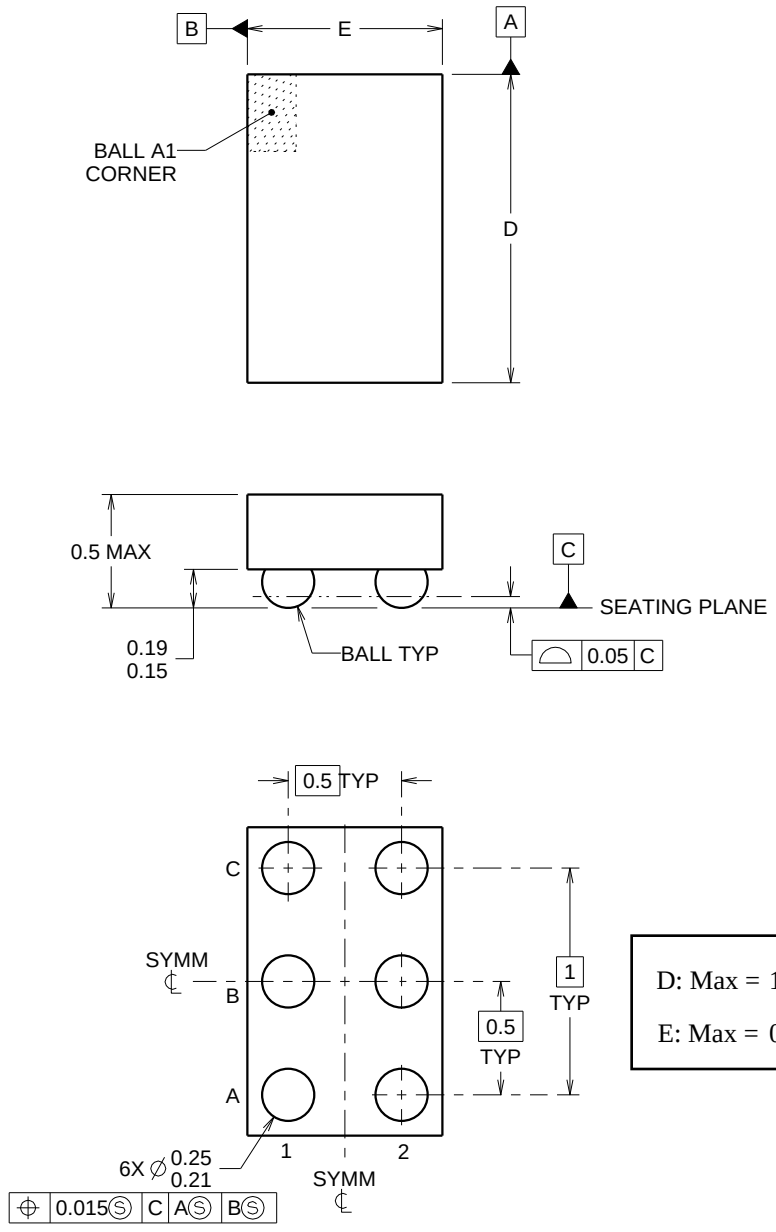
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

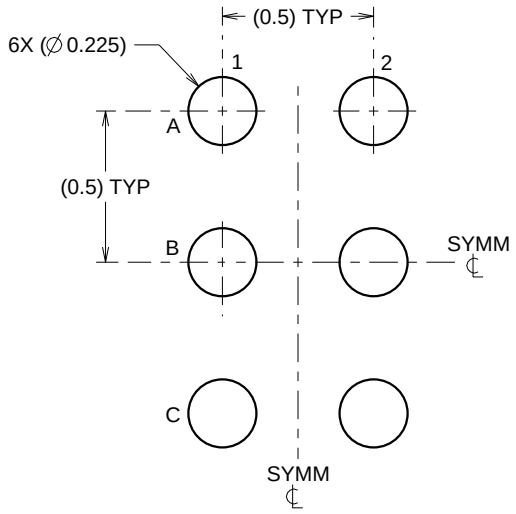
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

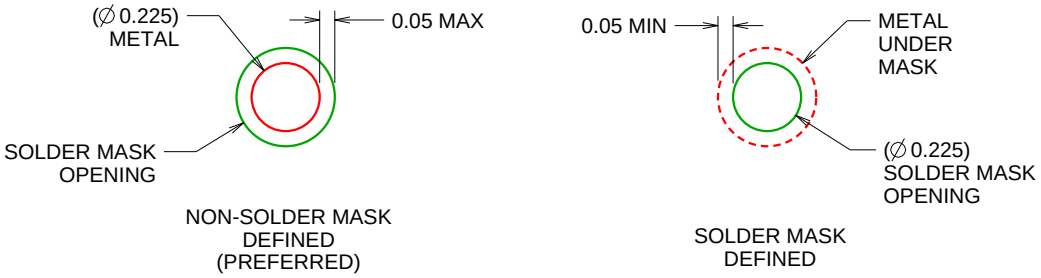
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

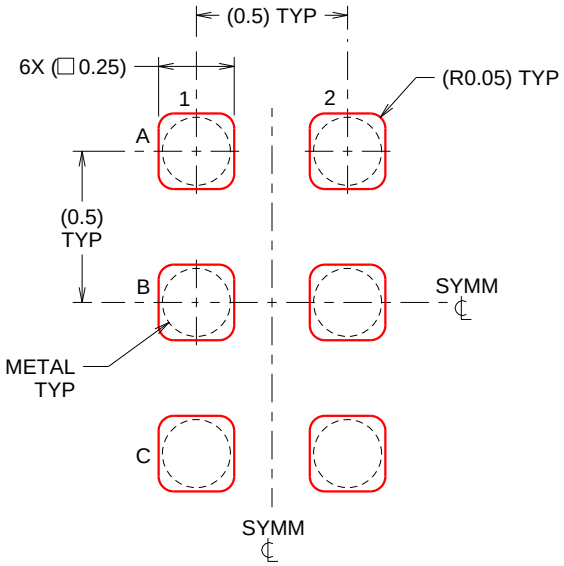


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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