







SN74LVC1G74 SCES794G - OCTOBER 2009 - REVISED SEPTEMBER 2021

SN74LVC1G74 Single Positive-Edge-Triggered D-Type Flip-Flop with Clear and Preset

1 Features

- Available in the Texas Instruments NanoFree[™] package
- Supports 5-V V_{CC} operation
- Inputs accept voltages to 5.5-V
- Supports down translation to V_{CC}
- Maximum t_{pd} of 5.9-ns at 3.3-V
- Low power consumption, 10-µA maximum I_{CC}
- ±24-mA output drive at 3.3-V
- Typical V_{OLP} (output ground bounce) $< 0.8-V \text{ at } V_{CC} = 3.3-V, T_A = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2-V \text{ at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- I_{off} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA per JESD 78. class II
- ESD protection exceeds JESD 22
 - 2000-V human-body model
 - 200-V machine model
 - 1000-V charged-device model

2 Applications

- Servers
- LED displays
- Network switch
- Telecom infrastructure
- Motor drivers
- I/O expanders

3 Description

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoFree™ package technology is a breakthrough in IC packaging concepts, using the die as the package.

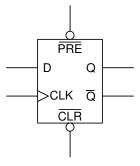
A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE									
	SM8 (8)	2.95 mm × 2.80 mm									
SN74LVC1G74	US8 (8)	2.30 mm × 2.00 mm									
SIN/4LVC1G/4	X2SON (8)	1.40 mm × 1.00 mm									
	UQFN (8)	1.50 mm × 1.50 mm									

For all available packages, see the orderable addendum at the end of the data sheet.



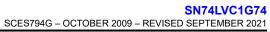
Simplified Schematic



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Changed I _{off} description in <i>Features</i>					
Changed I _{off} description in <i>Features</i>					
• Changed temperature range for DCT and DCU package from (-40°C to 85°C) to (-40°C to 125°C)	Cha	nges from Revision * (October 2009)	to Revisior	n A (November 2011)	Page





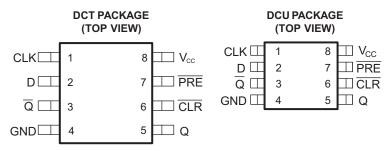


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•	Changed Timing Requirements table	. 7
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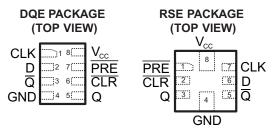


5 Pin Configuration and Functions



See mechanical drawings for dimensions.

Figure 5-1. DCT 8-Pin SM8 and DCU 8-Pin VSSOP Package Top View



See mechanical drawings for dimensions

Figure 5-2. DQE 8-Pin X2SON and RSE UQFN 8-Pin Package Top View

Pin Functions

	PIN	TYPE	DESCRIPTION		
NAME	NO.	ITPE	DESCRIPTION		
CLK	1	I	Clock input		
CLR	6	I	Clear input - Pull low to set Q output low		
D	2	I	Input		
GND	4	_	Ground		
PRE	7	I	Preset input - Pull low to set Q output high		
Q	5	0	Output		
Q	3	0	Inverted output		
V _{CC}	8	_	Supply		

Product Folder Links: SN74LVC1G74

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		·	MI	N MAX	UNIT
V _{CC}	Supply voltage range		-0.	5 6.5	V
VI	Input voltage range ⁽²⁾		-0.	5 6.5	V
Vo	Voltage range applied to any output in the high-impedance or	power-off state ⁽²⁾	-0.	5 6.5	V
Vo	Voltage range applied to any output in the high or low state ⁽²⁾	-0.	5 V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CC} or GND		±100	mA	
T _{stg}	Storage temperature range		-6	5 150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

	PARAMETER	DEFINITION	VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000	V
V _{(E}	(SD) Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

⁽³⁾ The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT	
.,	Cumply welfers	Operating	1.65	5.5	V	
V _{CC}	Supply voltage	Data retention only	1.5		V	
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}			
.,	High level in motor life and	V _{CC} = 2.3 V to 2.7 V	1.7		V	
V_{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	2		V	
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}			
		V _{CC} = 1.65 V to 1.95 V				
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Low level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V	
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		0.8	V	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}		
VI	Input voltage		0	5.5	V	
Vo	Output voltage		0	V _{CC}	V	
		V _{CC} = 1.65 V		-4		
		V _{CC} = 2.3 V		-8		
I _{OH}	High-level output current			-16	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 4.5 V		-32		
		V _{CC} = 1.65 V		4		
		V _{CC} = 2.3 V		8		
I _{OL}	Low-level output current			16	mA	
		V _{CC} = 3 V		24		
		V _{CC} = 4.5 V		32		
		V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20		
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		V _{CC} = 5 V ± 0.5 V		5		
		RSE Package	10	0.5		
_		DQE Package	-40	85	0.0	
T _A	Operating free-air temperature	DCT Package	40	0 125	°C	
		DCU Package	-4 0			

¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

6.4 Thermal Information

			SN74LV	/C1G74		
THERMAL METRIC(1)		DCT	DCU	RSE	DQE	UNIT
			8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	227	243	261	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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Product Folder Links: SN74LVC1G74

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

Р	ARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP(1) MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 5.5 V	V _{CC} – 0.1	
		I _{OH} = –4 mA	1.65 V	1.2	
\ <u>\</u>		I _{OH} = -8 mA	2.3 V	1.9	V
V _{OH}		I _{OH} = -16 mA	3 V	2.4	V
		I _{OH} = -24 mA	3 V	2.3	
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8	
		I _{OL} = 100 μA	1.65 V to 5.5 V	0.1	
		I _{OL} = 4 mA	1.65 V	0.45	
V		I _{OL} = 8 mA	2.3 V	0.3	V
V _{OL}		I _{OL} = 16 mA	- 3 V	0.4	•
		I _{OL} = 24 mA		0.55	
		I _{OL} = 32 mA	4.5 V	0.55	
I	Data or control inputs	V _I = 5.5 V or GND	0 to 5.5 V	±5	μΑ
I _{off}		V_I or $V_O = 5.5 \text{ V}$	0	±10	μA
I _{CC}		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V	10	μΑ
ΔI_{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V	500	μΑ
Ci		V _I = V _{CC} or GND	3.3 V	5	pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

		-40°C to 85°C								-40°C to 125°C					
PARAMETE R	FROM (INPUT)	(OUTPUT)	V _{CC} =	1.8 V	V _{CC} =	2.5 V	V _{CC} =	3.3 V	V _{cc} =	5 V	V _{CC} =	3.3 V	V _{cc} =	5 V	UNIT
	,	,	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}				80		175		175		200		175		200	MHz
+	С	LK	6.2		2.7		2.7		2		2.7		2		no
t _w	PRE or	CLR low	6.2		2.7		2.7		2		2.7		2		ns
+	D	ata	2.9		1.7		1.3		1.1		1.3		1.1		no
Lsu	PRE or C	LR inactive	1.9		1.4		1.2		1		1.2		1.2		ns
t _h			0		0.3		1.2		0.5		1.2		0.5		ns

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

		FROM TO (INPUT)	–40°C to 85°C							-	-40°C to	125°C			
PARAMETE R	-		V _{CC} =	V _{CC} = 1.8 V V _{CC} = 2.5 V		V _{CC} =	3.3 V	V _{CC} =	5 V	V _{CC} =	3.3 V	V _{CC} = 5 V		UNIT	
		(33.1.3.)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			80		175		175		200		175		200		MHz
	CLK	Q	4.8	13.4	2.2	7.1	2.2	5.9	1.4	4.1	2.2	7.9	1.4	6.1	
t _{pd}	CLK	Q	6	14.4	3	7.7	2.6	6.2	1.6	4.4	2.6	8.2	1.6	6.4	ns
	PRE or CLR low	Q or Q	4.4	12.9	2.3	7	1.7	5.9	1.6	4.1	1.7	7.9	1.6	6.1	



6.8 Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	$V_{CC} = 5 V$	UNIT
	PARAINETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNII
C_{pd}	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF

6.9 Typical Characteristics

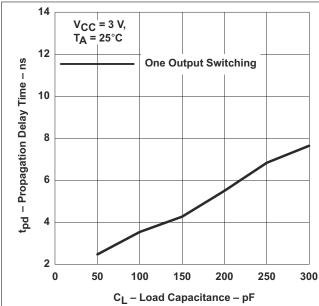


Figure 6-1. Propagation Delay (Low to High Transition)
vs Load Capacitance

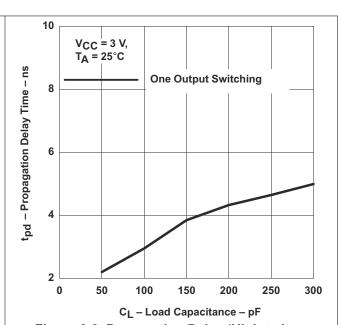


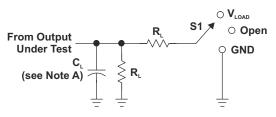
Figure 6-2. Propagation Delay (High to Low Transition)
vs Load Capacitance

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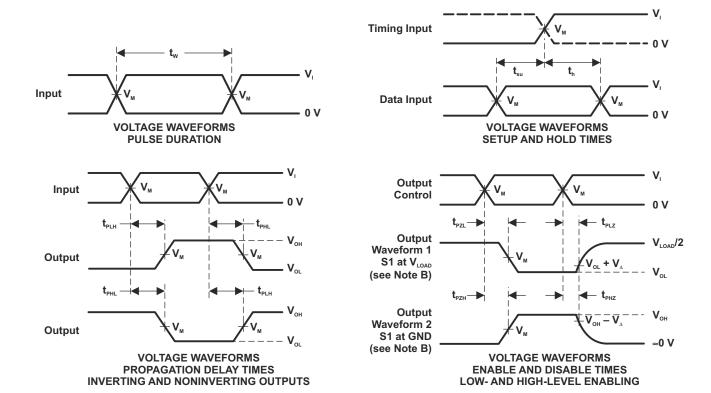
7 Parameter Measurement Information



TEST	S1
$t_{_{PLH}}/t_{_{PHL}}$	Open
$t_{_{PLZ}}/t_{_{PZL}}$	V _{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

V	INF	PUTS	V	V		_	\ \ \	
V _{cc}	V,	t,/t,	V _M	V _{LOAD}	C _L	R _∟	V_{Δ}	
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	1 k Ω	0.15 V	
2.5 V ± 0.2 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	30 pF	500 Ω	0.15 V	
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
5 V ± 0.5 V	V _{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	50 pF	500 Ω	0.3 V	



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{o} = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\mbox{\tiny PLZ}}$ and $\dot{t}_{\mbox{\tiny PHZ}}$ are the same as $t_{\mbox{\tiny dis}}.$
- F. $t_{\mbox{\tiny PZL}}$ and $t_{\mbox{\tiny PZH}}$ are the same as $t_{\mbox{\tiny en}}.$
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

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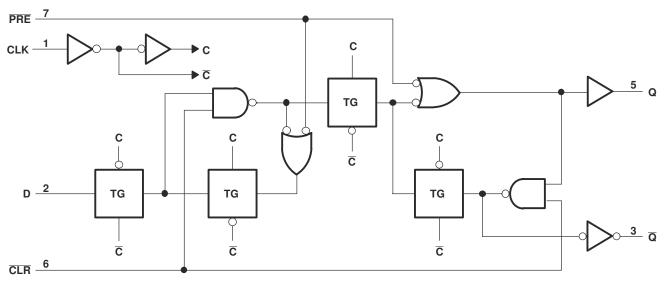
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8 Detailed Description

8.1 Overview

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



8.3 Feature Description

- · Allow down voltage translation
 - 5-V to 3.3-V
 - 5.0-V to 1.8-V
 - 3.3-V to 1.8-V
- · Inputs accept voltage levels up to 5.5-V
- I_{off} Feature
 - Can prevent backflow current that can damage device when powered down

8.4 Device Functional Modes

Table 8-1. Function Table

	INPUT	OUTP	UTS		
PRE	CLR	CLK	D	Q	Q
L	Н	X	Х	Н	L
Н	L	X	X	L	Н
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
Н	Н	↑	Н	Н	L
Н	Н	↑	L	L	Н
Н	Н	L	X	Q_0	\overline{Q}_0

(1) This configuration is nonstable; that is, it does not persist when \overline{PRE} or \overline{CLR} returns to its inactive (high) level.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) input sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The 330 Ω resistor and 22 pF capacitor shown in Figure 9-1 produce enough delay to meet the hold time requirement of the D input. To calculate the delay for a particular RC combination, use Equation 1. The delay with this RC combination is 5.03 ns

$$t_{\text{delav}} = -\text{RC In}(0.5) \approx 0.693 \text{ RC} \tag{1}$$

To ensure proper operation, check that the transition time of the RC circuit meets the transition time requirements of the device inputs listed in the Recommended Operating Conditions table. Transition time for an RC can be approximated with Equation 2.

$$t_l \approx 2.2 \text{ RC}$$
 (2)

9.2 Typical Power Button Circuit

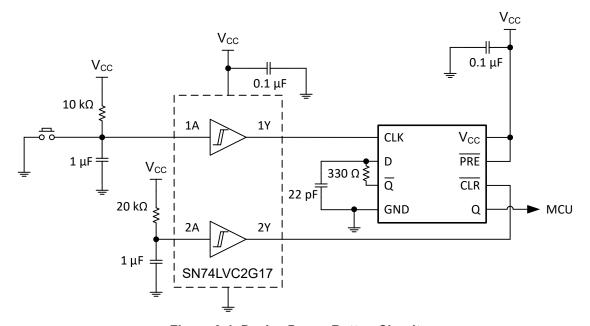


Figure 9-1. Device Power Button Circuit

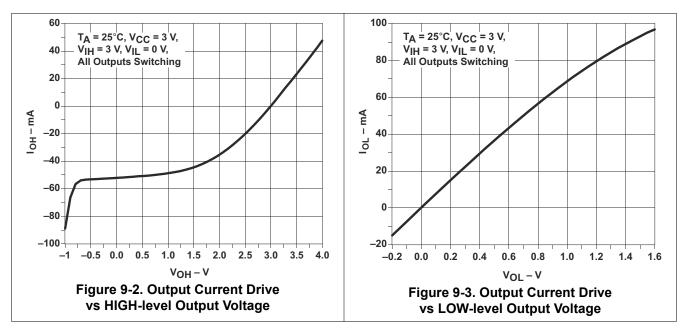
9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- 1. Recommended Input Conditions:
 - For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in the *Recommended Operating Conditions* table.
 - For specified high and low levels, see (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5-V at any valid V_{CC} .
- 2. Recommend Output Conditions:
 - Load currents should not exceed 50-mA per output and 100-mA total for the part.
 - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommonded Operating Conditions* table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended and if there are multiple V_{CC} terminals then .01- μ F or .022- μ F capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

11.2 Layout Example

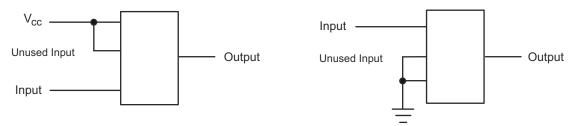


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
SN74LVC1G74DCTR	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(2WE5, N74) Z
SN74LVC1G74DCTR.B	Active	Production	SSOP (DCT) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(2WE5, N74) Z
SN74LVC1G74DCUR	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(N74J, N74Q, N74R)
SN74LVC1G74DCUR.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(N74J, N74Q, N74R)
SN74LVC1G74DCURG4	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N74R
SN74LVC1G74DCURG4.B	Active	Production	VSSOP (DCU) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	N74R
SN74LVC1G74DCUT	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(N74J, N74Q, N74R)
SN74LVC1G74DCUT.B	Active	Production	VSSOP (DCU) 8	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(N74J, N74Q, N74R)
SN74LVC1G74DQER	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74DQER.B	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74DQERG4	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74DQERG4.B	Active	Production	X2SON (DQE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74RSE2	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74RSE2.B	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74RSE2G4	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74RSE2G4.B	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74RSER	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74RSER.B	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74RSERG4	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP
SN74LVC1G74RSERG4.B	Active	Production	UQFN (RSE) 8	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DP

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

PACKAGE OPTION ADDENDUM

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- (3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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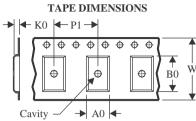
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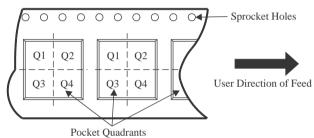
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

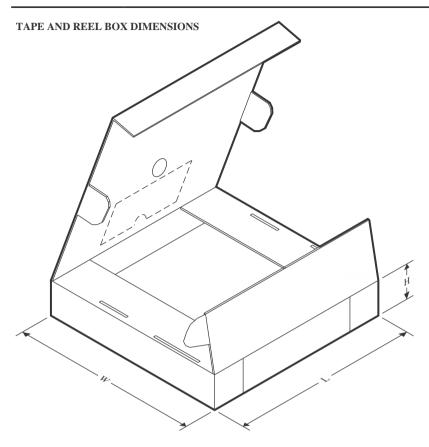


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G74DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1G74DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G74DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G74DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G74DQER	X2SON	DQE	8	5000	180.0	9.5	1.15	1.6	0.5	4.0	8.0	Q1
SN74LVC1G74DQERG4	X2SON	DQE	8	5000	180.0	9.5	1.15	1.6	0.5	4.0	8.0	Q1
SN74LVC1G74RSE2	UQFN	RSE	8	5000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q3
SN74LVC1G74RSE2G4	UQFN	RSE	8	5000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q3
SN74LVC1G74RSER	UQFN	RSE	8	5000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q2
SN74LVC1G74RSERG4	UQFN	RSE	8	5000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q2



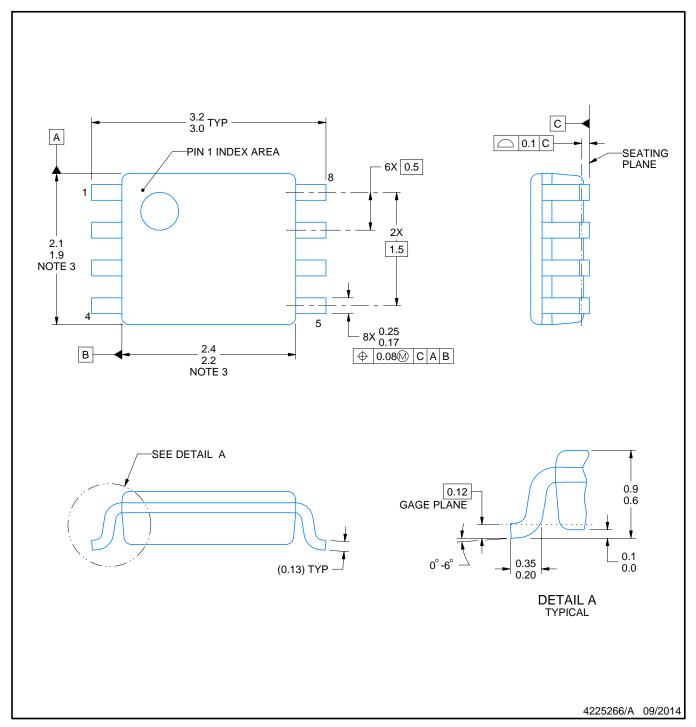
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*All dimensions are nominal

7 til dilitionolorio al o mominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G74DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC1G74DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC1G74DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G74DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC1G74DQER	X2SON	DQE	8	5000	184.0	184.0	19.0
SN74LVC1G74DQERG4	X2SON	DQE	8	5000	184.0	184.0	19.0
SN74LVC1G74RSE2	UQFN	RSE	8	5000	184.0	184.0	19.0
SN74LVC1G74RSE2G4	UQFN	RSE	8	5000	184.0	184.0	19.0
SN74LVC1G74RSER	UQFN	RSE	8	5000	184.0	184.0	19.0
SN74LVC1G74RSERG4	UQFN	RSE	8	5000	184.0	184.0	19.0





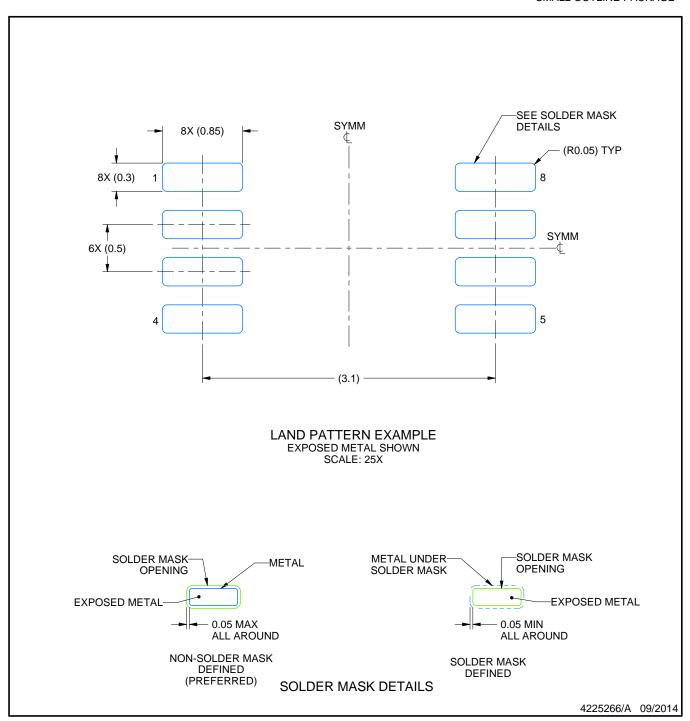
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-187 variation CA.

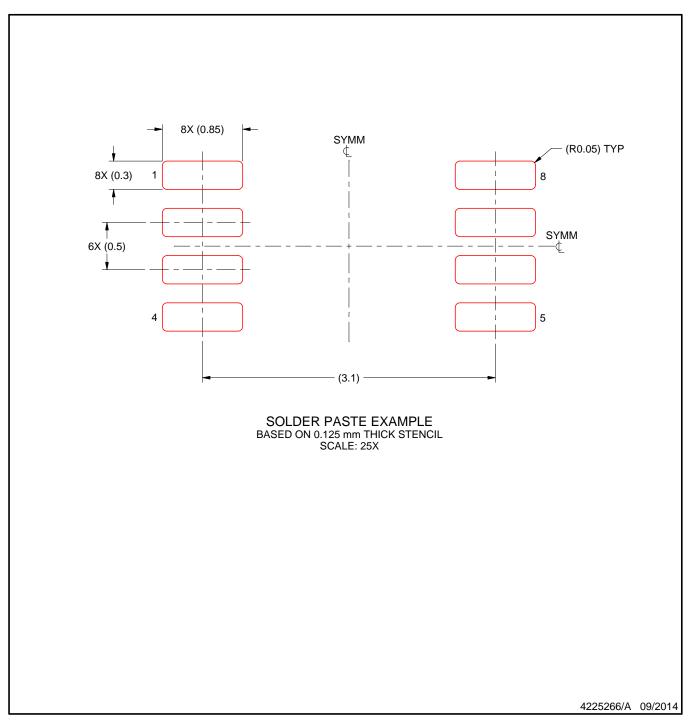




NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



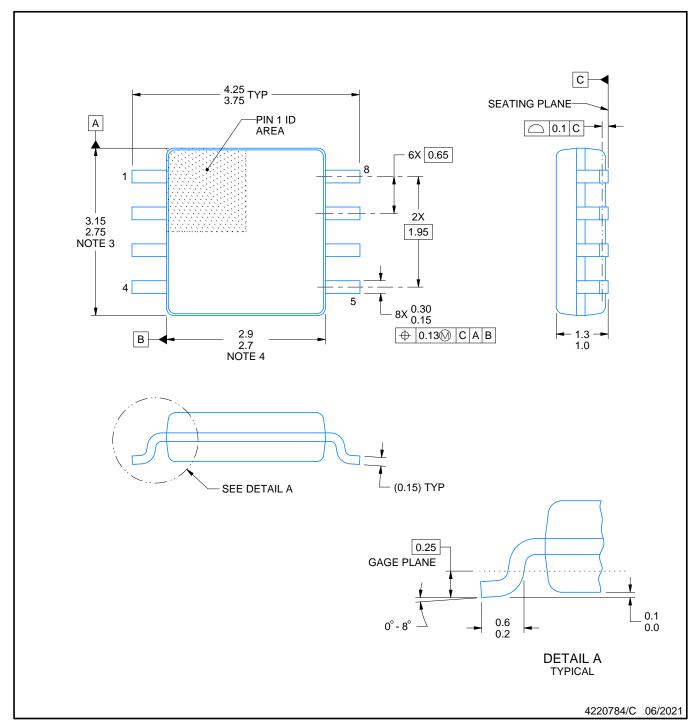


NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.







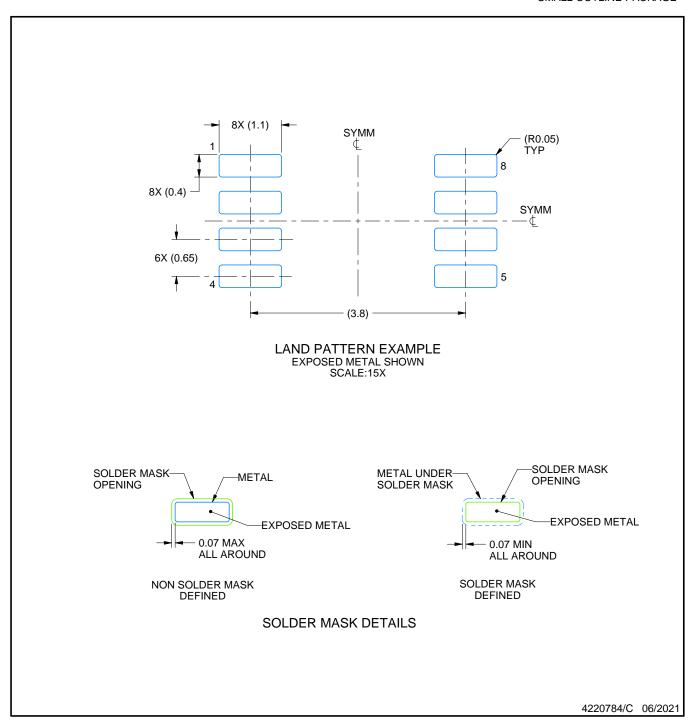
NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

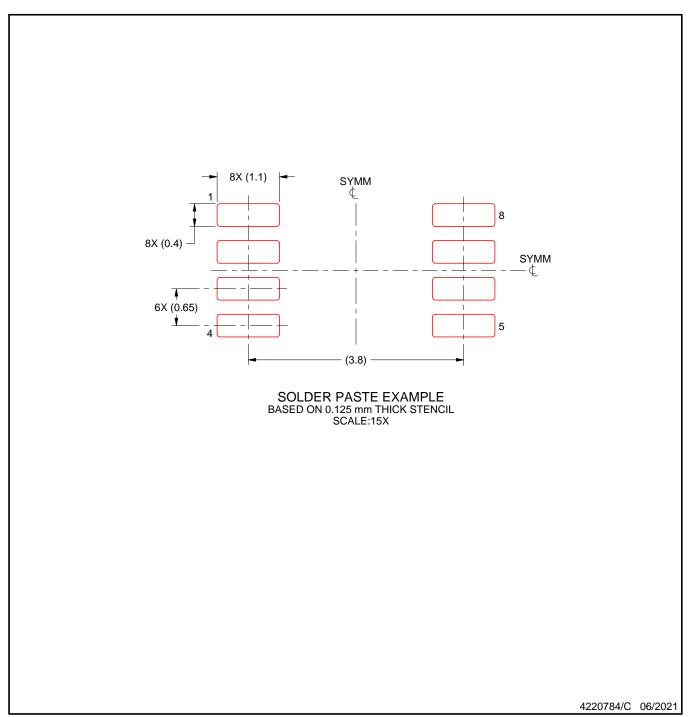




NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





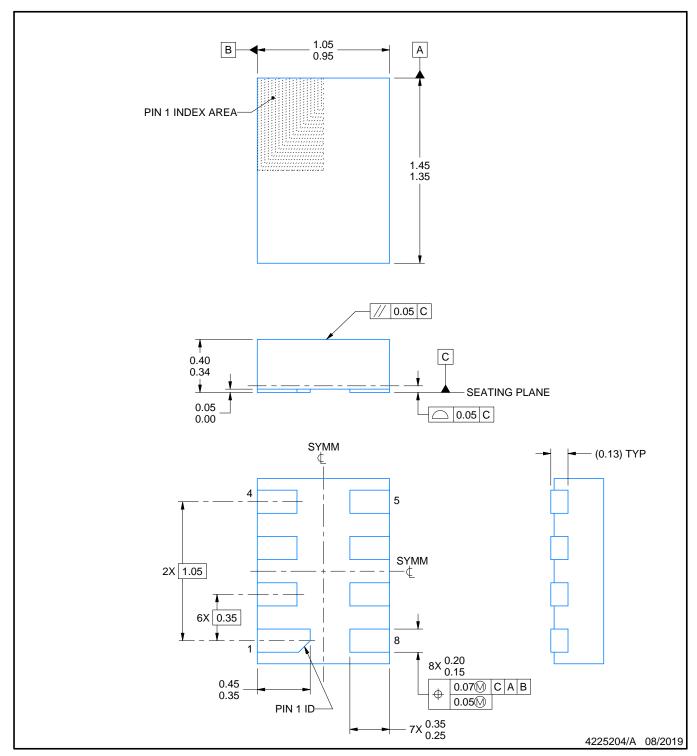
NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

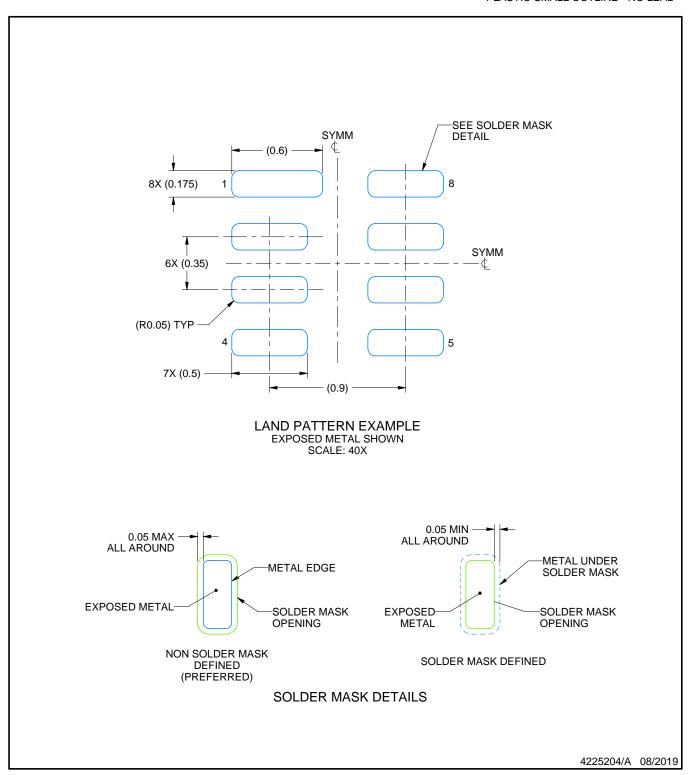
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This package complies to JEDEC MO-287 variation X2EAF.



PLASTIC SMALL OUTLINE - NO LEAD

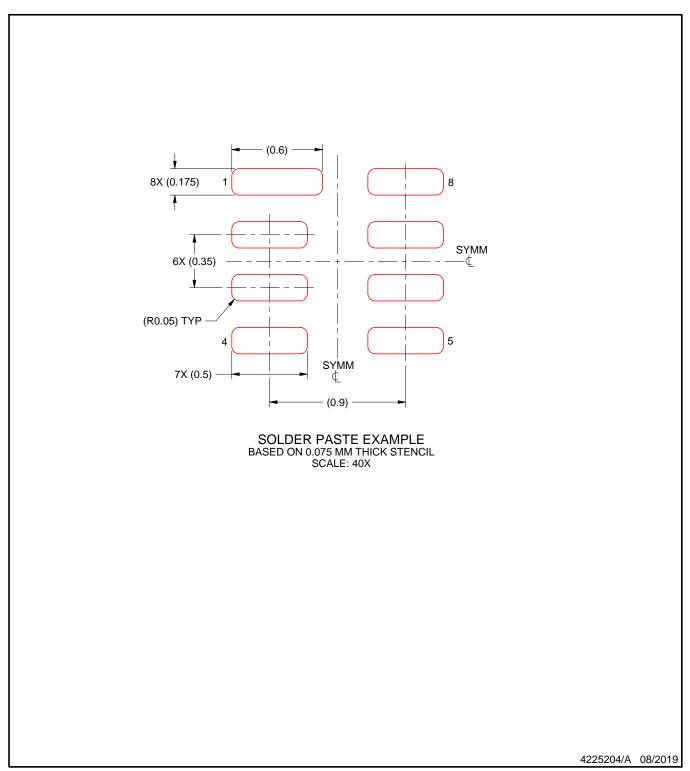


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC SMALL OUTLINE - NO LEAD



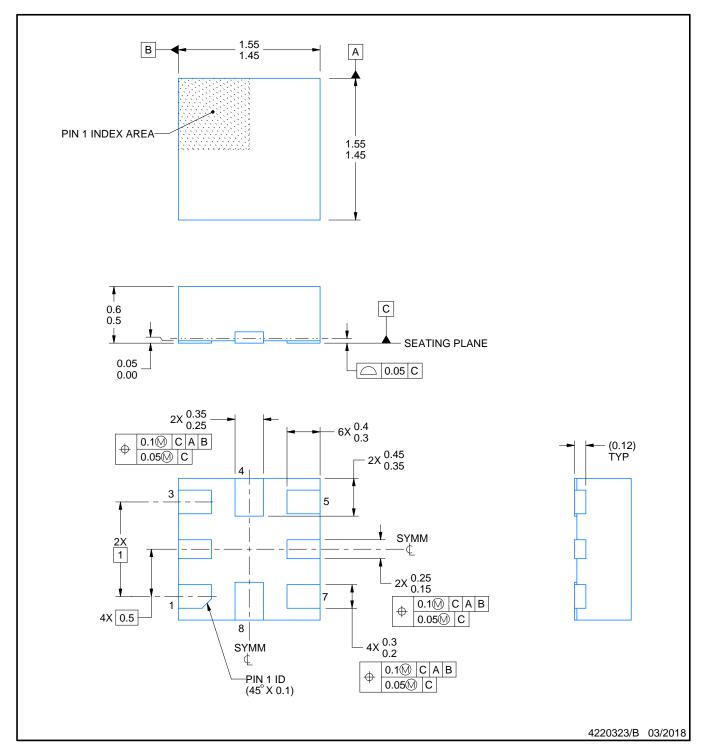
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





PLASTIC QUAD FLATPACK - NO LEAD

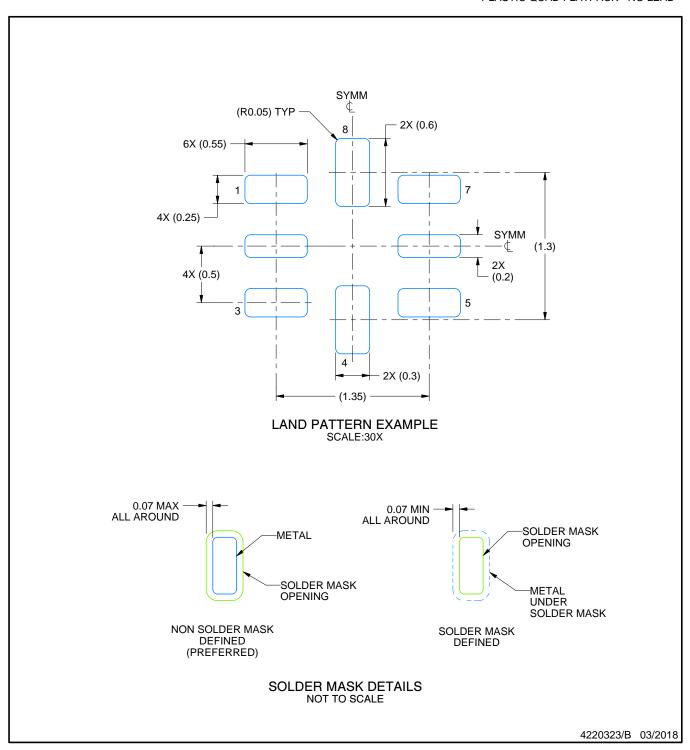


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.



PLASTIC QUAD FLATPACK - NO LEAD

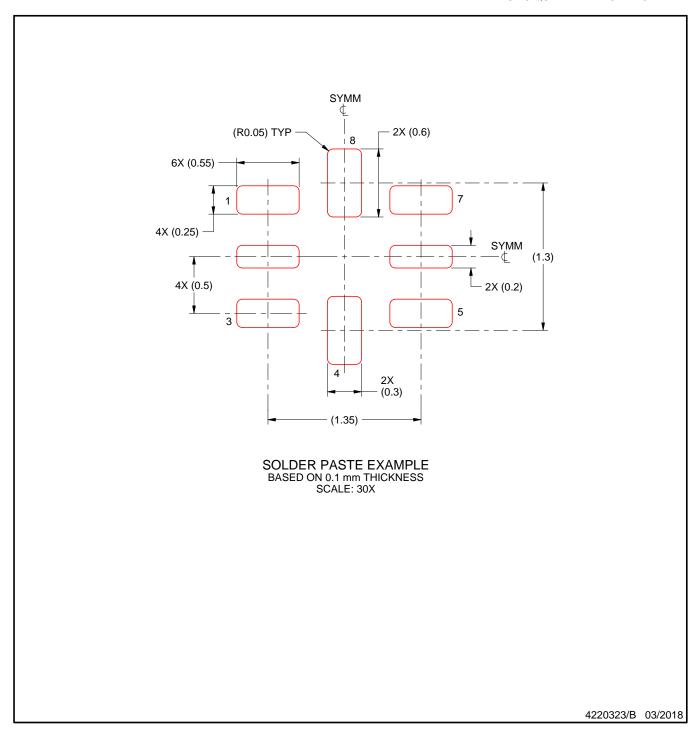


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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