

SN74LVC1G79B-Q1 Automotive Single D-Type Flip-Flop

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Operating range from 1.1V to 5.5V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Supports **partial-power-down** with back drive protection (I_{off})
- High push-pull output drive strength:
 - $\pm 32\text{mA}$ at 5V
 - $\pm 24\text{mA}$ at 3.3V
 - $\pm 8\text{mA}$ at 2.5V
 - $\pm 4\text{mA}$ at 1.8V
- Maximum propagation delay of 3.9ns at 5V
- Latch-up performance exceeds 100mA per JESD78 and AEC-Q100-004

2 Applications

- Test and measurement
- Enterprise switching
- Telecom infrastructure
- Motor drives

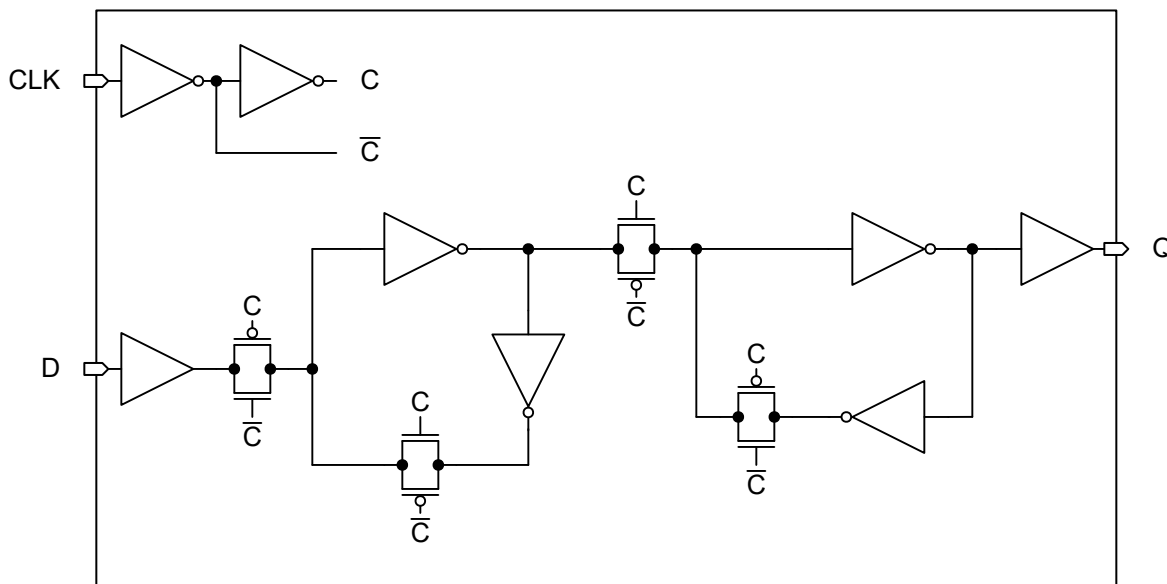
3 Description

The SN74LVC1G79B-Q1 is a single positive-edge-triggered D-type flip-flop. The logic value at the data input (D) is stored on the positive-going edge of the clock pulse (CLK) and output at the non-inverting output (Q).

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74LVC1G79B-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DTX (X2SON, 5)	1.1mm × 0.85mm	1.1mm × 0.85mm

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



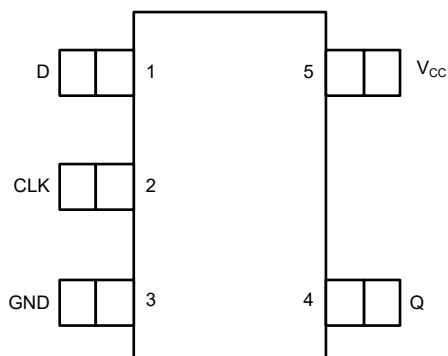
Logic Diagram



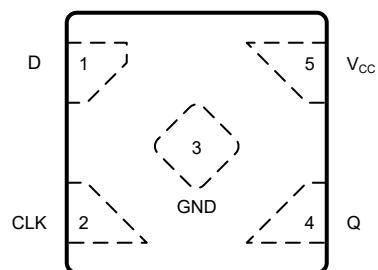
Table of Contents

1 Features	1	7.3 Feature Description.....	11
2 Applications	1	7.4 Device Functional Modes.....	13
3 Description	1	8 Application and Implementation	14
4 Pin Configuration and Functions	3	8.1 Application Information.....	14
5 Specifications	4	8.2 Typical Application.....	14
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	16
5.2 ESD Ratings.....	4	8.4 Layout.....	16
5.3 Recommended Operating Conditions.....	4	9 Device and Documentation Support	18
5.4 Thermal Information.....	5	9.1 Documentation Support.....	18
5.5 Electrical Characteristics.....	5	9.2 Receiving Notification of Documentation Updates....	18
5.6 Timing Characteristics	5	9.3 Support Resources.....	18
5.7 Switching Characteristics	6	9.4 Trademarks.....	18
5.8 Typical Characteristics.....	7	9.5 Electrostatic Discharge Caution.....	18
6 Parameter Measurement Information	9	9.6 Glossary.....	18
7 Detailed Description	11	10 Revision History	18
7.1 Overview.....	11	11 Mechanical, Packaging, and Orderable Information	19
7.2 Functional Block Diagram.....	11		

4 Pin Configuration and Functions



**Figure 4-1. DBV Package,
5-Pin SOT-23 (Top View)**



**Figure 4-2. DTX Package,
5-Pin X2SON (Transparent Top View)**

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	D	I	Data Input
2	CLK	I	Clocking Input
3	GND	G	Ground Pin
4	Q	O	Flip-flop Output
5	V _{CC}	P	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Supply, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0V		-50 mA
I _{OK}	Output clamp current	V _O < 0V		-50 mA
I _O	Continuous output current			±50 mA
I _O	Continuous output current through V _{CC} or GND			±100 mA
T _J	Junction temperature			150 °C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.1	5.5	V
V _I	Input voltage	0	5.5	V
V _O	Output voltage	High or low state	V _{CC}	V
V _{IH}	High-level input voltage	V _{CC} = 1.1V to 1.95V	0.65x V _{CC}	V
		V _{CC} = 2.3V to 2.7V	1.7	
		V _{CC} = 3V to 3.3V	2	
		V _{CC} = 4.5V to 5.5V	0.7x V _{CC}	
V _{IL}	Low-Level input voltage	V _{CC} = 1.1V to 1.95V	0.35x V _{CC}	V
		V _{CC} = 2.3V to 2.7V	0.7	
		V _{CC} = 3V to 3.3V	0.8	
		V _{CC} = 4.5V to 5.5V	0.3x V _{CC}	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.1V to 2.7V	20	ns/V
		V _{CC} = 3.3V ± 0.3V	10	
		V _{CC} = 5V ± 0.5V	5	
T _A	Operating free-air temperature	-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
DTX (XSON, 5)	5	393.6	103.2	331.8	69.8	331.9	179.9	°C/W
DBV (SOT-23, 5)	5	357.1	263.7	264.4	195.6	262.2	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = -100μA	1.1V to 5.5V	V _{CC} - 0.1			V
	I _{OH} = -4mA	1.65V	1.2			
	I _{OH} = -8mA	2.3V	1.9			
	I _{OH} = -12mA	2.7V	2.2			
	I _{OH} = -16mA	3V	2.4			
	I _{OH} = -24mA	3V	2.3			
	I _{OH} = -32mA	4.5V	3.8			
V _{OL}	I _{OL} = 100μA	1.1V to 5.5V	0.15			V
	I _{OL} = 4mA	1.65V	0.45			
	I _{OL} = 8mA	2.3V	0.3			
	I _{OL} = 12mA	2.7V	0.4			
	I _{OL} = 16mA	3V	0.4			
	I _{OL} = 24mA	3V	0.55			
	I _{OL} = 32mA	4.5V	0.55			
I _I	V _I = V _{CC} or GND	V _{CC} = 0V to 5.5V	±5			μA
I _{OFF}	V _I or V _O = V _{CC}	V _{CC} = 0V	±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	V _{CC} = 1.1V to 5.5V	10			μA
ΔI _{CC}	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND	3V to 5.5V	500			μA
C _I	V _I = V _{CC} or GND	3.3V	3.5			pF
C _O	V _O = V _{CC} or GND	3.3V	6.3			pF

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V _{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
f _{clock}	Clock frequency		1.2V ± 0.1V	35		MHz
			1.5V ± 0.12V	77		
			1.8V ± 0.15V	142		
			2.5V ± 0.2V	207		
			3.3V ± 0.3V	281		
			5.0V ± 0.5V	388		

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V _{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
t _W	Pulse duration	CLK high or low	1.2V ± 0.1V	9		ns
			1.5V ± 0.12V	3		
			1.8V ± 0.15V	3		
			2.5V ± 0.2V	2		
			3.3V ± 0.3V	2		
			5.0V ± 0.5V	2		
t _{SU}	Setup time	D high before CLK↑	1.2V ± 0.1V	6		ns
			1.5V ± 0.12V	2		
			1.8V ± 0.15V	2		
			2.5V ± 0.2V	1		
			3.3V ± 0.3V	1		
			5.0V ± 0.5V	1		
		D low before CLK↑	1.2V ± 0.1V	16		
			1.5V ± 0.12V	5		
			1.8V ± 0.15V	3		
			2.5V ± 0.2V	2		
			3.3V ± 0.3V	2		
			5.0V ± 0.5V	1		
t _H	Hold time	D after CLK↑	1.2V ± 0.1V	1		ns
			1.5V ± 0.12V	1		
			1.8V ± 0.15V	1		
			2.5V ± 0.2V	1		
			3.3V ± 0.3V	1		
			5.0V ± 0.5V	1		

5.7 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t _{pd}	CLK	Q	C _L = 15pF	1.2V ± 0.1V			62	ns
				1.5V ± 0.12V			13.6	
				1.8V ± 0.15V			9.1	
				2.5V ± 0.2V			5.3	
				3.3V ± 0.3V			3.9	
				5.0V ± 0.5V			3.3	
			C _L = 30pF	1.8V ± 0.15V			9.8	
				2.5V ± 0.2V			5.8	
			C _L = 50pF	3.3V ± 0.3V			4.7	
				5.0V ± 0.5V			3.9	

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
C_{pd}			$f = 10\text{MHz}$	1.8V		11		pF
				2.5V		12		
				3.3V		13		
				5V		15		

5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

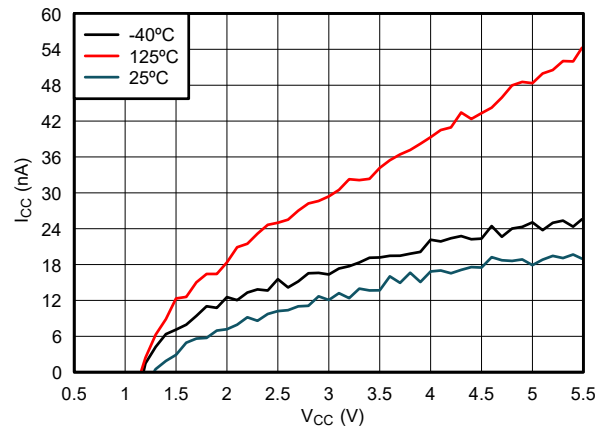


Figure 5-1. Supply Current Across Supply Voltage and Temperature

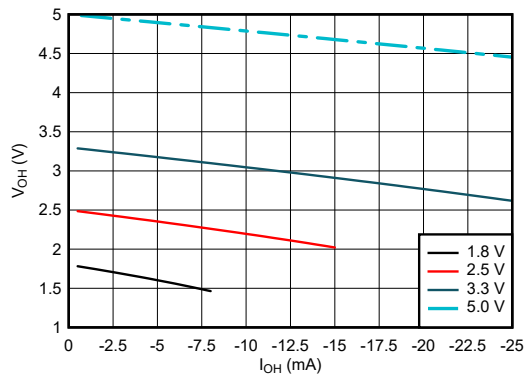


Figure 5-2. Output Voltage vs Current in HIGH State

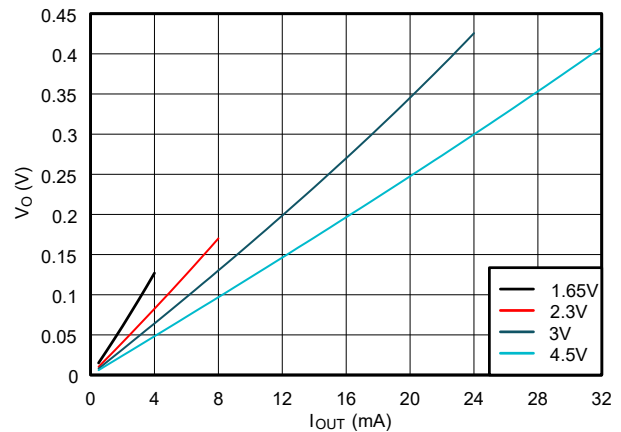


Figure 5-3. Output Voltage vs Current in LOW State

5.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

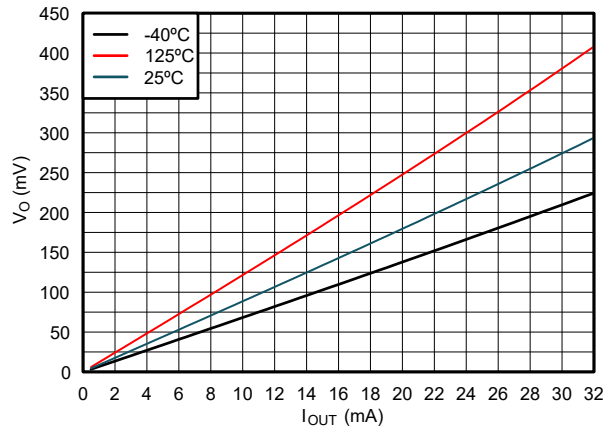


Figure 5-4. Output Voltage vs Current in LOW State; 4.5V Supply

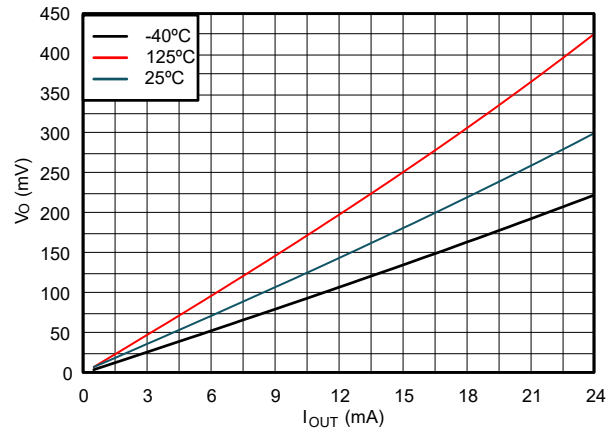


Figure 5-5. Output Voltage vs Current in LOW State; 3V Supply

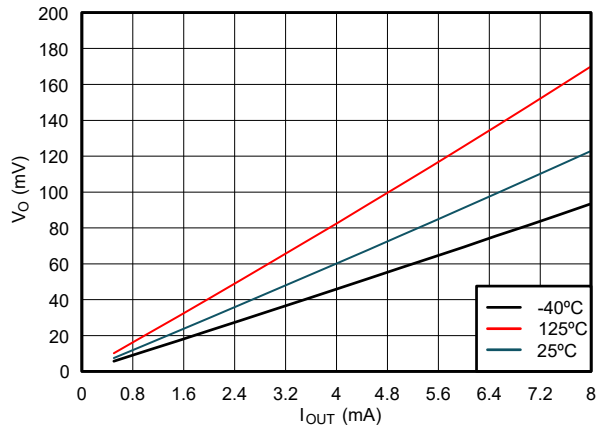


Figure 5-6. Output Voltage vs Current in LOW State; 2.3V Supply

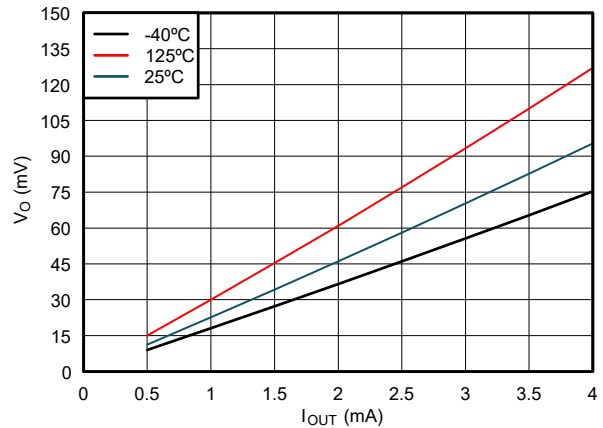


Figure 5-7. Output Voltage vs Current in LOW State; 1.65V Supply

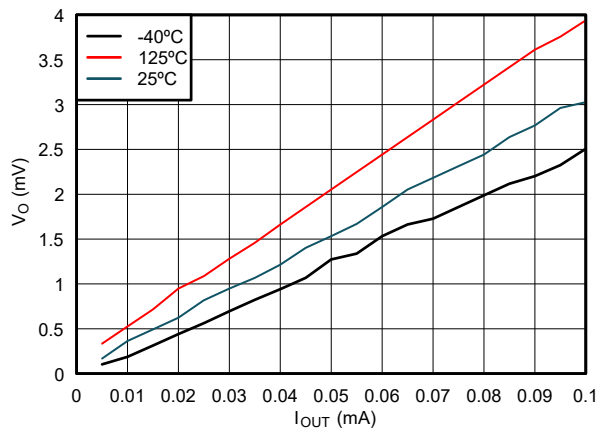


Figure 5-8. Output Voltage vs Current in LOW State; 1.38V Supply

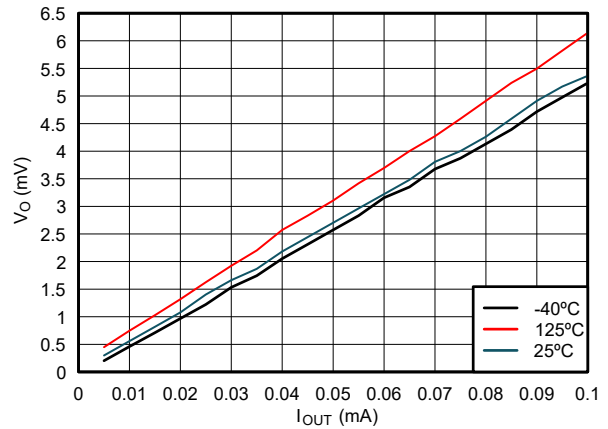


Figure 5-9. Output Voltage vs Current in LOW State; 1.1V Supply

6 Parameter Measurement Information

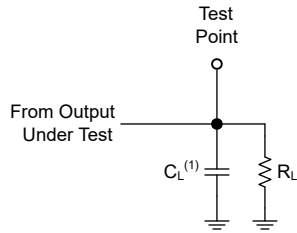
Phase relationships between waveforms are chosen arbitrarily for the examples listed in the following table. Generators with the following characteristics supply all input pulses : $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_f \leq 2.5\text{ns}$.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.

Table 6-1. Push-Pull Outputs

V_{CC}	V_t	R_L	C_L	ΔV
$1.2\text{V} \pm 0.1\text{V}$	$V_{CC}/2$	$2\text{k}\Omega$	15pF	0.1V
$1.5\text{V} \pm 0.12\text{V}$	$V_{CC}/2$	$2\text{k}\Omega$	15pF	0.1V
$1.8\text{V} \pm 0.15\text{V}$	$V_{CC}/2$	$1\text{k}\Omega$	$15\text{pF}/30\text{pF}$	0.15V
$2.5\text{V} \pm 0.2\text{V}$	$V_{CC}/2$	500Ω	$15\text{pF}/30\text{pF}$	0.15V
$3.3\text{V} \pm 0.3\text{V}$	1.5V	500Ω	$15\text{pF}/50\text{pF}$	0.3V
$5.0\text{V} \pm 0.5\text{V}$	1.5V	500Ω	$15\text{pF}/50\text{pF}$	0.3V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

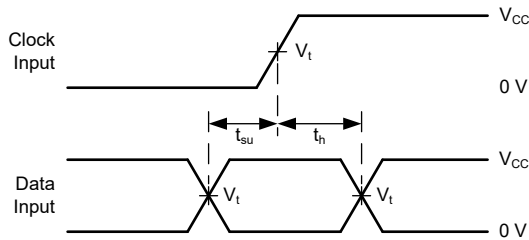


Figure 6-3. Voltage Waveforms, Setup and Hold Times

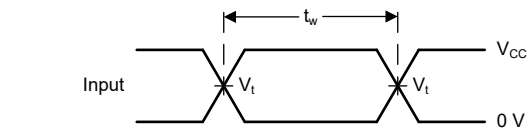
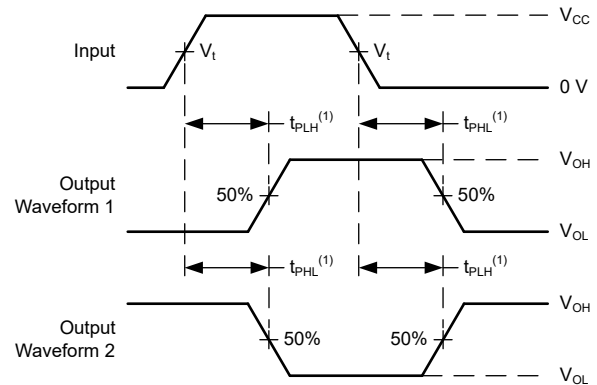
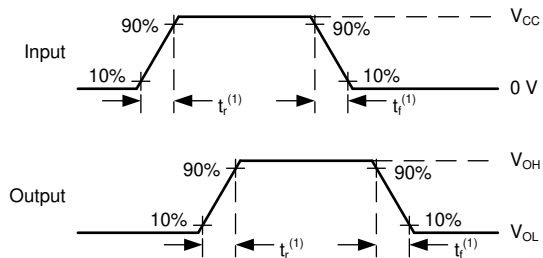


Figure 6-2. Voltage Waveforms, Pulse Duration



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_{tr} .

Figure 6-5. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74LVC1G79B-Q1 is a single positive-edge-triggered D-type flip-flop. Data at the input (D) is transferred to the output (Q) on the positive-going edge of the clock pulse when the setup time requirement is met. The clock triggering occurs at a voltage level, and is not directly related to the rise time of the clock pulse. After the hold-time interval the data at the input can be changed without affecting the level at the output.

7.2 Functional Block Diagram

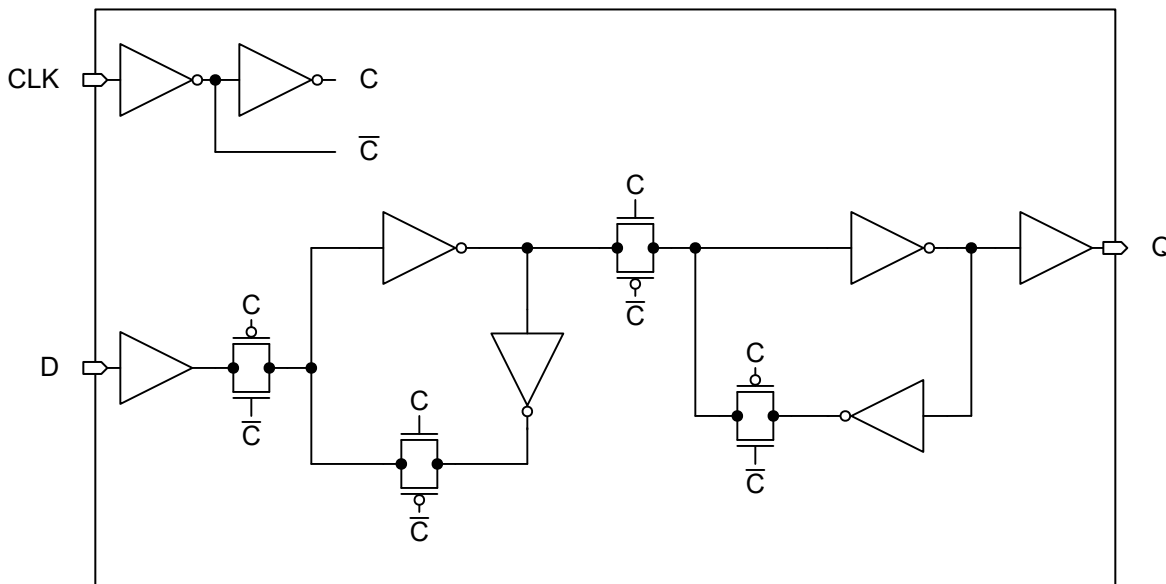


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.4 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10k Ω resistor, however, is recommended and typically meets all requirements.

7.3.5 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

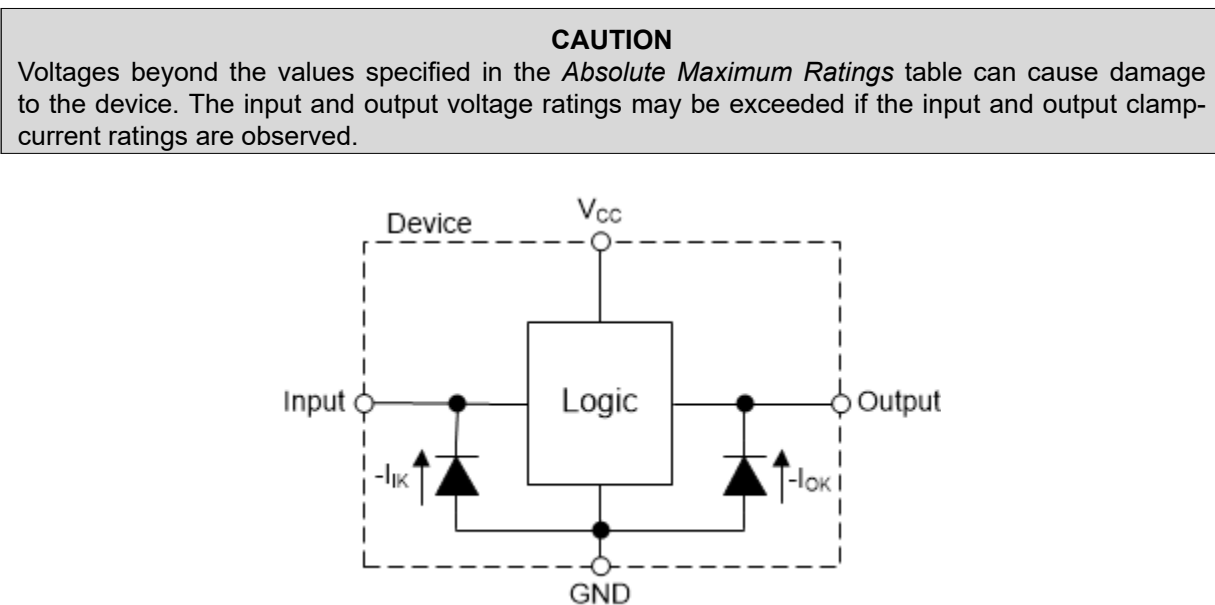


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.6 Over-Voltage Tolerant Inputs

The SN74LVC1G79B-Q1 includes over-voltage tolerant inputs. The input pins support high-state input voltages larger than the supply voltage by utilizing an input protection circuit that does not include a standard positive clamp diode. See *Recommended Operating Conditions* for the recommended input voltage.

CAUTION

Do not exceed the maximum input voltage range provided in *Absolute Maximum Ratings*. Exceeding the maximum input voltage range rating can cause immediate and permanent damage to the device.

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS ⁽¹⁾		OUTPUTS
CLK	D	Q
↑	H	H
↑	L	L
H, L, ↓	X	Q ₀

(1) H = High voltage level, L = Low voltage level, X = Don't care, ↑ = Transition from low to high level, ↓ = Transition from high to low level, Q₀ = Previous output state

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G79B-Q1 is used to store a single bit of data. The example provided in [Figure 8-1](#) uses a microcontroller (MCU) to provide the data and clock inputs; however, these inputs can come from any digital signal source. The output retains the previous state as long as power remains within the recommended operating range provided in the *Recommended Operating Conditions* table.

The output signal has an unknown state at the initial startup, meaning that it can start high or low. Clock in data to make the output deterministic.

8.2 Typical Application

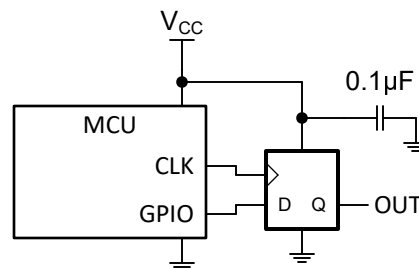


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC1G79B-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G79B-Q1 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC1G79B-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74LVC1G79B-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G79B-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74LVC1G79B-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Electrical Characteristics* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50 pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74LVC1G79B-Q1 to the receiving device.
3. Verify that the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

8.2.3 Application Curves

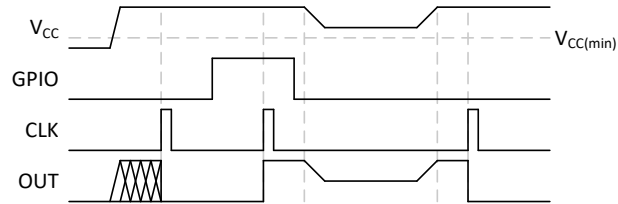


Figure 8-2. Data Retention With Supply Voltage Change

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each V_{CC} terminal has a good bypass capacitor to prevent power disturbance. For the SN74LVC1G79B-Q1, a 0.1 μ F bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

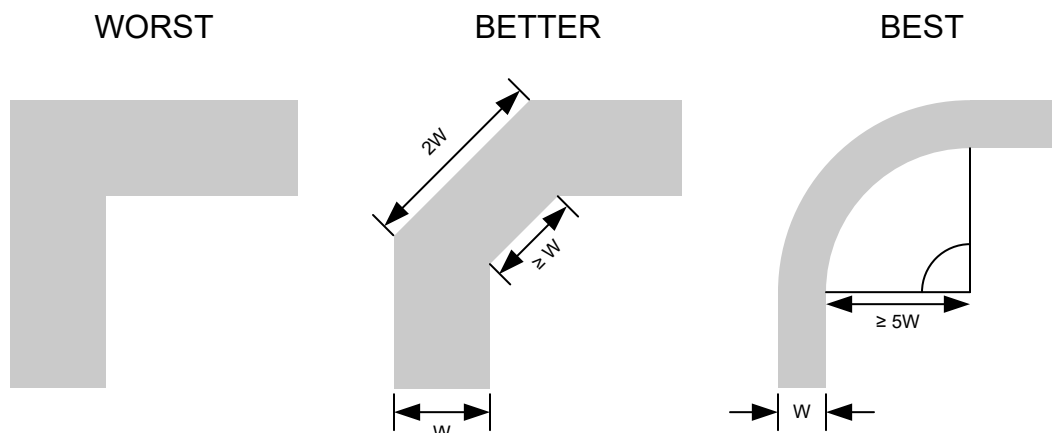


Figure 8-3. Example Trace Corners for Improved Signal Integrity

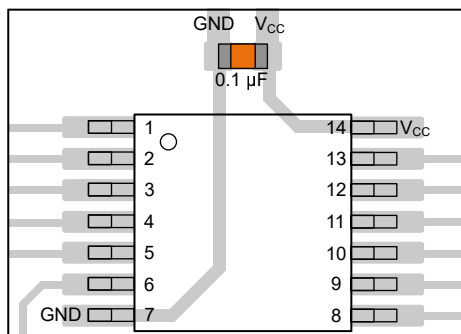


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

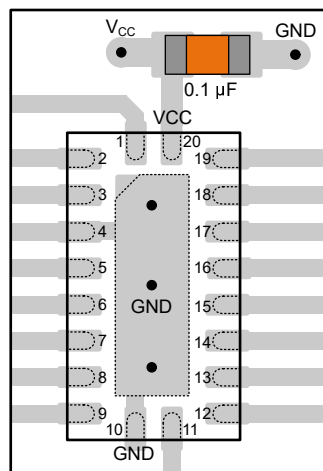


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

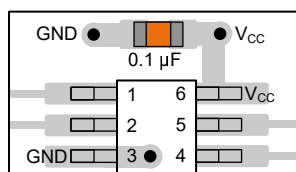


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

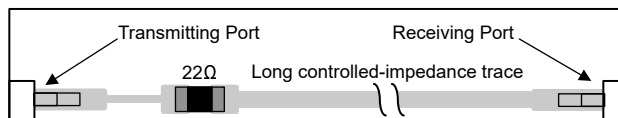


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

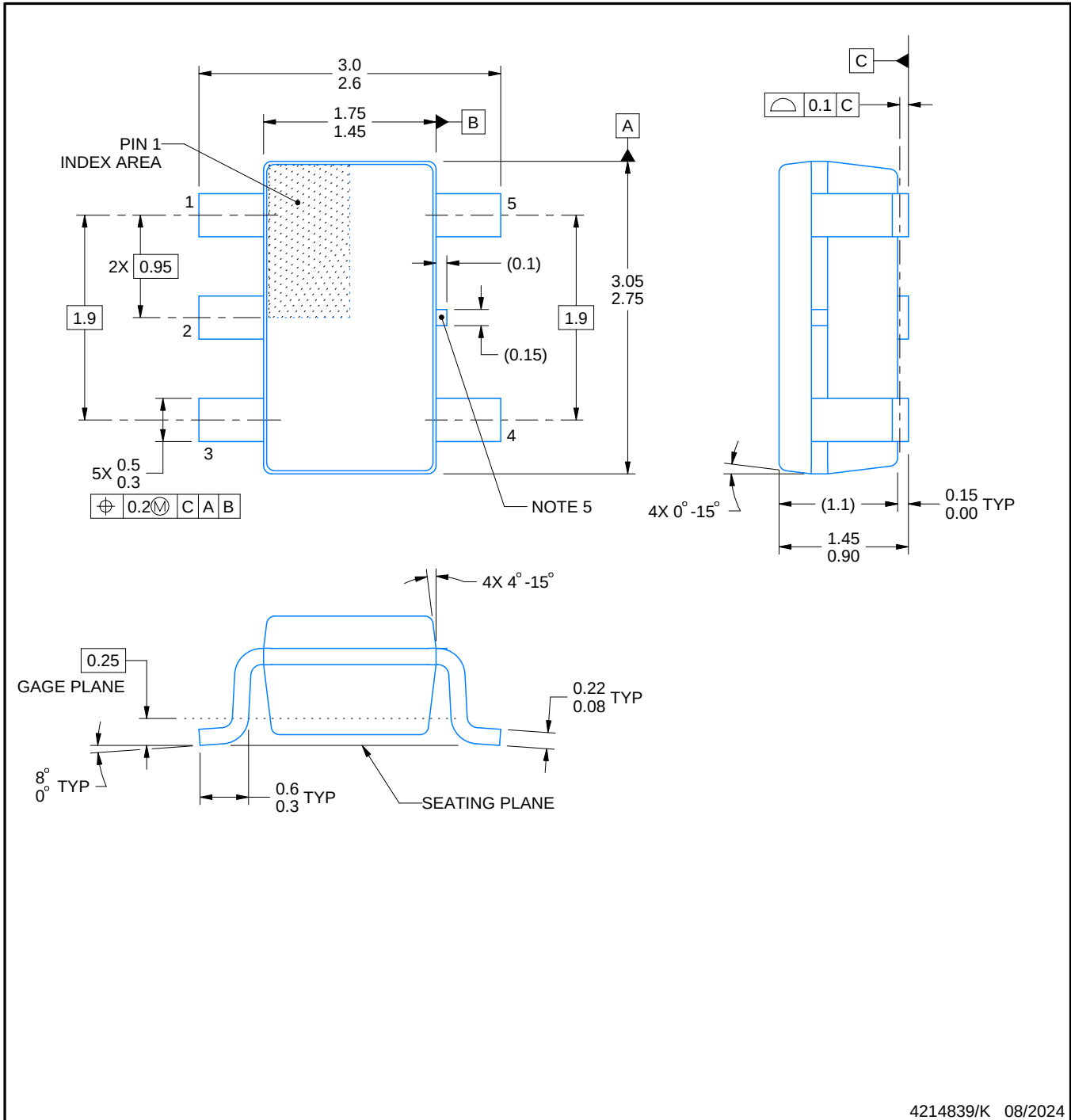


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

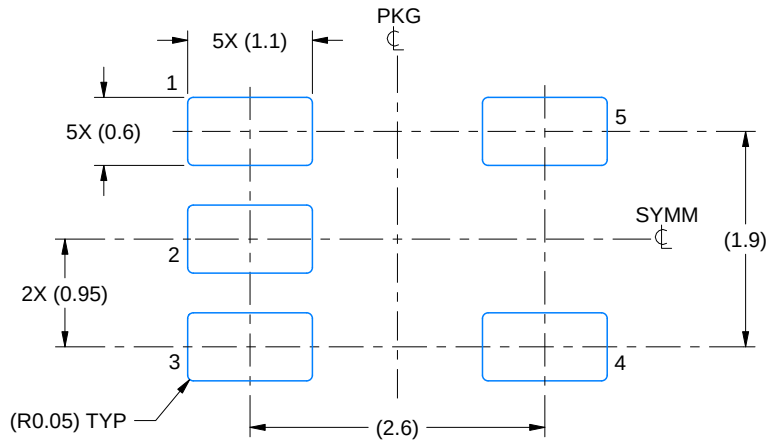
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

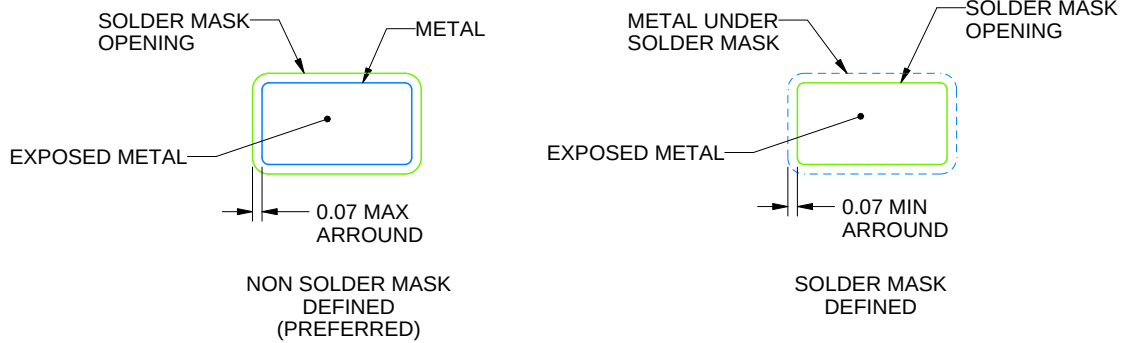
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

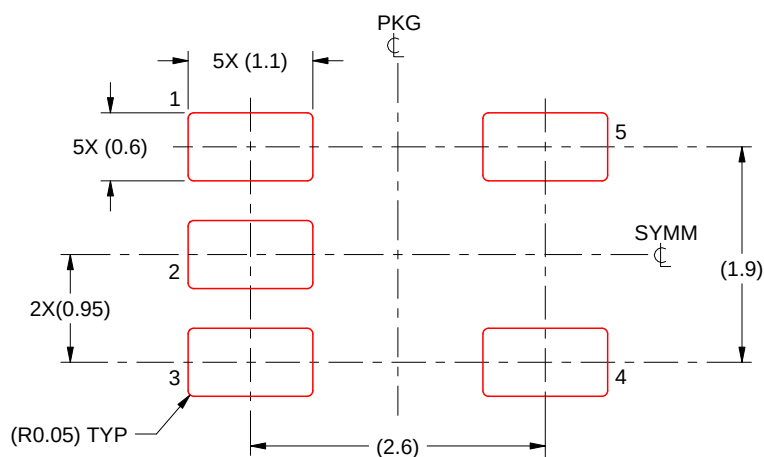
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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