

SN74LVC244B 1.1V - 3.6V; Octal Buffer or Driver with 3-State Outputs

1 Features

- Operating range from 1.65V to 3.6V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Maximum propagation delay of Maximum t_{pd} of 5.9ns @ 3.3V
- Supports [partial-power-down](#) with back drive protection (I_{off})
- High output drive strength:
 - $\pm 24\text{mA}$ at 3.3V
 - $\pm 8\text{mA}$ at 2.3V
 - $\pm 4\text{mA}$ at 1.65V

2 Applications

- [Drive an indicator LED](#)
- [Redrive a digital signal](#)
- [Drive a transmission line](#)
- [Hold a signal during controller reset](#)

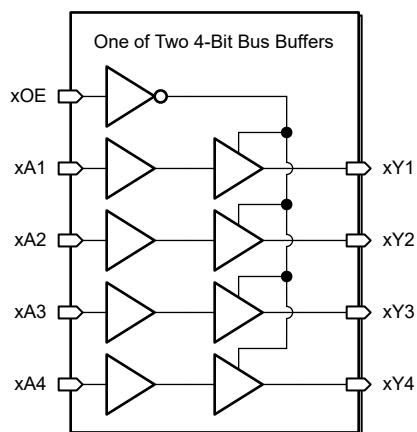
3 Description

The SN74LVC244B is an octal buffer with 3-state outputs. The device is configured into two banks of four drivers, each controlled by an output enable pin.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74LVC244B	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram



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4 Pin Configuration and Functions

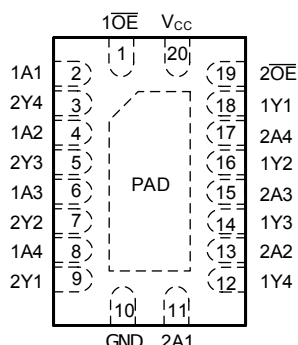


Figure 4-1. SN74LVC244B RKS Package (Top View)

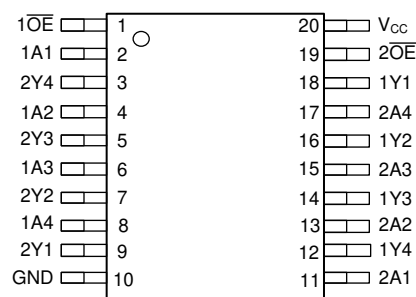


Figure 4-2. SN74LVC244B PW Package (Top View)

Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
OE1	1	I	Bank 1, output enable, active low
A1	2	I	Bank 1, channel 1 input
A2	3	O	Bank 2, channel 4 output
A3	4	I	Bank 1, channel 2 input
A4	5	O	Bank 2, channel 3 output
A5	6	I	Bank 1, channel 3 input
A6	7	O	Bank 2, channel 2 output
A7	8	I	Bank 1, channel 4 input
A8	9	O	Bank 2, channel 1 output
GND	10	G	Ground
Y8	11	I	Bank 2, channel 1 input
Y7	12	O	Bank 1, channel 4 output
Y6	13	I	Bank 2, channel 2 input
Y5	14	O	Bank 1, channel 3 output
Y4	15	I	Bank 2, channel 3 input
Y3	16	O	Bank 1, channel 2 output
Y2	17	I	Bank 2, channel 4 input
Y1	18	O	Bank 1, channel 1 output
OE2	19	I	Bank 2, output enable, active low
VCC	20	P	Positive supply
Thermal Pad ⁽²⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

(2) RKS package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
V _I	Input voltage range ⁽²⁾		-0.5	6.5	V
V _O	Output voltage range in the high-impedance or power-off state ⁽²⁾		-0.5	6.5	V
V _O	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0V		-50	mA
I _{OK}	Output clamp current	V _O < 0V		-50	mA
I _O	Continuous output current			±50	mA
I _O	Continuous output current through V _{CC} or GND			±100	mA
T _J	Junction temperature		-65	150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		1.1	3.6	V
V _I	Input voltage			5.5	V
V _O	Output voltage	(High or low state)		V _{CC}	V
V _O	Output voltage	3-state	0	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.1V to 1.95V	0.65 × V _{CC}		V
		V _{CC} = 2.3V to 2.7V	1.7		
		V _{CC} = 2.7V to 3.6V	2		
V _{IL}	Low-Level input voltage	V _{CC} = 1.1V to 1.95V		0.35 × V _{CC}	V
		V _{CC} = 2.3V to 2.7V		0.7	
		V _{CC} = 2.7V to 3.6V		0.8	
I _{OH}	High-level output current	V _{CC} = 1.8V		-4	mA
		V _{CC} = 2.3V		-8	
		V _{CC} = 2.7V		-12	
		V _{CC} = 3V		-24	
I _{OL}	Low-level output current	V _{CC} = 1.8V		4	mA
		V _{CC} = 2.3V		8	
		V _{CC} = 2.7V		12	
		V _{CC} = 3V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC ⁽¹⁾						UNIT
		R _{θJA}	R _{θJC(top)}	R _{θJB}	Ψ _{JT}	Ψ _{JB}	R _{θJC(bot)}	
PW (TSSOP)	20	120.3	62.5	82.4	16.0	81.5	N/A	°C/W
RKS (VQFN)	20	87.2	93.4	59.8	24.9	59.6	44.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = −100μA	1.1V to 3.6V	V _{CC} - 0.2			V _{CC} - 0.2			V
	I _{OH} = −4mA	1.5V	1.24			1.2			
	I _{OH} = −4mA	1.65V	1.29			1.2			
	I _{OH} = −8mA	2.3V	1.9			1.75			
	I _{OH} = −12mA	2.7V	2.2			2.2			
		3V	2.4			2.4			
	I _{OH} = −24mA	3V	2.3			2.2			
V _{OL}	I _{OH} = 100μA	1.1V to 3.6V	0.1			0.15			V
	I _{OH} = 4mA	1.5V	0.15			0.4			
	I _{OH} = 4mA	1.65V	0.24			0.45			
	I _{OH} = 8mA	2.3V	0.3			0.7			
	I _{OH} = 12mA	2.7V	0.4			0.4			
		3V	0.35			0.45			
	I _{OH} = 24mA	3V	0.55			0.55			
I _I	V _I = V _{CC} or GND	3.6V	±1			±5			μA
I _{off}	V _I or V _O = V _{CC}	0V	±1			±10			μA
I _{OZ}	V _O = V _{CC} or GND	3.6V	±1			±15			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V	1			40			μA
ΔI _{CC}	One input from 0V to V _{CC} , other inputs at V _{CC} or GND	2.7V to 3.6V	500			500			μA
C _I	V _I = V _{CC} or GND	3.3V	4.9			4.9			pF
C _O	V _O = V _{CC} or GND	3.3V	6.3			6.3			pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A	Y	$C_L = 15\text{pF}$	$1.2\text{V} \pm 0.1\text{V}$			27.1	ns
				$1.5\text{V} \pm 0.12\text{V}$			11.5	
			$C_L = 30\text{pF}$	$1.8\text{V} \pm 0.15\text{V}$			9	
				$2.5\text{V} \pm 0.2\text{V}$			5.5	
			$C_L = 50\text{pF}$	$3.3\text{V} \pm 0.3\text{V}$			4.8	
t_{en}	$\overline{OE}$	Y	$C_L = 15\text{pF}$	$1.2\text{V} \pm 0.1\text{V}$			35.4	ns
				$1.5\text{V} \pm 0.12\text{V}$			12.2	
			$C_L = 30\text{pF}$	$1.8\text{V} \pm 0.15\text{V}$			9.8	
				$2.5\text{V} \pm 0.2\text{V}$			6.4	
			$C_L = 50\text{pF}$	$3.3\text{V} \pm 0.3\text{V}$			6	
t_{dis}	$\overline{OE}$	Y	$C_L = 15\text{pF}$	$1.2\text{V} \pm 0.1\text{V}$			27.6	ns
				$1.5\text{V} \pm 0.12\text{V}$			13.3	
			$C_L = 30\text{pF}$	$1.8\text{V} \pm 0.15\text{V}$			10.9	
				$2.5\text{V} \pm 0.2\text{V}$			6.6	
			$C_L = 50\text{pF}$	$3.3\text{V} \pm 0.3\text{V}$			6.2	
$t_{sk(o)}$				$3.3\text{V} \pm 0.3\text{V}$			0.4	ns
C_{PD}		Outputs Enabled	$f = 10\text{MHz}$	1.8V			13.2	pF
				2.5V			13.8	
				3.3V			14.2	
		Outputs Disabled	$f = 10\text{MHz}$	1.8V			1.2	
				2.5V			1.3	
				3.3V			1.5	

5.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

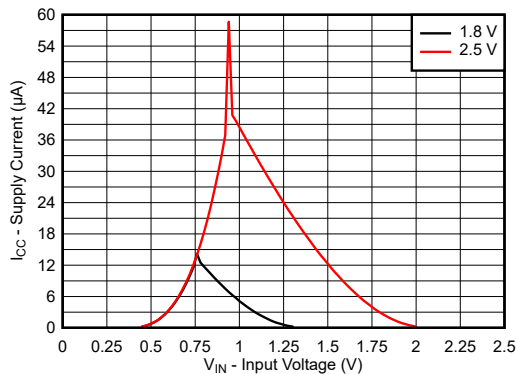


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

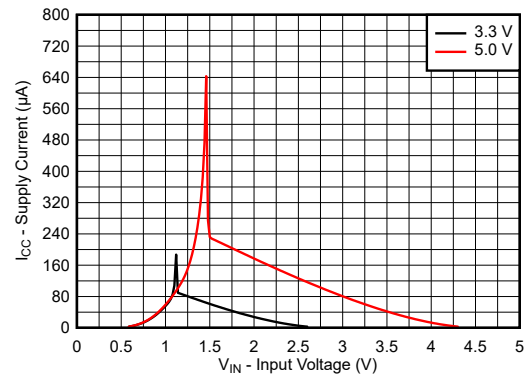


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

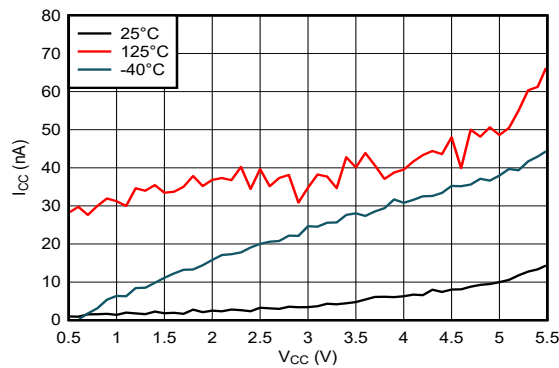


Figure 5-3. Supply Current Across Supply Voltage

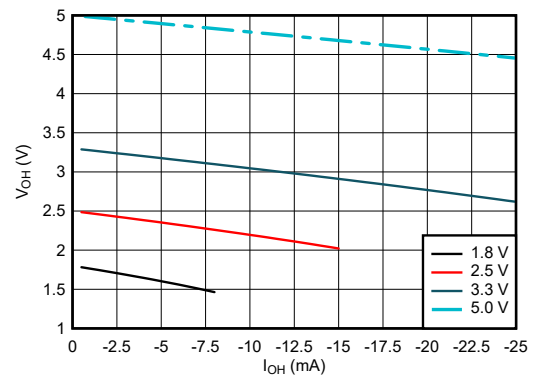


Figure 5-4. Output Voltage vs Current in HIGH State

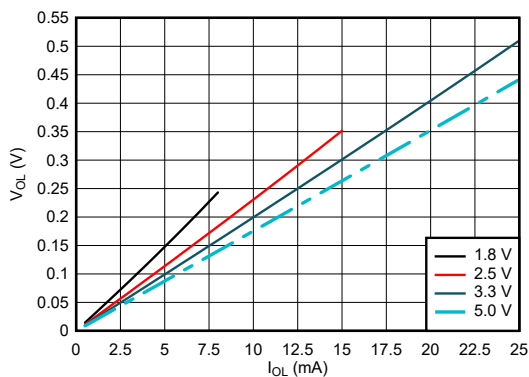


Figure 5-5. Output Voltage vs Current in LOW State

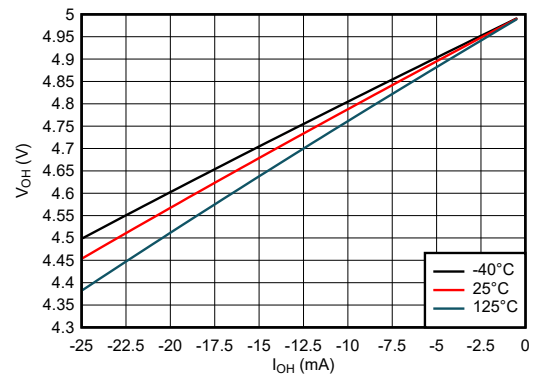


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

5.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

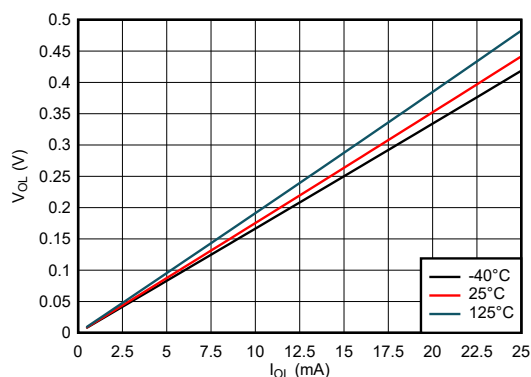


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

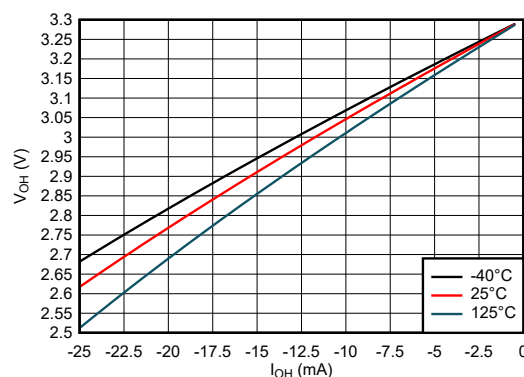


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

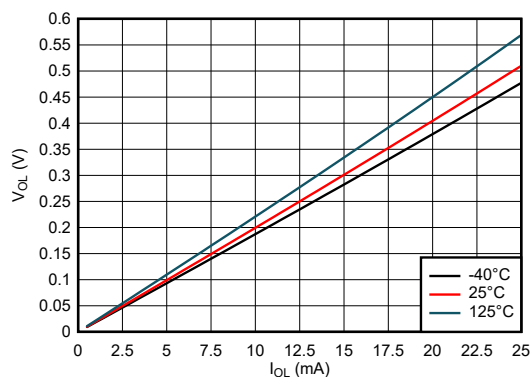


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

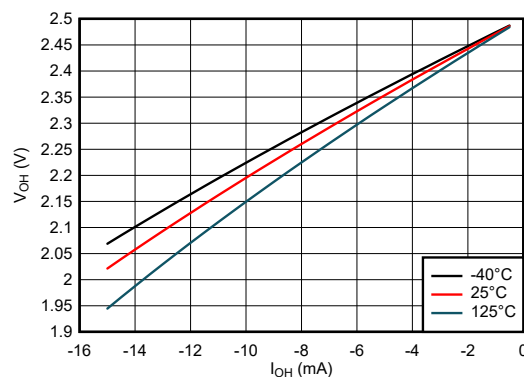


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

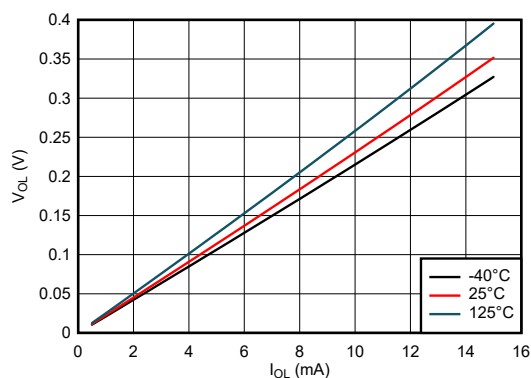


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

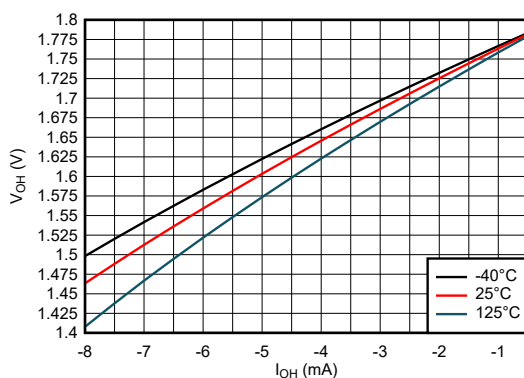


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

5.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

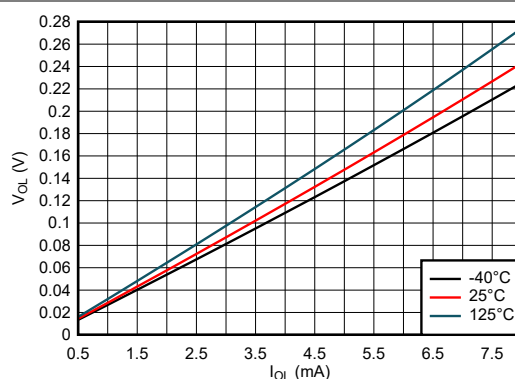


Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

6 Parameter Measurement Information

Phase relationships between waveforms are chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_f \leq 2.5\text{ns}$.

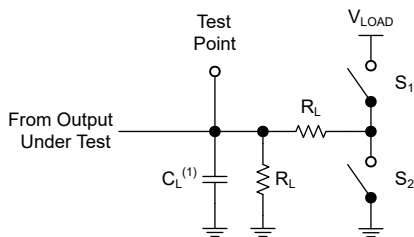
The outputs are measured individually with one input transition per measurement.

Table 6-1. 3-State Outputs

TEST	S1	S2
t_{PLH} , t_{PHL}	OPEN	OPEN
t_{PLZ} , t_{PZL}	CLOSED	OPEN
t_{PHZ} , t_{PZH}	OPEN	CLOSED

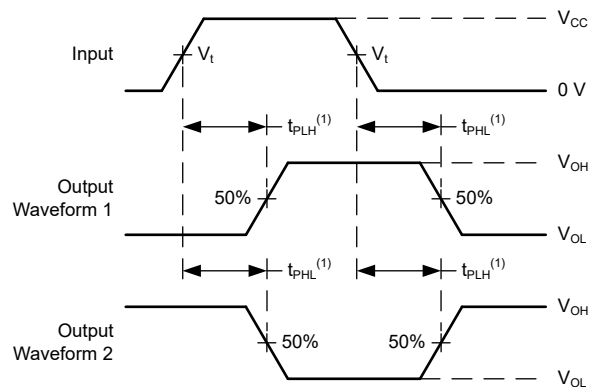
Table 6-2. 3-State or Open-Drain Outputs

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
$1.2\text{V} \pm 0.1\text{V}$	$V_{CC}/2$	$2\text{k}\Omega$	15pF	0.1V	$2 \times V_{CC}$
$1.5\text{V} \pm 0.12\text{V}$	$V_{CC}/2$	$2\text{k}\Omega$	15pF	0.1V	$2 \times V_{CC}$
$1.8\text{V} \pm 0.15\text{V}$	$V_{CC}/2$	$1\text{k}\Omega$	30pF	0.15V	$2 \times V_{CC}$
$2.5\text{V} \pm 0.2\text{V}$	$V_{CC}/2$	500Ω	30pF	0.15V	$2 \times V_{CC}$
2.7V	1.5V	500Ω	50pF	0.3V	6V
$3.3\text{V} \pm 0.3\text{V}$	1.5V	500Ω	50pF	0.3V	6V



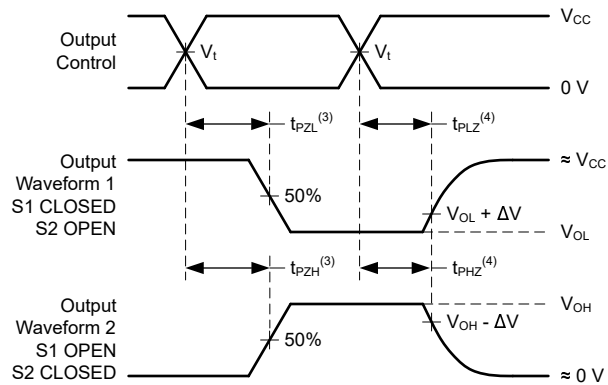
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

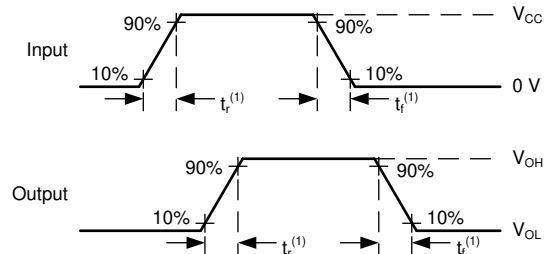
Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_{PZL} and t_{PZH} is the same as t_{en} .

(2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis} .

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74LVC244B contains 8 individual high speed CMOS buffers organized as two 4-bit buffers/line drives with 3-state outputs.

Each buffer performs the boolean logic function $xY_n = xA_n$, with x being the bank number and n being the channel number.

Each output enable ($x\overline{OE}$) controls four buffers. When the $x\overline{OE}$ pin is in the low state, the outputs of all buffers in the bank x are enabled. When the $x\overline{OE}$ pin is in the high state, the outputs of all buffers in the bank x are disabled. All disabled output are placed into the high-impedance state.

To put the device in the high-impedance state during power up or power down, tie both $\overline{OE}$ pins to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sinking capability of the driver and the leakage of the pin as defined in the *Electrical Characteristics* table.

7.2 Functional Block Diagram

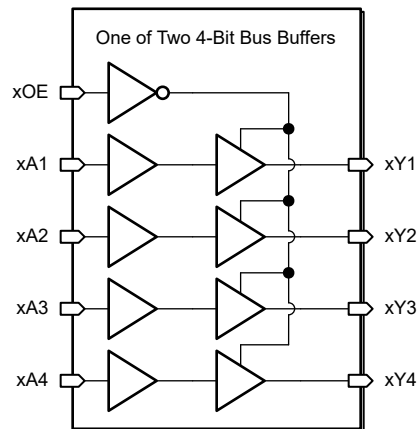


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

7.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10k Ω resistor, however, is recommended and typically meets all requirements.

7.3.4 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

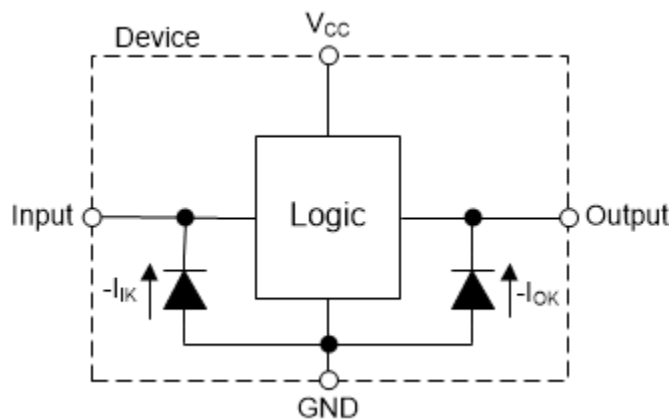


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVC244B.

Table 7-1. Function Table

INPUTS ⁽¹⁾		OUTPUTS
$\overline{OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care, Z = High-Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74LVC244B is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

8.2 Typical Application

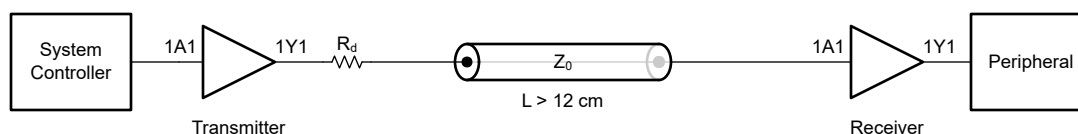


Figure 8-1. Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - For rise time and fall time specification, see $(\Delta t/\Delta V)$ in the *Recommended Operating Conditions* table.
 - For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the *Recommended Operating Conditions* table.
 - Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the *Recommended Operating Conditions* table at any valid V_{CC} .
- Recommended maximum Output Conditions:
 - Load currents must not exceed $(I_O \text{ max})$ per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
 - Outputs must not be pulled above V_{CC} .

8.2.3 Application Curves

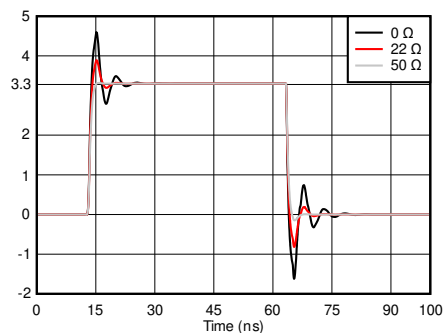


Figure 8-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor (R_d) Values

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1 μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1 μ F and 1 μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

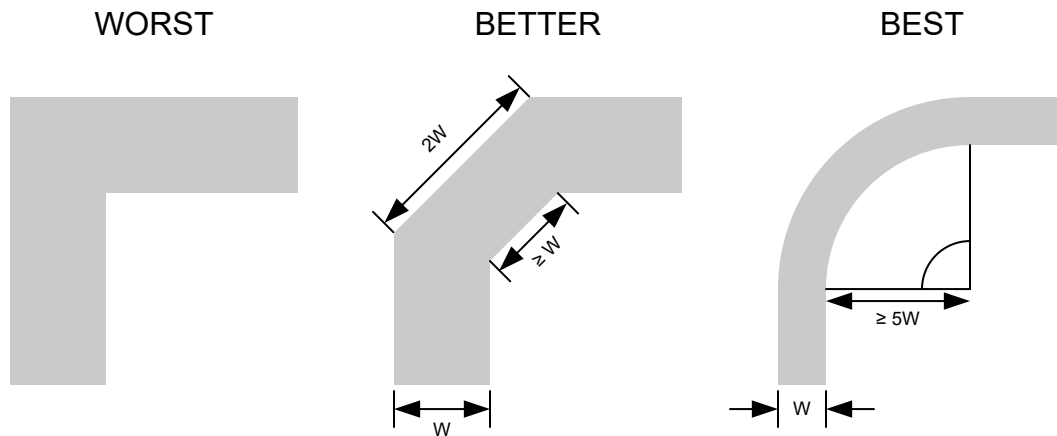


Figure 8-3. Example Trace Corners for Improved Signal Integrity

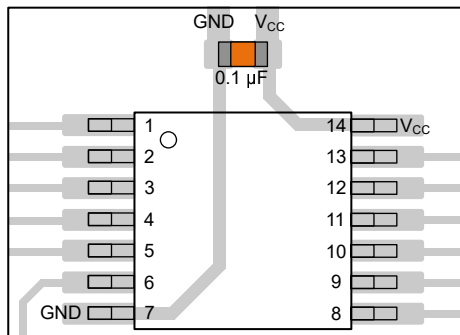


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

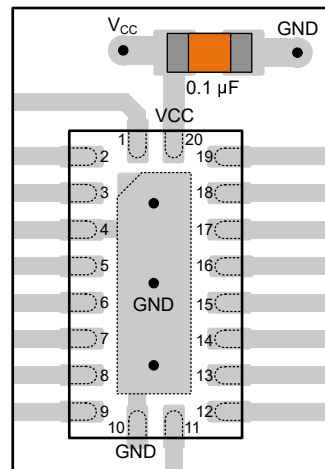


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

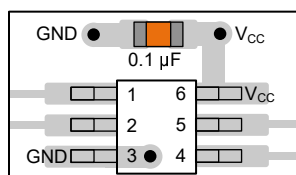


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

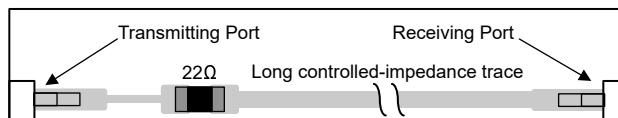


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

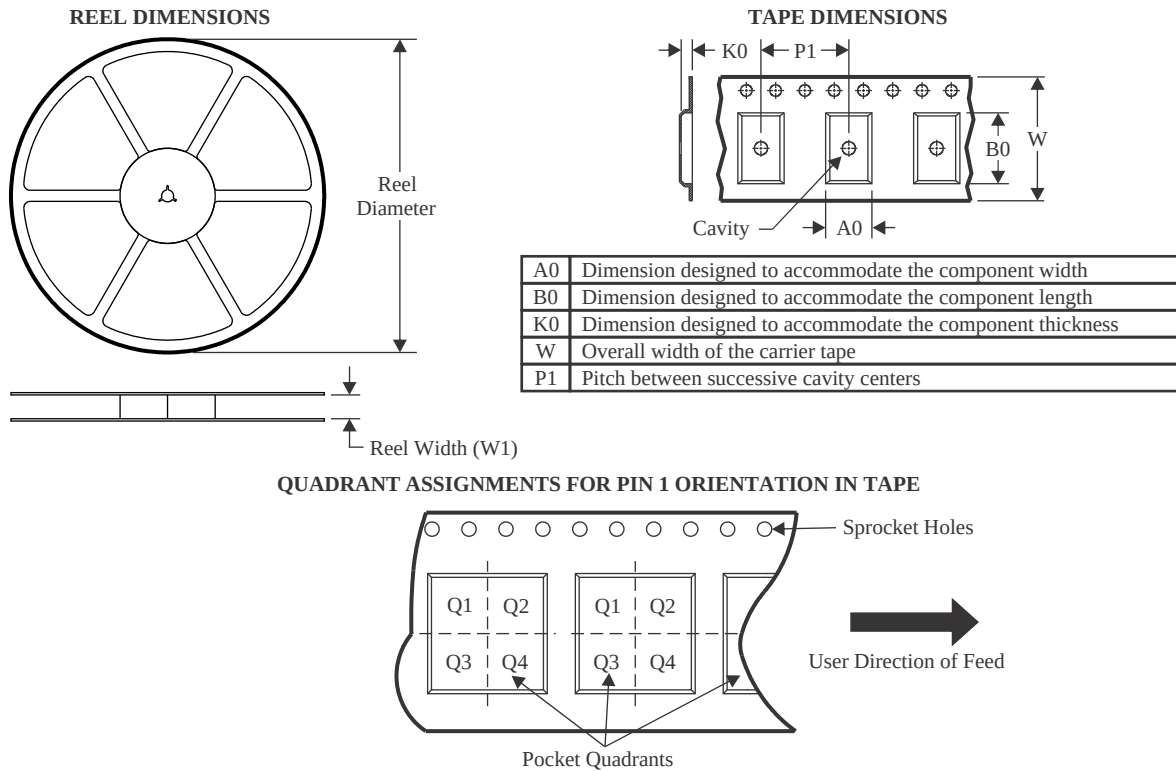
Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC244BRKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC244B

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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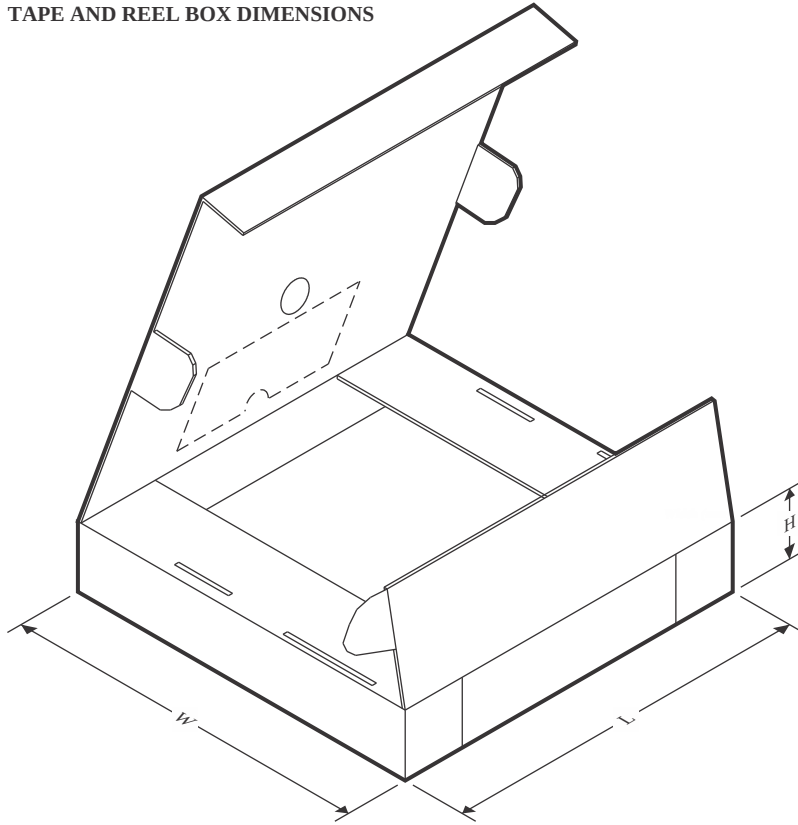
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC244BRKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC244BRKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

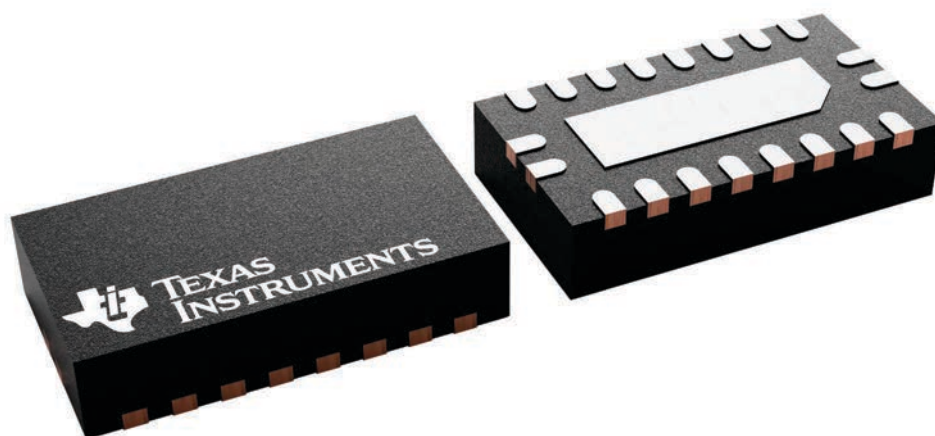
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



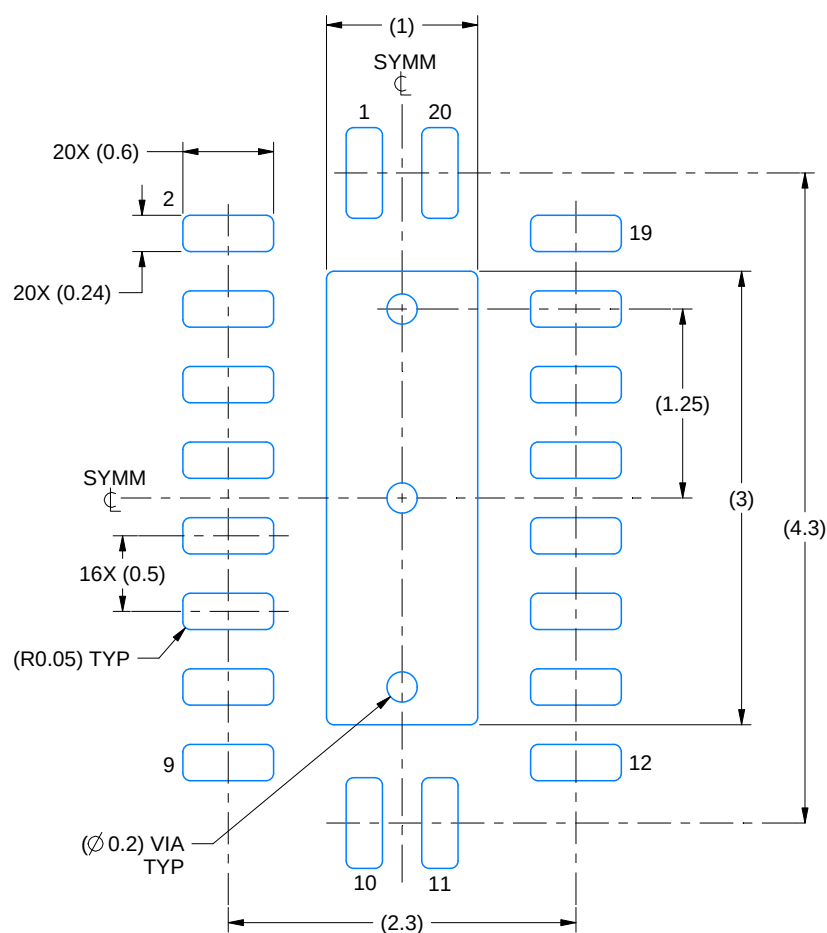
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1mm solder wetting on pins side wall. Available for wettable flank version only

EXAMPLE BOARD LAYOUT

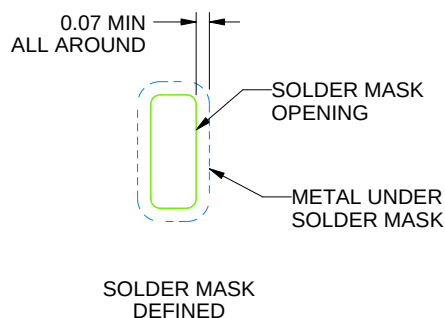
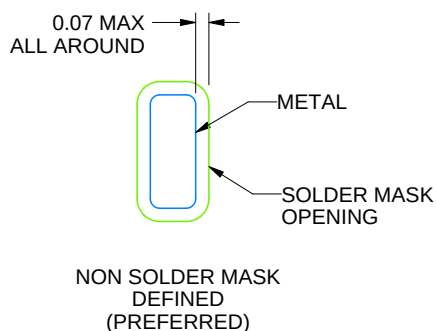
RKS0020C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4231497/B 03/2025

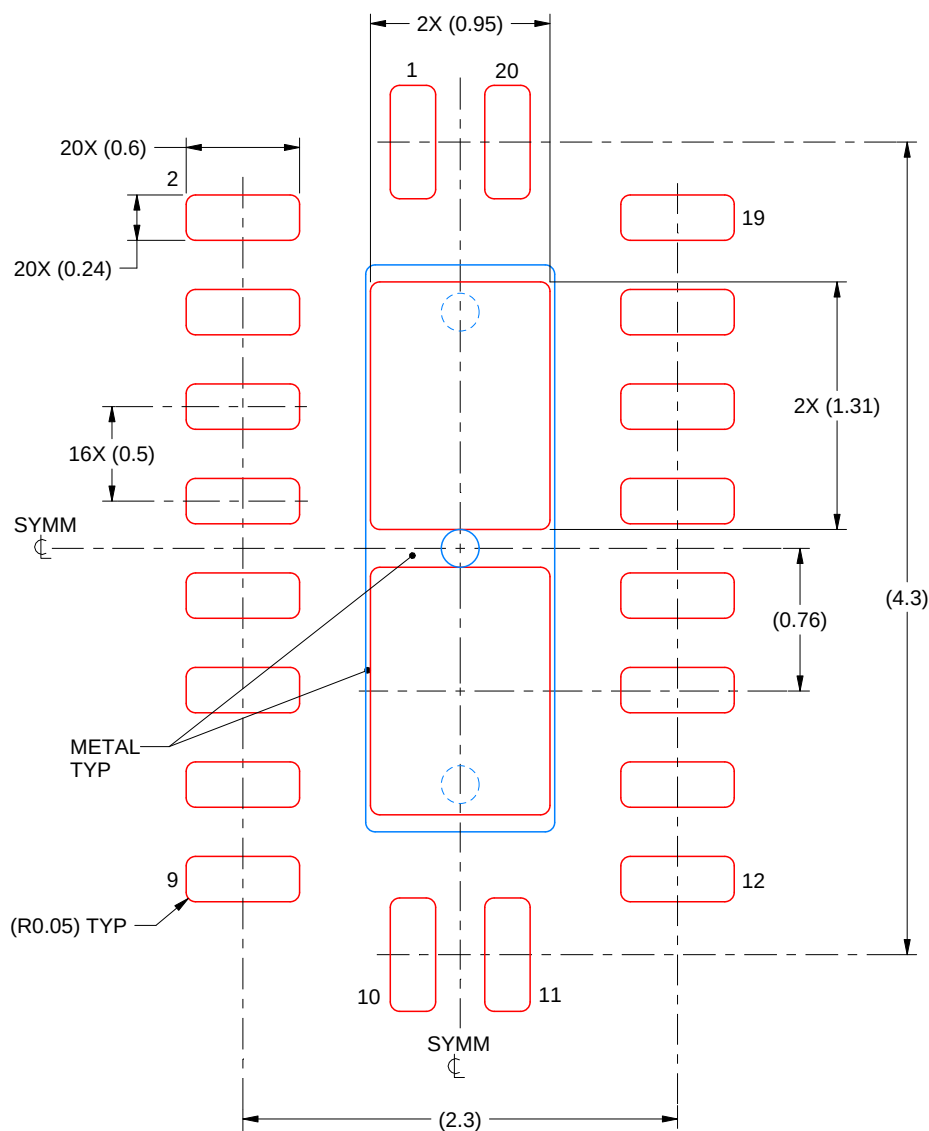
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

RKS0020C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE

BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4231497/B 03/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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