

## SN74LVC2G00-Q1 Automotive, Dual 2-Input Positive-NAND Gates

### 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Operating range from 1.65V to 3.6V
- Over-voltage tolerant inputs support up to 5.5V independent of  $V_{CC}$
- Maximum propagation delay of 3.8ns at 5V  $V_{CC}$
- Supports [partial-power-down](#) with back drive protection ( $I_{off}$ )
- High output drive strength:
  - $\pm 24\text{mA}$  at 3.3V
  - $\pm 8\text{mA}$  at 2.3V
  - $\pm 4\text{mA}$  at 1.65V

### 2 Applications

- [Alarm or tamper detect circuit](#)
- S-R latch

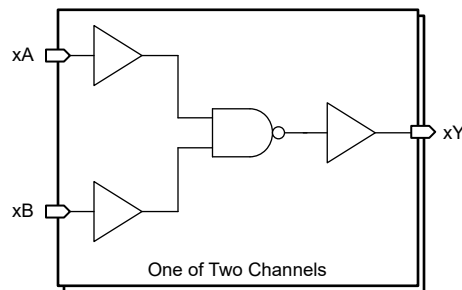
### 3 Description

The SN74LVC2G00-Q1 device is a dual 2-input positive NAND gate. Each gate performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

#### Package Information

| PART NUMBER    | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|----------------|------------------------|-----------------------------|--------------------------|
| SN74LVC2G00-Q1 | DCT (SSOP, 8)          | 4.1mm × 3mm                 | 3mm × 3mm                |

- (1) For more information, see [Mechanical, Packaging, and Orderable Information](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



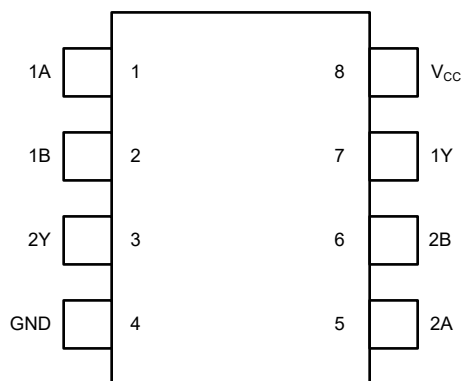
**Logic Diagram**



## Table of Contents

|                                                  |           |                                                                  |           |
|--------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                          | <b>1</b>  | 7.4 Device Functional Modes.....                                 | <b>12</b> |
| <b>2 Applications</b> .....                      | <b>1</b>  | <b>8 Application and Implementation</b> .....                    | <b>13</b> |
| <b>3 Description</b> .....                       | <b>1</b>  | 8.1 Application Information.....                                 | <b>13</b> |
| <b>4 Pin Configuration and Functions</b> .....   | <b>3</b>  | 8.2 Typical Application.....                                     | <b>13</b> |
| <b>5 Specifications</b> .....                    | <b>4</b>  | 8.3 Power Supply Recommendations.....                            | <b>15</b> |
| 5.1 Absolute Maximum Ratings.....                | <b>4</b>  | 8.4 Layout.....                                                  | <b>15</b> |
| 5.2 ESD Ratings.....                             | <b>4</b>  | <b>9 Device and Documentation Support</b> .....                  | <b>17</b> |
| 5.3 Recommended Operating Conditions.....        | <b>4</b>  | 9.1 Documentation Support.....                                   | <b>17</b> |
| 5.4 Thermal Information.....                     | <b>5</b>  | 9.2 Receiving Notification of Documentation Updates....          | <b>17</b> |
| 5.5 Electrical Characteristics .....             | <b>5</b>  | 9.3 Support Resources.....                                       | <b>17</b> |
| 5.6 Switching Characteristics.....               | <b>6</b>  | 9.4 Trademarks.....                                              | <b>17</b> |
| 5.7 Typical Characteristics.....                 | <b>7</b>  | 9.5 Electrostatic Discharge Caution.....                         | <b>17</b> |
| <b>6 Parameter Measurement Information</b> ..... | <b>10</b> | 9.6 Glossary.....                                                | <b>17</b> |
| <b>7 Detailed Description</b> .....              | <b>11</b> | <b>10 Revision History</b> .....                                 | <b>17</b> |
| 7.1 Overview.....                                | <b>11</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>18</b> |
| 7.2 Functional Block Diagram.....                | <b>11</b> |                                                                  |           |
| 7.3 Feature Description.....                     | <b>11</b> |                                                                  |           |

## 4 Pin Configuration and Functions



**Figure 4-1. DCT Package8-PinSSOP Top View**

**Table 4-1. Pin Functions**

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION       |
|-----------------|-----|---------------------|-------------------|
| NAME            | NO. |                     |                   |
| 1A              | 1   | I                   | Channel 1 input A |
| 1B              | 2   | I                   | Channel 1 input B |
| 1Y              | 7   | O                   | Channel 1 output  |
| 2A              | 5   | I                   | Channel 2 input A |
| 2B              | 6   | I                   | Channel 2 input B |
| 2Y              | 3   | O                   | Channel 2 output  |
| GND             | 4   | G                   | Ground            |
| V <sub>CC</sub> | 8   | P                   | Positive supply   |

(1) I = input, O = Output, P = Power, G = Ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                          |                     | MIN  | MAX                   | UNIT |
|------------------|----------------------------------------------------------|---------------------|------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage range                                     |                     | -0.5 | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                       |                     | -0.5 | 6.5                   | V    |
| V <sub>O</sub>   | Output voltage range <sup>(2)</sup>                      |                     | -0.5 | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                                      | V <sub>I</sub> < 0V |      | -50                   | mA   |
| I <sub>OK</sub>  | Output clamp current                                     | V <sub>O</sub> < 0V |      | -50                   | mA   |
| I <sub>O</sub>   | Continuous output current                                |                     |      | ±50                   | mA   |
| I <sub>O</sub>   | Continuous output current through V <sub>CC</sub> or GND |                     |      | ±100                  | mA   |
| T <sub>J</sub>   | Junction temperature                                     |                     | -65  | 150                   | °C   |
| T <sub>stg</sub> | Storage temperature                                      |                     | -65  | 150                   | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

|                    |                         |                                                                                        | VALUE | UNIT |
|--------------------|-------------------------|----------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup> | ±2000 | V    |
|                    |                         | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B          | ±1000 |      |

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Specifications  | Description               | Condition                        | MIN                    | MAX                    | UNIT |
|-----------------|---------------------------|----------------------------------|------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage            | Operating                        | 1.65                   | 5.5                    | V    |
|                 |                           | Functional                       | 1.2                    |                        |      |
| V <sub>I</sub>  | Input voltage             |                                  | 0                      | 5.5                    | V    |
| V <sub>O</sub>  | Output voltage            | (High or low state)              | 0                      | V <sub>CC</sub>        | V    |
| V <sub>IH</sub> | High-level input voltage  | V <sub>CC</sub> = 1.65V to 1.95V | 0.65 × V <sub>CC</sub> |                        | V    |
|                 |                           | V <sub>CC</sub> = 2.3V to 2.7V   | 1.7                    |                        |      |
|                 |                           | V <sub>CC</sub> = 3.0V to 3.6V   | 2                      |                        |      |
|                 |                           | V <sub>CC</sub> = 4.5V to 5.5V   | 0.7 × V <sub>CC</sub>  |                        |      |
| V <sub>IL</sub> | Low-Level input voltage   | V <sub>CC</sub> = 1.65V to 1.95V |                        | 0.35 × V <sub>CC</sub> | V    |
|                 |                           | V <sub>CC</sub> = 2.3V to 2.7V   |                        | 0.7                    |      |
|                 |                           | V <sub>CC</sub> = 3.0V to 3.6V   |                        | 0.8                    |      |
|                 |                           | V <sub>CC</sub> = 4.5V to 5.5V   |                        | 0.3 × V <sub>CC</sub>  |      |
| I <sub>OH</sub> | High-level output current | V <sub>CC</sub> = 1.65V          |                        | -4                     | mA   |
|                 |                           | V <sub>CC</sub> = 2.3V           |                        | -8                     |      |
|                 |                           | V <sub>CC</sub> = 3.0V           |                        | -16                    |      |
|                 |                           |                                  |                        | -24                    |      |
|                 |                           | V <sub>CC</sub> = 4.5V           |                        | -32                    |      |

over operating free-air temperature range (unless otherwise noted)

| Specifications      | Description                        | Condition                 | MIN | MAX | UNIT |
|---------------------|------------------------------------|---------------------------|-----|-----|------|
| $I_{OL}$            | Low-level output current           | $V_{CC} = 1.65V$          |     | 4   | mA   |
|                     |                                    | $V_{CC} = 2.3V$           |     | 8   |      |
|                     |                                    | $V_{CC} = 3.0V$           |     | 16  |      |
|                     |                                    |                           |     | 24  |      |
|                     |                                    | $V_{CC} = 4.5V$           |     | 32  |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 1.1V$ to $5.5V$ |     | 20  | ns/V |
| $T_A$               | Operating free-air temperature     |                           | -40 | 125 | °C   |

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | DCT    | UNIT |
|-------------------------------|----------------------------------------|--------|------|
|                               |                                        | 5 PINS |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance | 220    | °C/W |

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application note.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS                                                | $V_{CC}$                              | -40°C to 125°C |         |          | UNIT    |
|-----------------|----------------------------------------------------------------|---------------------------------------|----------------|---------|----------|---------|
|                 |                                                                |                                       | MIN            | TYP     | MAX      |         |
| $V_{OH}$        | $I_{OH} = -100\mu A$                                           | Over Recommended Operating Conditions | $V_{CC} - 0.1$ |         |          | V       |
| $V_{OH}$        | $I_{OH} = -4mA$                                                | 1.65V                                 | 1.2            |         |          | V       |
| $V_{OH}$        | $I_{OH} = -8mA$                                                | 2.3V                                  | 1.9            |         |          | V       |
| $V_{OH}$        | $I_{OH} = -12mA$                                               | 2.7V                                  | 2.2            |         |          | V       |
| $V_{OH}$        | $I_{OH} = -16mA$                                               | 3V                                    | 2.4            |         |          | V       |
| $V_{OH}$        | $I_{OH} = -24mA$                                               | 3V                                    | 2.3            |         |          | V       |
| $V_{OH}$        | $I_{OH} = -32mA$                                               | 4.5V                                  | 3.8            |         |          | V       |
| $V_{OL}$        | $I_{OL} = 100\mu A$                                            | Over Recommended Operating Conditions |                |         | 0.2      | V       |
| $V_{OL}$        | $I_{OL} = 4mA$                                                 | 1.65V                                 |                |         | 0.45     | V       |
| $V_{OL}$        | $I_{OL} = 8mA$                                                 | 2.3V                                  |                |         | 0.3      | V       |
| $V_{OL}$        | $I_{OL} = 12mA$                                                | 2.7V                                  |                |         | 0.4      | V       |
| $V_{OL}$        | $I_{OL} = 16mA$                                                | 3V                                    |                |         | 0.4      | V       |
| $V_{OL}$        | $I_{OL} = 24mA$                                                | 3V                                    |                |         | 0.55     | V       |
| $V_{OL}$        | $I_{OL} = 32mA$                                                | 4.5V                                  |                |         | 0.55     | V       |
| $I_I$           | $V_I = V_{CC}$ or GND                                          | $V_{CC} = 0V$ to $5.5V$               |                | $\pm 1$ | $\pm 5$  | $\mu A$ |
| $I_{off}$       | $V_I$ or $V_O = V_{CC}$                                        | $V_{CC} = 0V$                         |                | $\pm 1$ | $\pm 10$ | $\mu A$ |
| $I_{CC}$        | $V_I = V_{CC}$ or GND, $I_O = 0$                               | $V_{CC} = 1.65V$ to $5.5V$            |                | 1       | 10       | $\mu A$ |
| $\Delta I_{CC}$ | One input at $V_{CC} - 0.6V$ , other inputs at $V_{CC}$ or GND | 3.0V to 5.5V                          |                |         | 500      | $\mu A$ |
| $C_I$           | $V_I = V_{CC}$ or GND                                          | 3.3V                                  |                | 3.5     |          | pF      |
| $C_O$           | $V_O = V_{CC}$ or GND                                          | 3.3V                                  |                | 6.3     |          | pF      |

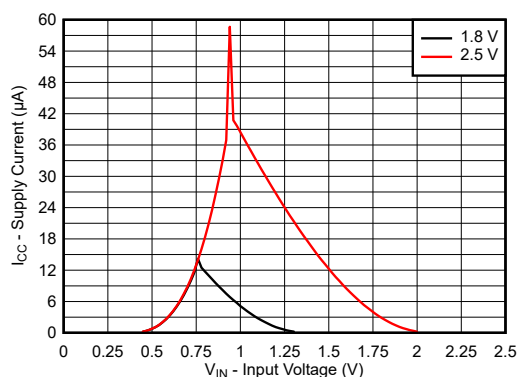
## 5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted). See *Parameter Measurement Information*

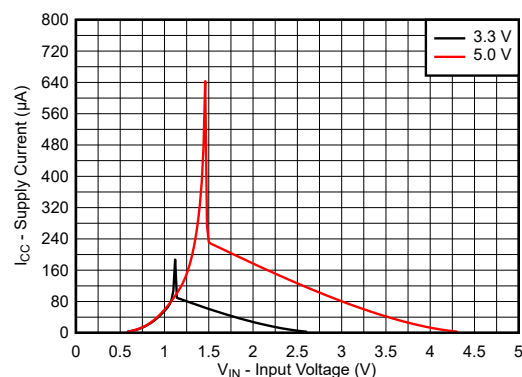
| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | –40°C to 125°C                    |     |                                  |     |                                  |     |                                |     | UNIT |
|-----------------|-----------------|----------------|-----------------------------------|-----|----------------------------------|-----|----------------------------------|-----|--------------------------------|-----|------|
|                 |                 |                | V <sub>CC</sub> = 1.8V<br>± 0.15V |     | V <sub>CC</sub> = 2.5V<br>± 0.2V |     | V <sub>CC</sub> = 3.3V<br>± 0.3V |     | V <sub>CC</sub> = 5V<br>± 0.5V |     |      |
|                 |                 |                | MIN                               | MAX | MIN                              | MAX | MIN                              | MAX | MIN                            | MAX |      |
| t <sub>pd</sub> | A or B          | Y              | 3.7                               | 9.4 | 1.6                              | 5.5 | 1.1                              | 4.9 | 1                              | 3.8 | ns   |

## 5.7 Typical Characteristics

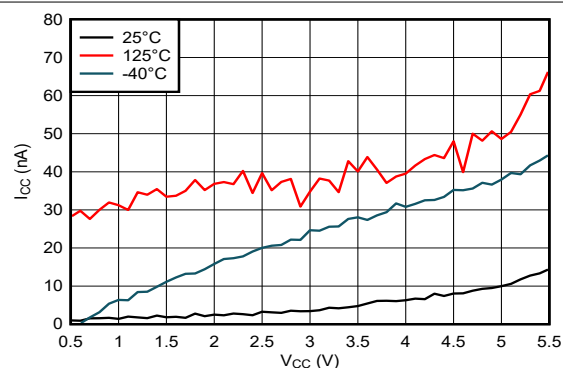
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



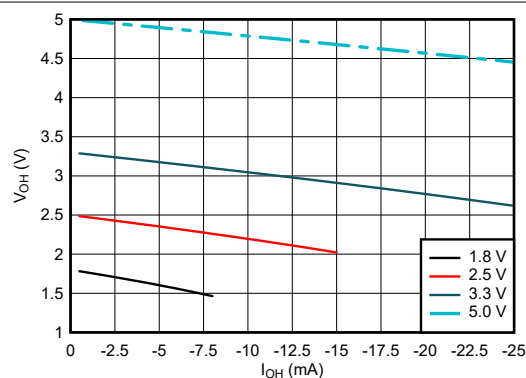
**Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply**



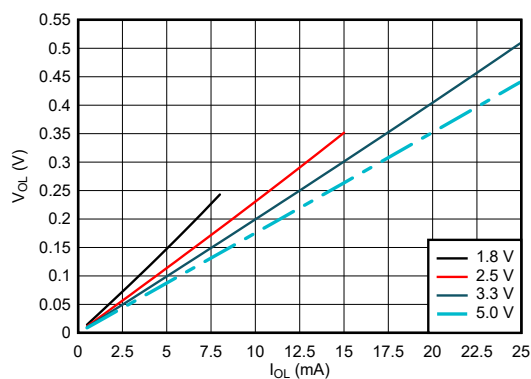
**Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply**



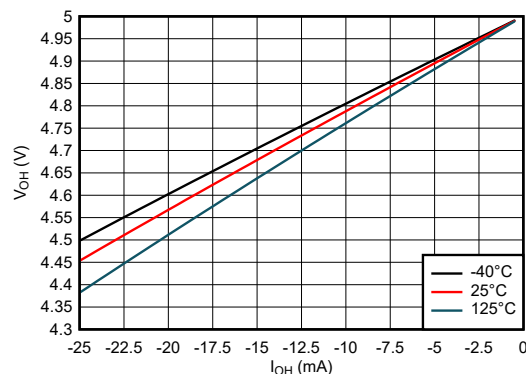
**Figure 5-3. Supply Current Across Supply Voltage**



**Figure 5-4. Output Voltage vs Current in HIGH State**



**Figure 5-5. Output Voltage vs Current in LOW State**



**Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply**

## 5.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

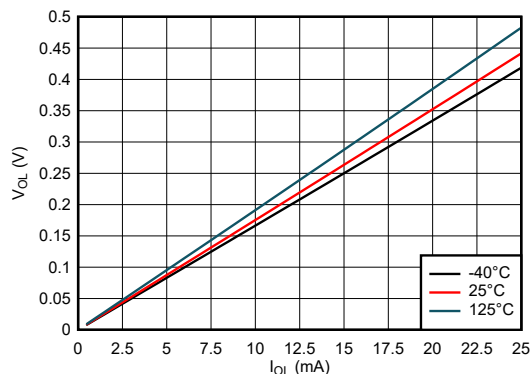


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

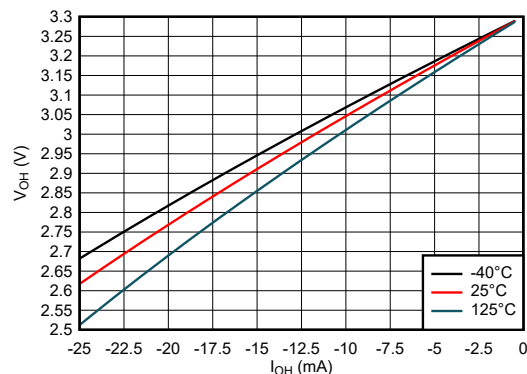


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

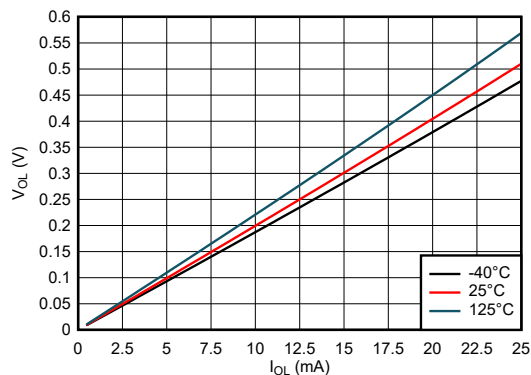


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

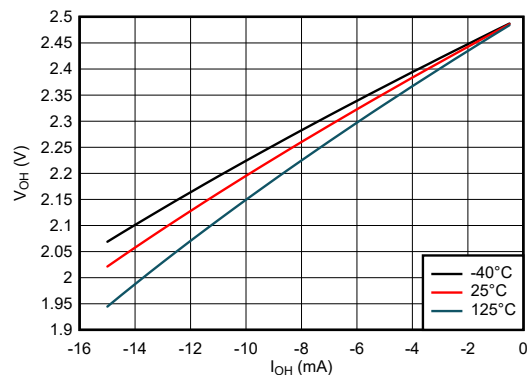


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

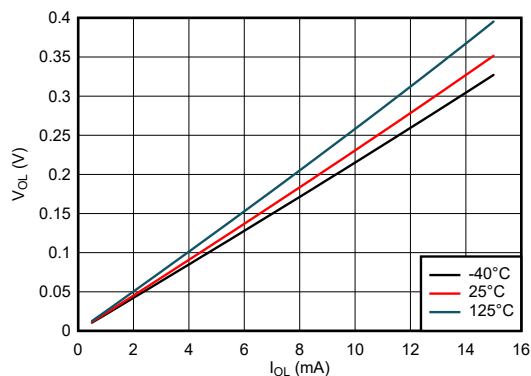


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

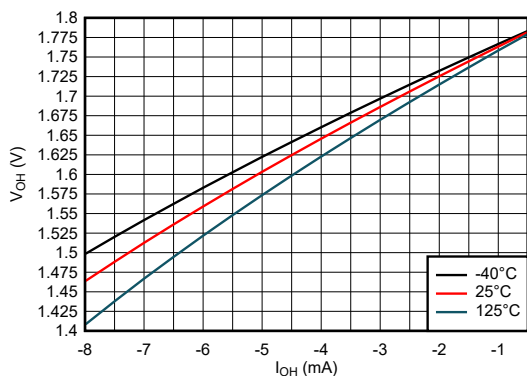
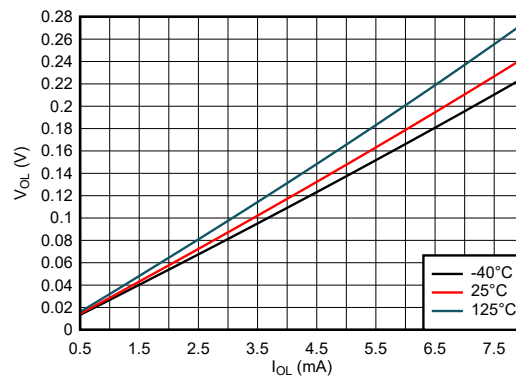


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

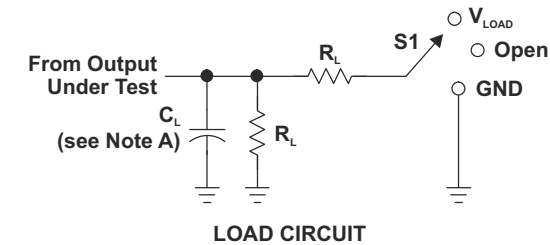
## 5.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$  (unless otherwise noted)



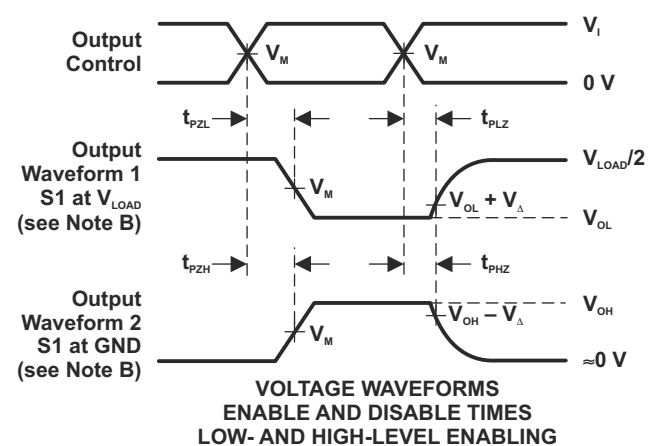
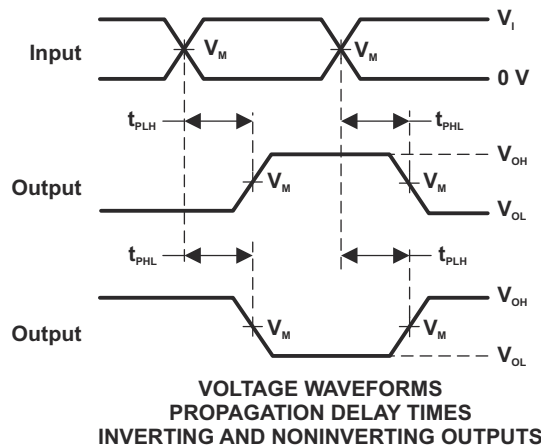
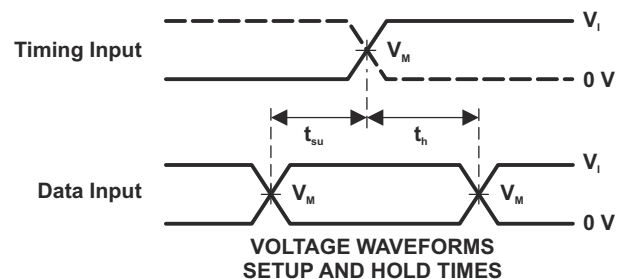
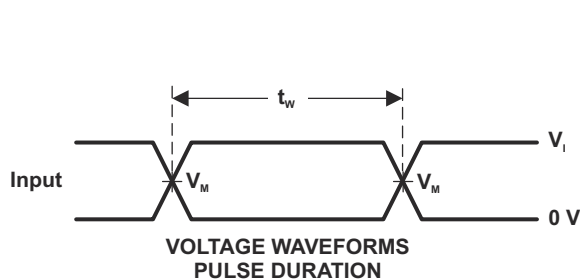
**Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply**

## 6 Parameter Measurement Information



| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{on}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

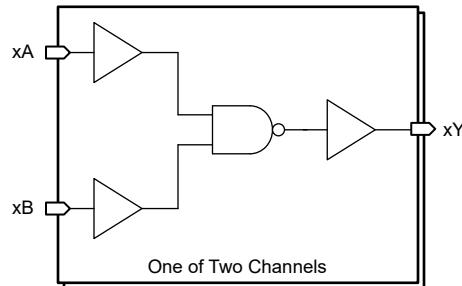
**Figure 6-1. Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

This device is a dual 2-input NAND Gate. Each gate performs the Boolean function  $Y = \overline{A \bullet B}$  in positive logic.

### 7.2 Functional Block Diagram



**Logic Diagram (Positive Logic)**

### 7.3 Feature Description

#### 7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

#### 7.3.2 Partial Power Down ( $I_{off}$ )

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

#### 7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

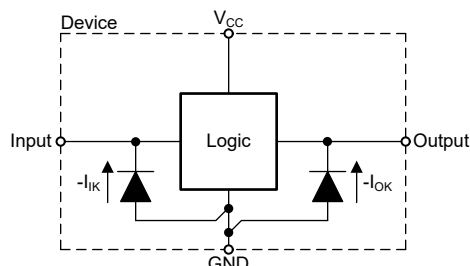
Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at  $V_{CC}$  or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10k $\Omega$  resistor, however, is recommended and typically meets all requirements.

#### 7.3.4 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

### CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.



**Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 7.3.5 Over-Voltage Tolerant Inputs

The SN74LVC2G00-Q1 includes over-voltage tolerant inputs. The input pins support high-state input voltages larger than the supply voltage by utilizing an input protection circuit that does not include a standard positive clamp diode. See *Recommended Operating Conditions* for the recommended input voltage.

### CAUTION

Do not exceed the maximum input voltage range provided in *Absolute Maximum Ratings*. Exceeding the maximum input voltage range rating can cause immediate and permanent damage to the device.

## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUTS |   | OUTPUT |
|--------|---|--------|
| A      | B | Y      |
| H      | H | L      |
| L      | X | H      |
| X      | L | H      |

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

In this application, two 2-input NAND gates are used to create an active-low SR latch as shown in the [Typical application block diagram](#). The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The SN74LVC2G00-Q1 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

### 8.2 Typical Application

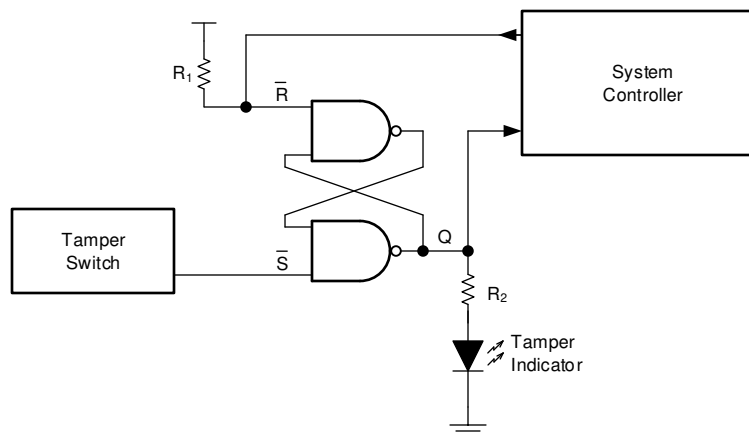


Figure 8-1. Typical application block diagram

#### 8.2.1 Design Requirements

##### 8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC2G00-Q1 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC2G00-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC2G00-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74LVC2G00-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 8.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC2G00-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC2G00-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Electrical Characteristics* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

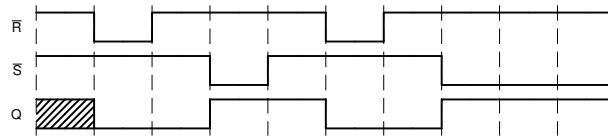
Refer to the *Feature Description* section for additional information regarding the outputs for this device.

#### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is  $\leq 50$ pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74LVC2G00-Q1 to the receiving device.

3. Verify that the resistive load at the output is larger than  $(V_{CC} / I_{O(max)})\Omega$ . Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

### 8.2.3 Application Curves



**Figure 8-2. Application timing diagram**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each  $V_{CC}$  terminal has a good bypass capacitor to prevent power disturbance. For the SN74LVC2G00-Q1, a 0.1 $\mu$ F bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 $\mu$ F and 1 $\mu$ F are commonly used in parallel.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

## 8.4.2 Layout Example

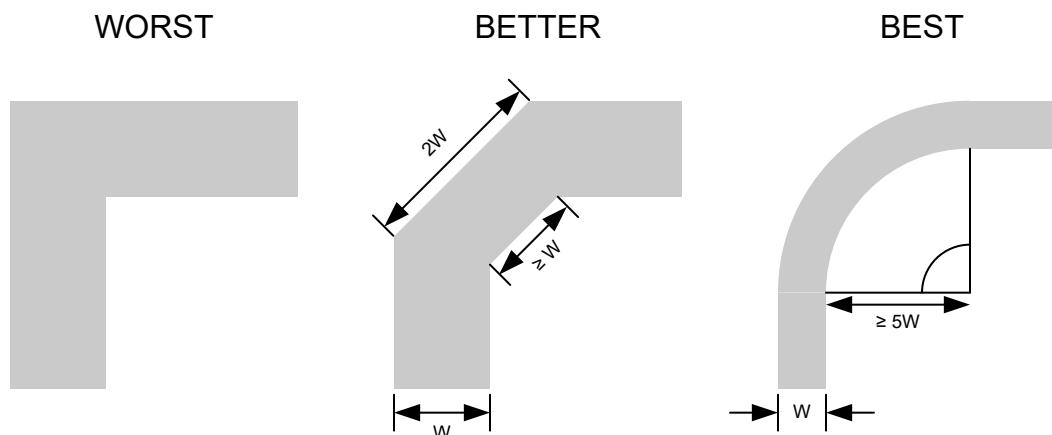


Figure 8-3. Example Trace Corners for Improved Signal Integrity

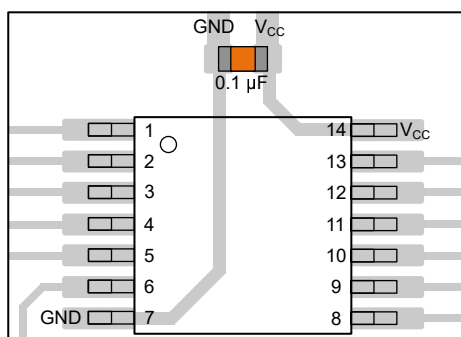


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

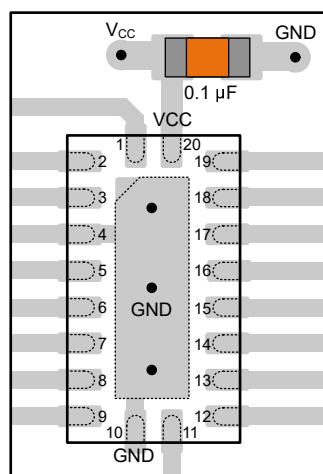


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

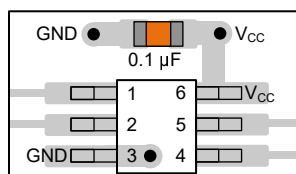


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

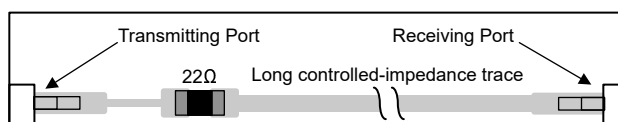


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and  \$C\_{pd}\$  Calculation](#) application note
- Texas Instruments, [Designing With Logic](#) application note
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#) application brief
- Texas Instruments, [Logic in Live-Insertion Applications With a Focus on GTLP](#) application note
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application note
- Texas Instruments, [Texas Instruments General Quality Guidelines](#)
- Texas Instruments, [Thermal Characteristics of SLL Packages and Devices](#) application note
- Texas Instruments, [Understanding Schmitt Triggers](#) application brief

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE           | REVISION | NOTES           |
|----------------|----------|-----------------|
| September 2026 | *        | Initial Release |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LVC2G00QDCTRQ1</a> | Active        | Production           | SSOP (DCT)   8 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -            | 46A5                |

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

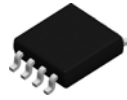
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC2G00-Q1 :

- Catalog : [SN74LVC2G00](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

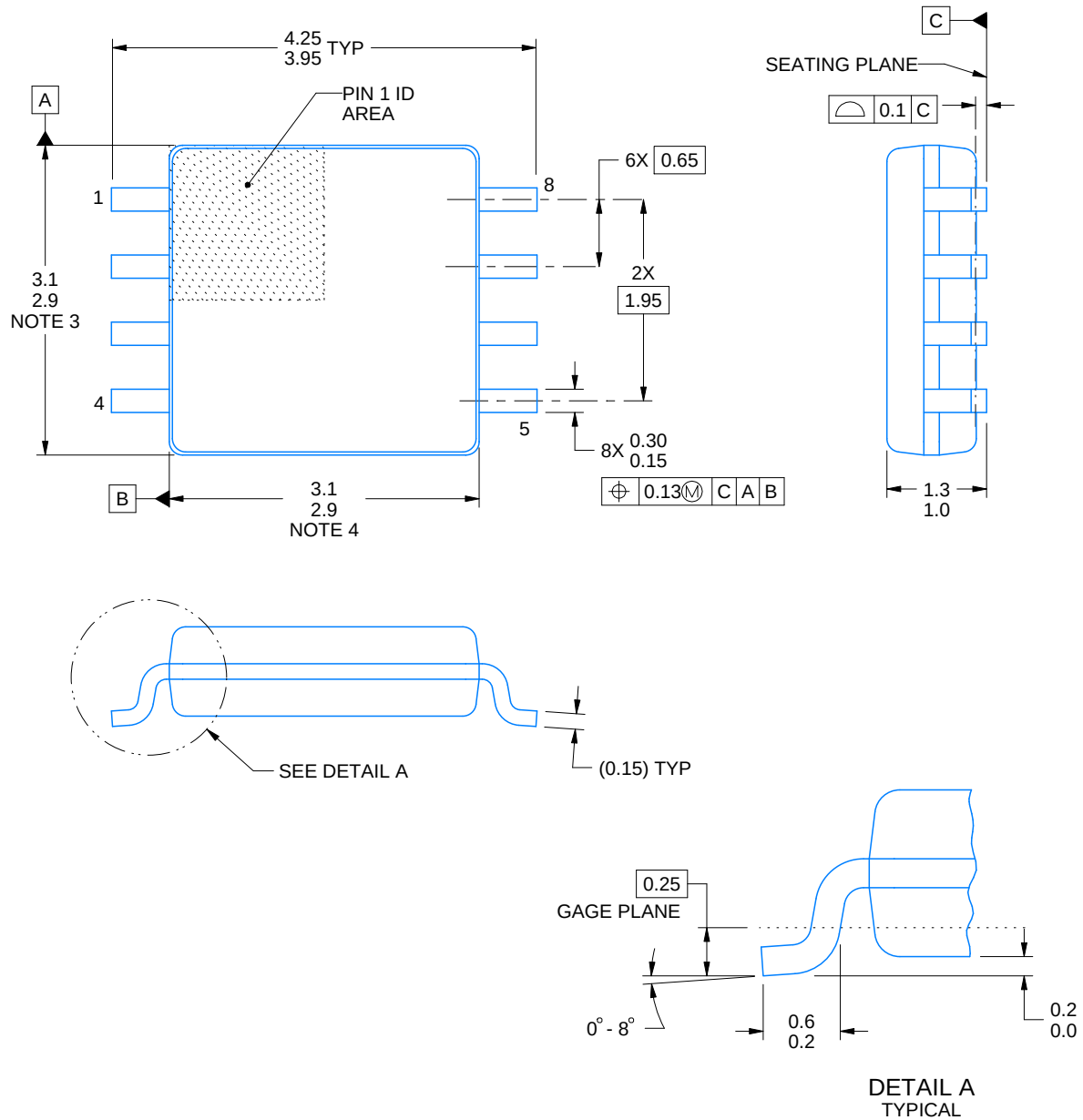


DCT0008A

## PACKAGE OUTLINE

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



4220784/D 10/2025

### NOTES:

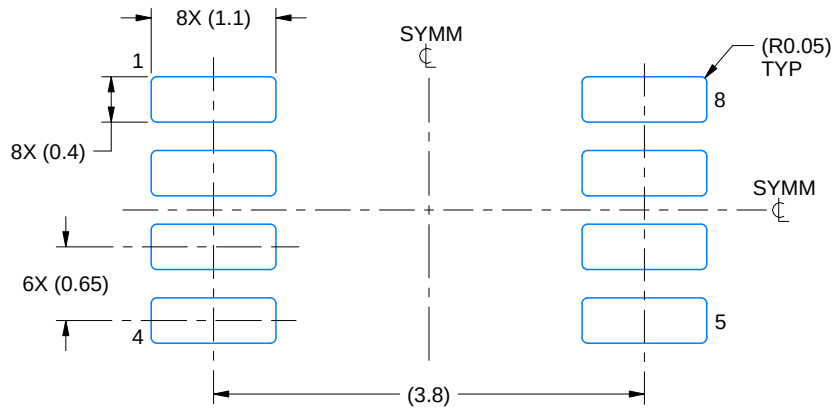
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

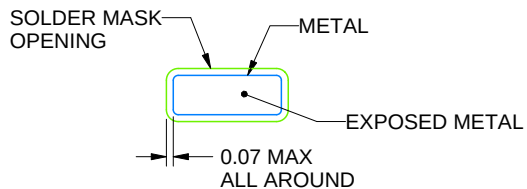
DCT0008A

SSOP - 1.3 mm max height

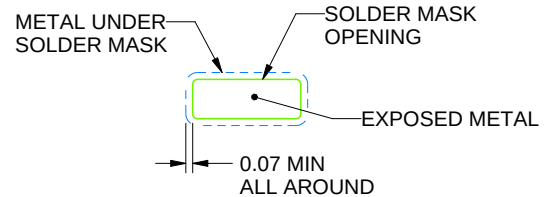
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

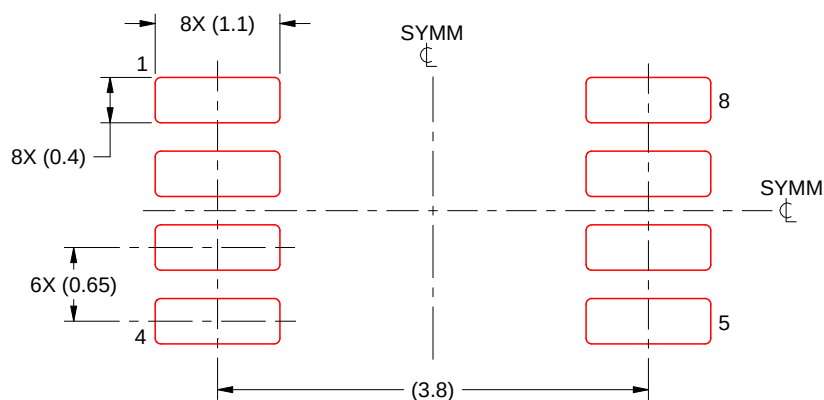
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025