

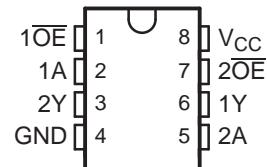
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Check for Samples: [SN74LVC2G125-Q1](#)

FEATURES

- Qualified for Automotive Applications
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.3 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

DCT OR DCU PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74LVC2G125-Q1 is a dual bus buffer gate designed for 1.65-V to 5.5-V V_{CC} operation. This device features dual line drivers with 3-state outputs. The outputs are disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|---------------|------------------------|---------------|-----------------------|---------------------------------|
| -40°C to 85°C | SSOP – DCT | Tape and reel | CLVC2G125IDCTRQ1 | C25--- |
| | VSSOP – DCU | Tape and reel | CLVC2G125IDCURQ1 | CCW_ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site.

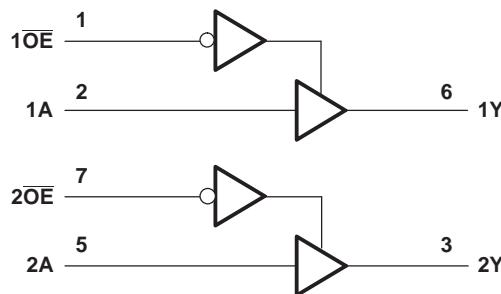
FUNCTION TABLE (EACH BUFFER)

| INPUTS | | OUTPUT Y |
|-----------------|---|-------------|
| \overline{OE} | A | |
| L | H | H |
| L | L | L |
| H | X | Z |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LOGIC DIAGRAM (POSITIVE LOGIC)

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ^{(2) (3)} | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current $V_I < 0$ | | -50 | mA |
| I_{OK} | Output clamp current $V_O < 0$ | | -50 | mA |
| I_O | Continuous output current | | ± 50 | mA |
| | Continuous current through V_{CC} or GND | | ± 100 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DCT package | 220 | °C/W |
| | | DCU package | 227 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|------------------------------------|---|------------------------|-----------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 3 V to 3.6 V | 2 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | | |
| | | V _{CC} = 3 V to 3.6 V | 0.8 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.3 × V _{CC} | | |
| V _I | Input voltage | | 0 | 5.5 | V |
| V _O | Output voltage | High or low state | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | -4 | mA |
| | | V _{CC} = 2.3 V | | -8 | |
| | | V _{CC} = 3 V | | -16 | |
| | | V _{CC} = 4.5 V | | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 3 V | | 16 | |
| | | V _{CC} = 4.5 V | | 24 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | V _{CC} = 3.3 V ± 0.3 V | | 10 | |
| | | V _{CC} = 5 V ± 0.5 V | | 5 | |
| T _A | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|-----------------------------|--|-----------------|-----------------------|--------------------|-----|------|
| V _{OH} | I _{OH} = -100 µA | | 1.65 V to 5.5 V | V _{CC} – 0.1 | | | V |
| | I _{OH} = -4 mA | | 1.65 V | 1.2 | | | |
| | I _{OH} = -8 mA | | 2.3 V | 1.9 | | | |
| | I _{OH} = -16 mA | | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | | | 2.3 | | | |
| | I _{OH} = -32 mA | | 4.5 V | 3.8 | | | |
| V _{OL} | I _{OL} = 100 µA | | 1.65 V to 5.5 V | | 0.1 | | V |
| | I _{OL} = 4 mA | | 1.65 V | | 0.45 | | |
| | I _{OL} = 8 mA | | 2.3 V | | 0.3 | | |
| | I _{OL} = 16 mA | | 3 V | 0.4 | | | |
| | I _{OL} = 24 mA | | | 0.55 | | | |
| | I _{OL} = 32 mA | | 4.5 V | 0.55 | | | |
| I _I | A or \overline{OE} inputs | V _I = 5.5 V or GND | | 0 to 5.5 V | | ±5 | µA |
| I _{off} | | V _I or V _O = 5.5 V | | 0 | | ±10 | µA |
| I _{OZ} | | V _O = 0 to 5.5 V | | 3.6 V | | 10 | µA |
| I _{CC} | | V _I = 5.5 V or GND, I _O = 0 | | 1.65 V to 5.5 V | | 10 | µA |
| ΔI _{CC} | | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | | 3 V to 5.5 V | | 500 | µA |
| C _i | Data inputs | V _I = V _{CC} or GND | | 3.3 V | 3.5 | | pF |
| | Control inputs | | | | 4 | | |
| C _o | | V _O = V _{CC} or GND | | 3.3 V | | 6.5 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

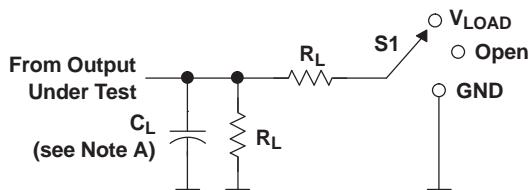
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 1.8 V ± 0.15 V | V _{CC} = 2.5 V ± 0.2 V | V _{CC} = 3.3 V ± 0.3 V | V _{CC} = 5 V ± 0.5 V | UNIT | |
|------------------|-----------------|----------------|-------------------------------------|------------------------------------|------------------------------------|----------------------------------|---------|------------|
| | | | MIN | MAX | MIN | MAX | | |
| t _{pd} | A | Y | 3.3 | 9.1 | 1.5 | 4.8 | 1.4 4.3 | 1 3.7 ns |
| t _{en} | \overline{OE} | Y | 4 | 9.9 | 1.9 | 5.6 | 1.2 4.7 | 1.2 3.8 ns |
| t _{dis} | \overline{OE} | Y | 1.5 | 11.6 | 1 | 5.8 | 1.4 4.6 | 1 3.4 ns |

Operating Characteristics

T_A = 25°

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | V _{CC} = 5 V | UNIT | |
|-----------------|-------------------------------|-------------------------------|-------------------------|-------------------------|-----------------------|------|----|
| | | TYP | TYP | TYP | TYP | | |
| C _{pd} | Power dissipation capacitance | Outputs enabled f = 10 MHz | 19 | 19 | 20 | 22 | pF |
| | | | 2 | 2 | 2 | 3 | |

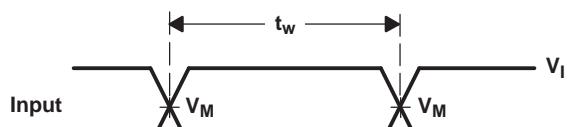
PARAMETER MEASUREMENT INFORMATION



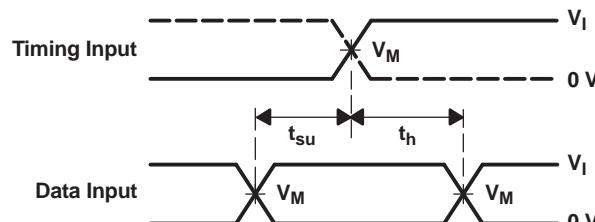
| TEST | S_1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

LOAD CIRCUIT

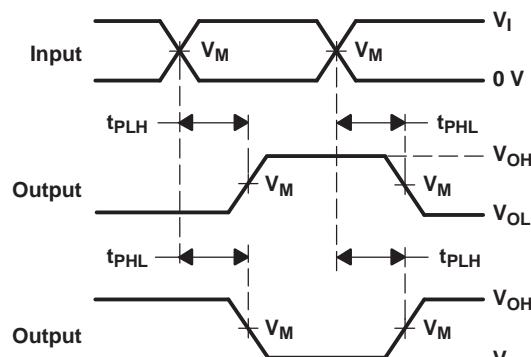
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|------------------------------------|----------|-----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8 \text{ V} \pm 0.15 \text{ V}$ | V_{CC} | $\leq 2 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | V_{CC} | $\leq 2 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 3 V | $\leq 2.5 \text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5 \text{ V} \pm 0.5 \text{ V}$ | V_{CC} | $\leq 2.5 \text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



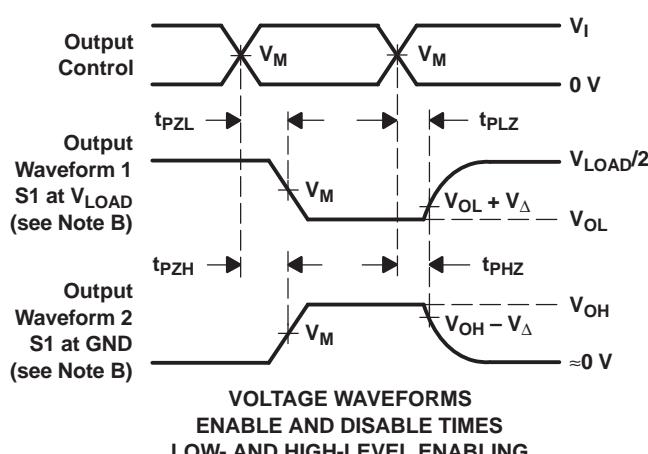
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CLVC2G125IDCTRQ1 | Active | Production | SSOP (DCT) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C25 Z |
| CLVC2G125IDCTRQ1.B | Active | Production | SSOP (DCT) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C25 Z |
| CLVC2G125IDCURQ1 | Active | Production | VSSOP (DCU) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CCWR |
| CLVC2G125IDCURQ1.B | Active | Production | VSSOP (DCU) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CCWR |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC2G125-Q1 :

- Catalog : [SN74LVC2G125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CLVC2G125IDCURQ1 | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

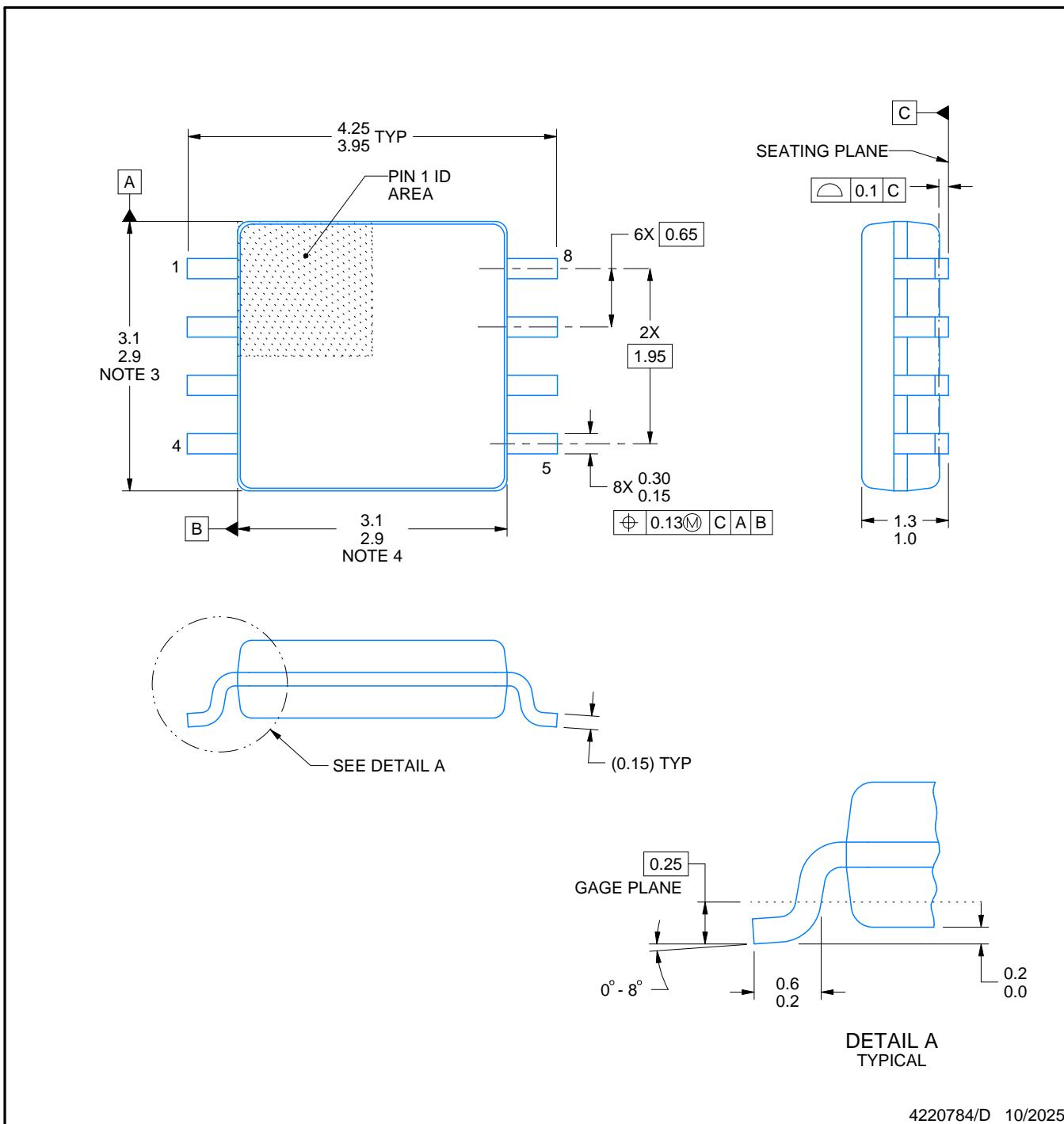
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CLVC2G125IDCURQ1 | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |



PACKAGE OUTLINE

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



NOTES:

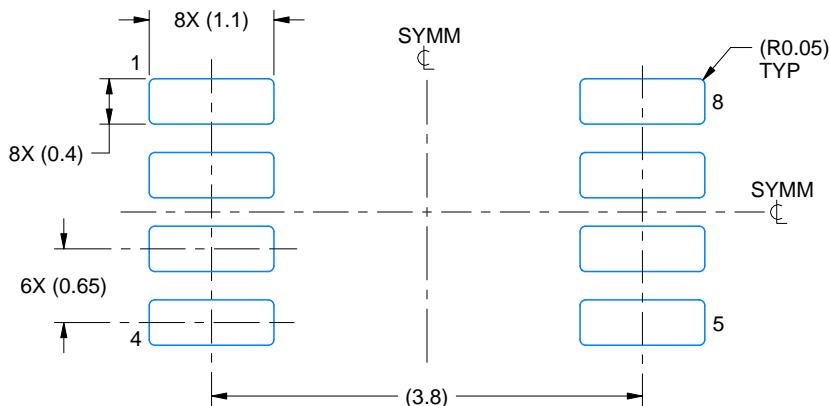
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

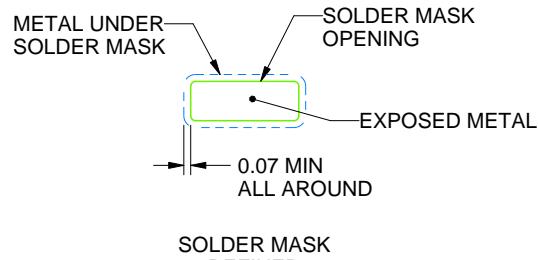
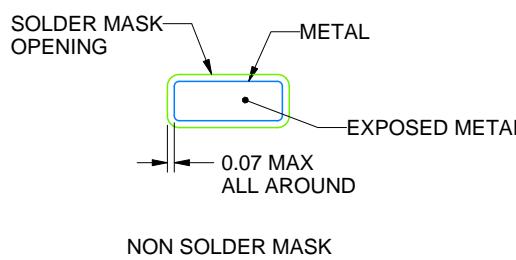
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

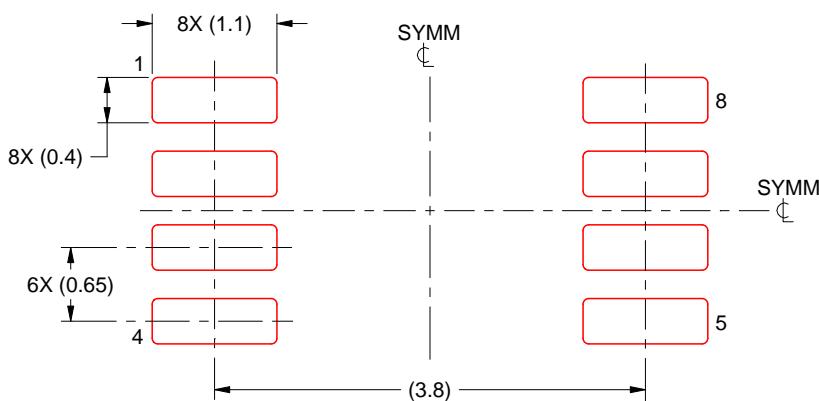
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

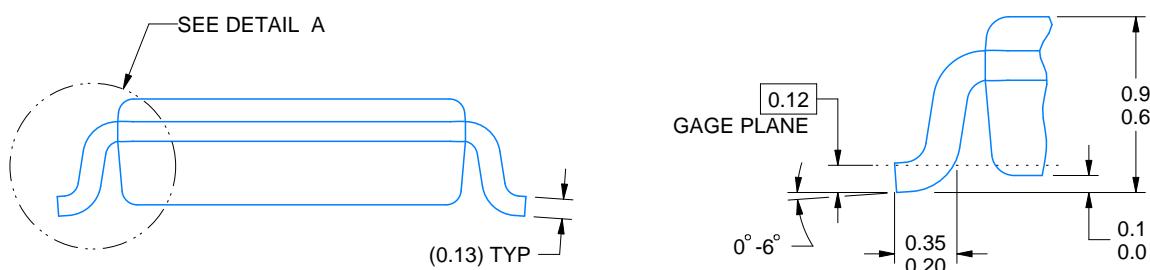
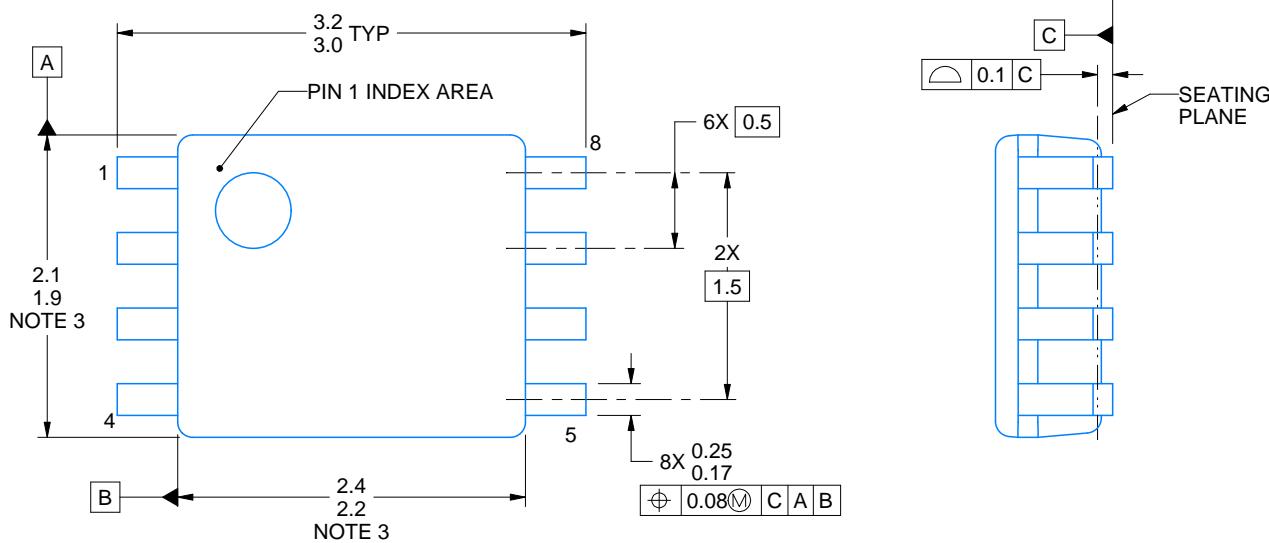
PACKAGE OUTLINE

DCU0008A



VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



DETAIL A TYPICAL

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

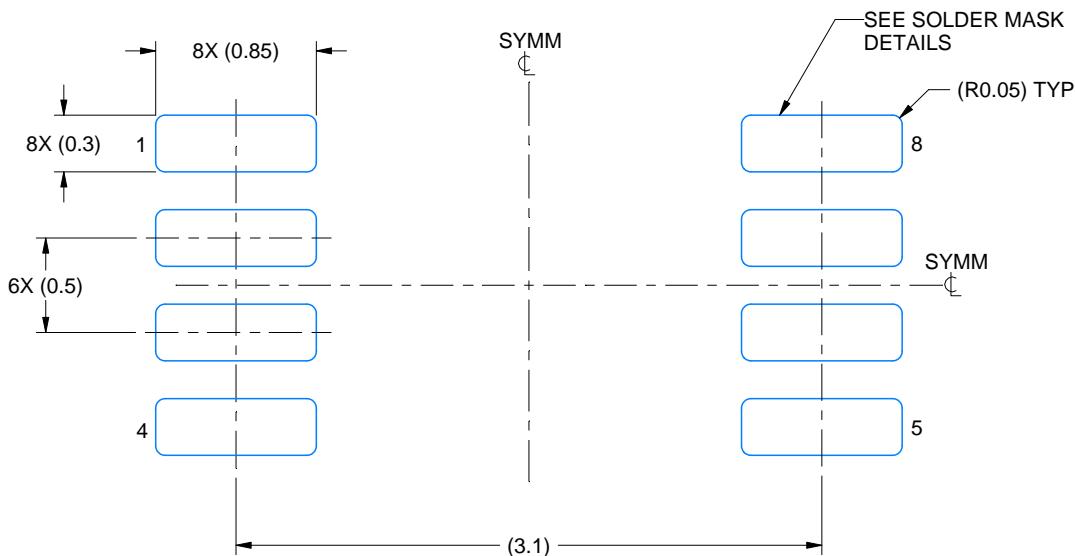
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EXAMPLE BOARD LAYOUT

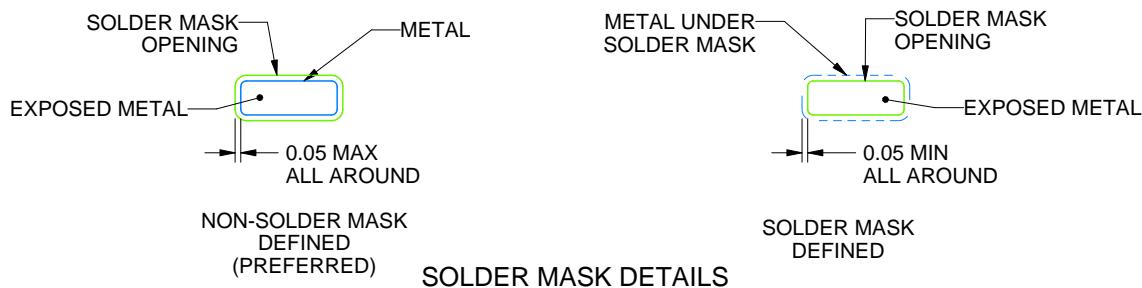
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

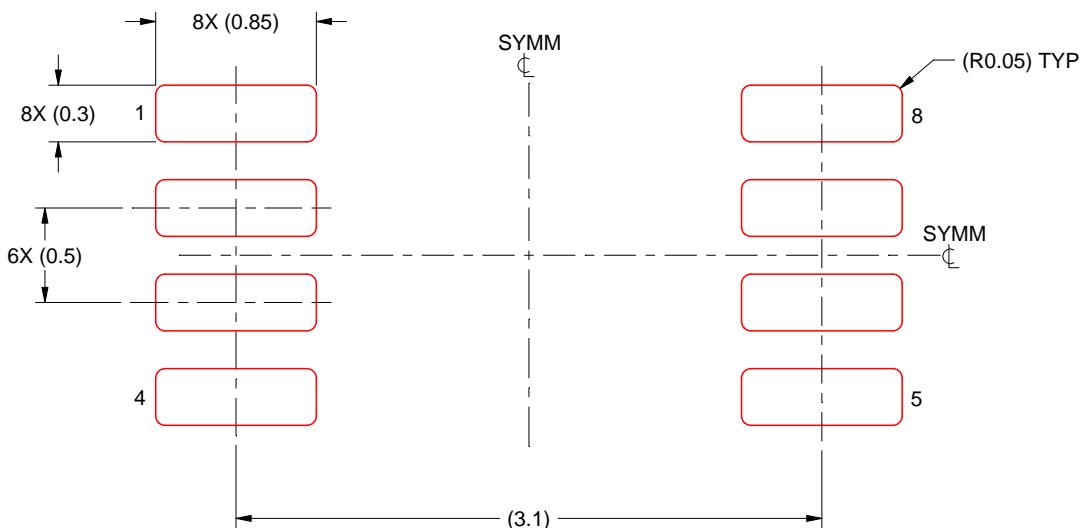
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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