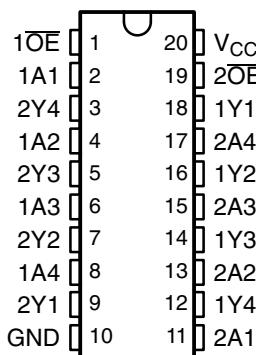


**SN54LVTH240, SN74LVTH240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS**

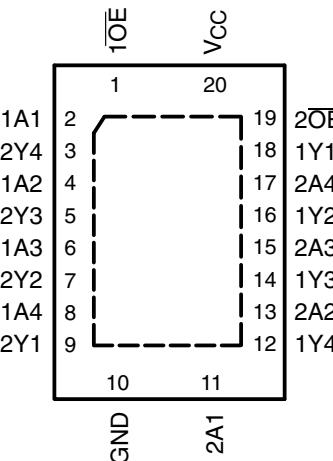
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

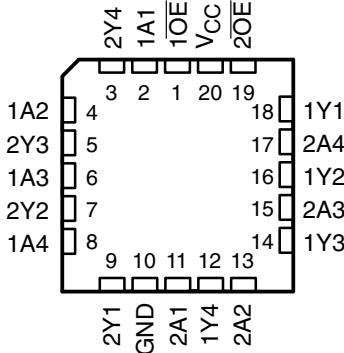
SN54LVTH240 . . . J OR W PACKAGE
SN74LVTH240 . . . DB, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVTH240 . . . RGY PACKAGE
(TOP VIEW)



SN54LVTH240 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	SN74LVTH240RGYR	LXH240
	SOIC – DW	Tube	LVTH240
		SN74LVTH240DW	
	SOP – NS	SN74LVTH240NSR	LVTH240
	SSOP – DB	SN74LVTH240DBR	LXH240
	TSSOP – PW	Tube	LXH240
		SN74LVTH240PW	
-55°C to 125°C	Tape and reel	SN74LVTH240PWR	LXH240
		SN74LVTH240GQNR	
	VFBGA – GQN	SN74LVTH240ZQNR	LXH240
-55°C to 125°C	CDIP – J	SNJ54LVTH240J	SNJ54LVTH240J
	CFP – W	SNJ54LVTH240W	SNJ54LVTH240W
	LCCC – FK	SNJ54LVTH240FK	SNJ54LVTH240FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54LVTH240, SN74LVTH240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS**

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description/ordering information (continued)

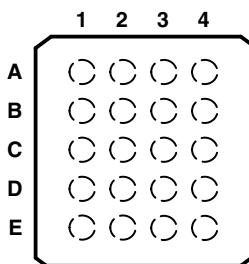
These devices are organized as two 4-bit buffer/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the devices pass data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**SN74LVTH240 . . . GQN OR ZQN PACKAGE
(TOP VIEW)**



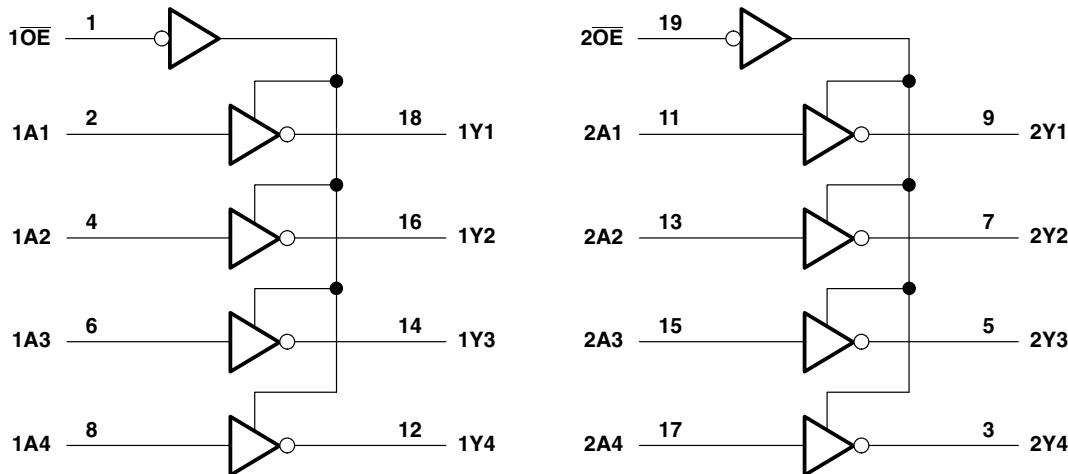
terminal assignments

	1	2	3	4
A	1A1	$1\overline{OE}$	V_{CC}	$2\overline{OE}$
B	1A2	2A4	2Y4	1Y1
C	1A3	2Y3	2A3	1Y2
D	1A4	2A2	2Y2	1Y3
E	GND	2Y1	2A1	1Y4

**FUNCTION TABLE
(each 4-bit buffer)**

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	L
L	L	H
H	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

**SN54LVTH240, SN74LVTH240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS**

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recommended operating conditions (see Note 5)

		SN54LVTH240		SN74LVTH240		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage			0.8	0.8	V
V _I	Input voltage			5.5	5.5	V
I _{OH}	High-level output current			-24	-32	mA
I _{OL}	Low-level output current			48	64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate			200	200	μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SN54LVTH240, SN74LVTH240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH240			SN74LVTH240			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2				2	
		$I_{OH} = -32 \text{ mA}$						
V_{OL}	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24 \text{ mA}$		0.5			0.5	
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4			0.4	
		$I_{OL} = 32 \text{ mA}$		0.5			0.5	
		$I_{OL} = 48 \text{ mA}$		0.55				
		$I_{OL} = 64 \text{ mA}$					0.55	
I_I	Control inputs	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		10			10	μA
		$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$	1			1	
			$V_I = 0$		-5		-5	
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_{I(\text{hold})}$	Data inputs	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	75			75	μA
			$V_I = 2 \text{ V}$	-75			-75	
		$V_{CC} = 3.6 \text{ V}^\ddagger$	$V_I = 0 \text{ to } 3.6 \text{ V}$				500 -750	
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $\text{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $\text{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\S	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3 \text{ V or } 0$			3			3	pF
C_o	$V_O = 3 \text{ V or } 0$			7			7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

**SN54LVTH240, SN74LVTH240
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS**

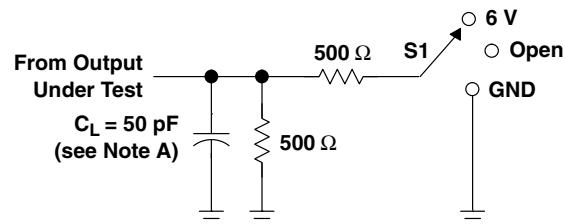
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

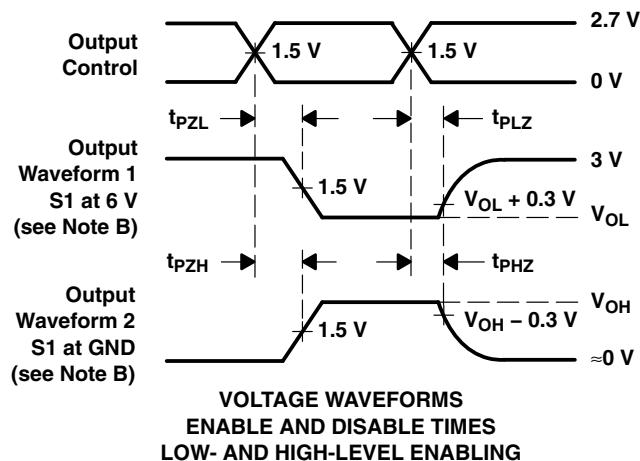
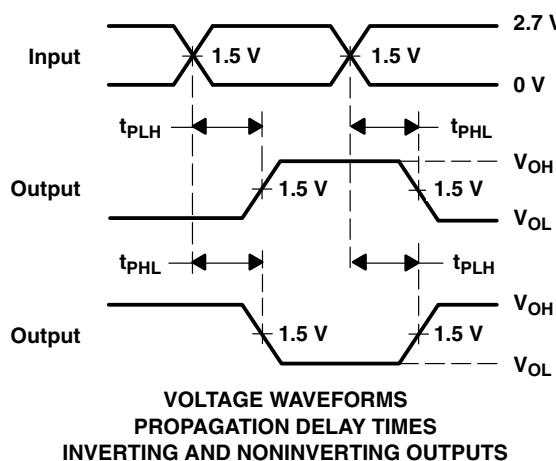
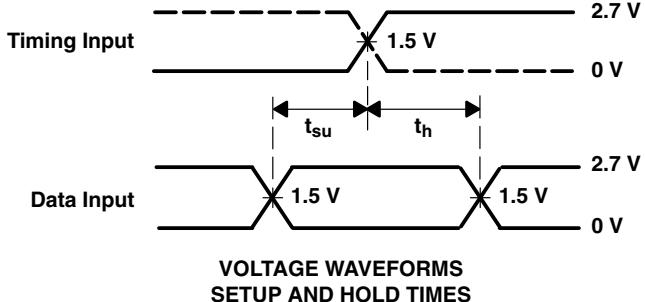
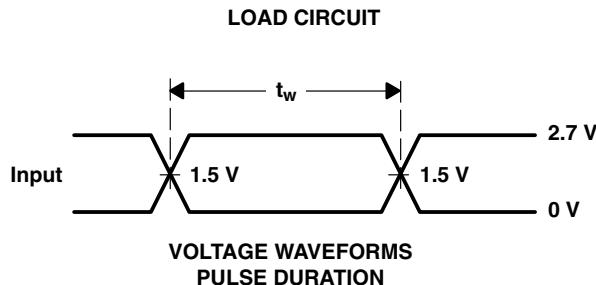
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH240		SN74LVTH240				UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP [†]	MAX	
t_{PLH}	A	Y	0.9	4.3	5.1	1.1	2.2	3.8	4.6	ns
t_{PHL}			1.2	4.7	4.9	1.3	2.6	4	4.2	
t_{PZH}	\overline{OE}	Y	1	5.7	6.7	1.1	2.6	4.6	5.6	ns
t_{PZL}			1.2	5.5	6.2	1.4	2.7	4.4	5	
t_{PHZ}	\overline{OE}	Y	1	5.1	5.2	2	2.9	4.4	4.6	ns
t_{PLZ}			1.1	5.4	5.4	1.8	3	4.3	4.3	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- The outputs are measured one at a time with one transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9950801Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9950801Q2A SNJ54LVTH240FK
5962-9950801QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9950801QR A SNJ54LVTH240J
5962-9950801QSA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9950801QS A SNJ54LVTH240W
SN74LVTH240DBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240DBR.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240DBRG4	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240DBRG4.B	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240DW.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240DWR.B	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240DWRE4	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240NSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240NSR.B	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240NSRG4	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240NSRG4.B	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH240
SN74LVTH240PW	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240PW.B	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240PWG4	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240PWG4.B	Active	Production	TSSOP (PW) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240
SN74LVTH240PWR.B	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH240

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LVTH240FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9950801Q2A SNJ54LVTH 240FK
SNJ54LVTH240J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9950801QR A SNJ54LVTH240J
SNJ54LVTH240W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9950801QS A SNJ54LVTH240W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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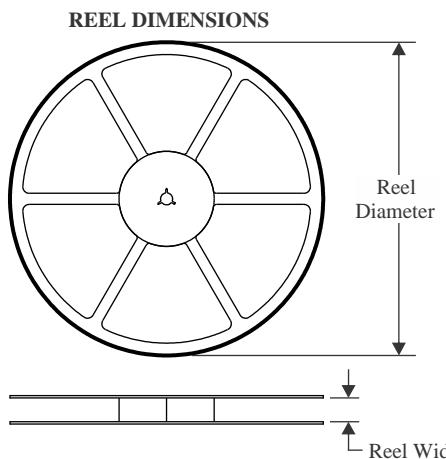
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVTH240, SN74LVTH240 :

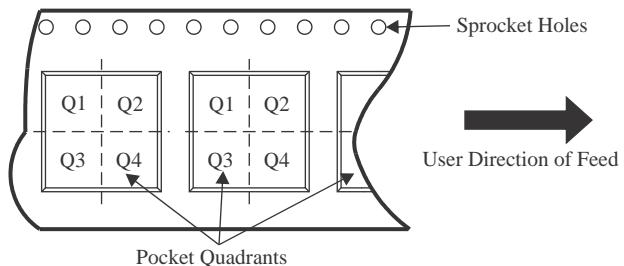
- Catalog : [SN74LVTH240](#)
- Military : [SN54LVTH240](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


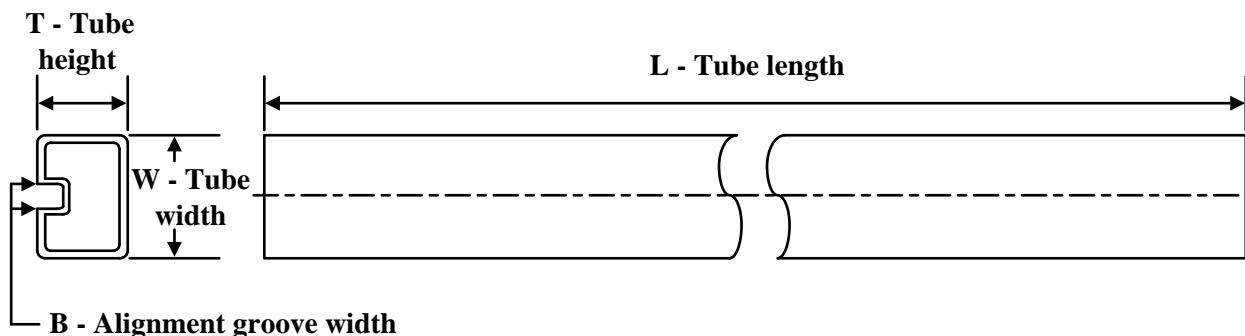
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH240DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVTH240DBRG4	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVTH240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVTH240NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVTH240NSRG4	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVTH240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH240DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVTH240DBRG4	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVTH240DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVTH240NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVTH240NSRG4	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVTH240PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
5962-9950801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74LVTH240DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVTH240DW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVTH240PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVTH240PW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVTH240PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVTH240PWG4.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54LVTH240FK	FK	LCCC	20	55	506.98	12.06	2030	NA

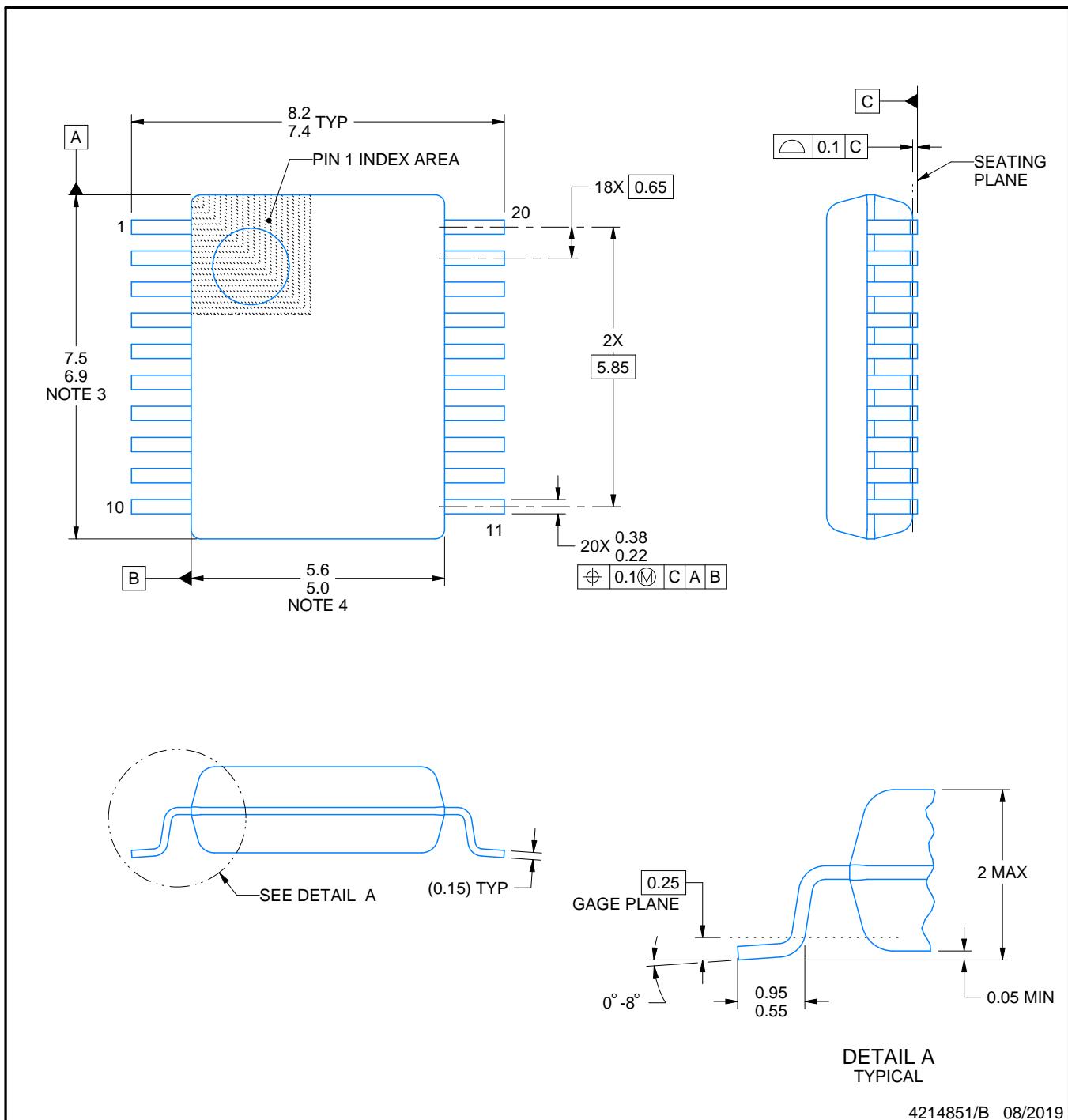
PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

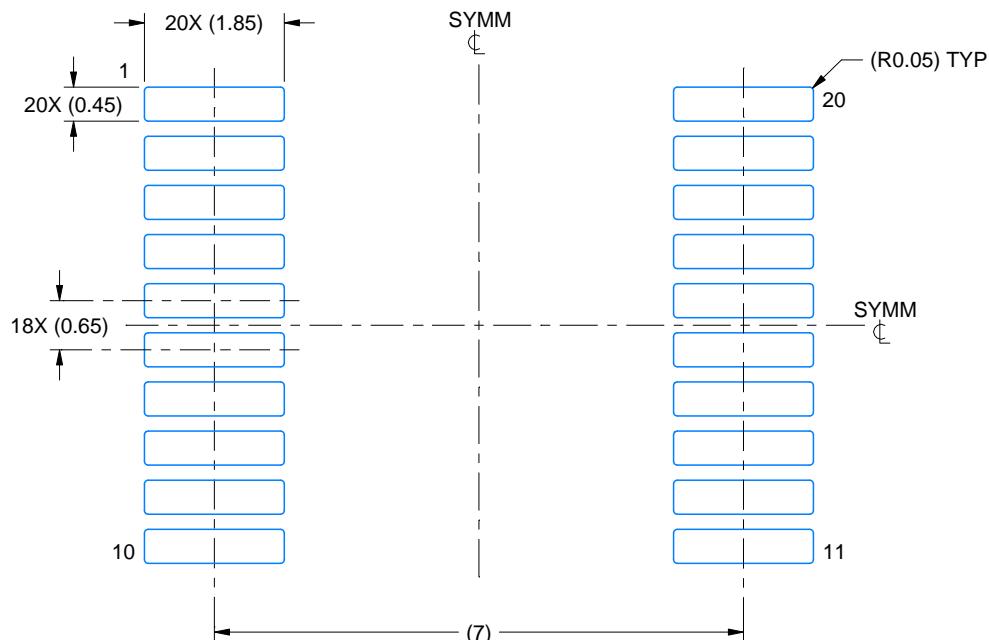
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

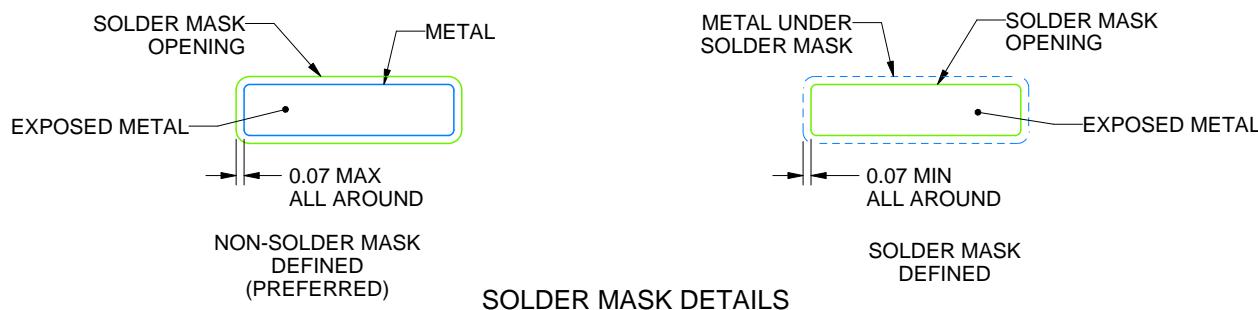
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

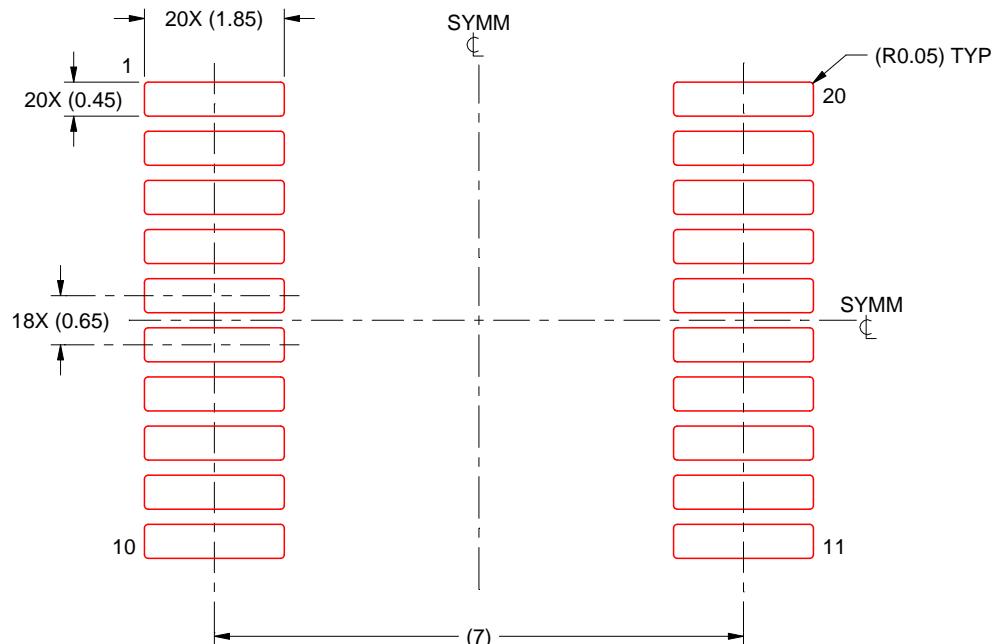
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



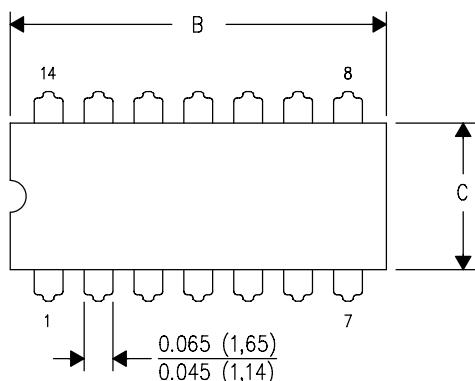
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

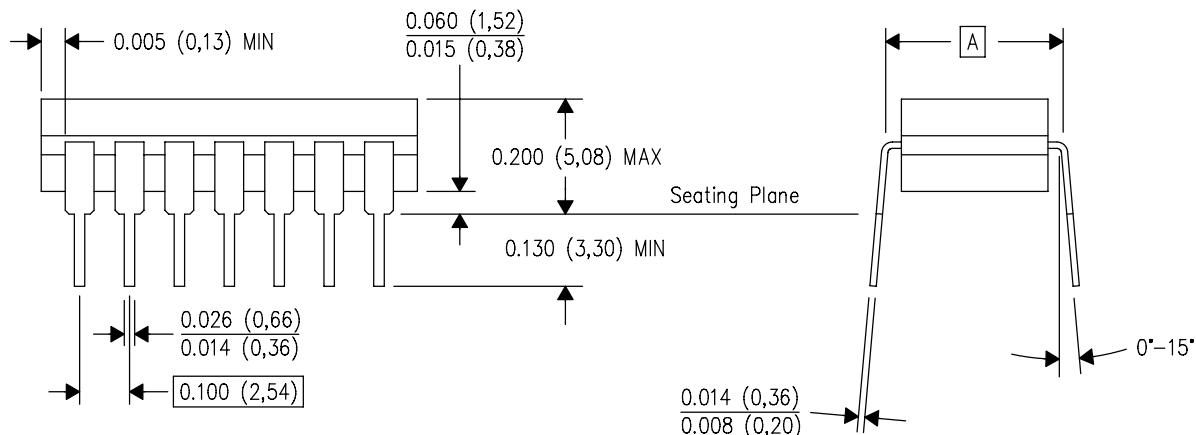
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

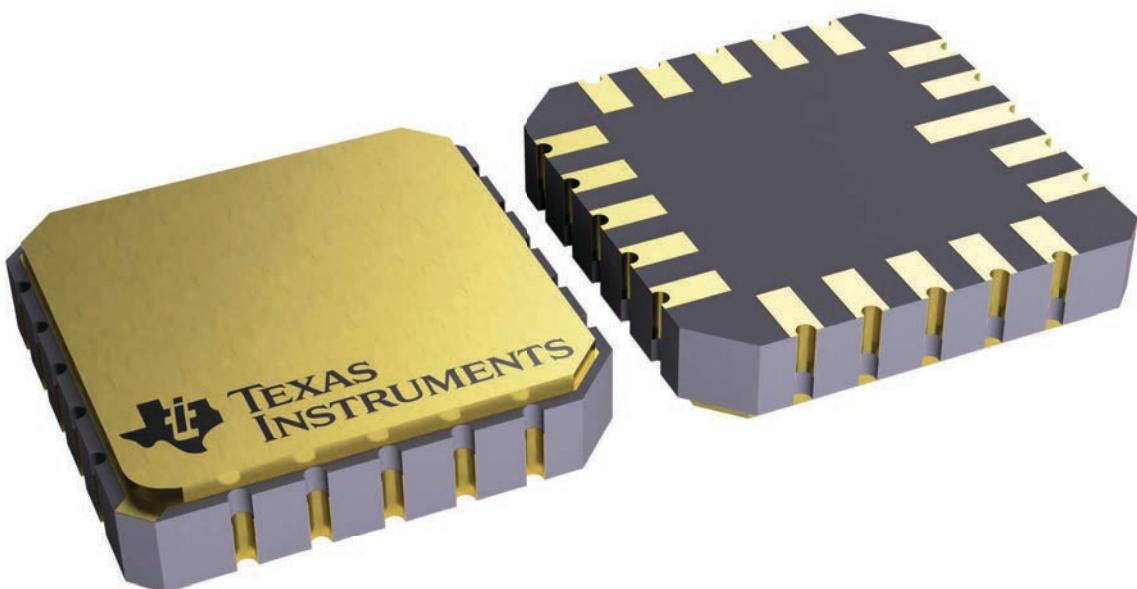
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

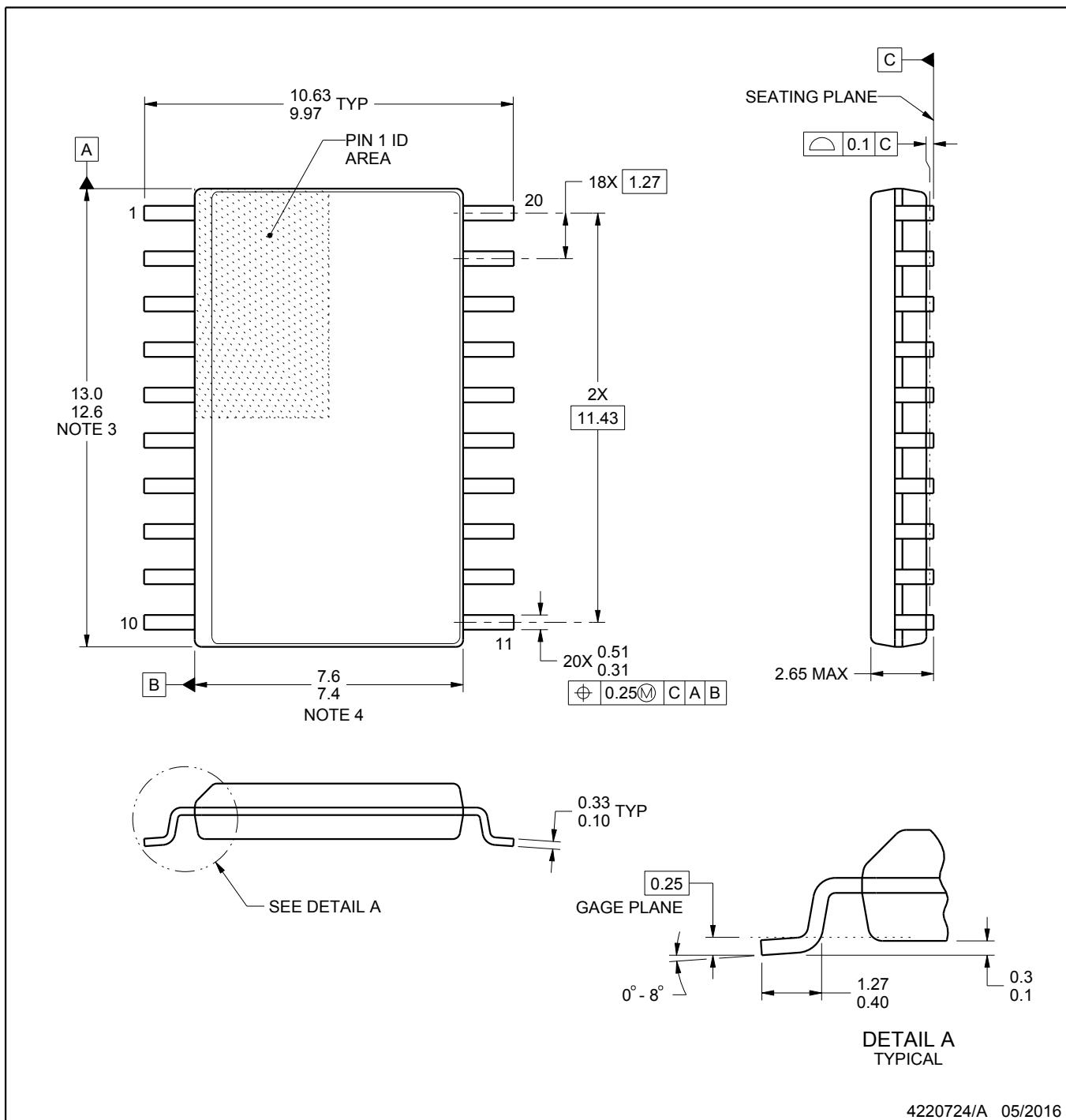
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

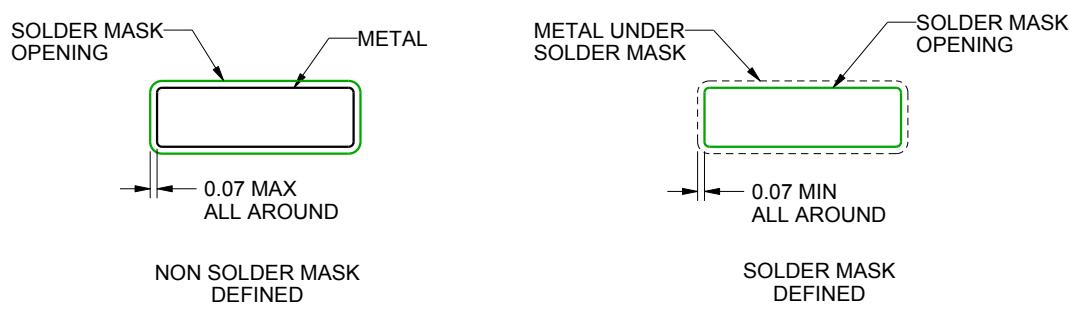
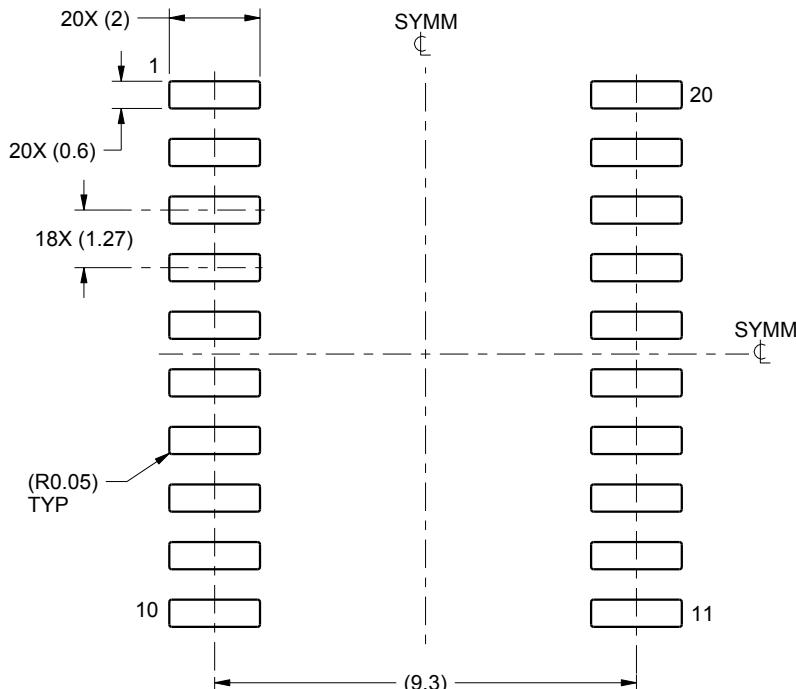
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

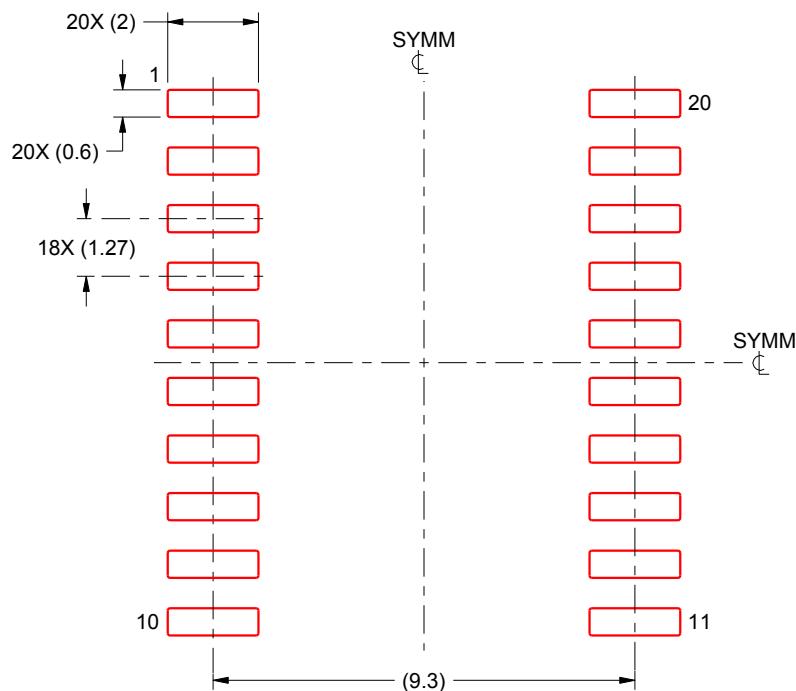
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

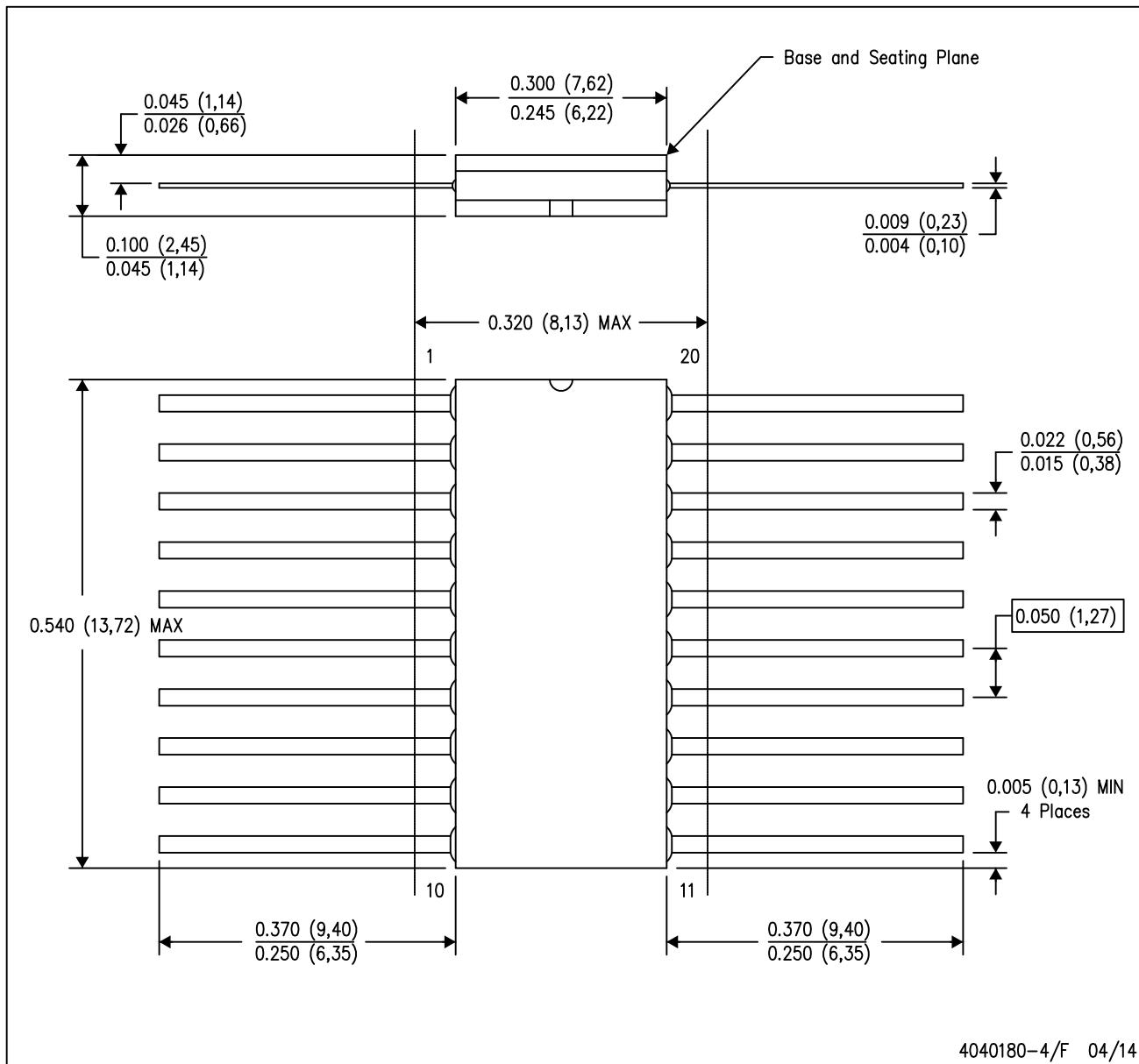
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

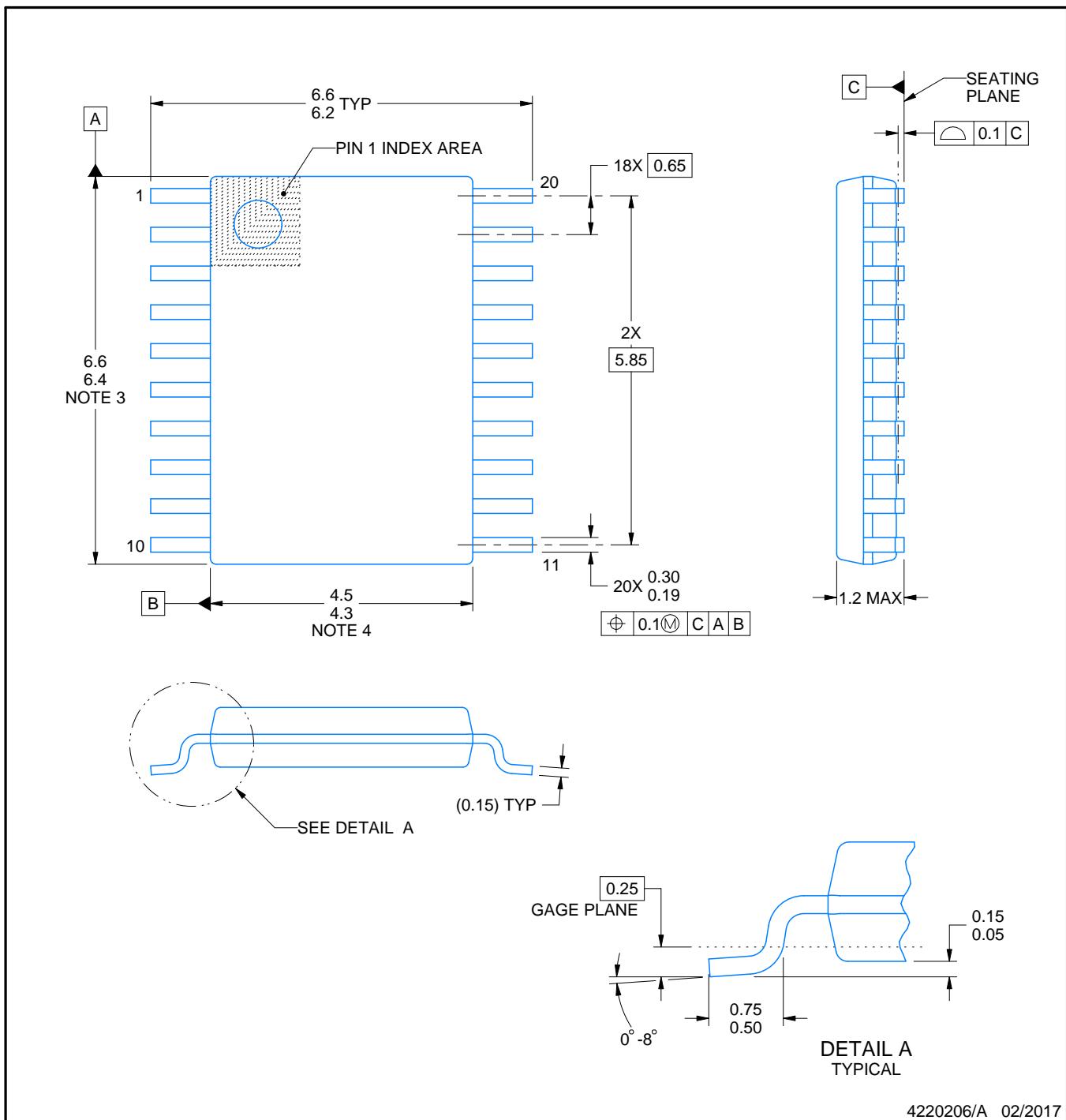
PACKAGE OUTLINE

PW0020A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

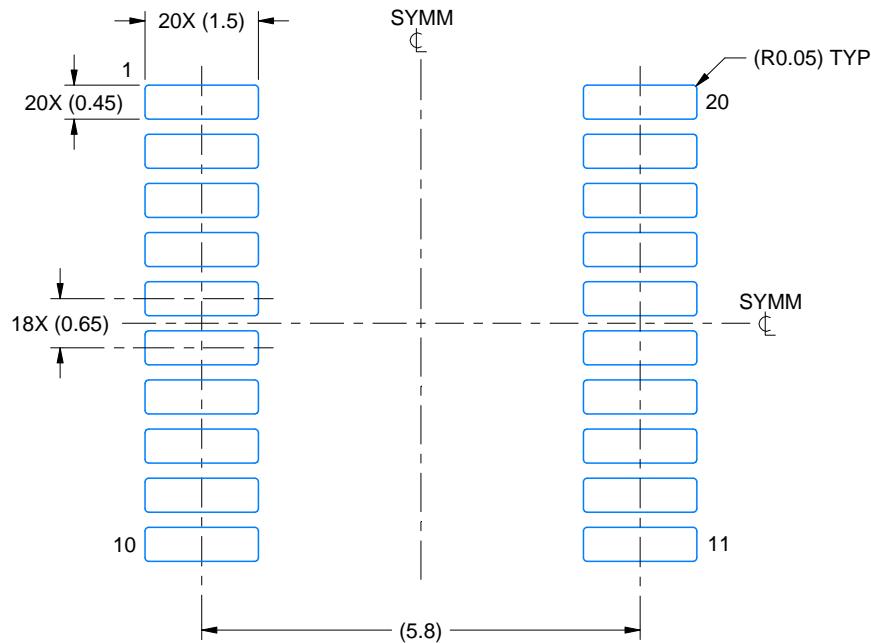
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

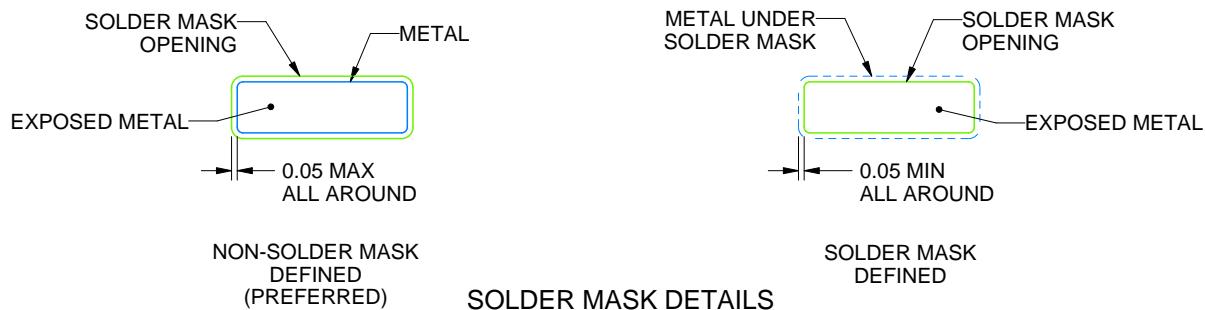
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

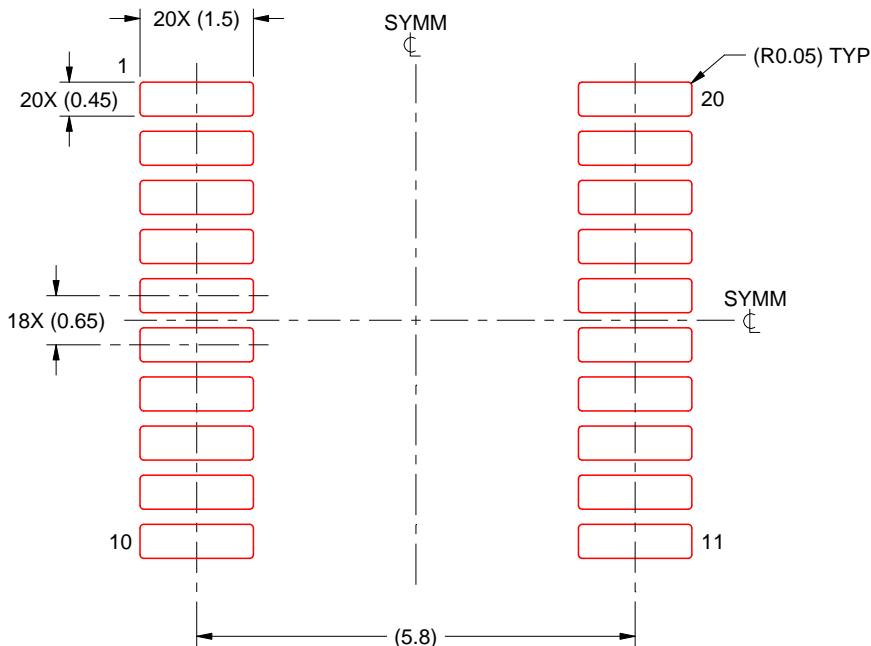
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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