28-Bit to 56-Bit Registered Buffer With Address Parity Test One Pair to Four Pair Differential Clock PLL Driver

Check for Samples: SN74SSQEC32882

FEATURES

- **JEDEC SSTE32882**
- **1-to-2 Register Outputs and 1-to-4 Clock Pair Outputs Support Stacked DDR3 RDIMMs**
- **CKE Powerdown Mode for Optimized System Power Consumption**
- **1.5V/1.35V/1.25V Phase Lock Loop Clock Driver for Buffering One Differential Clock Pair (CK and $\overline{CK}$) and Distributing to Four Differential Outputs**
- **1.5V/1.35V/1.25V CMOS Inputs**
- **Checks Parity on Command and Address (CS-Gated) Data Inputs**
- **Configurable Driver Strength**
- **Uses Internal Feedback Loop**
- **Optimized Power Consumption**

APPLICATIONS

- **DDR3 Registered DIMMs up to DDR3-1866**
- **DDR3L Registered DIMMs up to DDR3L-1600**
- **DDR3U Registered DIMMs up to DDR3U-1333**
- **Single-, Dual- and Quad-Rank RDIMM**

DESCRIPTION

This 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for operation on DDR3 registered DIMMs with V_{DD} of 1.5 V, on DDR3L registered DIMMs with V_{DD} of 1.35 V and on DDR3U registered DIMMs with V_{DD} of 1.25 V.

All inputs are 1.5 V, 1.35V and 1.25 V CMOS compatible. All outputs are CMOS drivers optimized to drive DRAM signals on terminated traces in DDR3 RDIMM applications. The clock outputs Yn and $\overline{Yn}$ and control net outputs DxCKEn, DxCSn and DxODTn can be driven with a different strength and skew to optimize signal integrity, compensate for different loading and equalize signal travel speed.

The SN74SSQEC32882 has two basic modes of operation associated with the Quad Chip Select Enable ($\overline{QCSEN}$) input. When the $\overline{QCSEN}$ input pin is open (or pulled high), the component has two chip select inputs, $\overline{DCS0}$ and $\overline{DCS1}$, and two copies of each chip select output, $\overline{QACS0}$, $\overline{QACS1}$, $\overline{QBCS0}$ and $\overline{QBCS1}$. This is the "QuadCS disabled" mode. When the $\overline{QCSEN}$ input pin is pulled low, the component has four chip select inputs $\overline{DCS[3:0]}$, and four chip select outputs, $\overline{QCS[3:0]}$. This is the "QuadCS enabled" mode. Through the remainder of this specification, $\overline{DCS[n:0]}$ will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{QxCS[n:0]}$ will indicate all of the chip select outputs.

The device also supports a mode where a single device can be mounted on the back side of a DIMM. If MIRROR=HIGH, Input Bus Termination (IBT) has to stay enabled for all input signals in this case.

The SN74SSQEC32882 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going HIGH, and $\overline{CK}$ going LOW. This data could be either re-driven to the outputs or it could be used to access device internal control registers.

The input bus data integrity is protected by a parity function. All address and command input signals are added up and the last bit of the sum is compared to the parity signal delivered by the system at the input PAR_IN one clock cycle later. If they do not match the device pulls the open drain output $\overline{ERROUT}$ LOW. The control signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{DCS[n:0]}$) are not part of this computation.

The SN74SSQEC32882 implements different power saving mechanisms to reduce thermal power dissipation and to support system power down states. By disabling unused outputs the power consumption is further reduced.

The package is optimized to support high density DIMMs. By aligning input and output positions towards DIMM finger signal ordering and SDRAM ballout the device de-scrambles the DIMM traces allowing low cross talk design with low interconnect latency.

Edge controlled outputs reduce ringing and improve signal eye opening at the SDRAM inputs.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. ORDERING INFORMATION

$T_{CASE(max)}$	PACKAGE(1)		ORDERABLE (2) PART NUMBER	TOP-SIDE MARKING
See Table 4	176ZAL	Tape and Reel	SN74SSQEC32882ZALR	EC32882S

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

APPLICATION INFORMATION

Vendor Specific SPD Content

SPD EEPROM on DDR3 RDIMMs has 3 vendor specific bytes for vendor and revision ID. This information can be sued by the system BIOS. The following table shows the correct values for SN74SSQEC32882.

Table 2. Vendor specific SPD content for SN74SSQEC32882

Byte	Value	Description
65	0x80	Vendor ID, part 1
66	0x97	Vendor ID, part 2
67	0x3D	Revision ID

Application Reports

For additional Information on SN74SSQEC32882 DDR3 Register please review the following application reports:

- DDR3 Register CMR programming
- DDR3 RDIMM SPD settings
- Yn phase shift on SN74SSQEA32882
- DDR3 Register IBT Measurement

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings Over Operating Free-Air Temperature Range(1)

PARAMETER			VALUE	UNIT
V_{DD}	Supply voltage		–0.4 to +1.975	V
V_I	Receiver input voltage	See (2) and (3)	–0.4 to V_{DD} + 0.5	V
V_{REF}	Reference voltage		–0.4 to V_{DD} + 0.5	V
V_O	Driver output voltage	See (2) and (3)	–0.4 to V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	–50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		±100	mA
T_{stg}	Storage temperature		–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 1.975 V maximum.

Table 4. Case Temperature vs Speed Node

PARAMETER		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	UNIT
$T_{case(max)}$	Maximum case temperature (1)	+109	+108	+106	+103	+101	°C

(1) The temperature values fit to JEDEC RAW cards A, B, and C. The user must keep T_{case} below the specified values in order to keep the junction temperature below +125°C. Other combinations of features and termination resistors can require lower case temperature and extra cooling. These combinations depend on the specific application.

PACKAGE INFORMATION

Pinout Configuration

The package is a 8mm × 13.5mm 176-pin BGA with 0.65mm ball pitch in a 11 × 20 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

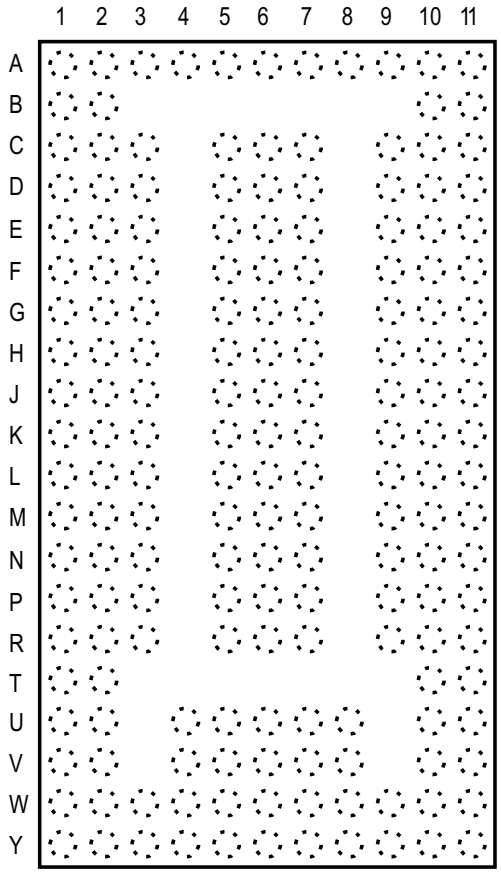


Figure 1. Pinout Configuration

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74SSQEC32882ZALR	Active	Production	NFBGA (ZAL) | 176	2000 | LARGE T&R	Yes	SNAGCU	Level-3-250C-168 HR	0 to 85	EC32882S
SN74SSQEC32882ZALR.A	Active	Production	NFBGA (ZAL) | 176	2000 | LARGE T&R	Yes	SNAGCU	Level-3-250C-168 HR	0 to 85	EC32882S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

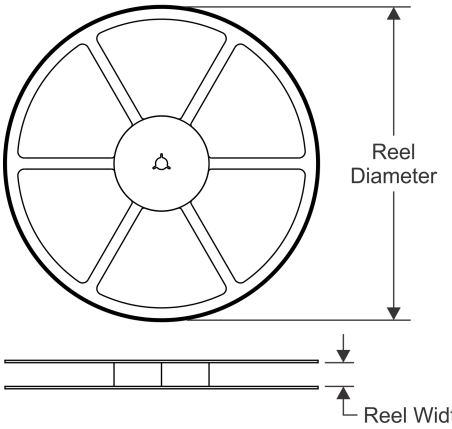
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

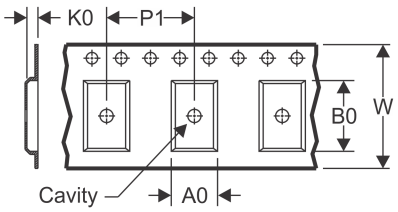
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

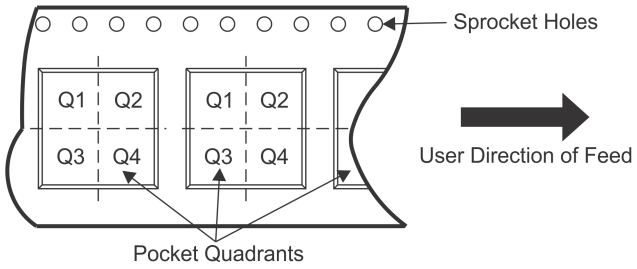


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

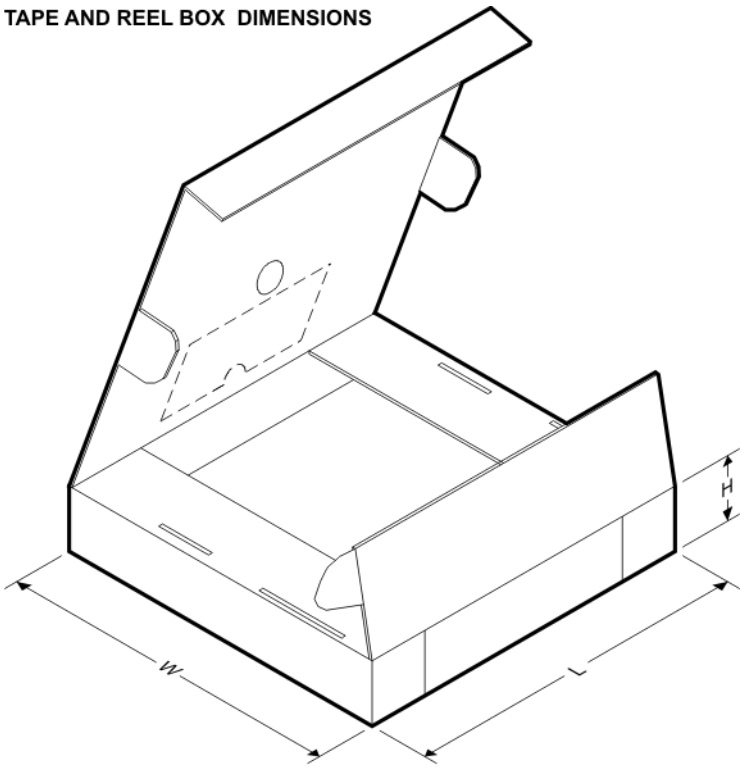
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSQEC32882ZALR	NFBGA	ZAL	176	2000	330.0	24.4	8.3	13.8	1.8	12.0	24.0	Q1

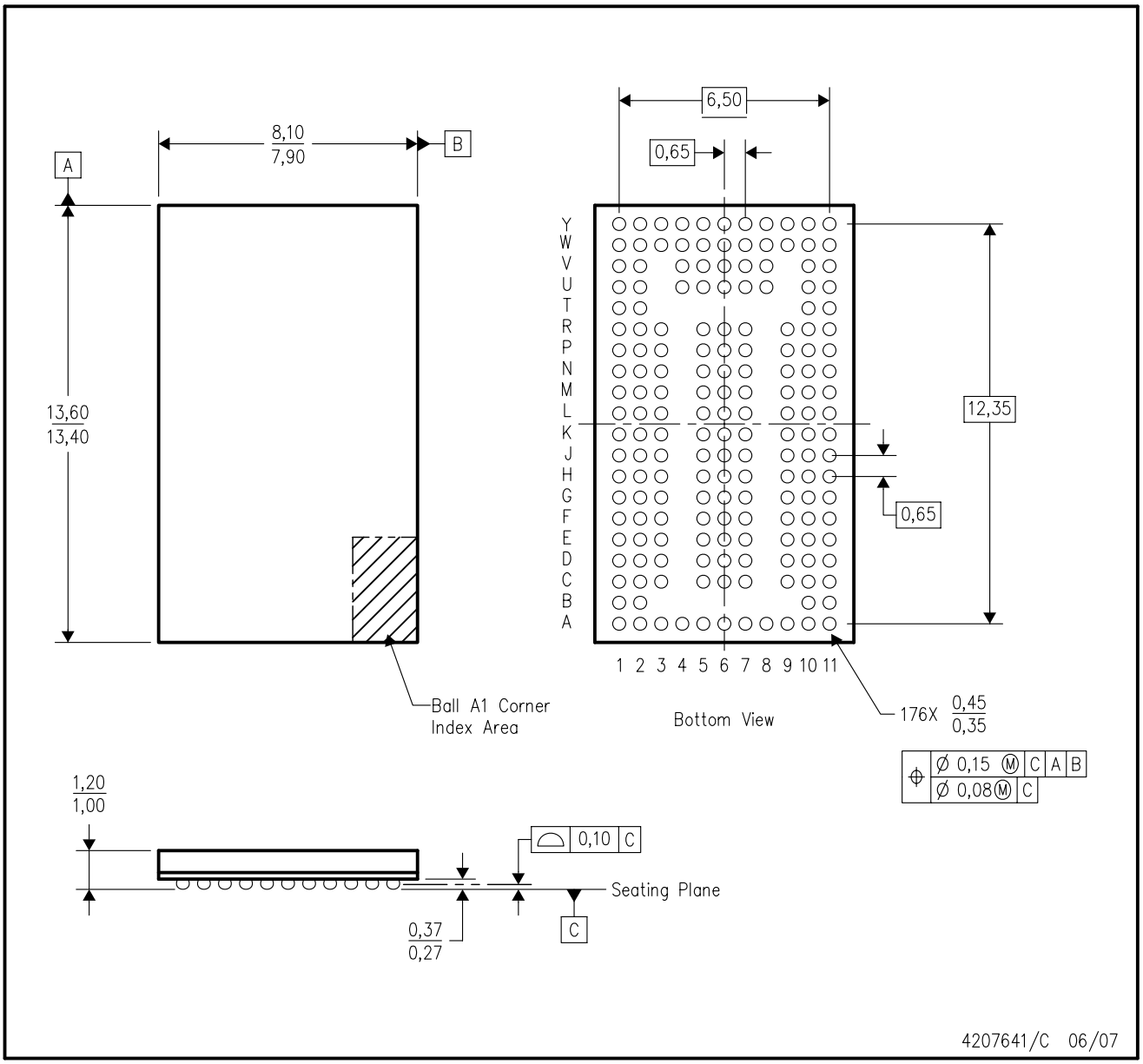
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSQEC32882ZALR	NFBGA	ZAL	176	2000	336.6	336.6	31.8

ZAL (R–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This package is lead–free.

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