SN74UVP1G04 Low-Power Single Inverter Gate

1 Features

- Extended low-voltage operation with 0.63V to 3.6V supply range
- Extended operating temperature range: –40°C to 125°C
- Low power consumption
  - Typical I_{CC} = 10nA
  - Typical input leakage I_I = 3nA
  - Typical output off-state leakage current I_{OZ} = 100nA
  - Typical partial-power-down I_{OFF} 0.2uA
- 3.6V tolerant input to support down translation
- Maximum t_{pd} of 9.5ns at 3.3V
- Drop-in compatible with AUP family and V_{CC} extended from 0.8V to 0.63V

2 Applications

- PC and notebooks
- Data center
- Building automation
- Mobile phones
- Wearables
- Wired networking

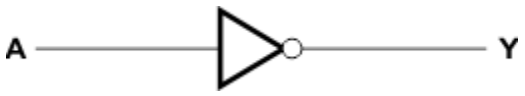
3 Description

The SN74UVP1G04 device is a low-power single inverter that performs the Boolean function Y = $\overline{A}$.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
SN74UVP1G04	DBV (SOT-23, 5)	2.90mm × 1.60mm
	DCK (SC-70, 5)	2.00mm × 1.25mm
	DRY (USON, 6)	1.45mm × 1.00mm
	DSF (X2SON, 6)	1.00mm x 1.00mm
	DPW (X2SON, 5)	0.80mm × 0.80mm

(1) For more information, see Section 11.
(2) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

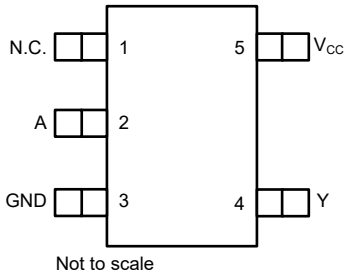


Figure 4-1. DBV or DCK Package, 5-Pin SOT-23 or SC-70 (Top View)

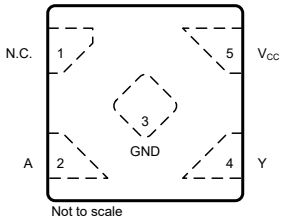


Figure 4-2. DPW Package, 5-Pin X2SON (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DPW, DBV, DCK		
N.C.	1	—	Not internally connected
A	2	I	Input A
GND	3	G	Ground pin
Y	4	O	Output Y (push pull)
VCC	5	P	Power pin

(1) I = Input, O = Output, G = Ground, P = Power

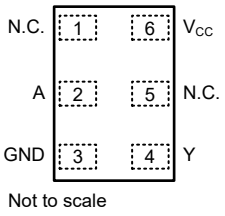


Figure 4-3. DRY or DSF Package, 5-Pin USON or X2SON (Top View)

Table 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DSF, DRY		
N.C.	1, 5	—	Not internally connected
A	2	I	Input A
GND	3	G	Ground pin
Y	4	O	Output Y (push pull)
VCC	6	P	Power pin

(1) I = Input, O = Output, G = Ground, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6	V
V_I	Input voltage range(2)		-0.5	6	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		0.63	3.6	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 0.63V to 0.77V	0.65 x Vcc		V
		V_{CC} = 0.72V to 0.88V	0.65 x Vcc		
		V_{CC} = 0.9V to 1.1V	0.65 x Vcc		
		V_{CC} = 1.08V to 1.32V	0.65 x Vcc		
		V_{CC} = 1.35V to 1.65V	0.65 x Vcc		
		V_{CC} = 1.62V to 1.98V	0.65 x Vcc		
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3.0V to 3.6V	2		

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5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{IL}	Low-Level input voltage	V_{CC} = 0.63V to 0.77V		0.35 x Vcc	V
		V_{CC} = 0.72V to 0.88V		0.35 x Vcc	
		V_{CC} = 0.9V to 1.1V		0.35 x Vcc	
		V_{CC} = 1.08V to 1.32V		0.35 x Vcc	
		V_{CC} = 1.35V to 1.65V		0.35 x Vcc	
		V_{CC} = 1.62V to 1.98V		0.35 x Vcc	
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3.0V to 3.6V		0.8	
I_{OH}	High-level output current	V_{CC} = 0.63V		-0.2	mA
		V_{CC} = 0.72V		-0.5	
		V_{CC} = 0.9V		-0.7	
		V_{CC} = 1.08V		-1.1	
		V_{CC} = 1.35V		-1.7	
		V_{CC} = 1.62V		-1.9	
		V_{CC} = 2.3V		-3.1	
		V_{CC} = 3.0V		-4	
I_{OL}	Low-level output current	V_{CC} = 0.63V		0.2	mA
		V_{CC} = 0.72V		0.5	
		V_{CC} = 0.9V		0.7	
		V_{CC} = 1.08V		1.1	
		V_{CC} = 1.35V		1.7	
		V_{CC} = 1.62V		1.9	
		V_{CC} = 2.3V		3.1	
		V_{CC} = 3.0V		4	
Δt/Δv	Input transition rise or fall rate	V_{cc} = 0.65V to 3.6V		200	ns/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23, 5)	5	298.6	240.2	134.6	114.5	133.9	n/a	°C/W
DCK (SC-70, 5)	5	314.4	128.7	100.6	7.1	99.8	n/a	°C/W
DRY (USON, 6)	6	554.9	385.4	388.2	159.0	384.1	n/a	°C/W
DSF (X2SON, 6)	6	407.1	232.0	306.9	40.3	306.0	n/a	°C/W
DPW (X2SON, 5)	5	291.8	224.2	245.8	31.4	245.6	195.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH}= –20µA	0.63V to 3.6V	V_{CC} – 0.1			V
	I_{OH}= –0.7mA	1.0V	0.65			
	I_{OH}= –1.1mA	1.2V	0.97			
	I_{OH}= –1.7mA	1.5V	1.24			
	I_{OH}= –1.9mA	1.65V	1.4			
	I_{OH}= –3.1mA	2.3V	1.99			
	I_{OH}= –3.5mA	2.7V	2.35			
	I_{OH}= –4mA	3V	2.67			
V_{OL}	I_{OL}= 20µA	0.63V to 3.6V			0.15	V
	I_{OL}= 0.7mA	1.0V			0.35	
	I_{OL}= 1.1mA	1.2V			0.25	
	I_{OL}= 1.7mA	1.5V			0.23	
	I_{OL}= 1.9mA	1.65V			0.23	
	I_{OL}= 3.1mA	2.3V			0.26	
	I_{OL}= 3.5mA	2.7V			0.27	
	I_{OL}= 4mA	3V			0.29	
I_I	V_I = V_{CC} or GND	V_{CC} = 0V to 3.6V		±0.003	±0.5	µA
I_{OFF}	V_I or V_O = V_{CC}	V_{CC} = 0V		±0.2	±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 0.63V to 3.6V		0.01	1.4	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	3.3V			60	uA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs sweeping from GND to V_{CC}	3.3V			1800	µA
C_I	V_I = V_{CC} or GND	3.3V		4.4		pF
C_O	V_O = V_{CC} or GND	3.3V		2.6		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CONDITION	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	C_L = 5pF	0.7V ± 0.07V			132	ns
				0.8V ± 0.08V			83	ns
			C_L = 10pF	1.0V ± 0.1V			29	ns
				1.2V ± 0.12V			11	ns
			C_L = 15pF	1.5V ± 0.15V			7	ns
				1.8V ± 0.18V			5	ns
			C_L = 30pF	2.5V ± 0.2V			6	ns
				3.3V ± 0.3V			5	ns

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over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

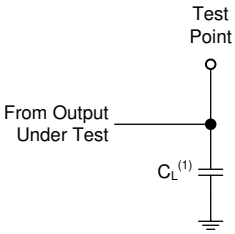
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CONDITION	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}			f = 10MHz	0.7V		5		pF
				0.8V		6		pF
				1.0V		6		pF
				1.2V		5		pF
				1.5V		5		pF
				1.8V		5		pF
				2.5V		5		pF
				3.3V		4		pF

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6 Parameter Measurement Information

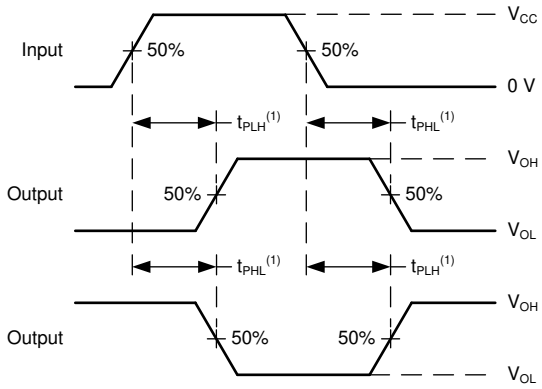
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 3ns.

The outputs are measured individually with one input transition per measurement.



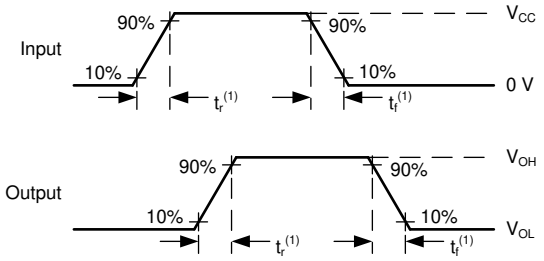
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as the transition time.

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

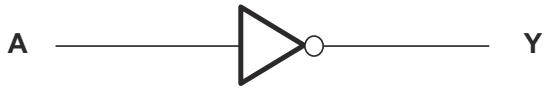
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7 Detailed Description

7.1 Overview

The SN74UVP1G04 device contains inverter gate and performs the Boolean function Y = $\overline{A}$. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.4 Device Functional Modes

The Function Table lists the functional modes for SN74UVP1G04.

Table 7-1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UVP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family provides very low static and dynamic power consumption across the entire V_{CC} range, resulting in an increased battery life. This product also maintains excellent signal integrity. The device has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

8.2 Typical Application

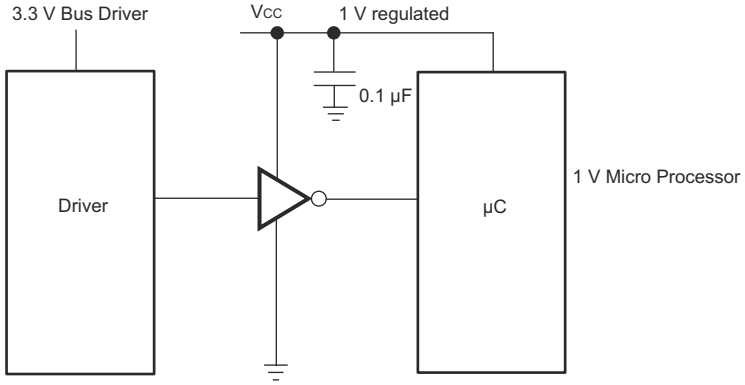


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention. Bus contention can drive currents that exceed maximum limits.

8.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specs. See (Δt/ΔV) in *Section 5.3*
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Section 5.3*
   - Inputs are overvoltage tolerant allowing them to go as high as 3.6V at any valid V_{CC}
2. Recommend output conditions
   - Load currents must not exceed 20mA on the output and 50mA total for the part
   - Do not pull outputs above V_{CC}

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each V_{CC} terminal has a good bypass capacitor to prevent power disturbance. For the SN74UVP1G04, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

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8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

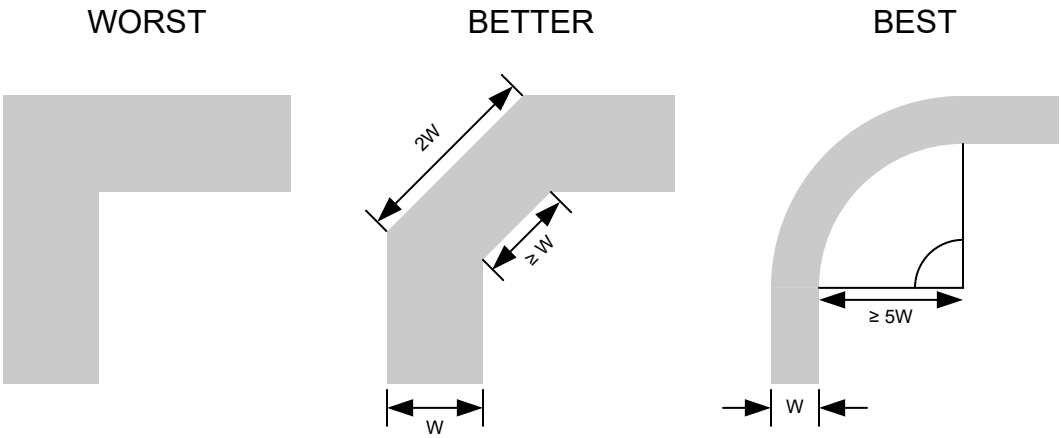


Figure 8-2. Example Trace Corners for Improved Signal Integrity

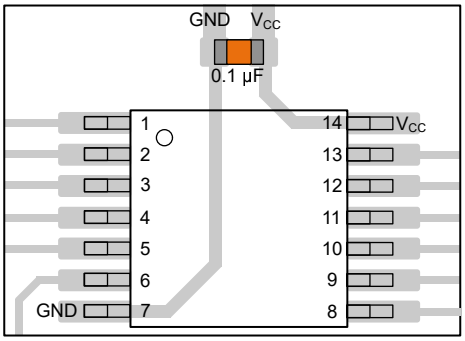


Figure 8-3. Example Bypass Capacitor Placement for TSSOP and Similar Packages

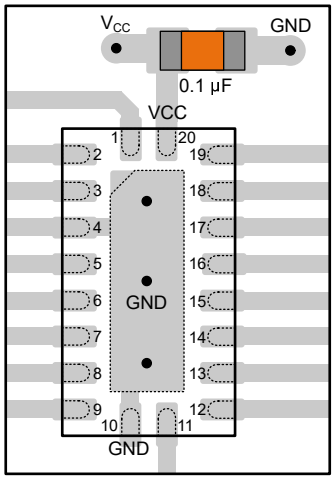


Figure 8-4. Example Bypass Capacitor Placement for WQFN and Similar Packages

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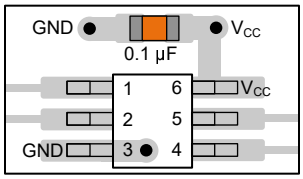


Figure 8-5. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

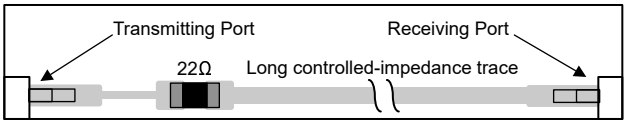


Figure 8-6. Example Damping Resistor Placement for Improved Signal Integrity

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application brief
- Texas Instruments, *Logic in Live-Insertion Applications With a Focus on GTLP* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Texas Instruments General Quality Guidelines*
- Texas Instruments, *Thermal Characteristics of SLL Packages and Devices* application note
- Texas Instruments, *Understanding Schmitt Triggers* application brief

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2026) to Revision A (October 2026)	Page
• Changed the document status from *Advance Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN74UVP1G04DBVR	Active	Preproduction	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-	
PSN74UVP1G04DCKR	Active	Preproduction	SC70 (DCK) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-	
PSN74UVP1G04DPWR	Active	Preproduction	X2SON (DPW) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-	
PSN74UVP1G04DRYR	Active	Preproduction	SON (DRY) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-	
PSN74UVP1G04DSFR	Active	Preproduction	SON (DSF) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74UVP1G04 :

- Automotive : SN74UVP1G04-Q1

NOTE: Qualified Version Definitions:

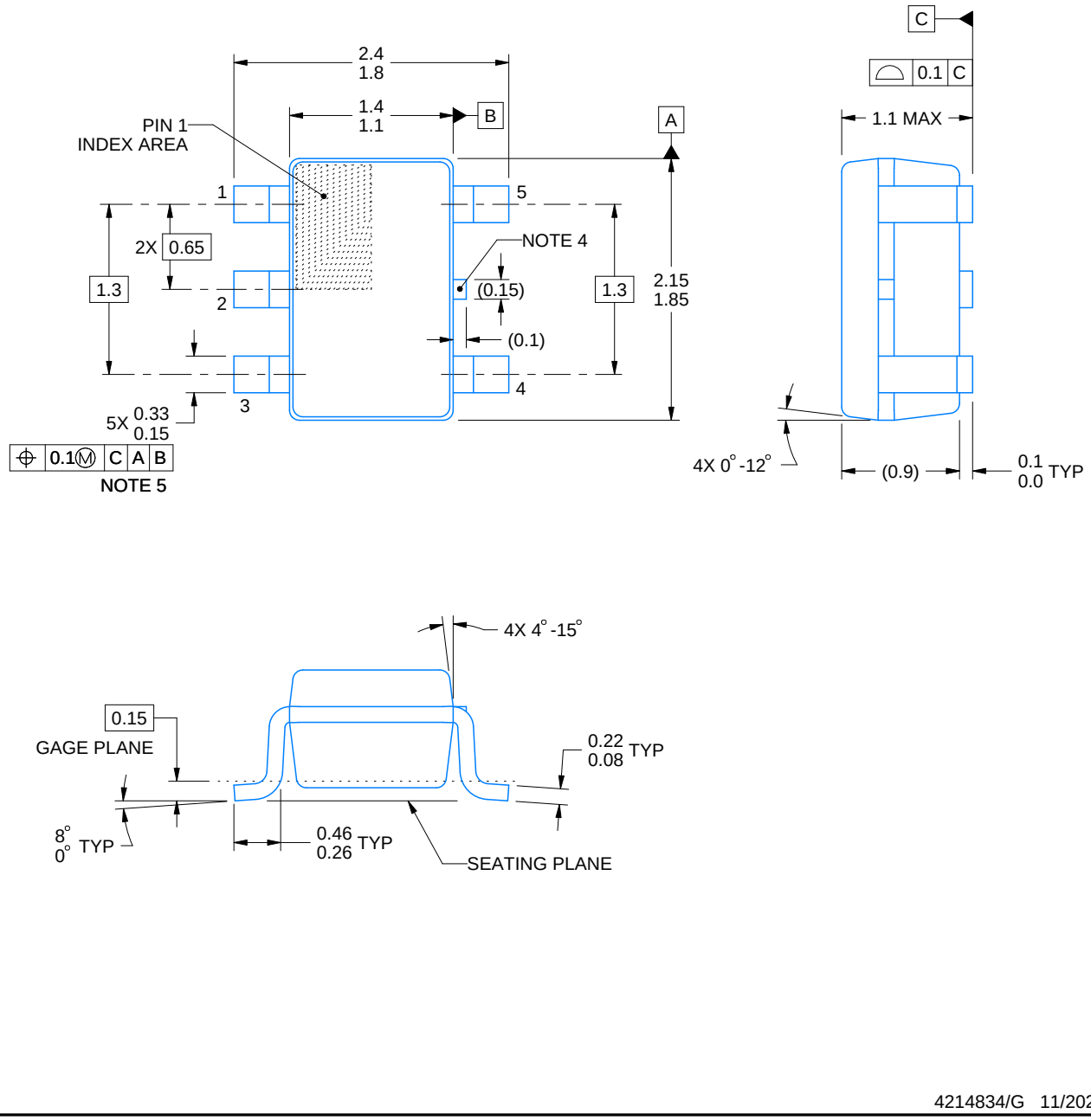
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

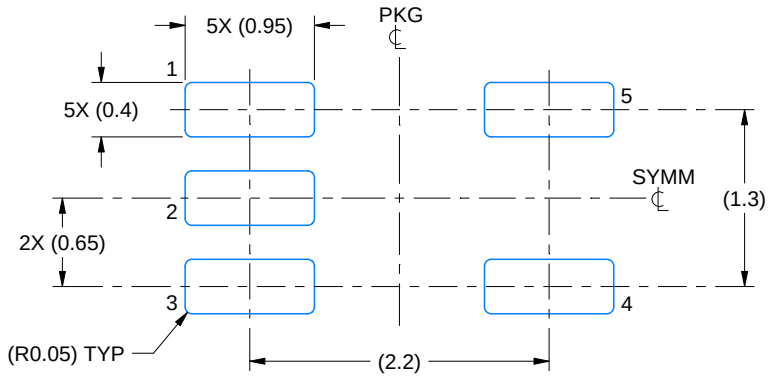
SMALL OUTLINE TRANSISTOR



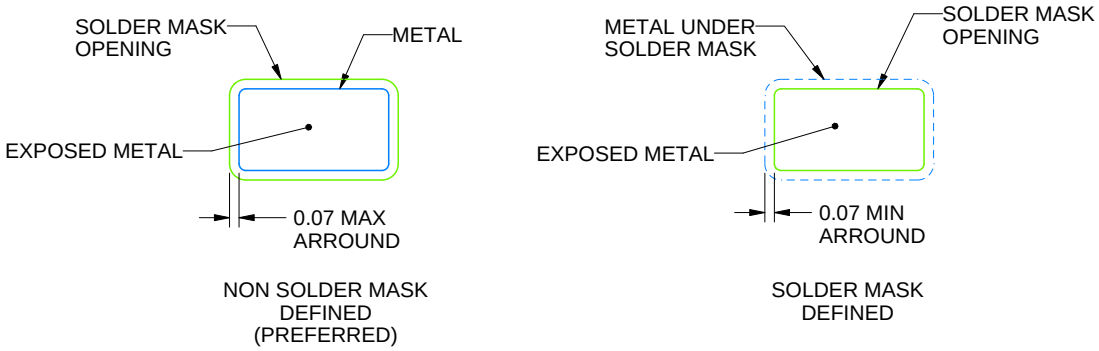
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

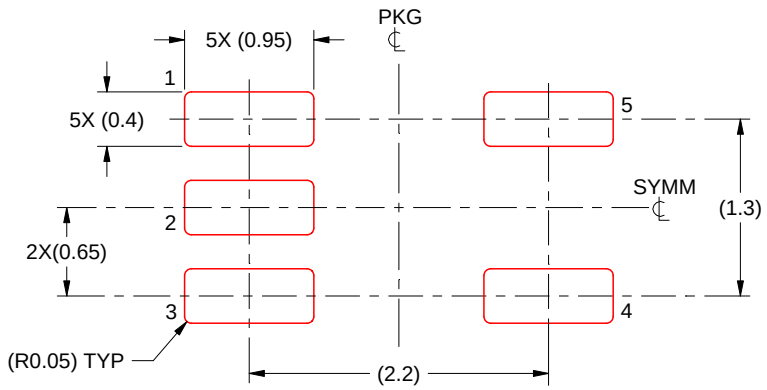


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

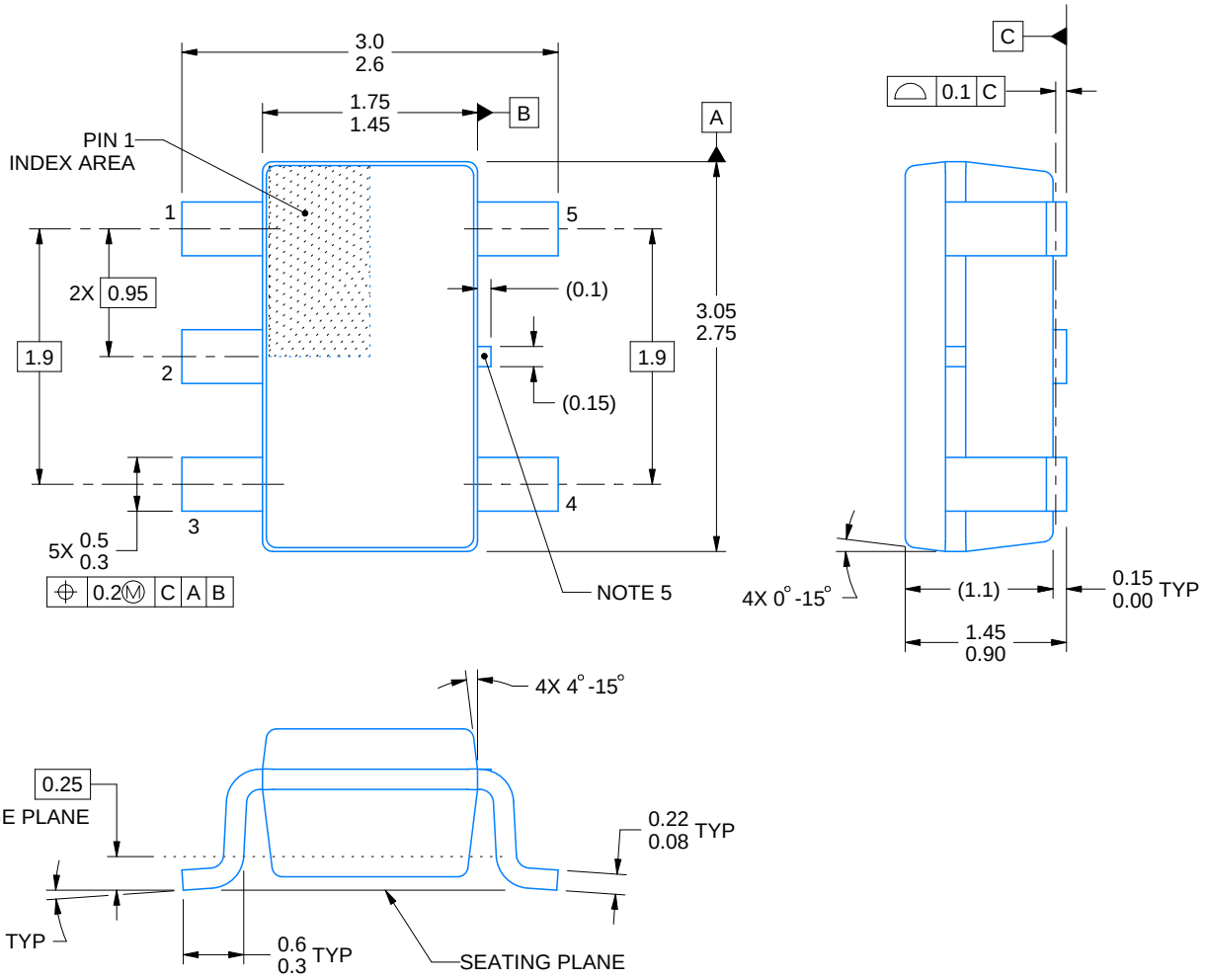
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

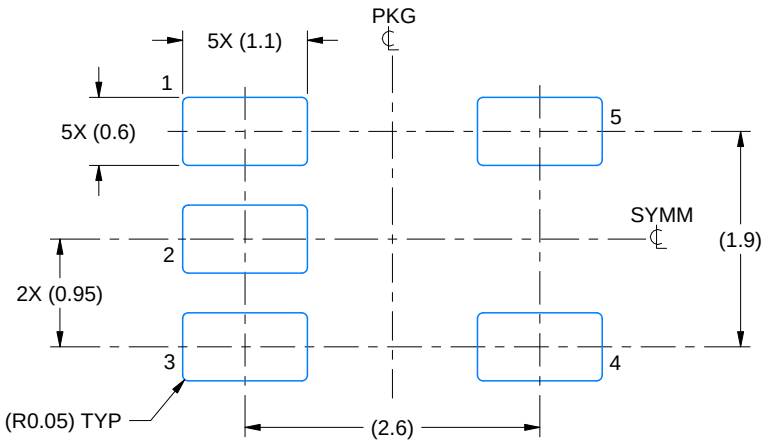
SMALL OUTLINE TRANSISTOR



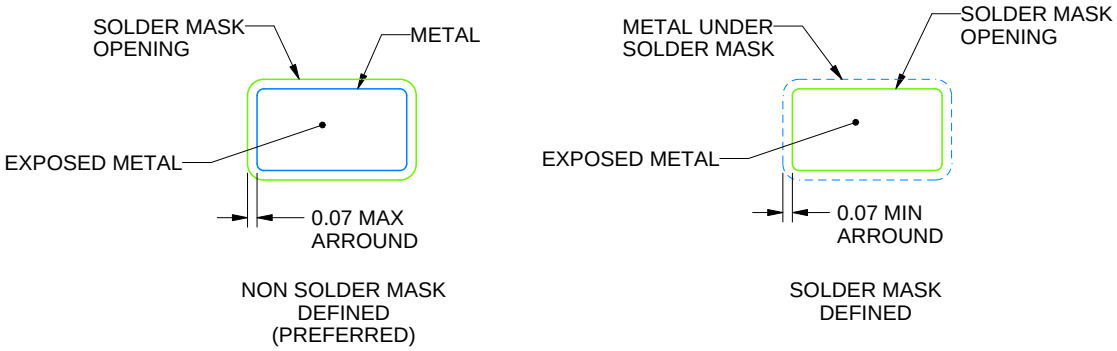
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

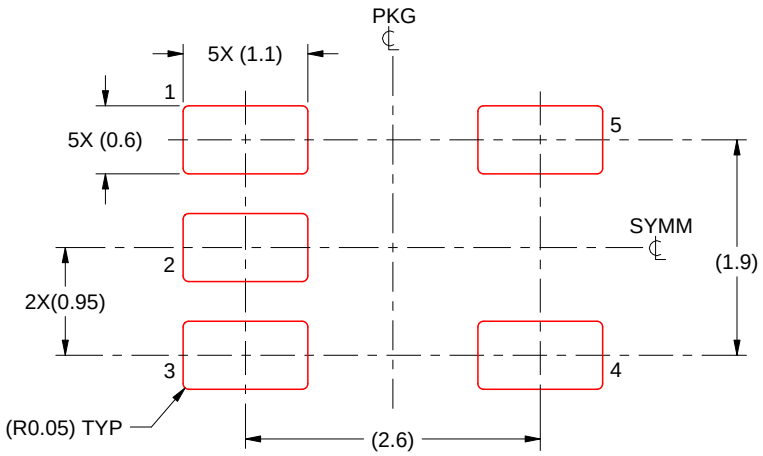


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



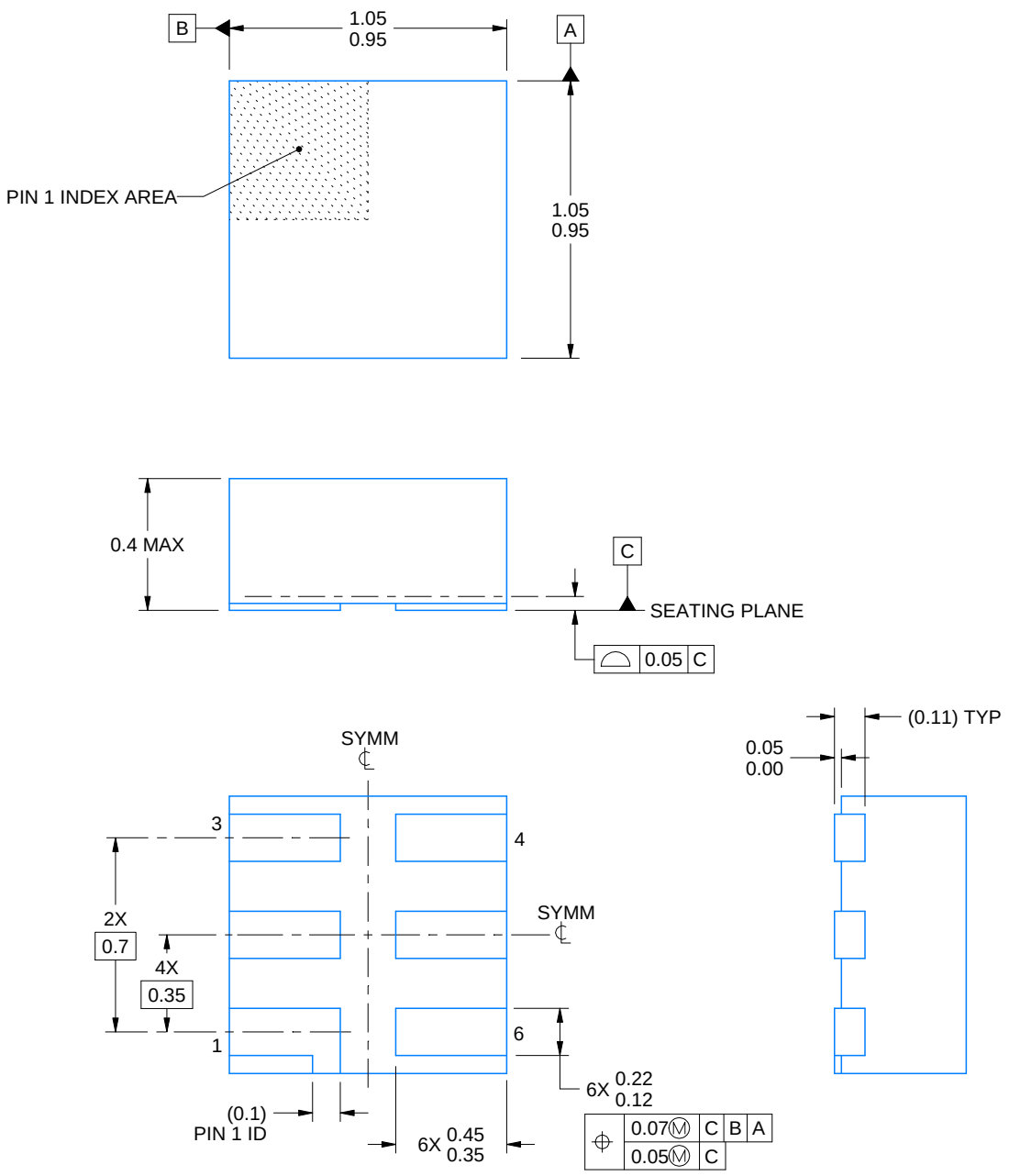
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

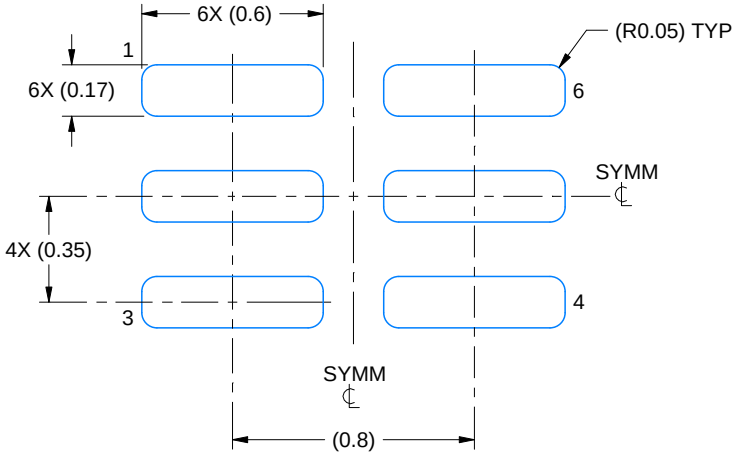
PLASTIC SMALL OUTLINE - NO LEAD



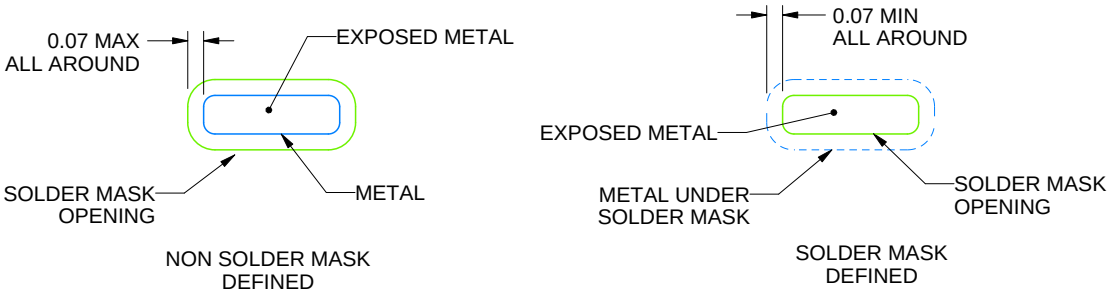
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

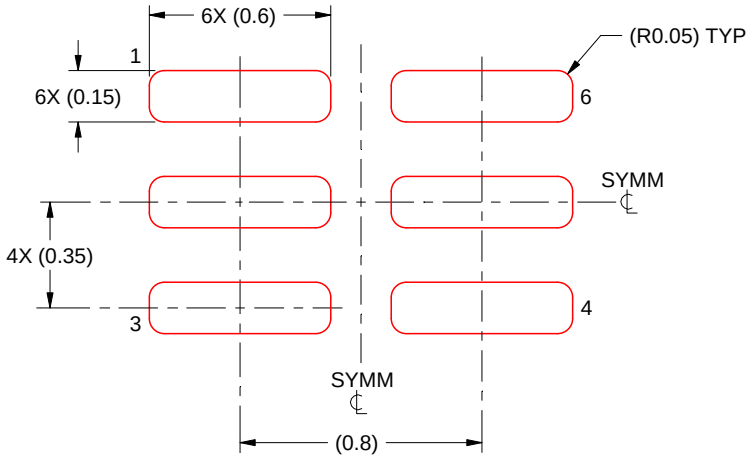
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D

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