SN74UVP1G06-Q1 Low-Power Single Inverter With Open-Drain Outputs

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Extended low-voltage operation with 0.63V to 3.6V supply range
- Extended operating temperature range: –40°C to 125°C
- Low power consumption
  - Typical I_{CC} = 10nA
  - Typical input leakage I_I = 3nA
  - Typical output off-state leakage current I_{OZ} = 100nA
  - Typical partial-power-down I_{OFF} 0.2uA
- 3.6V tolerant input to support down translation
- Maximum t_{pd} of 9.5ns at 3.3V
- Drop-in compatible with AUP1G family and V_{CC} extended from 0.8V to 0.63V

2 Applications

- Advanced driver assistance systems (ADAS)
- Body electronics and lighting
- Infotainment and cluster

3 Description

The SN74UVP1G06-Q1 device is a low-power single inverter with open drain output, and performs the Boolean function $Y = \overline{A}$.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
SN74UVP1G06-Q1	DBV (SOT-23, 5)	2.90mm × 1.60mm
SN74UVP1G06-Q1	DCK (SC-70, 5)	2.00mm × 1.25mm
	DTX (X2SON, 5)	1.10mm × 0.85mm
	DRY (USON, 6)	1.45mm × 1.00mm

(1) For more information, see Section 11.
(2) The body size (length × width) is a nominal value and does not include pins



Logic Diagram

ADVANCE INFORMATION

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

ADVANCE INFORMATION

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....5
5.5 Electrical Characteristics....5
5.6 Switching Characteristics....6
6 Parameter Measurement Information....7
7 Detailed Description....8
7.1 Overview....8
7.2 Functional Block Diagram....8
7.3 Feature Description....8
7.4 Device Functional Modes....8
8 Application and Implementation....10
8.1 Application Information....10
8.2 Typical Application....10
8.3 Design Requirements....10
8.4 Application Curves....12
8.5 Power Supply Recommendations....12
8.6 Layout....12
9 Device and Documentation Support....14
9.1 Documentation Support....14
9.2 Receiving Notification of Documentation Updates....14
9.3 Support Resources....14
9.4 Trademarks....14
9.5 Electrostatic Discharge Caution....14
9.6 Glossary....14
10 Revision History....14
11 Mechanical, Packaging, and Orderable Information....15
11.1 Tape and Reel Information....15
11.2 Mechanical Data....17

Copyright © 2026 Texas Instruments Incorporated

4 Pin Configuration and Functions

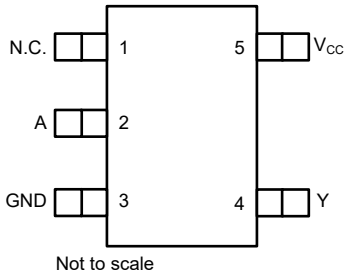


Figure 4-1. DBV or DCK Package, 5-Pin SOT-23 or SC-70 (Top View)

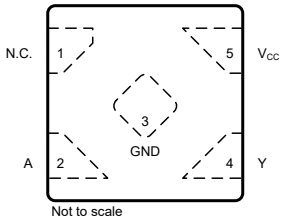


Figure 4-2. or DTX Package, 5-Pin X2SON (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DBV, DCK, DTX		
N.C.	1	—	Not internally connected
A	2	I	Input A
GND	3	G	Ground pin
Y	4	O	Output Y (push pull)
VCC	5	P	Power pin

(1) I = Input, O = Output, G = Ground, P = Power

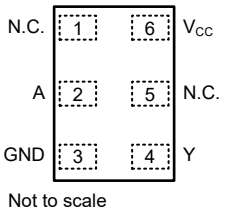


Figure 4-3. DRY Package, 5-Pin USON or X2SON (Top View)

Table 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DRY		
N.C.	1, 5	—	Not internally connected
A	2	I	Input A
GND	3	G	Ground pin
Y	4	O	Output Y (push pull)
VCC	6	P	Power pin

(1) I = Input, O = Output, G = Ground, P = Power

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6	V
V_I	Input voltage range(2)		-0.5	6	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range (2)		-0.5	6	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		0.63	3.6	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 0.63V to 0.77V	0.65 × Vcc		V
		V_{CC} = 0.72V to 0.88V	0.65 × Vcc		
		V_{CC} = 0.9V to 1.1V	0.65 × Vcc		
		V_{CC} = 1.08V to 1.32V	0.65 × Vcc		
		V_{CC} = 1.35V to 1.65V	0.65 × Vcc		
		V_{CC} = 1.62V to 1.98V	0.65 × Vcc		
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3.0V to 3.6V	2		

Copyright © 2026 Texas Instruments Incorporated

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{IL}	Low-Level input voltage	V_{CC} = 0.63V to 0.77V		0.35 × Vcc	V
		V_{CC} = 0.72V to 0.88V		0.35 × Vcc	
		V_{CC} = 0.9V to 1.1V		0.35 × Vcc	
		V_{CC} = 1.08V to 1.32V		0.35 × Vcc	
		V_{CC} = 1.35V to 1.65V		0.35 × Vcc	
		V_{CC} = 1.62V to 1.98V		0.35 × Vcc	
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3.0V to 3.6V		0.8	
I_{OL}	Low-level output current	V_{CC} = 0.63V		0.2	mA
		V_{CC} = 0.72V		0.5	
		V_{CC} = 0.9V		0.7	
		V_{CC} = 1.08V		1.1	
		V_{CC} = 1.35V		1.7	
		V_{CC} = 1.62V		1.9	
		V_{CC} = 2.3V		3.1	
		V_{CC} = 3.0V		4	
Δt/Δv	Input transition rise or fall rate	V_{cc} = 0.65V to 3.6V		200	ns/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23, 5)	5	298.6	240.2	134.6	114.5	133.9	n/a	°C/W
DCK (SC-70, 5)	5	314.4	128.7	100.6	7.1	99.8	n/a	°C/W
DTX (X2SON, 5)	5							°C/W
DRY (USON, 6)	6	554.9	385.4	388.2	159.0	384.1	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	I_{OL}= 20μA	0.63V to 3.6V			0.15	V
	I_{OL}= 0.7mA	1.0V			0.35	
	I_{OL}= 1.1mA	1.2V			0.25	
	I_{OL}= 1.7mA	1.5V			0.23	
	I_{OL}= 1.9mA	1.65V			0.23	
	I_{OL}= 3.1mA	2.3V			0.26	
	I_{OL}= 3.5mA	2.7V			0.27	
	I_{OL}= 4mA	3V			0.29	
I_I	V_I = V_{CC} or GND	V_{CC} = 0V to 3.6V		±0.003	±0.5	μA
I_{OFF}	V_I or V_O = V_{CC}	V_{CC} = 0V		±0.2	±1	μA
I_{OZ}	V_O = V_{CC} or GND	3.6V		±0.1	±1.5	μA

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{CC}	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 0.63V to 3.6V		0.01	1.4	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	3.3V			60	µA
C_I	V_I = V_{CC} or GND	3.3V		4.4		pF
C_O	V_O = V_{CC} or GND	3.3V		2.59		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CONDITION	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	C_L = 5pF	0.7V ± 0.07V			302	ns
				0.8V ± 0.08V			105.5	ns
			C_L = 10pF	1.0V ± 0.1V			25.1	ns
				1.2V ± 0.12V			16.4	ns
			C_L = 15pF	1.5V ± 0.15V			5.7	ns
				1.8V ± 0.18V			6.1	ns
			C_L = 30pF	2.5V ± 0.2V			7	ns
				3.3V ± 0.3V			10.1	ns
C_{pd}			f = 10MHz	0.7V		0.46		pF
				0.8V		0.47		pF
				1.0V		0.47		pF
				1.2V		0.47		pF
				1.5V		0.49		pF
				1.8V		0.53		pF
				2.5V		0.72		pF
				3.3V		1		pF

ADVANCE INFORMATION

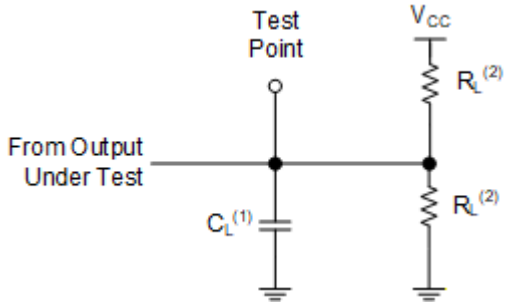
Copyright © 2026 Texas Instruments Incorporated

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 3 ns.

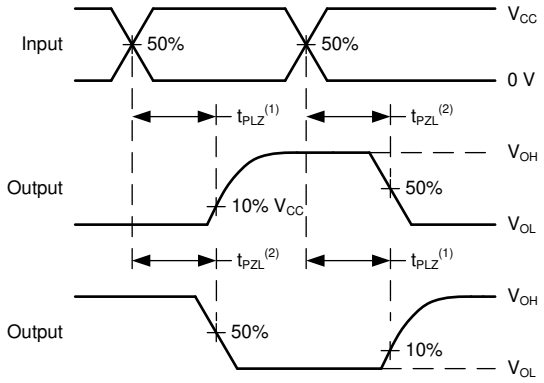
The outputs are measured individually with one input transition per measurement.

TEST	R_L	C_L	ΔV	V_{CC}
t_{pd}	20KΩ	5pF	0.07V	0.7V
			0.08V	0.8V
		10pF	0.1V	1.0V
	5KΩ	10pF	0.12V	1.2V
		15pF	0.15V	1.5V
			0.18V	1.8V
		30pF	0.2V	2.5V
			0.3V	3.3V



(1) C_L includes probe and test-fixture capacitance.
(2) R_L = 5kΩ or 20kΩ for enable and disable time measurement. R_L = 1MΩ for measuring propagation delays, setup and hold times, and pulse width.

Figure 6-1. Load Circuit for Open-Drain Outputs



(1) If R_L = 5kΩ, the time between t_{PLZ} and t_{PZL} is the same as disable and enable time.
(2) If R_L = 1MΩ, t_{PLZ} and t_{PZL} are the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The SN74UVP1G06-Q1 device contains one open-drain inverter with a maximum sink current of 32mA. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

7.2 Functional Block Diagram

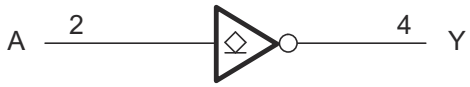


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Open-Drain CMOS Outputs

Open-drain outputs are included in SN74UVP1G06-Q1. Open-drain outputs can only drive the output low. When in the high logical state, outputs are in a high-impedance state, meaning outputs neither source nor sink current (with the exception of minor leakage current as defined in the *Electrical Characteristics* table). In the high-impedance state, the output voltage is not controlled by SN74UVP1G06-Q1 and is dependent on external factors.

Because of the high-impedance state, an external pull-up resistor is required to define a logic high. Without a pull-up resistor, the output will float and have an undefined logic level. The resistor value depends on factors like parasitic capacitance and power consumption; typically, a 10kΩ resistor is suitable.

The drive capability of SN74UVP1G06-Q1 can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, outputs can drive higher currents than SN74UVP1G06-Q1 is designed to handle continuously. Limit the device output power to avoid damage due to overcurrent. Follow the electrical and thermal limits defined in the *Absolute Maximum Ratings* at all times. See the *Recommended Operating Conditions* table for the maximum output voltage that can be externally connected to SN74UVP1G06-Q1.

Leave unused open-drain CMOS outputs disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at V_{CC} or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10kΩ resistor, however, is recommended and typically meets all requirements.

7.4 Device Functional Modes

Function Table lists the functional modes of the SN74UVP1G06-Q1.

Table 7-1. Function Table

INPUT A	OUTPUT Y
L	Hi-Z

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

Table 7-1. Function Table (continued)

INPUT A	OUTPUT Y
H	L

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74UVP1G06-Q1 is a high-drive CMOS device that can be used in an LED application. The device can sink 32mA of current at 4.5V making it appropriate for high-drive applications. The device is good for high-speed applications up to 100MHz. The inputs are 5.5V tolerant allowing it to translate up or down to V_{CC}. Figure 8-1 shows a simple LED driver application for a single channel of the device.

8.2 Typical Application

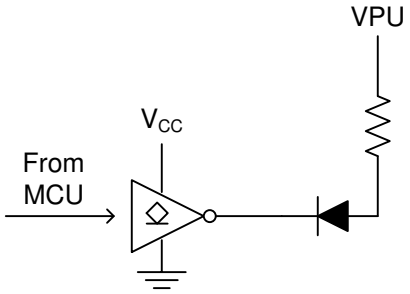


Figure 8-1. Typical Application Diagram

8.3 Design Requirements

8.3.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74UVP1G06-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74UVP1G06-Q1 can drive a load with a total capacitance less than or equal to 30 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74UVP1G06-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.3.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74UVP1G06-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74UVP1G06-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.3.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.3.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74UVP1G06-Q1 to the receiving device.
3. Verify that the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

8.4 Application Curves

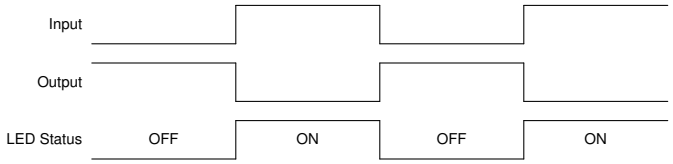


Figure 8-2. Application Curve

8.5 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.6 Layout

8.6.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.6.2 Layout Example

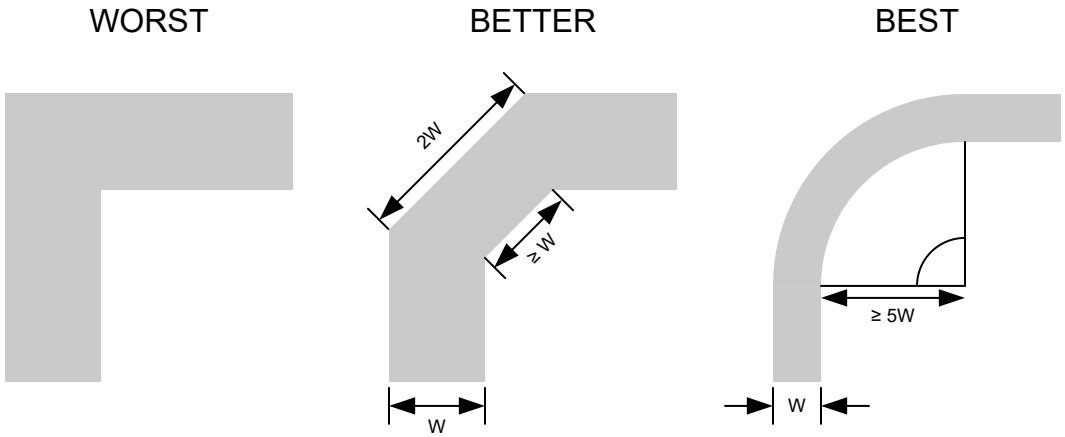


Figure 8-3. Example Trace Corners for Improved Signal Integrity

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

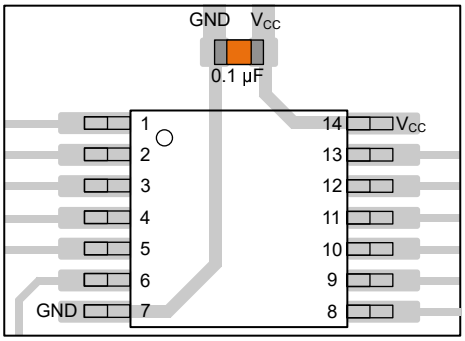


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

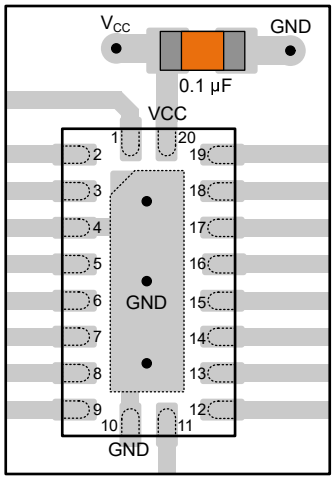


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

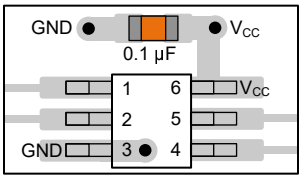


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

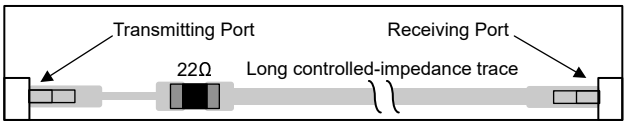


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2026	*	Initial Release

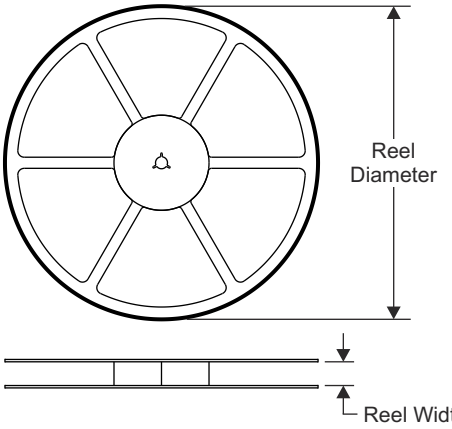
Copyright © 2026 Texas Instruments Incorporated

11 Mechanical, Packaging, and Orderable Information

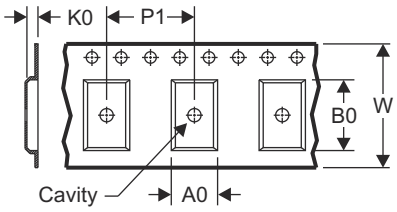
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

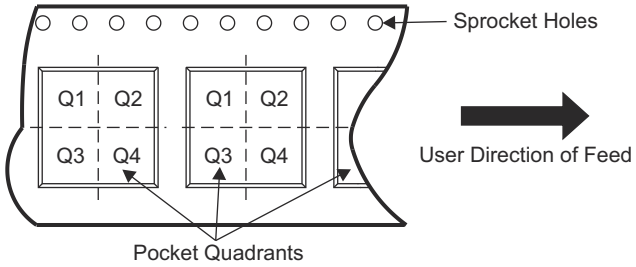


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



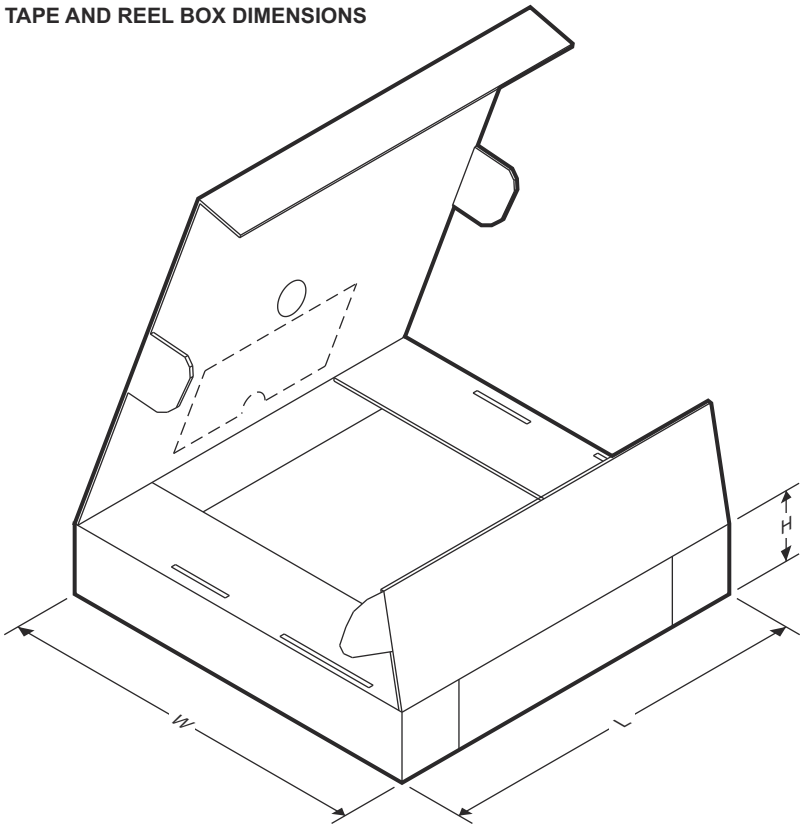
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PSN74UVP1G06DBVRQ1	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PSN74UVP1G06DCKRQ1	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
PSN74UVP1G06DRYRQ1	USON	DRY	5	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
PSN74UVP1G06DTXRQ1	X2SON	DTX	5	3000	180.0	8.4	1.0	1.25	0.48	2.0	8.0	Q1

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PSN74UVP1G06DBVRQ1	SOT-23	DBV	5	3000	208.0	191.0	35.0
PSN74UVP1G06DCKRQ1	SC70	DCK	5	3000	208.0	191.0	35.0
PSN74UVP1G06DRYRQ1	USON	DRY	5	5000	184.0	184.0	19.0
PSN74UVP1G06DTXRQ1	X2SON	DTX	5	3000	210.0	185.0	35.0

Copyright © 2026 Texas Instruments Incorporated

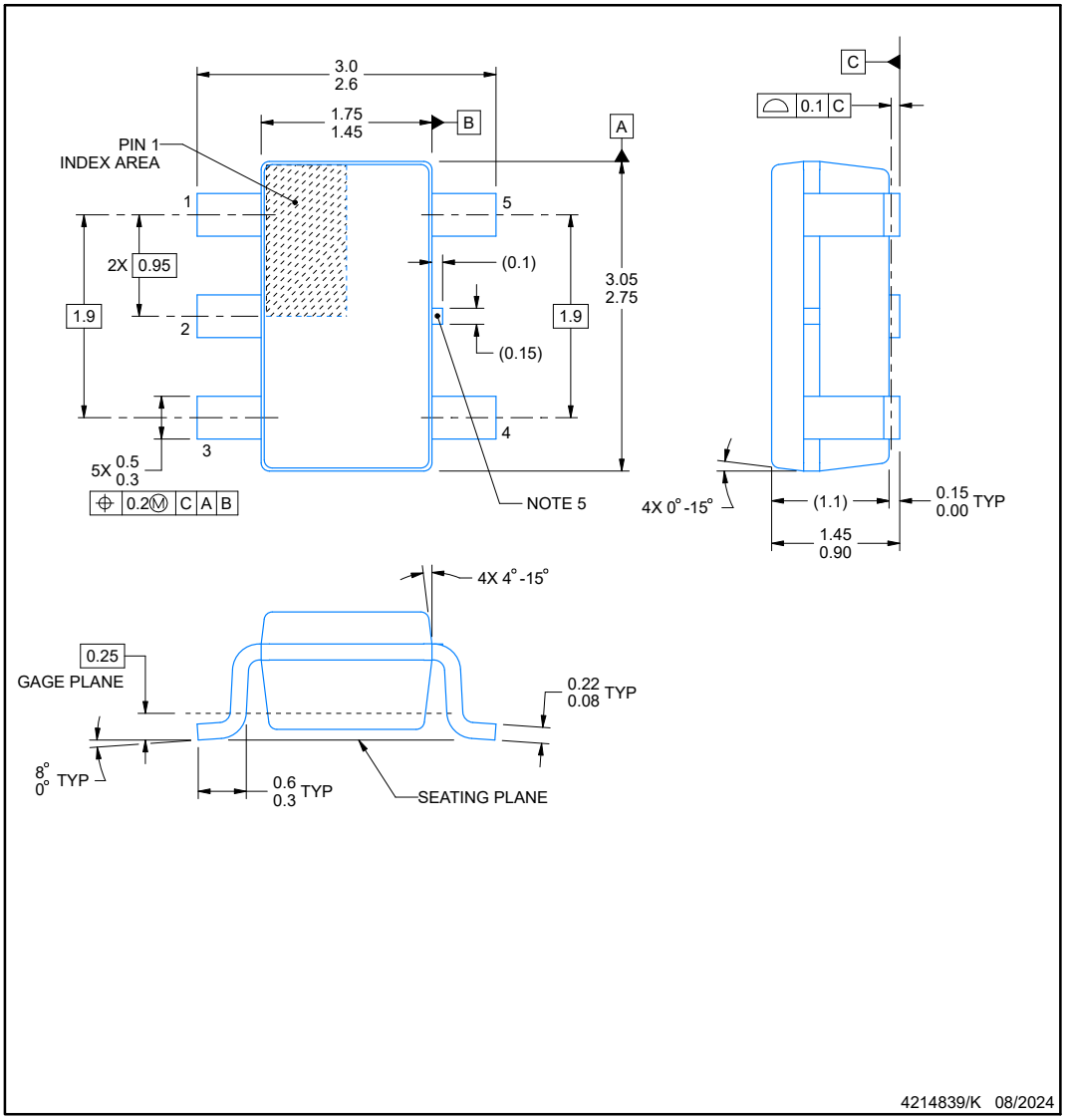
11.2 Mechanical Data



PACKAGE OUTLINE

DBV0005A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

ADVANCE INFORMATION

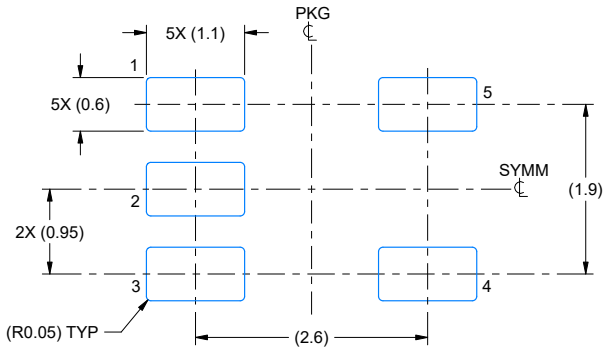
Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

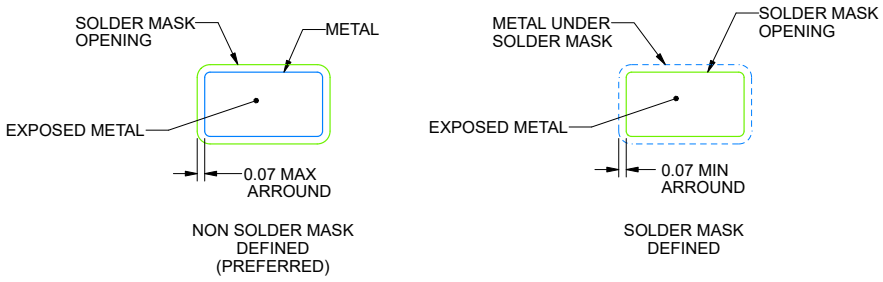
EXAMPLE BOARD LAYOUT

DBV0005A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

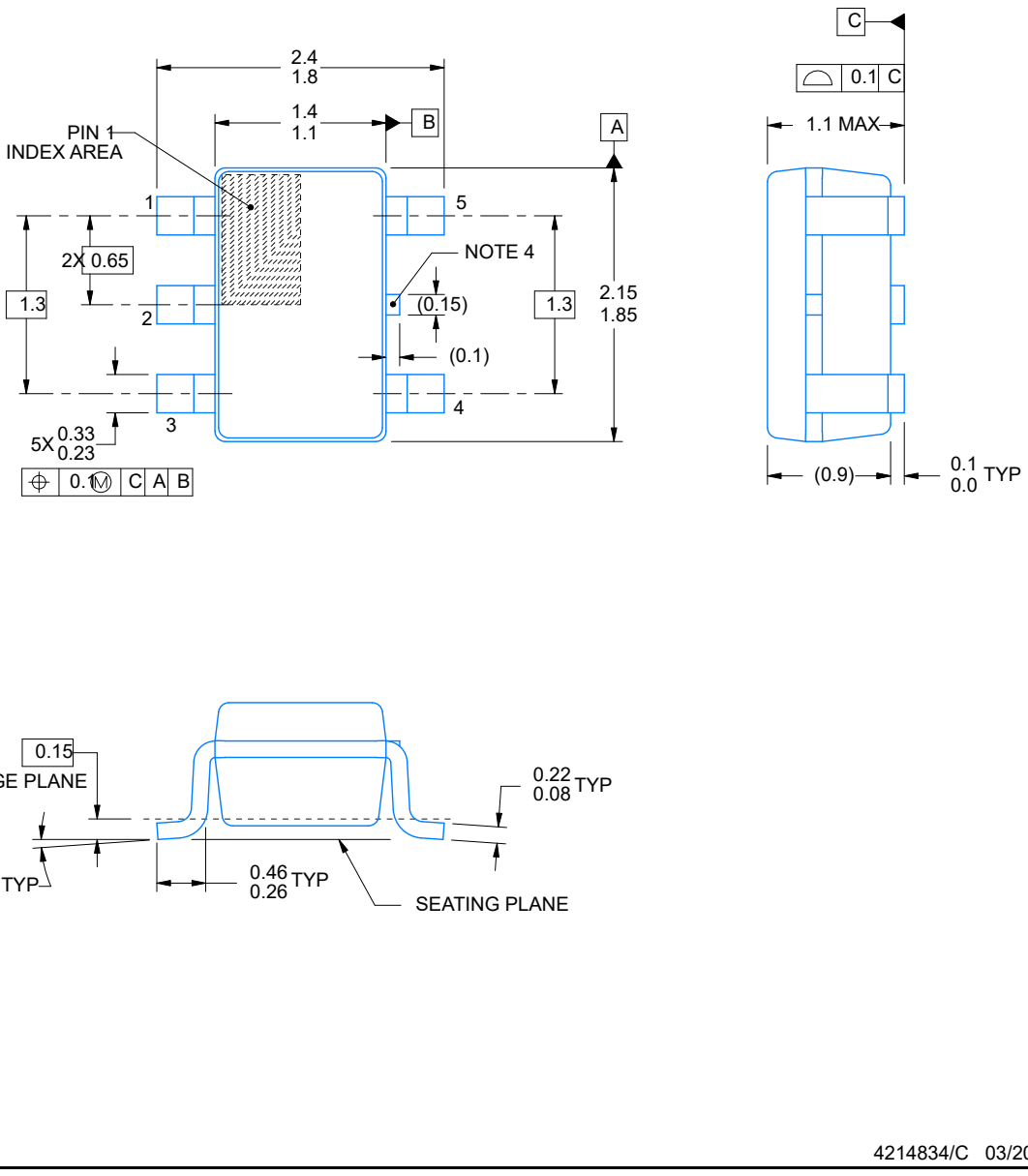
Copyright © 2026 Texas Instruments Incorporated

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dim ensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

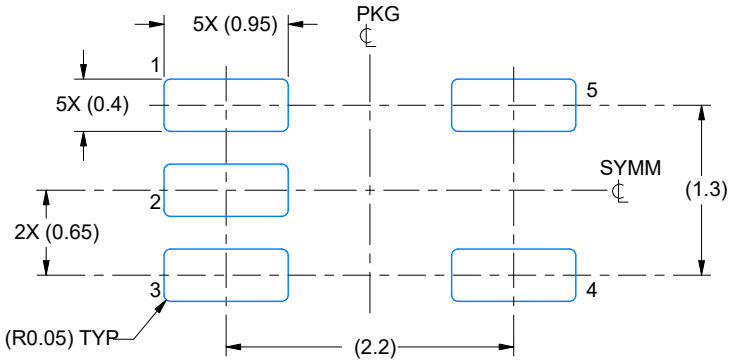
EXAMPLE BOARD LAYOUT

DCK0005A

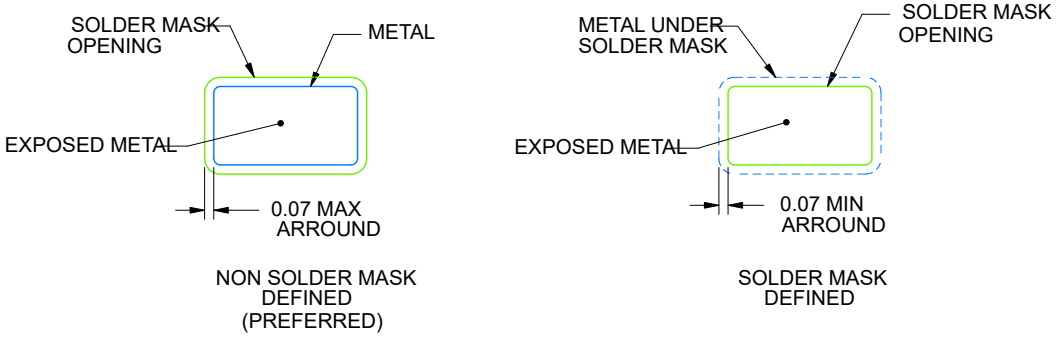
SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR

ADVANCE INFORMATION



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/C 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

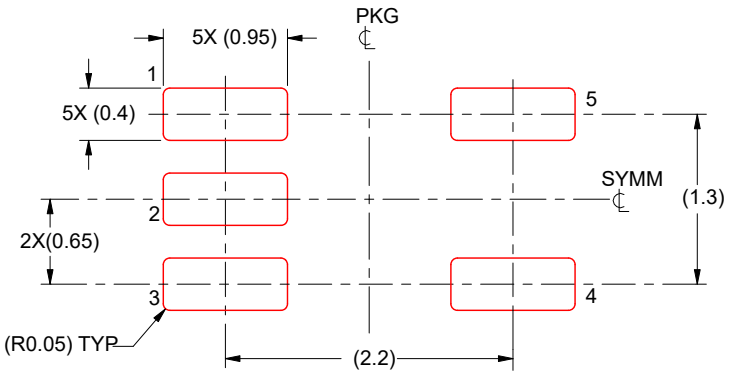
Copyright © 2026 Texas Instruments Incorporated

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

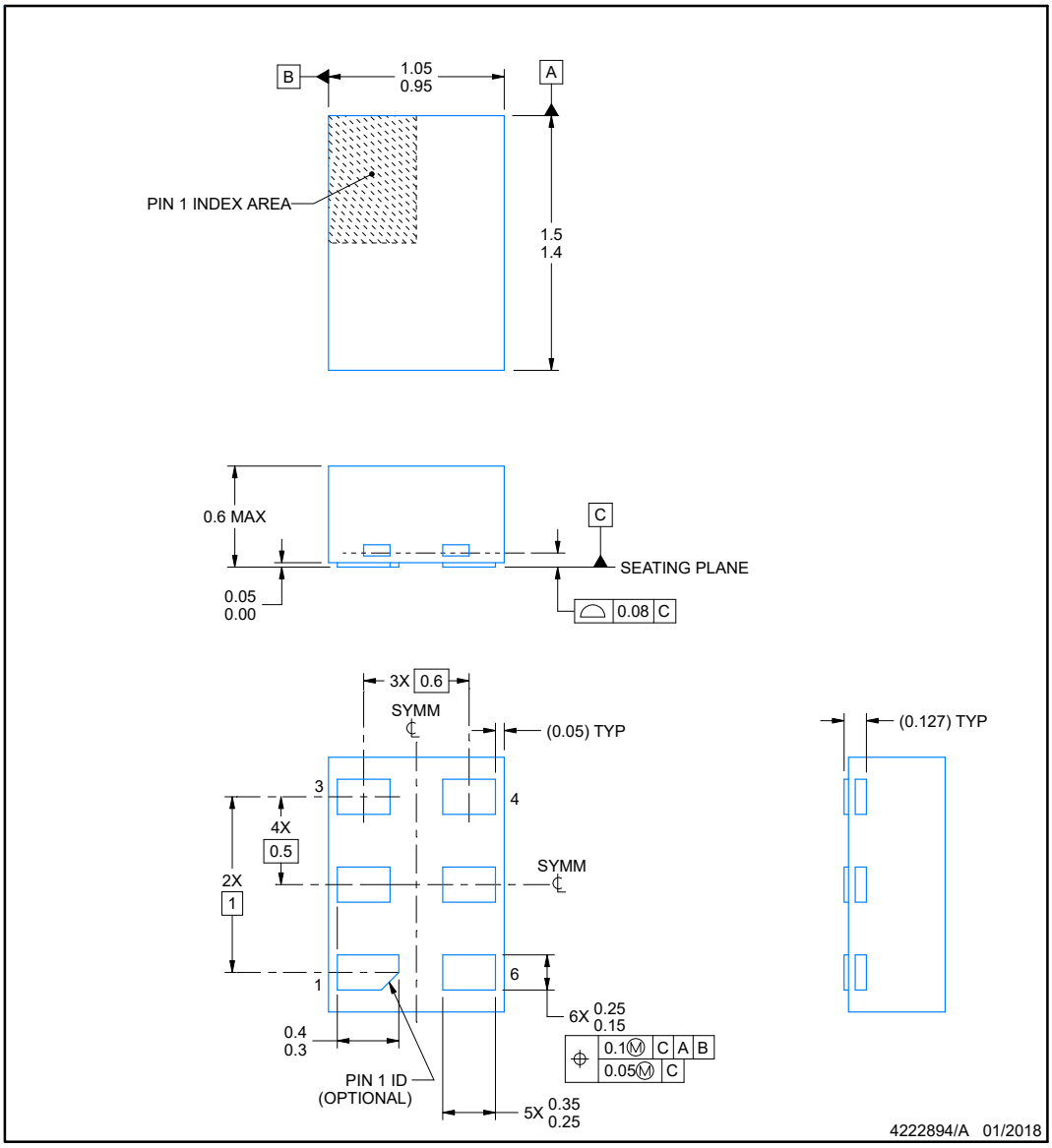
PACKAGE OUTLINE

DRY0006A



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

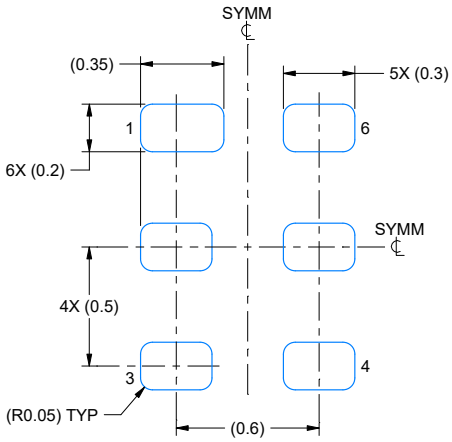
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Copyright © 2026 Texas Instruments Incorporated

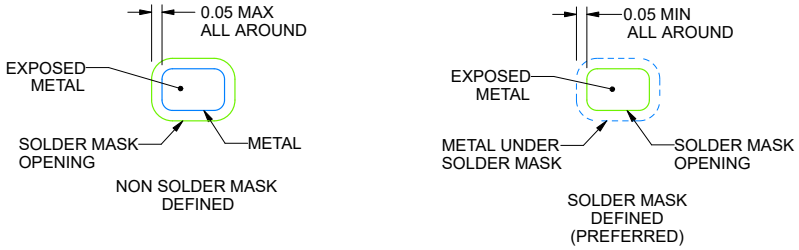
EXAMPLE BOARD LAYOUT

DRY0006A — **USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

ADVANCE INFORMATION

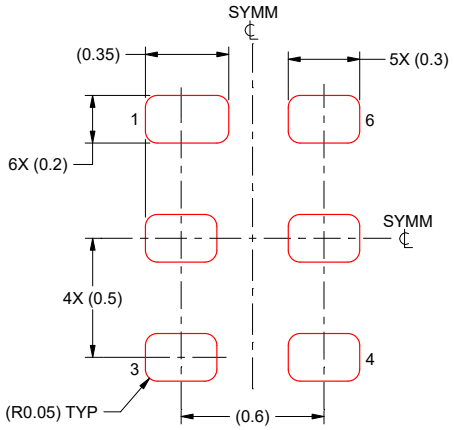
Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DRY0006A — **USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Copyright © 2026 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN74UVP1G06DBVRQ1	Active	Preproduction	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PSN74UVP1G06DCKRQ1	Active	Preproduction	SC70 (DCK) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PSN74UVP1G06DRYRQ1	Active	Preproduction	SON (DRY) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PSN74UVP1G06DTXRQ1	Active	Preproduction	X2SON (DTX) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74UVP1G06-Q1 :

- Catalog : SN74UVP1G06

NOTE: Qualified Version Definitions:

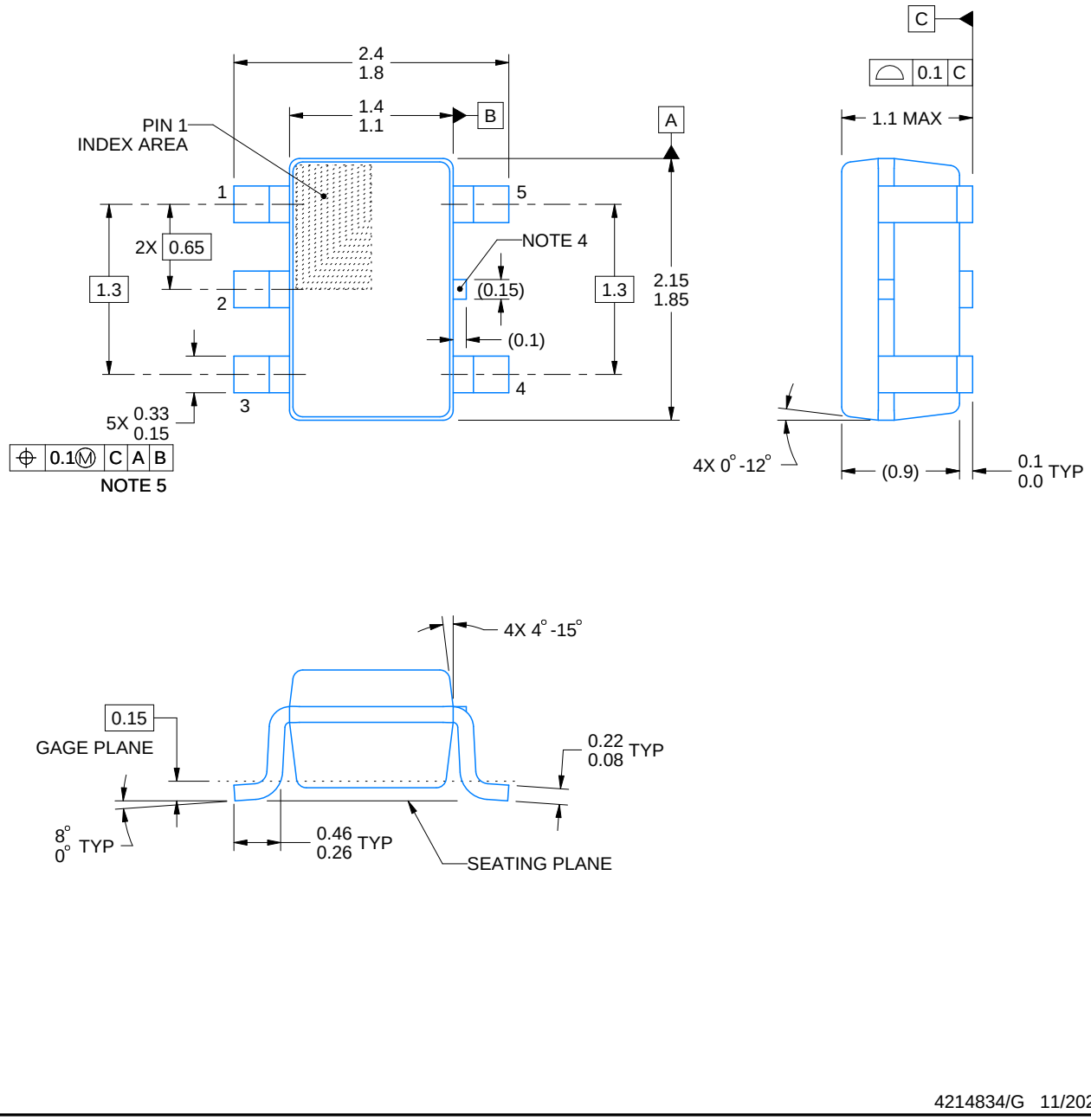
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

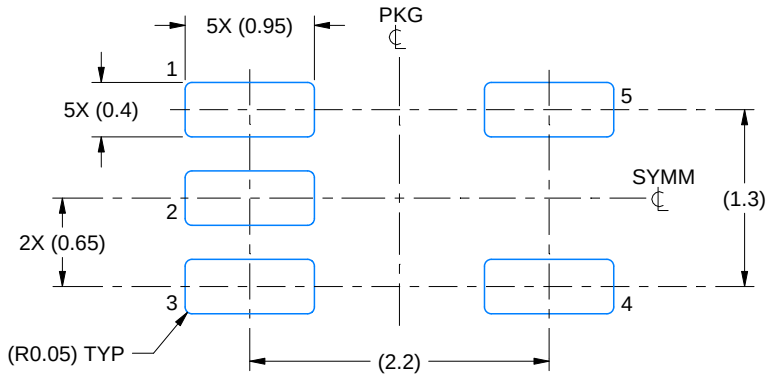
SMALL OUTLINE TRANSISTOR



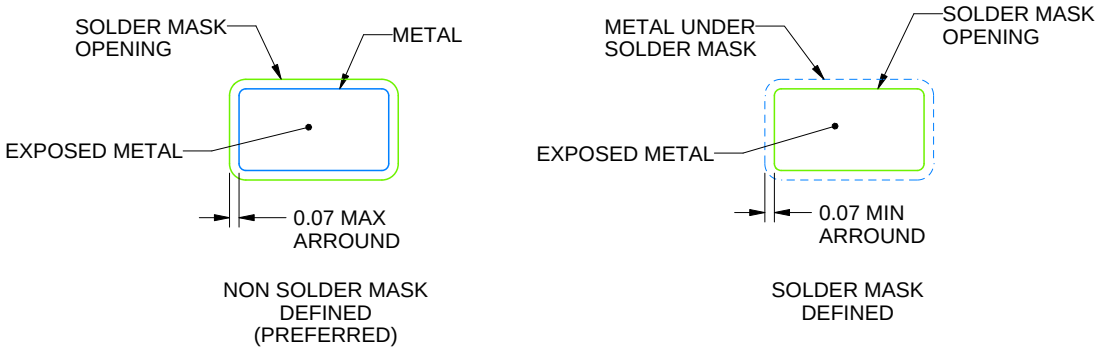
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

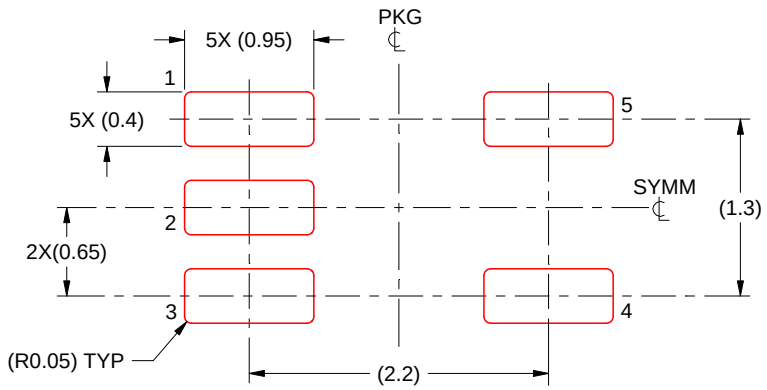


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

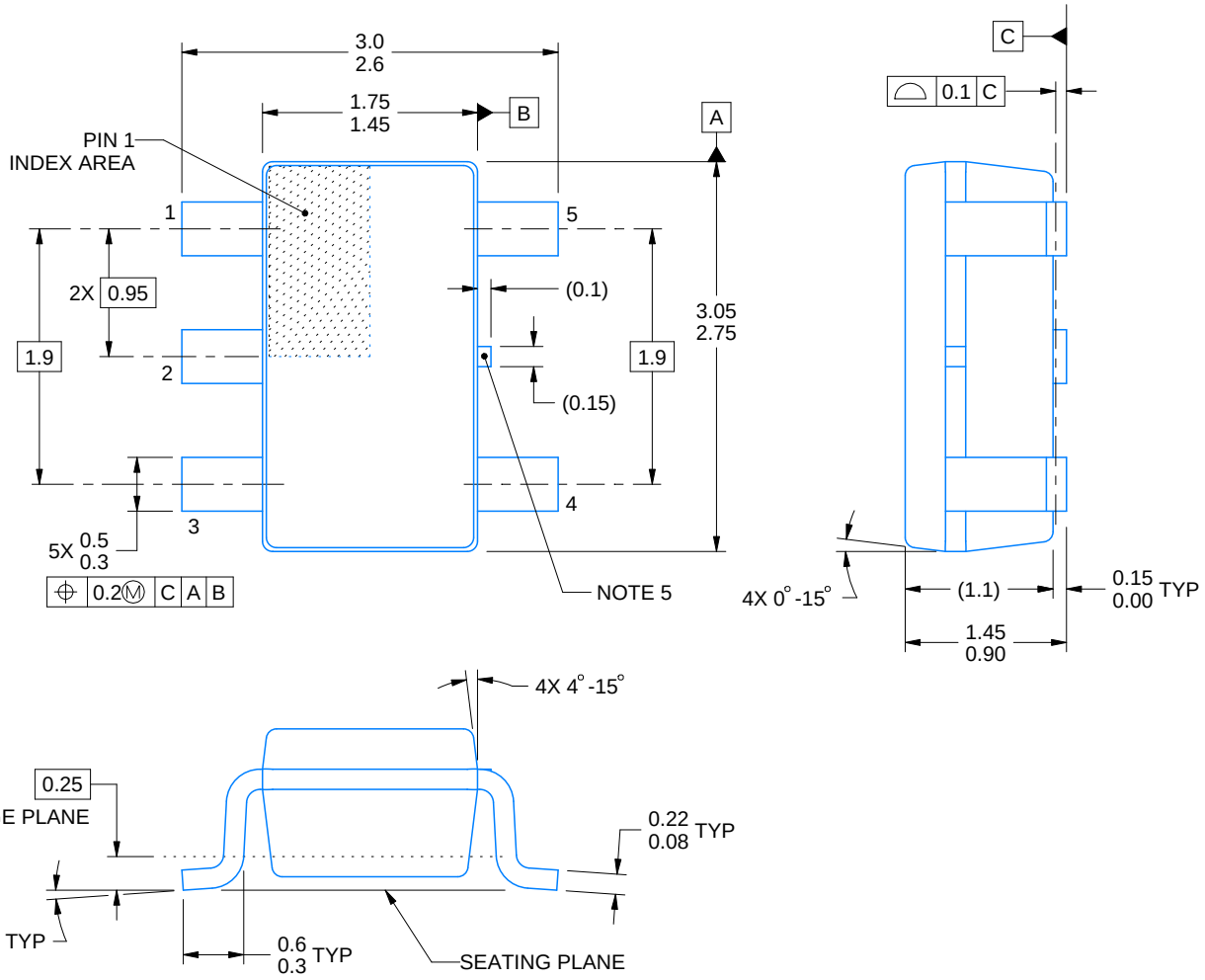
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

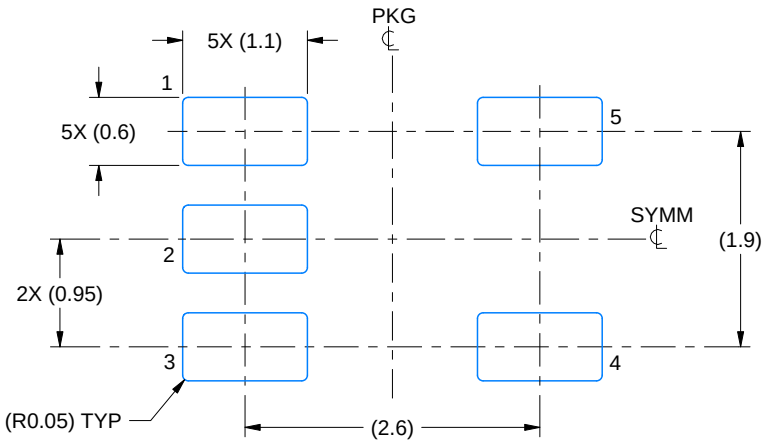
SMALL OUTLINE TRANSISTOR



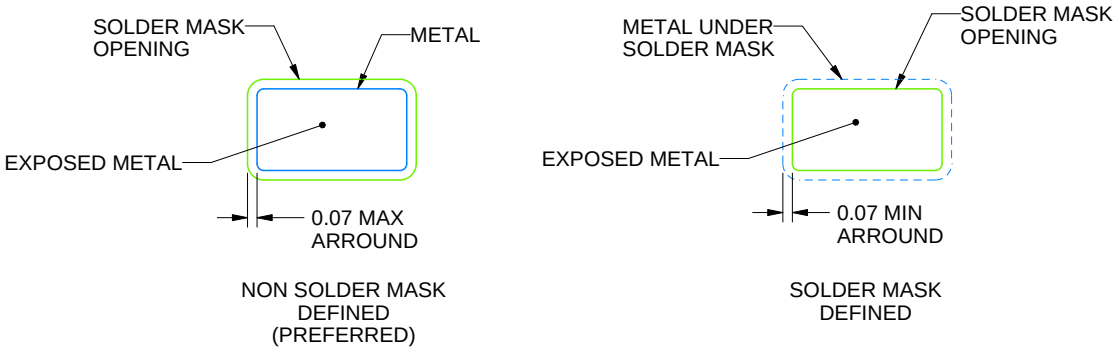
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

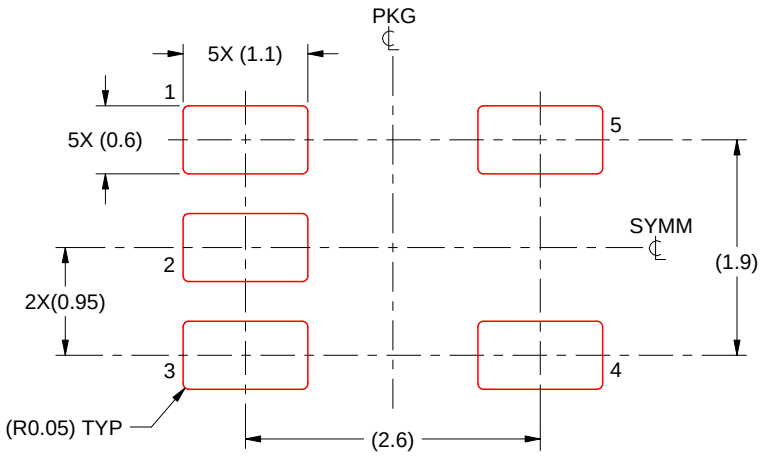


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



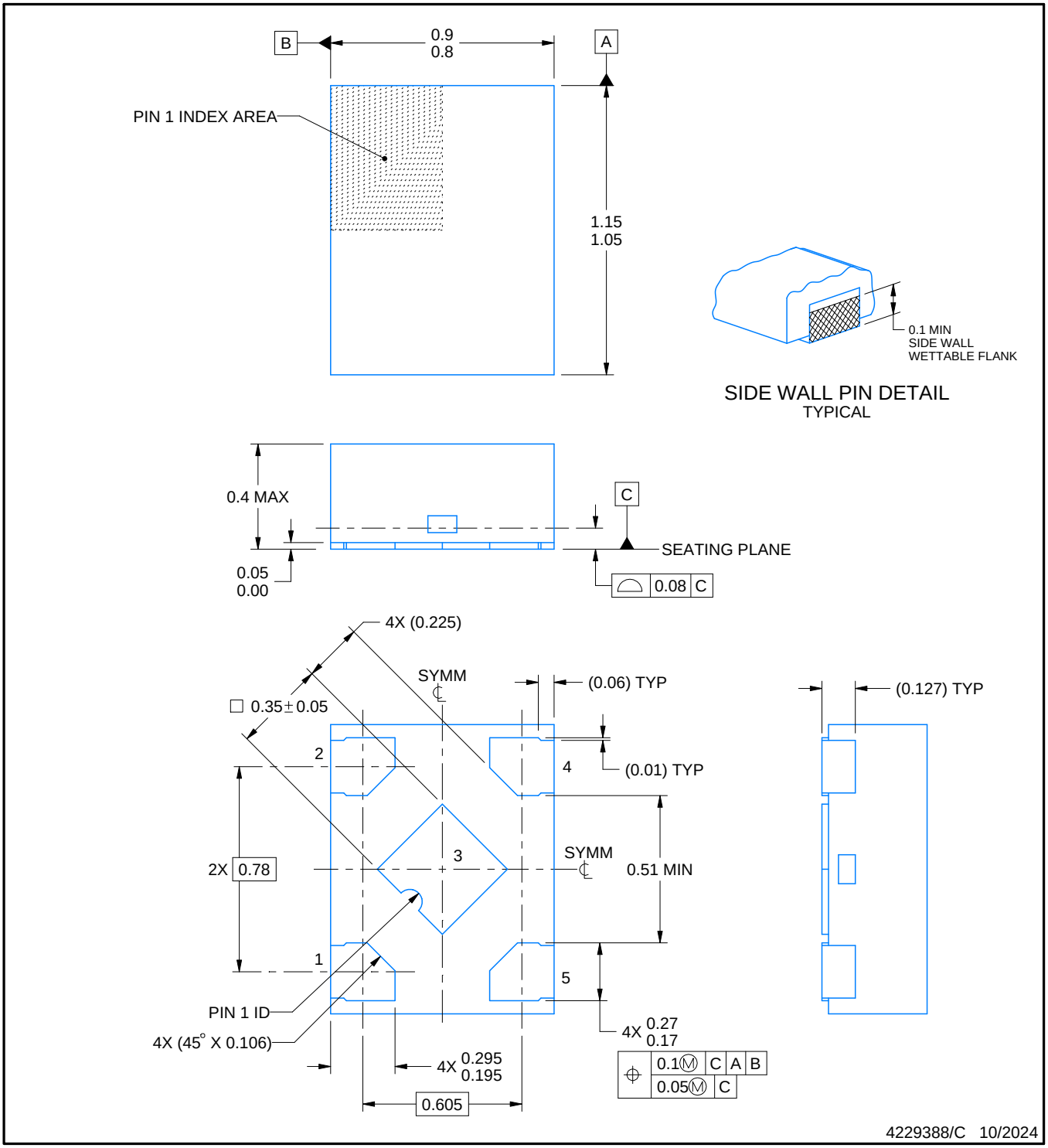
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DTX0005A

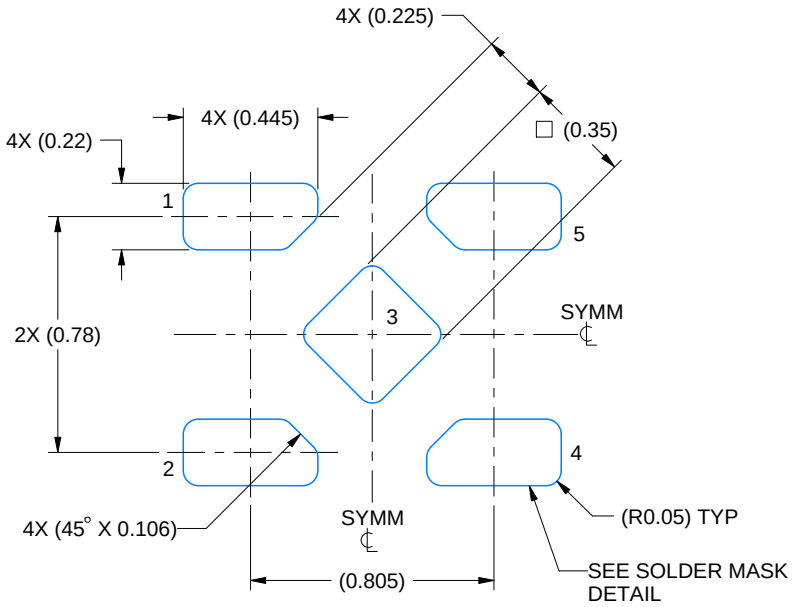
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

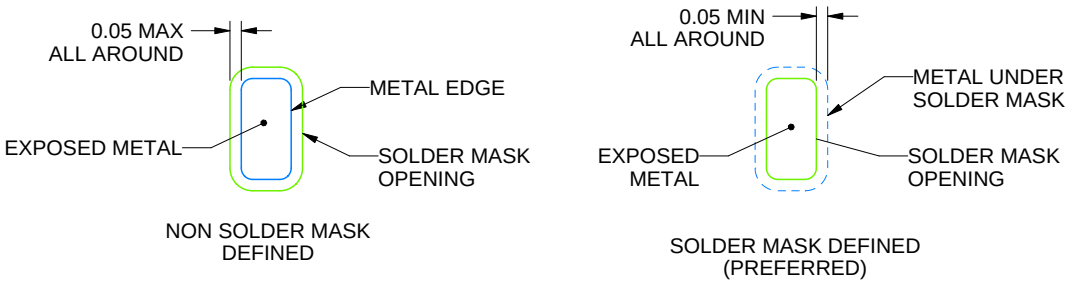


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

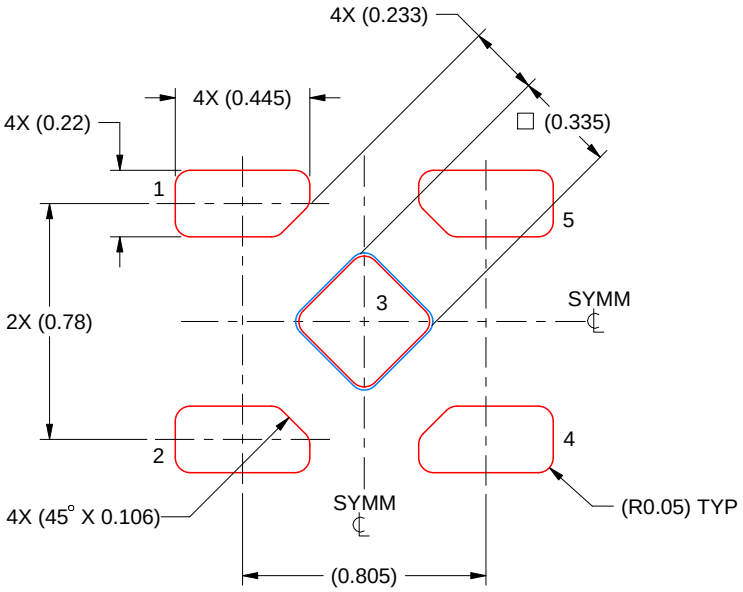


SOLDER MASK DETAILS

4229388/C 10/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

PRINTED SOLDER PASTE COVERAGE BY AREA UNDER PACKAGE
PAD 5: 92%

4229388/C 10/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025