SN74UVP1G07 Low-Power Single Buffer/Driver With Open-Drain Outputs

1 Features

- Extended low-voltage operaion with 0.63V to 3.6V supply range
- Extended operating temperature range: –40°C to 125°C
- Low power consumption
  - Typical of I_{CC} = 10nA
  - Typical input leakage I_I = 3nA
  - Typical output off-state leakage current I_{OZ} = 100nA
  - Typical Partial-Power-Down I_{OFF} 0.2uA
- 3.6-V tolerant input to support down translation
- Maximum t_{pd} of 9.5ns at 3.3V
- Drop-in compatible with AUP1G family and V_{CC} extended from 0.8V to 0.63V

2 Applications

- PC and Notebooks
- Data Center
- Building Automation
- Mobile Phones
- Wearables
- Wired networking

3 Description

The SN74UVP1G07 device is a single-buffer gate with open-drain output.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
SN74UVP1G07	DBV (SOT-23, 5)	2.90mm × 1.60mm
	DCK (SC-70, 5)	2.00mm × 1.25mm
	DRY (USON, 6)	1.45mm × 1.00mm
	DSF (X2SON, 6)	1.00mm × 1.00mm
	DPW (X2SON, 5)	0.80mm × 0.80mm

(1) For more information, see Section 11.
(2) The body size (length × width) is a nominal value and does not include pins.

Simplified Schematic

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

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Table of Contents

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4 Pin Configuration and Functions

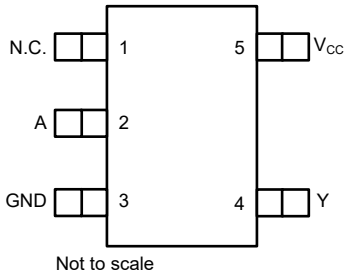

Figure 4-1. DBV or DCK Package, 5-Pin SOT-23 or SC-70 (Top View)

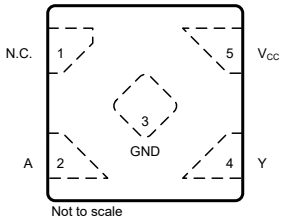

Figure 4-2. DPW Package, 5-Pin X2SON (Top View)

Table 4-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DBV,DCK, DTX	DPW		
N.C.	1	1	—	Not internally connected
A	2	2	I	
GND	3	3	G	Ground pin
Y	4	4	O	Output Y (open drain)
VCC	5	5	P	Power pin

(1) I = Input, O = Output, G = Ground, P = Power

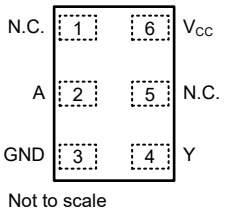

Figure 4-3. DRY or DSF Package, 5-Pin USON or X2SON (Top View)

Table 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DSF, DRY		
N.C.	1, 5	—	Not internally connected
A	2	I	Input A
GND	3	G	Ground pin
Y	4	O	Output Y (open drain)
VCC	6	P	Power pin

(1) I = Input, O = Output, G = Ground, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6	V
V_I	Input voltage range(2)		-0.5	6	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range (2)		-0.5	6	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		0.63	3.6	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 0.63V to 0.77V	0.65 x Vcc		V
		V_{CC} = 0.72V to 0.88V	0.65 x Vcc		
		V_{CC} = 0.9V to 1.1V	0.65 x Vcc		
		V_{CC} = 1.08V to 1.32V	0.65 x Vcc		
		V_{CC} = 1.35V to 1.65V	0.65 x Vcc		
		V_{CC} = 1.62V to 1.98V	0.65 x Vcc		
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3.0V to 3.6V	2		

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5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{IL}	Low-Level input voltage	V_{CC} = 0.63V to 0.77V		0.35 x Vcc	V
		V_{CC} = 0.72V to 0.88V		0.35 x Vcc	
		V_{CC} = 0.9V to 1.1V		0.35 x Vcc	
		V_{CC} = 1.08V to 1.32V		0.35 x Vcc	
		V_{CC} = 1.35V to 1.65V		0.35 x Vcc	
		V_{CC} = 1.62V to 1.98V		0.35 x Vcc	
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3.0V to 3.6V		0.8	
I_{OL}	Low-level output current	V_{CC} = 0.63V		0.2	mA
		V_{CC} = 0.72V		0.5	
		V_{CC} = 0.9V		0.7	
		V_{CC} = 1.08V		1.1	
		V_{CC} = 1.35V		1.7	
		V_{CC} = 1.62V		1.9	
		V_{CC} = 2.3V		3.1	
		V_{CC} = 3.0V		4	
Δt/Δv	Input transition rise or fall rate	V_{cc} = 0.65V to 3.6V		200	ns/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23, 5)	5	298.6	240.2	134.6	114.5	133.9	n/a	°C/W
DCK (SC-70, 5)	5	314.4	128.7	100.6	7.1	99.8	n/a	°C/W
DRY (USON, 6)	6	554.9	385.4	388.2	159.0	384.1	n/a	°C/W
DSF (X2SON, 6)	6	407.1	232.0	306.9	40.3	306.0	n/a	°C/W
DPW (X2SON, 5)	5	291.8	224.2	245.8	31.4	245.6	195.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	I_{OL}= 20µA	0.63V to 3.6V			0.15	V
	I_{OH}= 0.7mA	1.0V			0.35	
	I_{OH}= 1.1mA	1.2V			0.25	
	I_{OH}= 1.7mA	1.5V			0.23	
	I_{OH}= 1.9mA	1.65V			0.23	
	I_{OH}= 3.1mA	2.3V			0.26	
	I_{OH}= 3.5mA	2.7V			0.27	
	I_{OH}= 4mA	3V			0.29	
I_I	V_I = V_{CC} or GND	V_{CC} = 0V to 3.6V		±0.003	±0.5	µA
I_{OFF}	V_I or V_O = V_{CC}	V_{CC} = 0V		±0.2	±1	µA

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5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{OZ}	V_O = V_{CC} or GND	3.6V		±0.1	±1.5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 0.63V to 3.6V		0.01	1.4	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	3.3V			60	µA
C_I	V_I = V_{CC} or GND	3.3V		4.4		pF
C_O	V_O = V_{CC} or GND	3.3V		2.59		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CONDITION	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	C_L = 5pF	0.7V ± 0.07V			320	ns
				0.8V ± 0.08V			117.3	ns
			C_L = 10pF	1.0V ± 0.1V			28.4	ns
				1.2V ± 0.12V			16.4	ns
			C_L = 15pF	1.5V ± 0.15V			6.3	ns
				1.8V ± 0.18V			5.9	ns
			C_L = 30pF	2.5V ± 0.2V			6.6	ns
				3.3V ± 0.3V			9.5	ns
C_{pd}			f = 10MHz	0.7V		0.67		pF
				0.8V		0.67		pF
				1.0V		0.70		pF
				1.2V		0.71		pF
				1.5V		0.72		pF
				1.8V		0.75		pF
				2.5V		0.95		pF
				3.3V		1.23		pF

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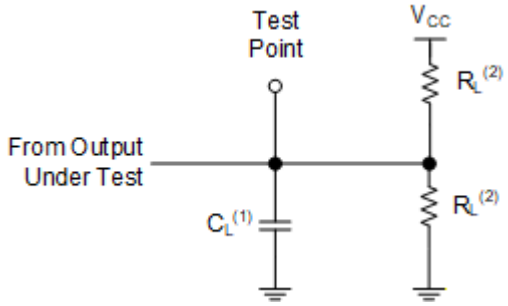
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 3 ns.

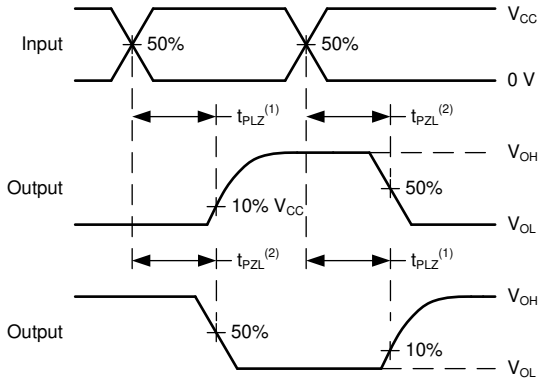
The outputs are measured individually with one input transition per measurement.

TEST	R_L	C_L	ΔV	V_{CC}
t_{pd}	20KΩ	5pF	0.07 V	0.7V
			0.08 V	0.8 V
		10pF	0.1 V	1.0V
	5KΩ	10pF	0.12 V	1.2 V
		15pF	0.15 V	1.5V
			0.18 V	1.8 V
		30pF	0.2 V	2.5V
			0.3 V	3.3 V



(1) C_L includes probe and test-fixture capacitance.
(2) R_L = 5kΩ or 20kΩ for enable and disable time measurement. R_L = 1MΩ for measuring propagation delays, setup and hold times, and pulse width.

Figure 6-1. Load Circuit for Open-Drain Outputs



(1) If R_L = 5kΩ, the time between t_{PLZ} and t_{PZL} is the same as disable and enable time.
(2) If R_L = 1MΩ, t_{PLZ} and t_{PZL} are the same as t_{pd}.

Figure 6-2. Voltage Waveforms Propagation Delays

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7 Detailed Description

7.1 Overview

The SN74UVP1G07 device is a single buffer gate with open drain output. The output of this single buffer/driver is open drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram

7.3 Feature Description

- Wide operating V_{CC} range of 0.63 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{OFF} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- Low noise due to slower edge rates

7.4 Device Functional Modes

Function Table

INPUT A	OUTPUT Y
H	H/Z
L	L

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UVP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

8.2 Typical Application

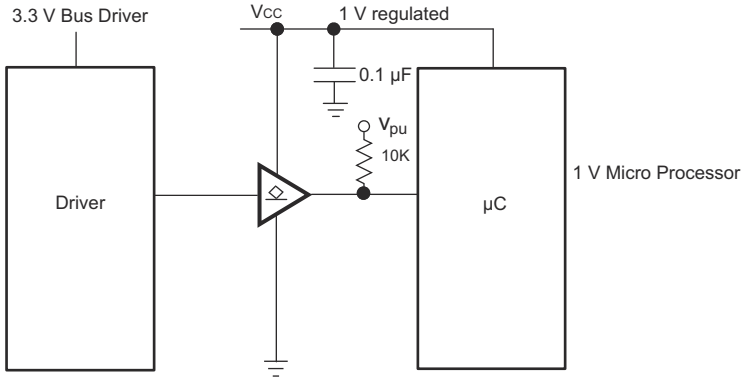

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

8.2.2 Detailed Design Procedure

1. Recommended Input conditions
   - Rise time and fall time specs. See (Δt/ΔV) in *Section 5.3*
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Section 5.3*
   - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}
2. Recommend output conditions
   - Load currents should not exceed 20 mA on the output and 50 mA total for the part

8.3 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Section 5.3* table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1µF is recommended; if there are multiple V_{CC} pins, then 0.01µF or 0.022µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1µF and a 1µF are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for best results.

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8.4 Layout

8.4.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 8-2 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

8.4.2 Layout Example

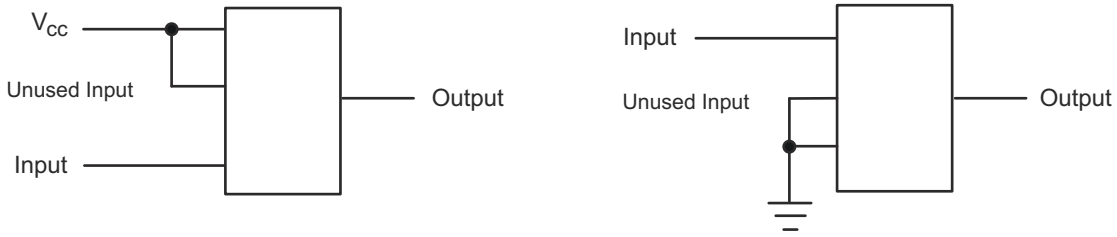

Figure 8-2. Layout Diagram

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

ADVANCE INFORMATION

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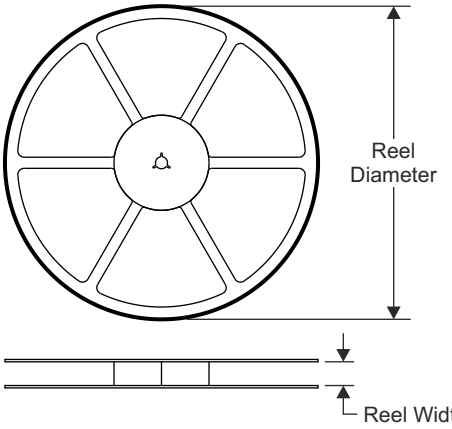
11 Mechanical, Packaging, and Orderable Information

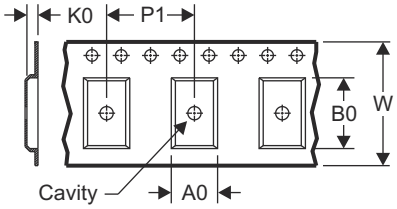
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

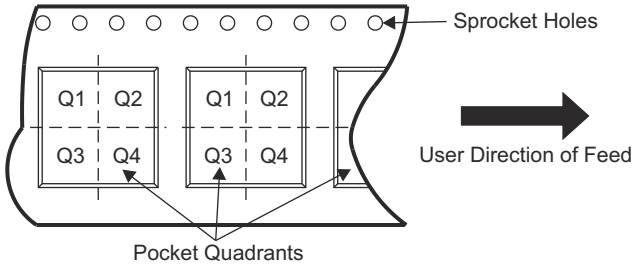


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PSN74UVP1G07DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
PSN74UVP1G07DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
PSN74UVP1G07DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
PSN74UVP1G07DRYR	USON	DRY	5	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
PSN74UVP1G07DSFR	USON	DSF	5	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

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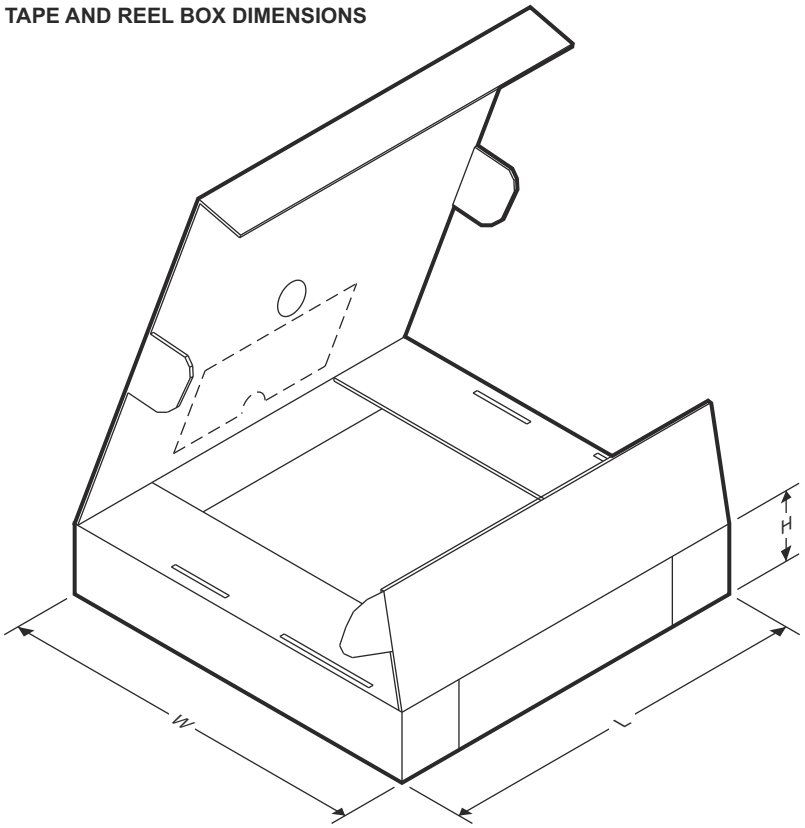
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PSN74UVP1G07DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
PSN74UVP1G07DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
PSN74UVP1G07DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
PSN74UVP1G07DRYR	USON	DRY	5	5000	184.0	184.0	19.0
PSN74UVP1G07DSFR	USON	DSF	5	5000	210.0	185.0	35.0

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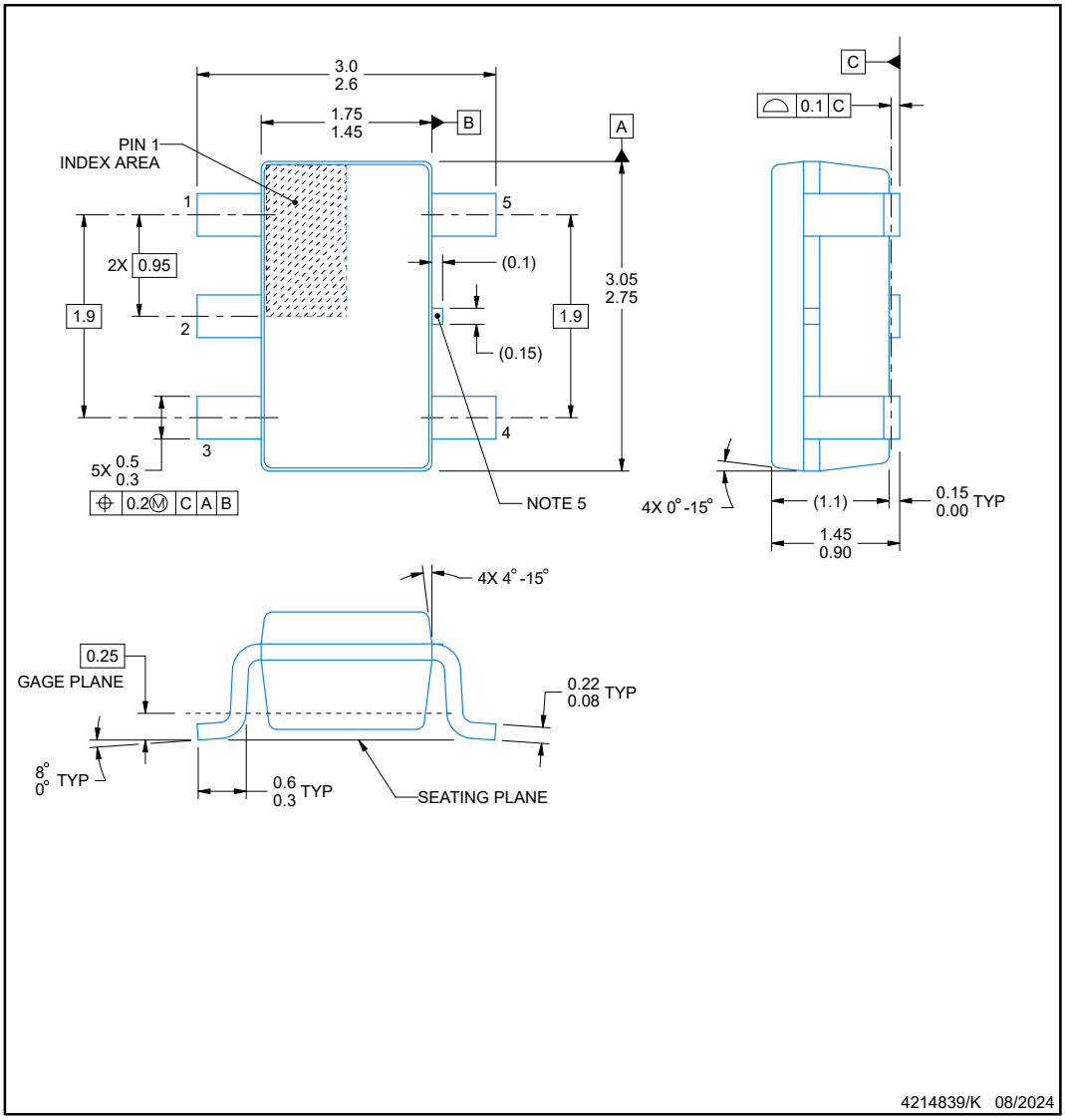
11.2 Mechanical Data

PACKAGE OUTLINE

DBV0005A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

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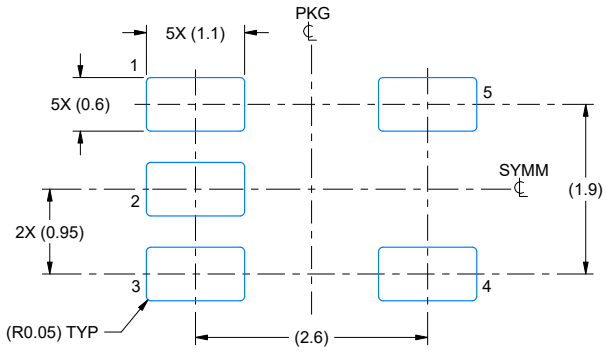
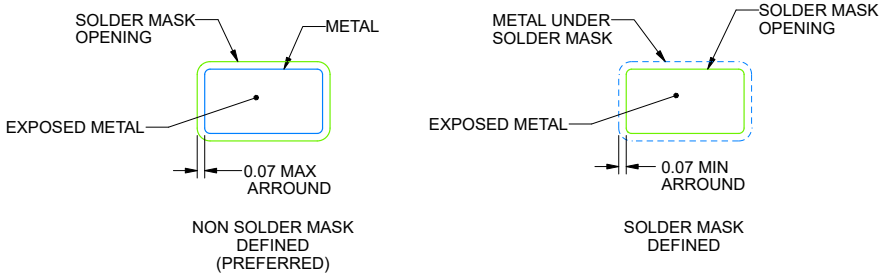
EXAMPLE BOARD LAYOUT

DBV0005A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

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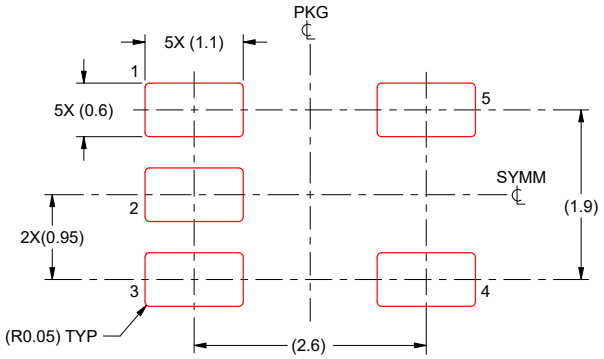
EXAMPLE STENCIL DESIGN

DBV0005A — **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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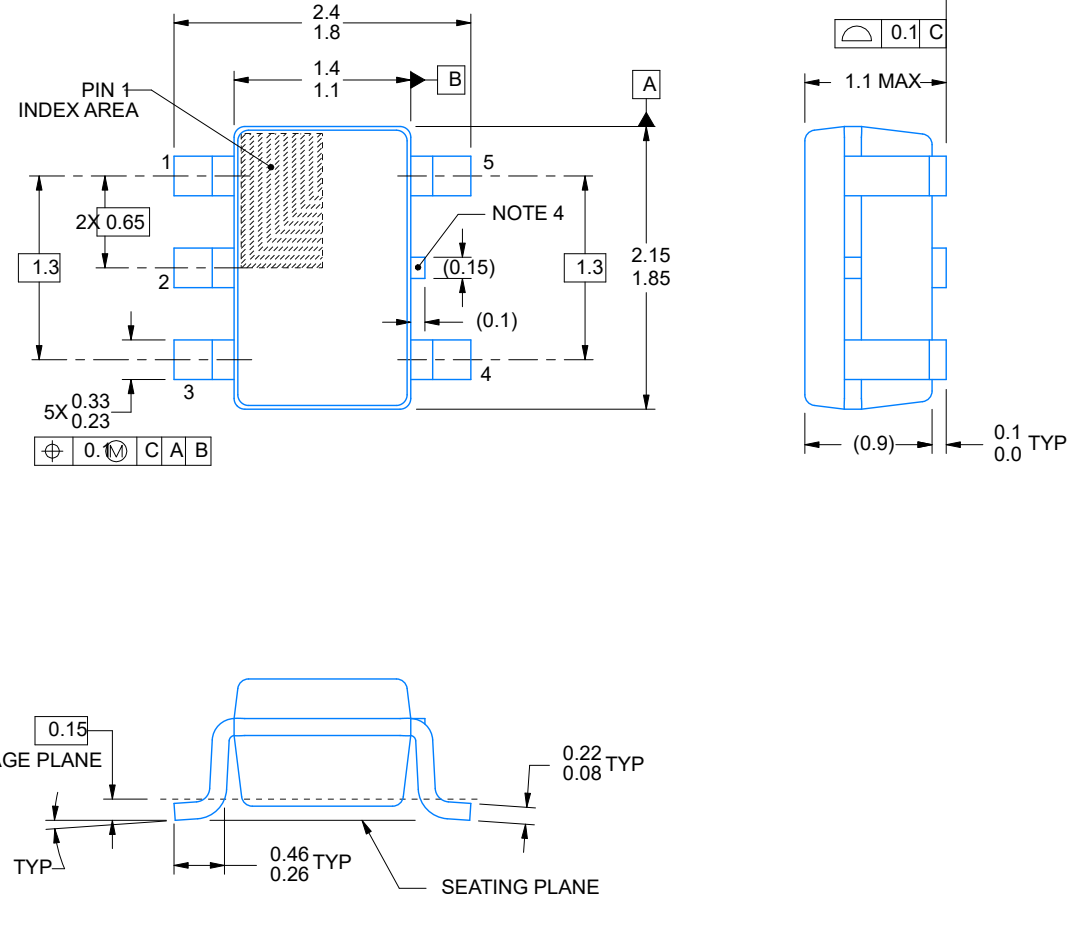
PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/C 03/2023

ADVANCE INFORMATION

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dim ensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.

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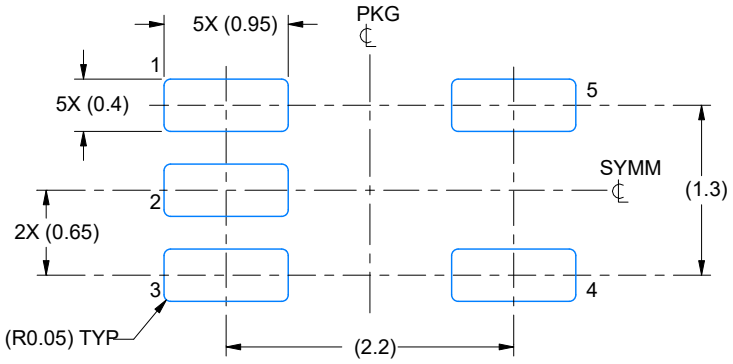
EXAMPLE BOARD LAYOUT

DCK0005A

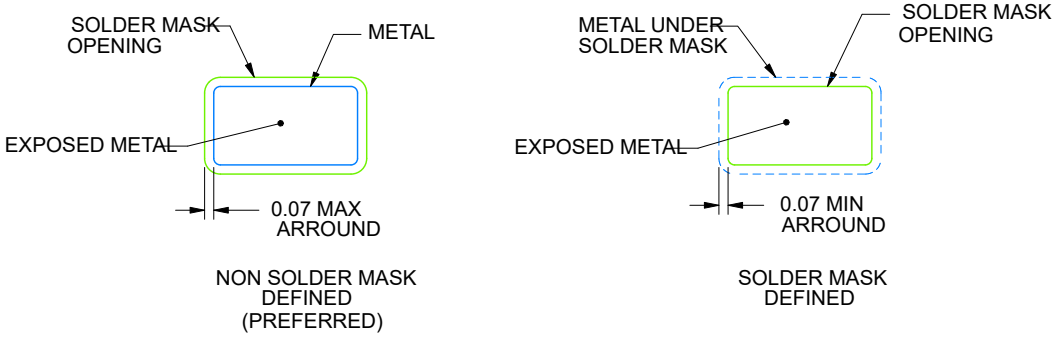
SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR

ADVANCE INFORMATION



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/C 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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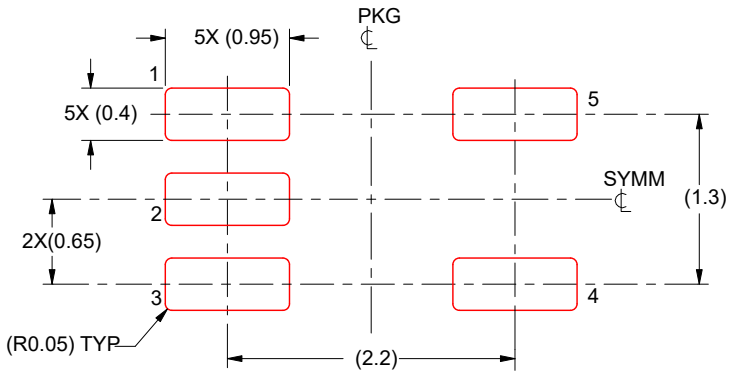
EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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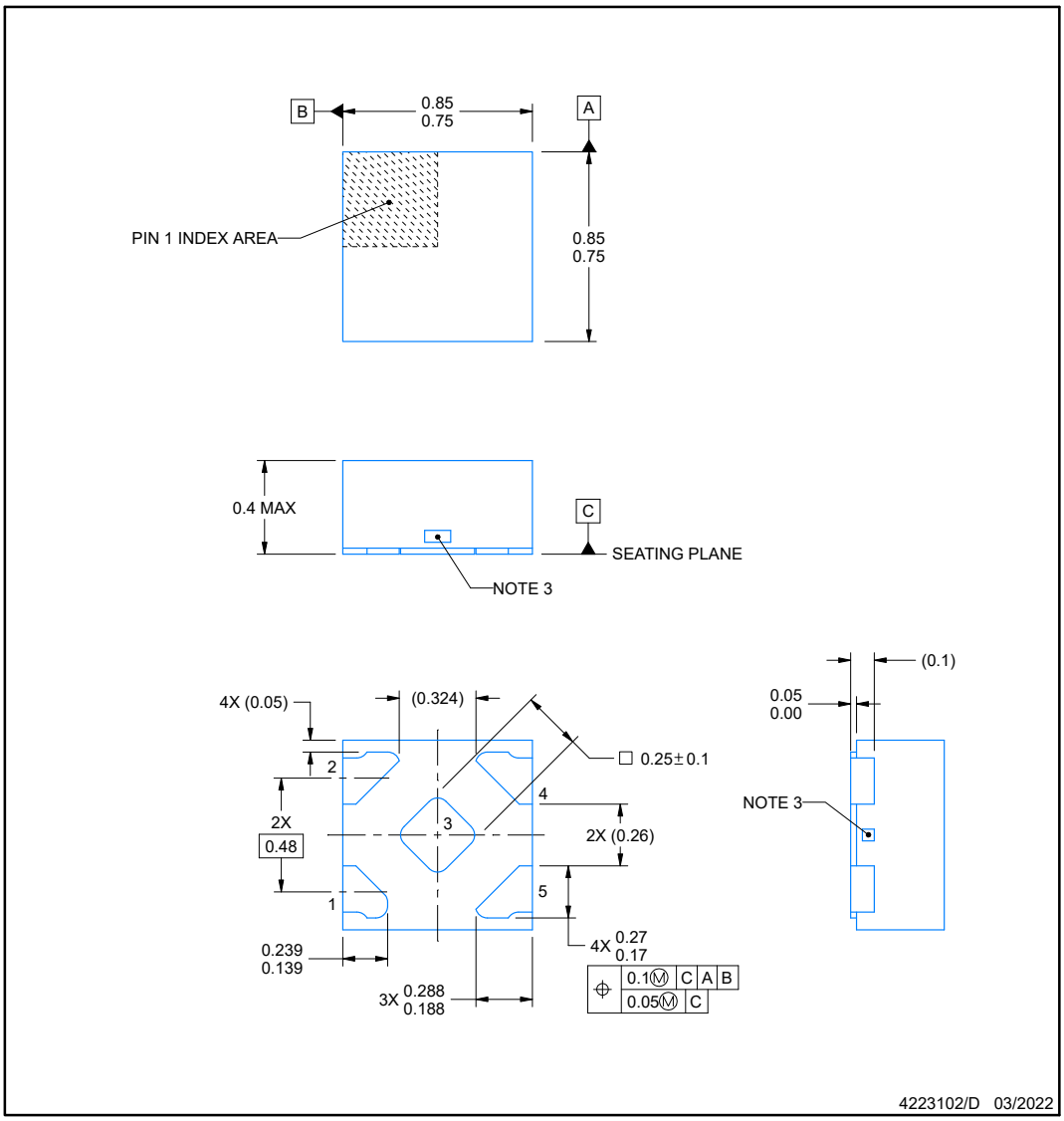
PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

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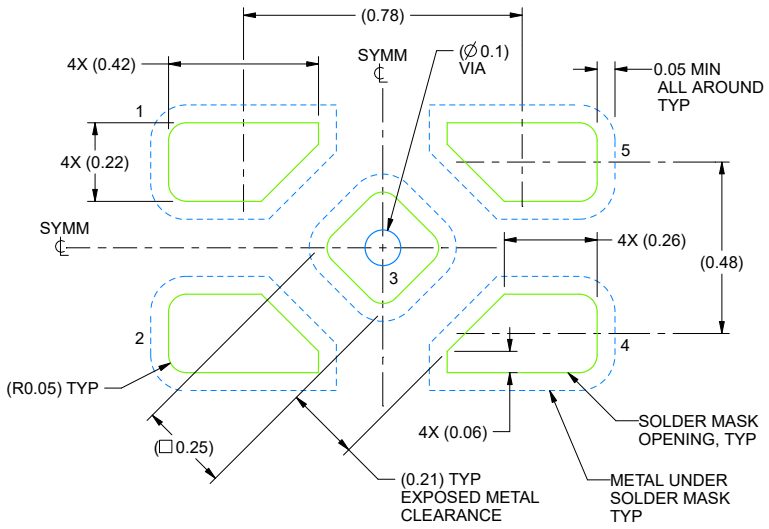
EXAMPLE BOARD LAYOUT

DPW0005A — **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

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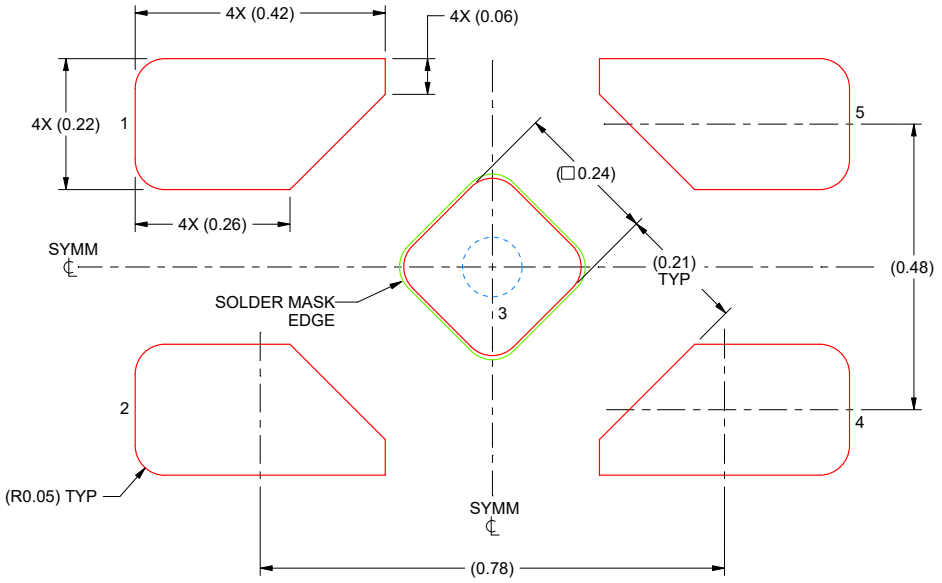
EXAMPLE STENCIL DESIGN

DPW0005A — **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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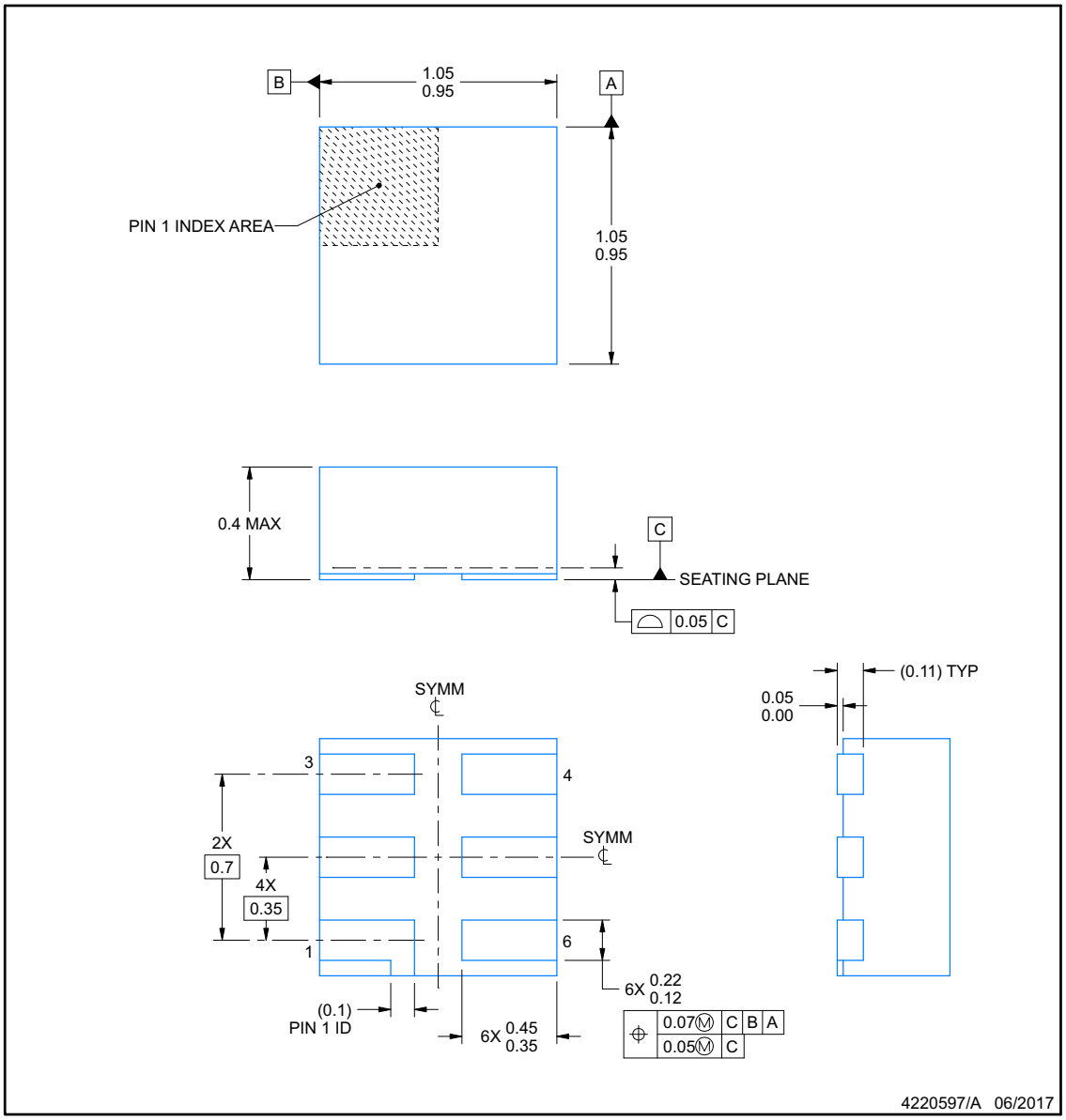
PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

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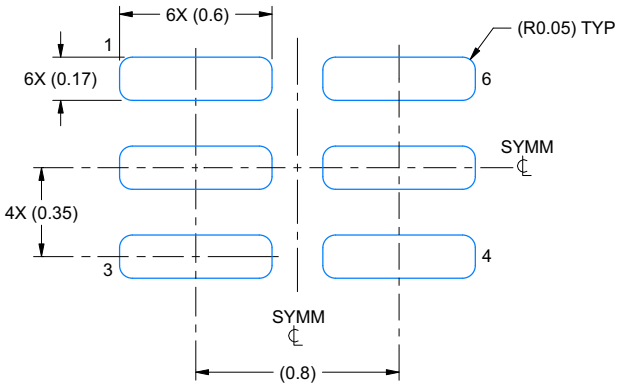
EXAMPLE BOARD LAYOUT

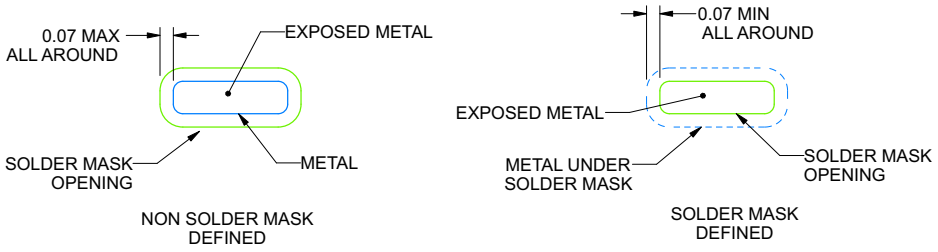
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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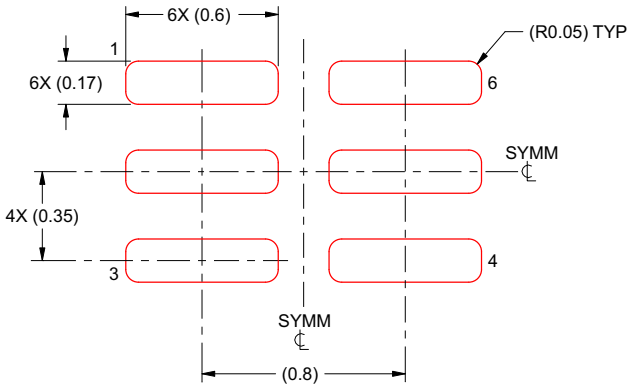
EXAMPLE STENCIL DESIGN

DSF0006A — **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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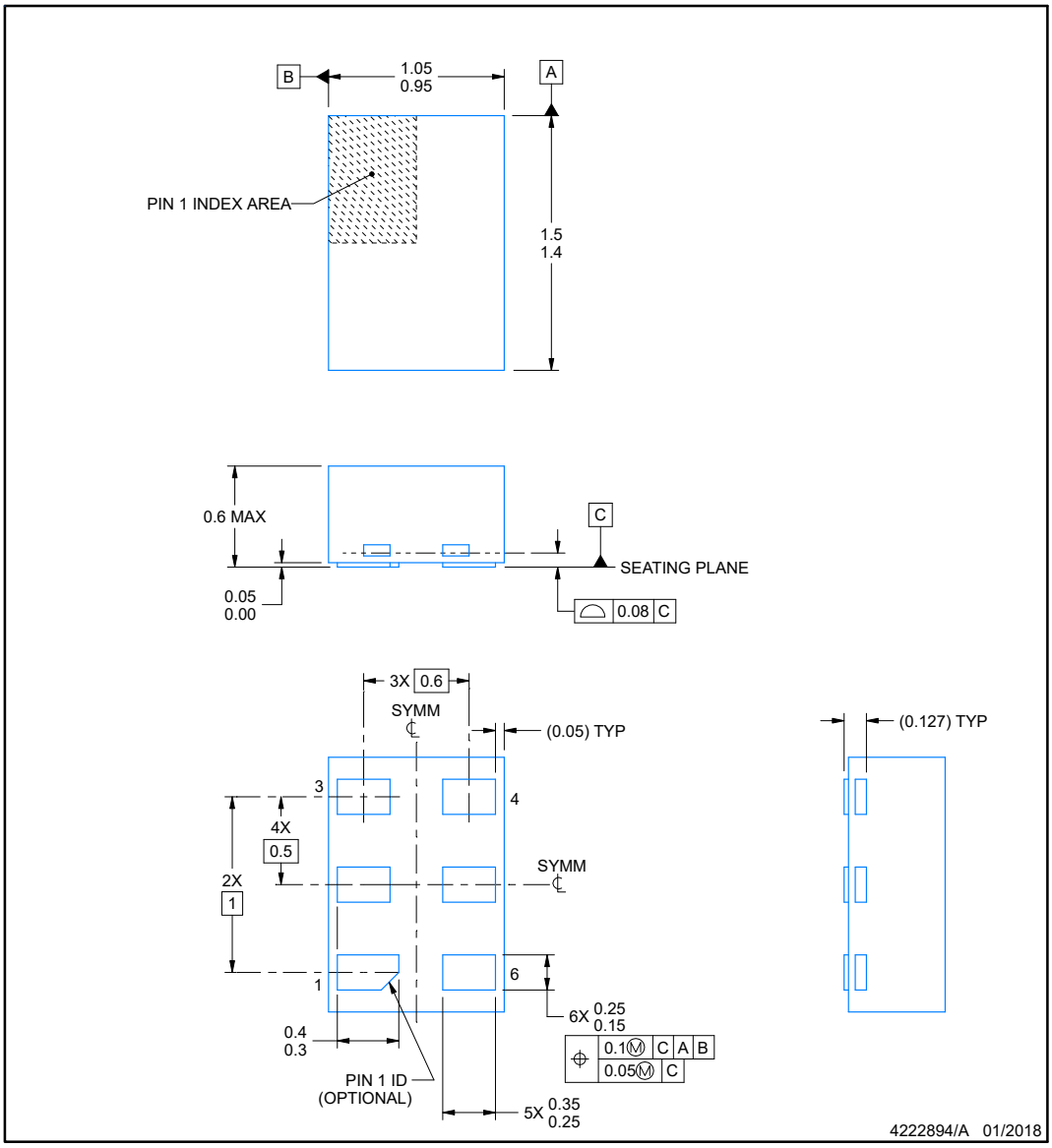
PACKAGE OUTLINE

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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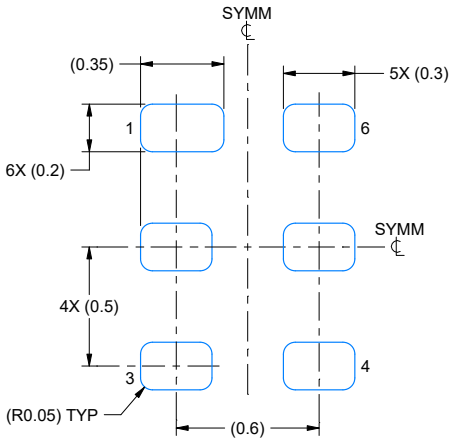
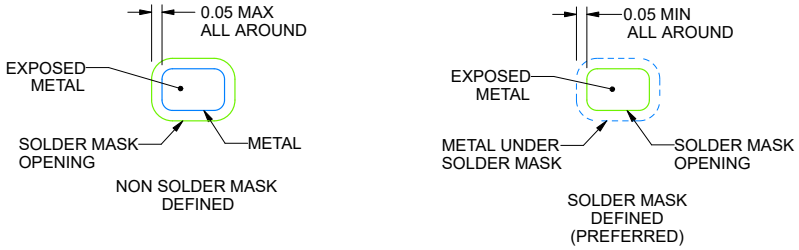
EXAMPLE BOARD LAYOUT

DRY0006A — **USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

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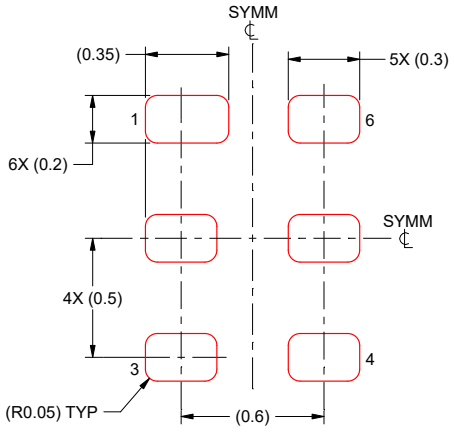
EXAMPLE STENCIL DESIGN

DRY0006A — **USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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