# SN74UVP1G16 Inverting Buffer with Schmitt-Trigger Input and Open-Drain Output

## 1 Features

- Extended low-voltage operation with 0.63V to 3.6V supply range
- Extended operating temperature range: –40°C to 125°C
- Low power consumption
  – Typical $I_{CC}$ = 10nA
  – Typical input leakage $I_I$ = 3nA
  – Typical output off-state leakage current $I_{OZ}$ = 100nA
  – Typical partial-power-down $I_{OFF}$ 0.2uA
- 3.6V tolerant input to support down translation
- Maximum $t_{pd}$ of 9.5ns at 3.3V
- Drop-in compatible with AUP1G family and $V_{CC}$ extended from 0.8V to 0.63V

## 2 Applications

- PC and notebooks
- Data center
- Building automation
- Mobile phones
- Wearables
- Wired networking

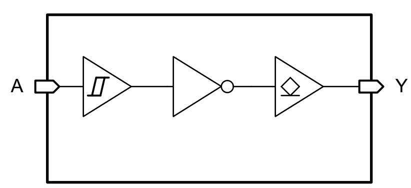
## 3 Description

The SN74UVP1G16 device is an Inverter Buffer with a Schmitt-Trigger input and an Open-Drain output.

**Package Information**

| PART NUMBER | PACKAGE (1) | PACKAGE SIZE (2) |
|---|---|---|
| SN74UVP1G16 | DBV (SOT-23, 5) | 2.90mm × 1.60mm |
| SN74UVP1G16 | DCK (SC-70, 5) | 2.00mm × 1.25mm |
| | DRY (USON, 6) | 1.45mm × 1.00mm |
| | DSF (X2SON, 6) | 1.00mm × 1.00mm |
| | DPW (X2SON, 5) | 0.80mm × 0.80mm |

(1) For more information, see Section 13.
(2) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram**

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## 4 Pin Configuration and Functions

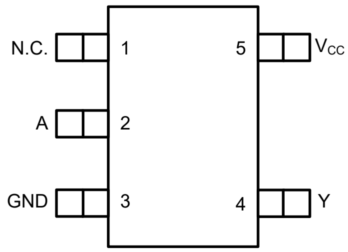


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**Figure 4-1. DBV or DCK Package, 5-Pin SOT-23 or SC-70 (Top View)**

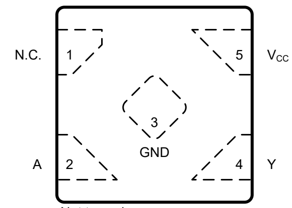


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**Figure 4-2. DPW Package, 5-Pin X2SON (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | DPW, DBV, DCK | | |
| N.C. | 1 | — | Not internally connected |
| A | 2 | I | Input A |
| GND | 3 | G | Ground pin |
| Y | 4 | O | Output Y (push pull) |
| VCC | 5 | P | Power pin |

(1) I = Input, O = Output, G = Ground, P = Power

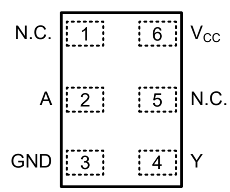


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**Figure 4-3. DRY or DSF Package, 5-Pin USON or X2SON (Top View)**

**Table 4-2. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | DSF, DRY | | |
| N.C. | 1, 5 | — | Not internally connected |
| A | 2 | I | Input A |
| GND | 3 | G | Ground pin |
| Y | 4 | O | Output Y (push pull) |
| VCC | 6 | P | Power pin |

(1) I = Input, O = Output, G = Ground, P = Power

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 6 | V |
| $V_I$ | Input voltage range[(2)] | | -0.5 | 6 | V |
| $V_O$ | Output voltage range[(2)] | | -0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | Output voltage range [(2)] | | -0.5 | 6 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0V | | -50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0V | | -50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| $I_O$ | Continuous output current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | -65 | 150 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)] | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Specifications | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 0.63 | 3.6 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | 5.5 | V |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 0.63V | | 0.2 | mA |
| | | $V_{CC}$ = 0.72V | | 0.5 | |
| | | $V_{CC}$ = 0.9V | | 0.7 | |
| | | $V_{CC}$ = 1.08V | | 1.1 | |
| | | $V_{CC}$ = 1.35V | | 1.7 | |
| | | $V_{CC}$ = 1.62V | | 1.9 | |
| | | $V_{CC}$ = 2.3V | | 3.1 | |
| | | $V_{CC}$ = 3.0V | | 4 | |
| $T_A$ | Operating free-air temperature | | -40 | 125 | °C |

### 5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC[1] | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $R_{\theta JA}$ | $R_{\theta JC(top)}$ | $R_{\theta JB}$ | $\Psi_{JT}$ | $\Psi_{JB}$ | $R_{\theta JC(bot)}$ | |
| DBV (SOT-23, 5) | 5 | 298.6 | 240.2 | 134.6 | 114.5 | 133.9 | n/a | °C/W |
| DCK (SC-70, 5) | 5 | 314.4 | 128.7 | 100.6 | 7.1 | 99.8 | n/a | °C/W |
| DRY (USON, 6) | 6 | 554.9 | 385.4 | 388.2 | 159.0 | 384.1 | n/a | °C/W |
| DSF (X2SON, 6) | 6 | 407.1 | 232.0 | 306.9 | 40.3 | 306.0 | n/a | °C/W |
| DPW (X2SON, 5) | 5 | 291.8 | 224.2 | 245.8 | 31.4 | 245.6 | 195.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

### 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive-going input threshold voltage | 0.63V | 0.3 | | 0.42 | V |
| | | 0.65V | 0.31 | | 0.43 | |
| | | 0.72V | 0.35 | | 0.47 | |
| | | 0.9V | 0.45 | | 0.57 | |
| | | 1.08V | 0.56 | | 0.68 | |
| | | 1.35V | 0.71 | | 0.87 | |
| | | 1.5V | 0.79 | | 0.98 | |
| | | 1.62V | 0.86 | | 1.07 | |
| | | 1.95V | 1.07 | | 1.33 | |
| | | 2.3V | 1.33 | | 1.62 | |
| | | 2.5V | 1.47 | | 1.78 | |
| | | 2.7V | 1.63 | | 1.94 | |
| | | 3V | 1.86 | | 2.18 | |
| | | 3.6V | 2.33 | | 2.67 | |
| $V_{T-}$ | Negative-going input threshold voltage | 0.63V | 0.15 | | 0.31 | V |
| | | 0.65V | 0.16 | | 0.32 | |
| | | 0.72V | 0.19 | | 0.34 | |
| | | 0.9V | 0.25 | | 0.42 | |
| | | 1.08V | 0.32 | | 0.49 | |
| | | 1.35V | 0.42 | | 0.59 | |
| | | 1.5V | 0.48 | | 0.64 | |
| | | 1.62V | 0.52 | | 0.68 | |
| | | 1.95V | 0.6 | | 0.78 | |
| | | 2.3V | 0.69 | | 0.88 | |
| | | 2.5V | 0.73 | | 0.92 | |
| | | 2.7V | 0.78 | | 0.97 | |
| | | 3V | 0.85 | | 1.03 | |
| | | 3.6V | 1.01 | | 1.21 | |

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### 5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\Delta V_T$ | Hysteresis ($V_{T+} – V_{T–}$) | 0.63V | 0.08 | | 0.18 | V |
| | | 0.65V | 0.08 | | 0.18 | |
| | | 0.72V | 0.09 | | 0.2 | |
| | | 0.9V | 0.13 | | 0.24 | |
| | | 1.08V | 0.17 | | 0.27 | |
| | | 1.35V | 0.23 | | 0.33 | |
| | | 1.5V | 0.27 | | 0.41 | |
| | | 1.62V | 0.3 | | 0.47 | |
| | | 1.95V | 0.38 | | 0.65 | |
| | | 2.3V | 0.53 | | 0.84 | |
| | | 2.5V | 0.63 | | 0.94 | |
| | | 2.7V | 0.74 | | 1.04 | |
| | | 3V | 0.92 | | 1.19 | |
| | | 3.6V | 1.26 | | 1.49 | |
| $V_{OL}$ | $I_{OL}$= 20μA | 0.63V to 3.6V | | | 0.15 | V |
| | $I_{OL}$= 0.7mA | 1.0V | | | 0.35 | |
| | $I_{OL}$= 1.1mA | 1.2V | | | 0.25 | |
| | $I_{OL}$= 1.7mA | 1.5V | | | 0.23 | |
| | $I_{OL}$= 1.9mA | 1.65V | | | 0.23 | |
| | $I_{OL}$= 3.1mA | 2.3V | | | 0.26 | |
| | $I_{OL}$= 3.5mA | 2.7V | | | 0.27 | |
| | $I_{OL}$= 4mA | 3V | | | 0.29 | |
| $I_I$ | $V_I = V_{CC}$ or GND | $V_{CC}$ = 0V to 3.6V | | ±0.003 | ±0.5 | μA |
| $I_{OFF}$ | $V_I$ or $V_O = V_{CC}$ | $V_{CC}$ = 0V | | ±0.2 | ±1 | μA |
| $I_{OZ}$ | $V_O = V_{CC}$ or GND | 3.6V | | ±0.1 | ±1.5 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | $V_{CC}$ = 0.63V to 3.6V | | 0.01 | 1.4 | μA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | 3.3V | | | 60 | μA |
| $C_I$ | $V_I = V_{CC}$ or GND | 3.3V | | 4.4 | | pF |
| $C_O$ | $V_O = V_{CC}$ or GND | 3.3V | | 2.59 | | pF |

### 5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CONDITION | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A | Y | $C_L$ = 5pF | 0.7V ± 0.07V | | | 319.8 | ns |
| | | | | 0.8V ± 0.08V | | | 121.3 | ns |
| | | | $C_L$ = 10pF | 1.0V ± 0.1V | | | 34.3 | ns |
| | | | | 1.2V ± 0.12V | | | 19.5 | ns |
| | | | $C_L$ = 15pF | 1.5V ± 0.15V | | | 8.8 | ns |
| | | | | 1.8V ± 0.18V | | | 7.7 | ns |
| | | | $C_L$ = 30pF | 2.5V ± 0.2V | | | 8.2 | ns |
| | | | | 3.3V ± 0.3V | | | 11.1 | ns |

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CONDITION | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $C_{pd}$ | | | f = 10MHz | 0.7V | | 0.7 | | pF |
| | | | | 0.8V | | 0.8 | | pF |
| | | | | 1.0V | | 0.9 | | pF |
| | | | | 1.2V | | 0.9 | | pF |
| | | | | 1.5V | | 1 | | pF |
| | | | | 1.8V | | 1.2 | | pF |
| | | | | 2.5V | | 1.5 | | pF |
| | | | | 3.3V | | 1.9 | | pF |

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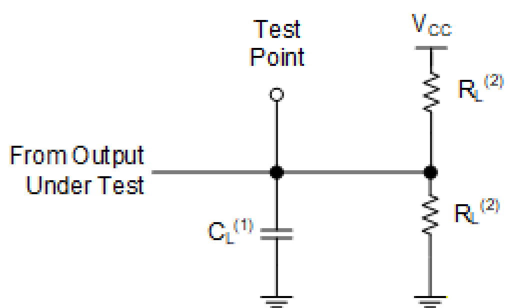
## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O$ = 50Ω, $t_t$ < 3 ns.

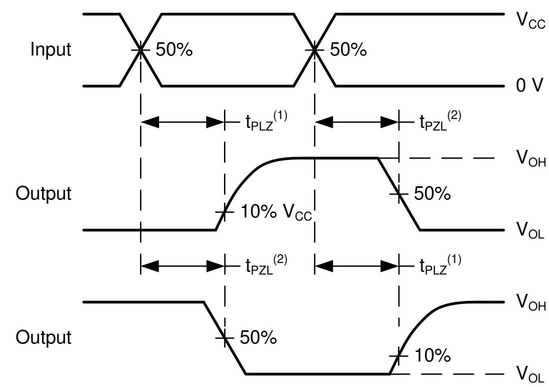
The outputs are measured individually with one input transition per measurement.

| TEST | $R_L$ | $C_L$ | ΔV | $V_{CC}$ |
|---|---|---|---|---|
| $t_{pd}$ | 20KΩ | 5pF | 0.07V | 0.7V |
| | | | 0.08V | 0.8V |
| | | 10pF | 0.1V | 1.0V |
| | 5KΩ | 10pF | 0.12V | 1.2V |
| | | 15pF | 0.15V | 1.5V |
| | | | 0.18V | 1.8V |
| | | 30pF | 0.2V | 2.5V |
| | | | 0.3V | 3.3V |




(1) $C_L$ includes probe and test-fixture capacitance.
(2) $R_L$ = 5kΩ or 20kΩ for enable and disable time measurement. $R_L$ = 1MΩ for measuring propagation delays, setup and hold times, and pulse width.

**Figure 6-1. Load Circuit for Open-Drain Outputs**



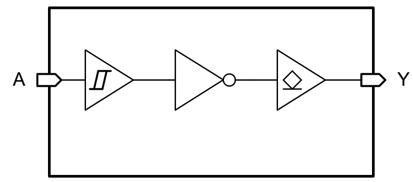

(1) If $R_L$ = 5kΩ, the time between $t_{PLZ}$ and $t_{PZL}$ is the same as disable and enable time.
(2) If $R_L$ = 1MΩ, $t_{PLZ}$ and $t_{PZL}$ are the same as $t_{pd}$.

**Figure 6-2. Voltage Waveforms Propagation Delays**

# 7 Overview

The SN74UVP1G16 device contains one open-drain inverter with a maximum sink current of 32mA. This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

# 8 Functional Block Diagram

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# 9 Detailed Description

## 9.1 Feature Description

### *9.1.1 Open-Drain CMOS Outputs*

Open-drain outputs are included in SN74UVP1G16. Open-drain outputs can only drive the output low. When in the high logical state, outputs are in a high-impedance state, meaning outputs neither source nor sink current (with the exception of minor leakage current as defined in the *Electrical Characteristics* table). In the high-impedance state, the output voltage is not controlled by SN74UVP1G16 and is dependent on external factors.

Because of the high-impedance state, an external pull-up resistor is required to define a logic high. Without a pull-up resistor, the output will float and have an undefined logic level. The resistor value depends on factors like parasitic capacitance and power consumption; typically, a 10kΩ resistor is suitable.

The drive capability of SN74UVP1G16 can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, outputs can drive higher currents than SN74UVP1G16 is designed to handle continuously. Limit the device output power to avoid damage due to overcurrent. Follow the electrical and thermal limits defined in the *Absolute Maximum Ratings* at all times. See the *Recommended Operating Conditions* table for the maximum output voltage that can be externally connected to SN74UVP1G16.

Leave unused open-drain CMOS outputs disconnected.

### *9.1.2 CMOS Schmitt-Trigger Inputs*

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, properly terminating unused inputs is still recommended. Driving the inputs with slow transitioning signals increases dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

# 10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 10.1 Application Information

In this application, an open-drain inverter is used to drive an LED as shown in Figure 10-1.

## 10.2 Typical Application

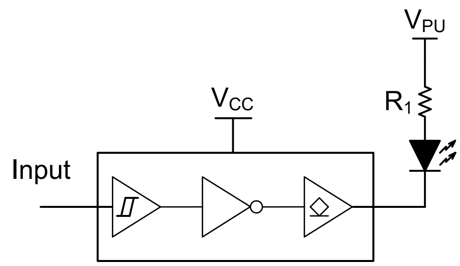


**Figure 10-1. Typical Application Block Diagram**

### *10.2.1 Design Requirements*

#### 10.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74UVP1G16 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74UVP1G16 can drive a load with a total capacitance less than or equal to 30 nF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, TI recommends adding a series resistor between the output and capacitor to prevent excessive current.

The SN74UVP1G16 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

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**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 10.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74UVP1G16 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74UVP1G16 has no input signal transition rate requirements because the device has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the Electrical Characteristics . This hysteresis value provides the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the Typical Characteristics .

Refer to the *Feature Description* for additional information regarding the inputs for this device.

#### 10.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### *10.2.2 Detailed Design Procedure*

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SN74UVP1G16 to the receiving device.
3. Verify that the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$)Ω. Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

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### 10.3 Application Curves

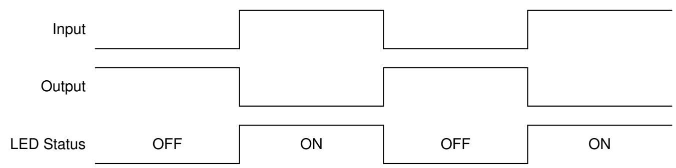



**Figure 10-2. Application Curve**

### 10.4 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal must have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

### 10.5 Layout

#### *10.5.1 Layout Guidelines*

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

#### *10.5.2 Layout Example*

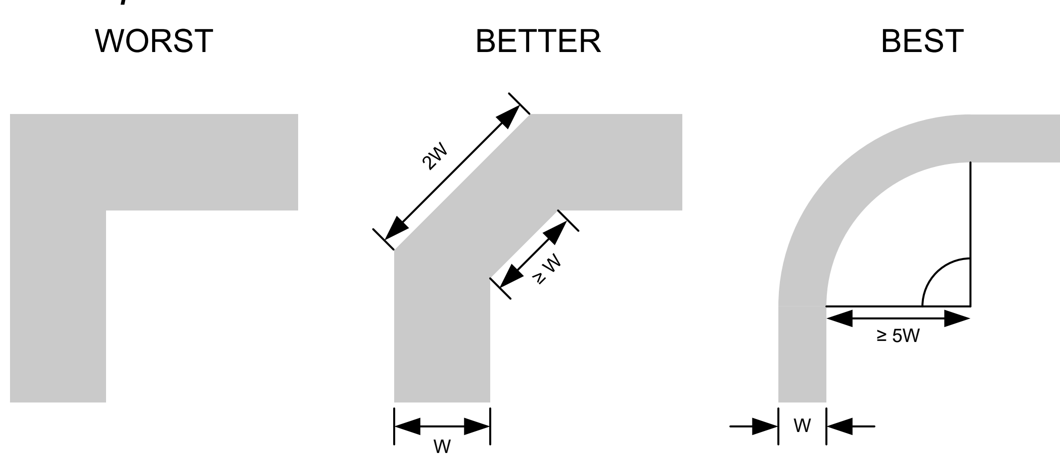



**Figure 10-3. Example Trace Corners for Improved Signal Integrity**

ADVANCE INFORMATION

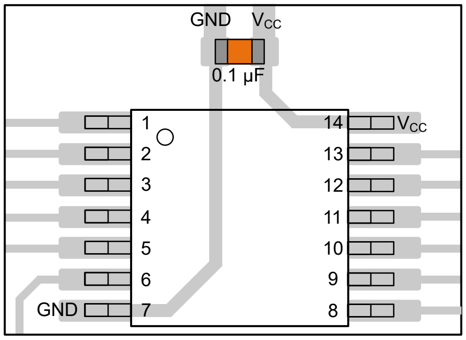



**Figure 10-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

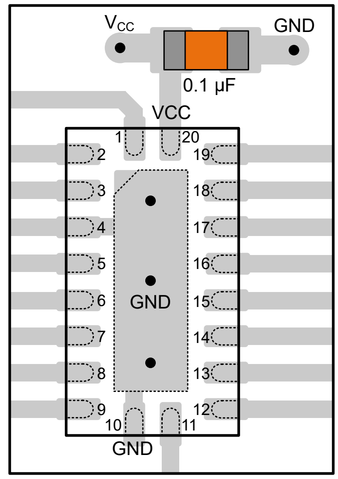



**Figure 10-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**

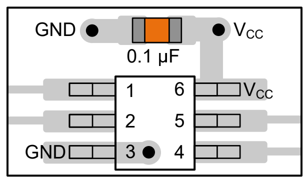



**Figure 10-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

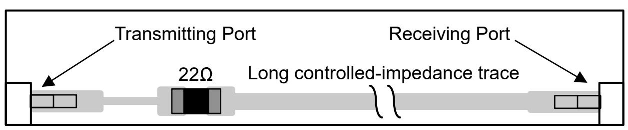



**Figure 10-7. Example Damping Resistor Placement for Improved Signal Integrity**

ADVANCE INFORMATION

# 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 11.1 Documentation Support

### *11.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
| --- | --- | --- |
| August 2026 | * | Initial Release |

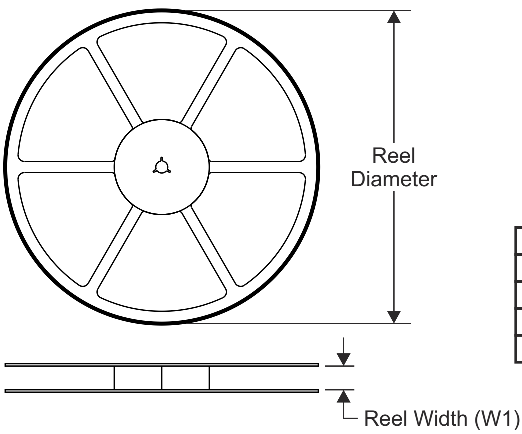
ADVANCE INFORMATION

# 13 Mechanical, Packaging, and Orderable Information

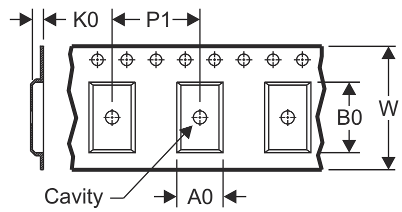
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 13.1 Tape and Reel Information

**REEL DIMENSIONS**

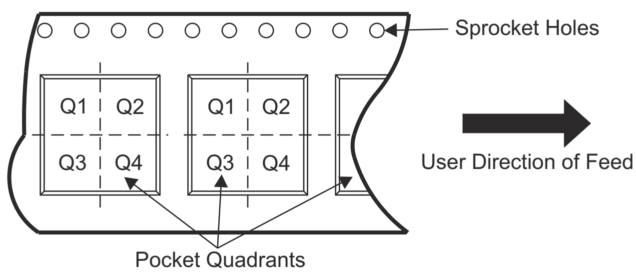



**TAPE DIMENSIONS**



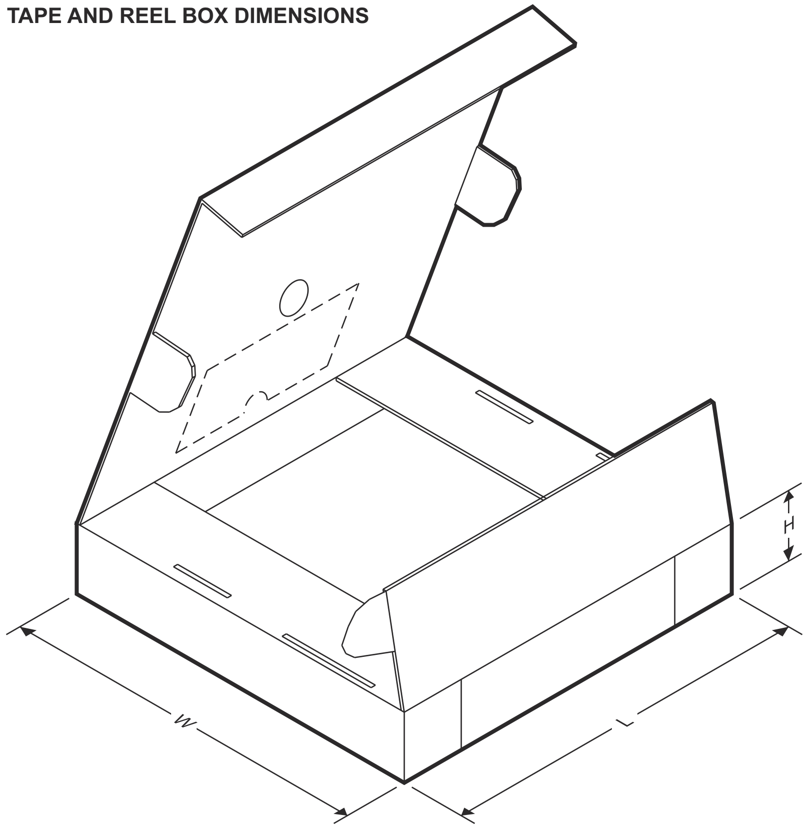

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PSN74UVP1G16DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| PSN74UVP1G16DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| PSN74UVP1G16DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| PSN74UVP1G16DRYR | USON | DRY | 5 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| PSN74UVP1G16DSFR | USON | DSF | 5 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PSN74UVP1G16DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| PSN74UVP1G16DCKR | SC70 | DCK | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| PSN74UVP1G16DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| PSN74UVP1G16DRYR | USON | DRY | 5 | 5000 | 184.0 | 184.0 | 19.0 |
| PSN74UVP1G16DSFR | USON | DSF | 5 | 5000 | 210.0 | 185.0 | 35.0 |

ADVANCE INFORMATION

ADVANCE INFORMATION

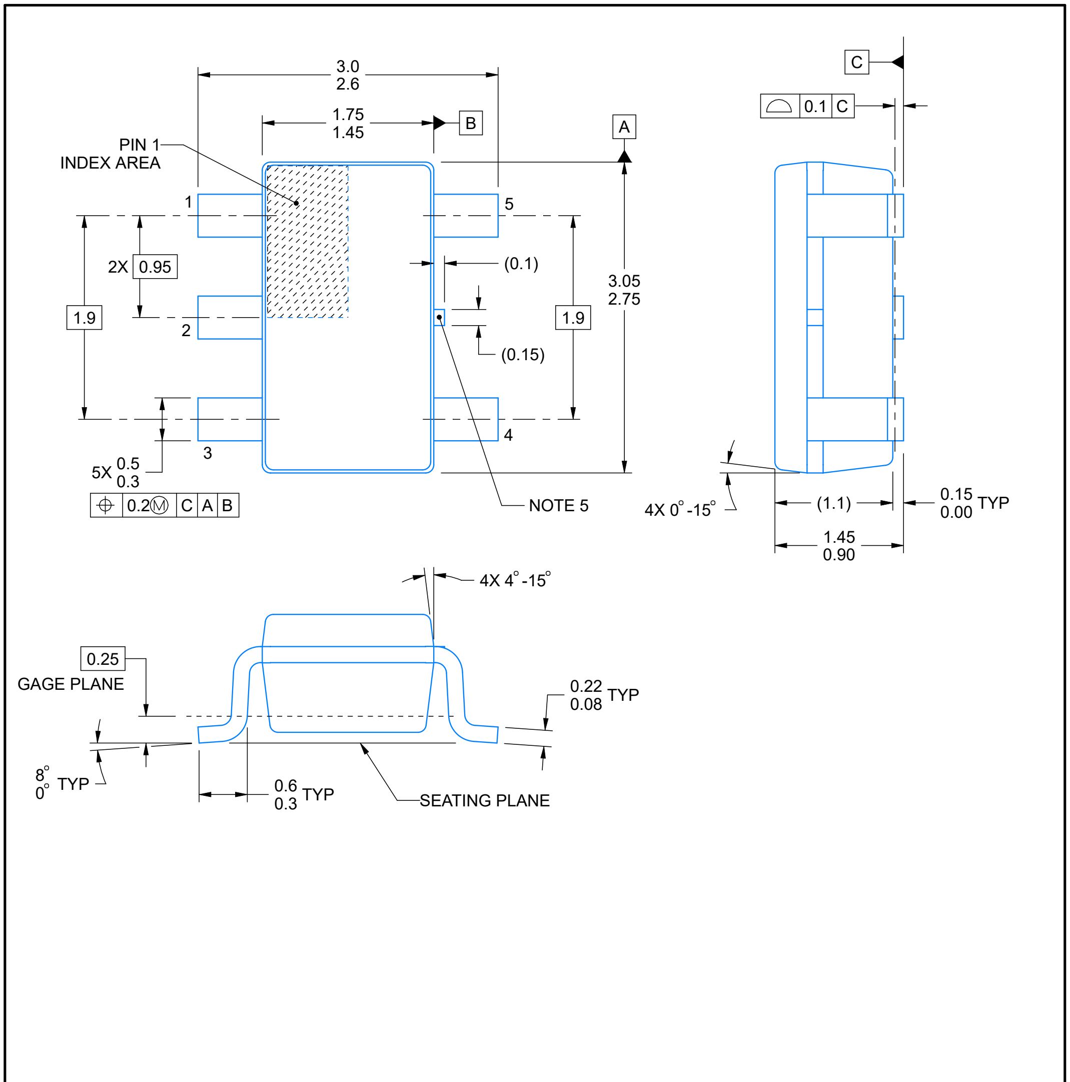
## 13.2 Mechanical Data

**DBV0005A**

**PACKAGE OUTLINE**

**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

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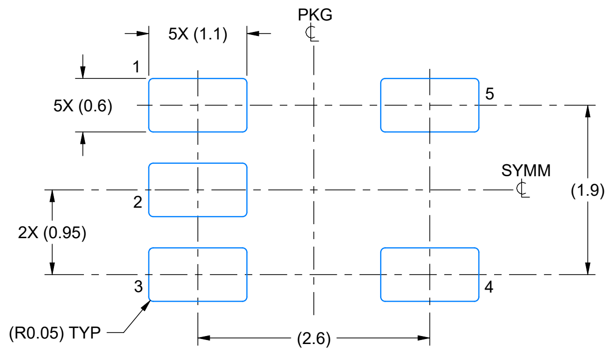
# EXAMPLE BOARD LAYOUT

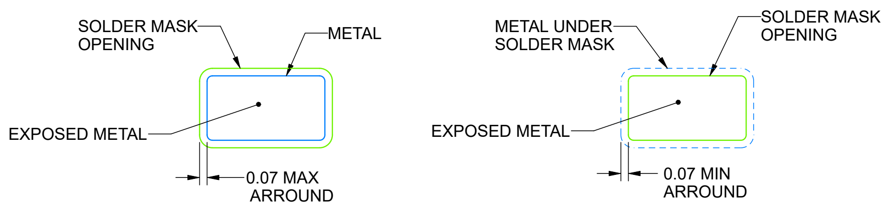
## DBV0005A

**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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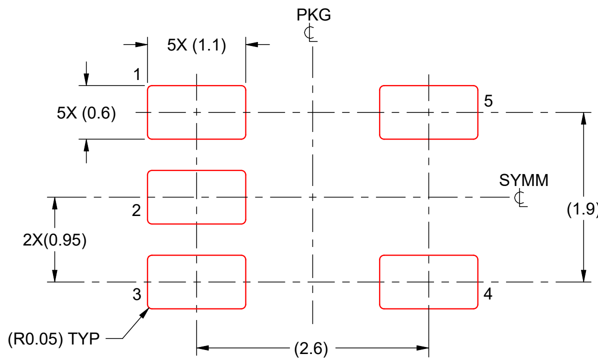
ADVANCE INFORMATION

ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

**DBV0005A** **SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

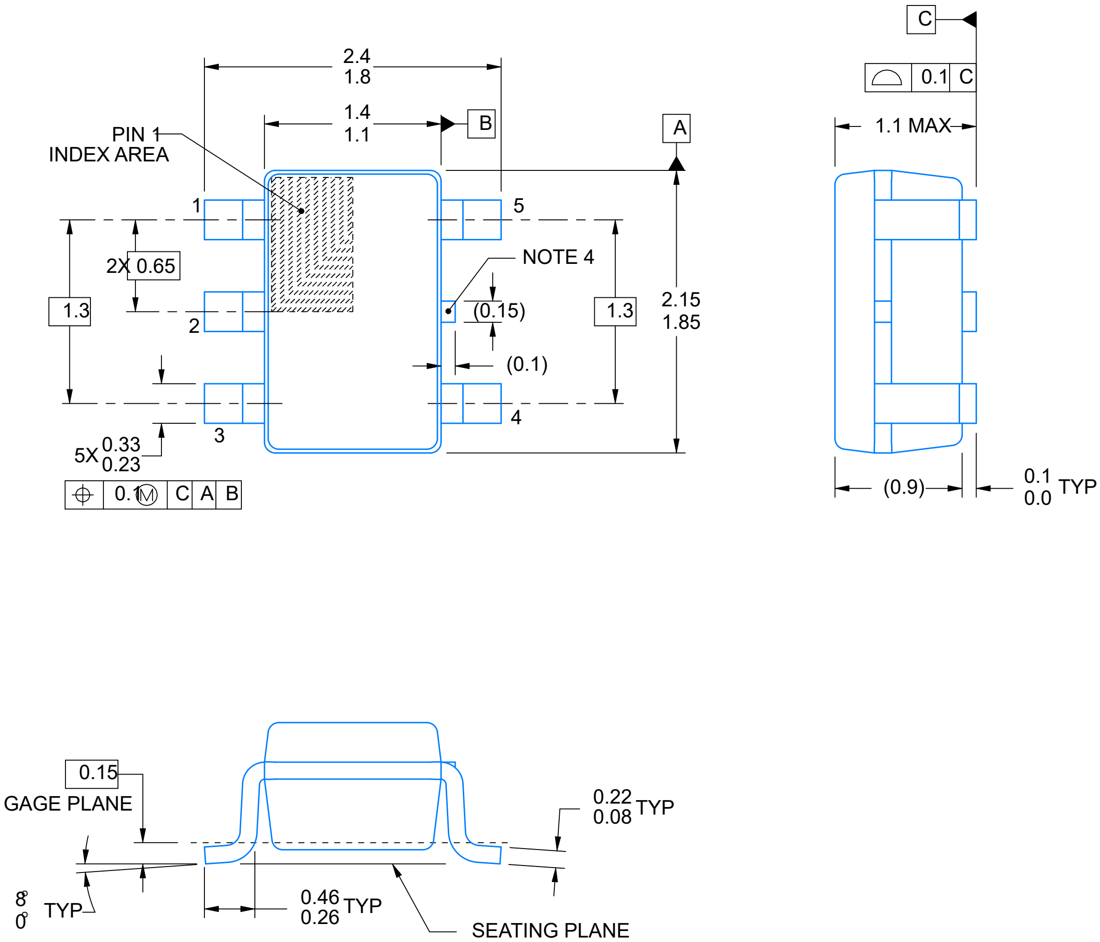
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR




4214834/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dim ensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.

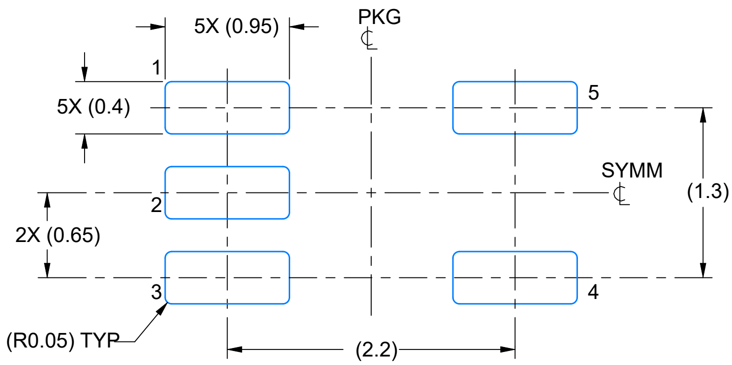
ADVANCE INFORMATION

# EXAMPLE BOARD LAYOUT

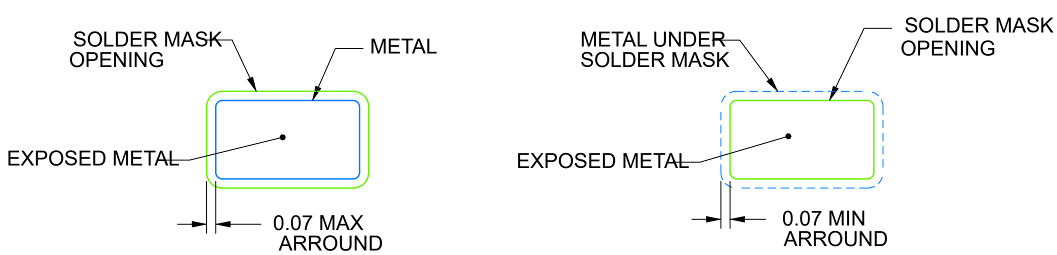
## DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X




NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214834/C 03/2023

NOTES: (continued)

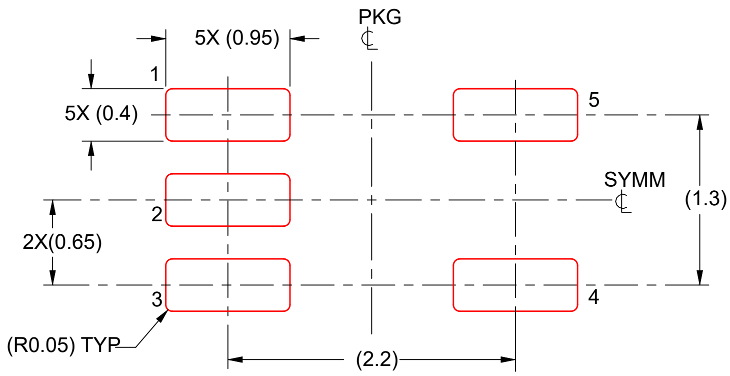
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DCK0005A

## SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/C 03/2023

ADVANCE INFORMATION

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

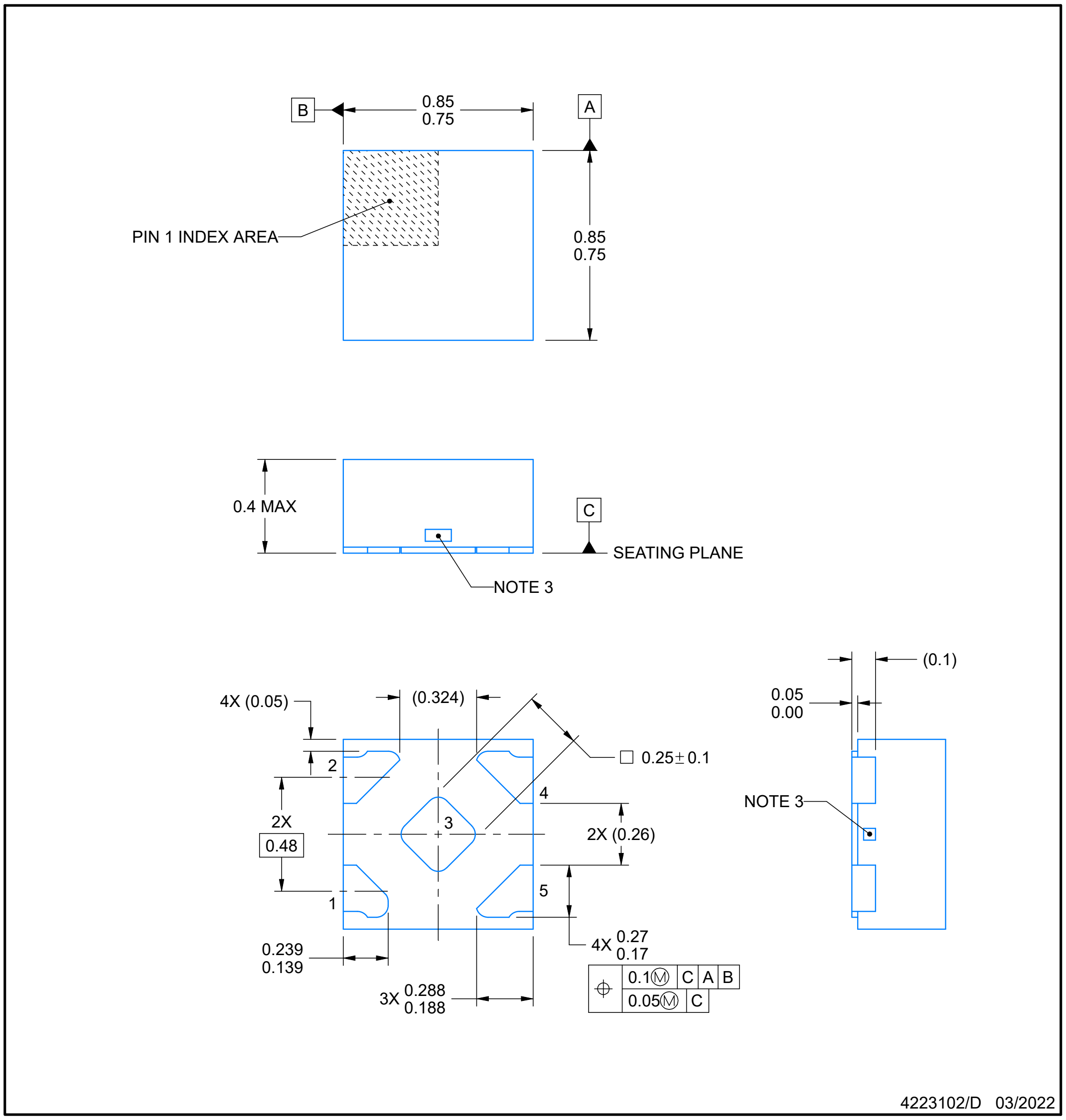
ADVANCE INFORMATION

# PACKAGE OUTLINE

## DPW0005A

**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



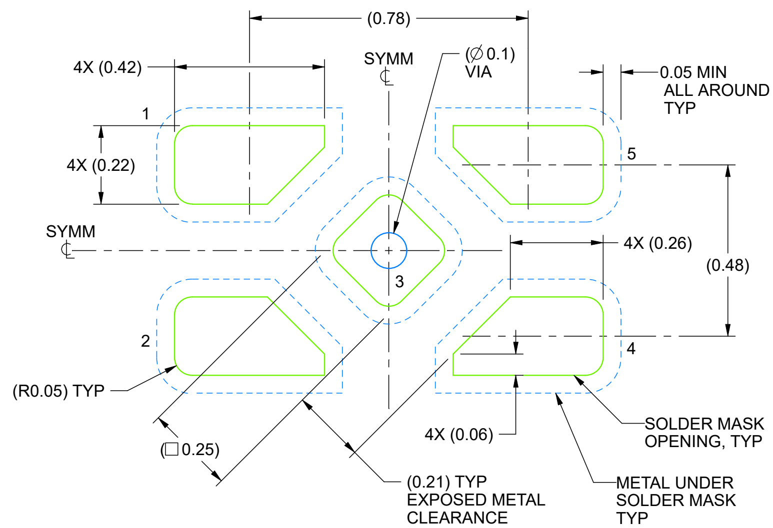

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

# EXAMPLE BOARD LAYOUT

**DPW0005A** **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

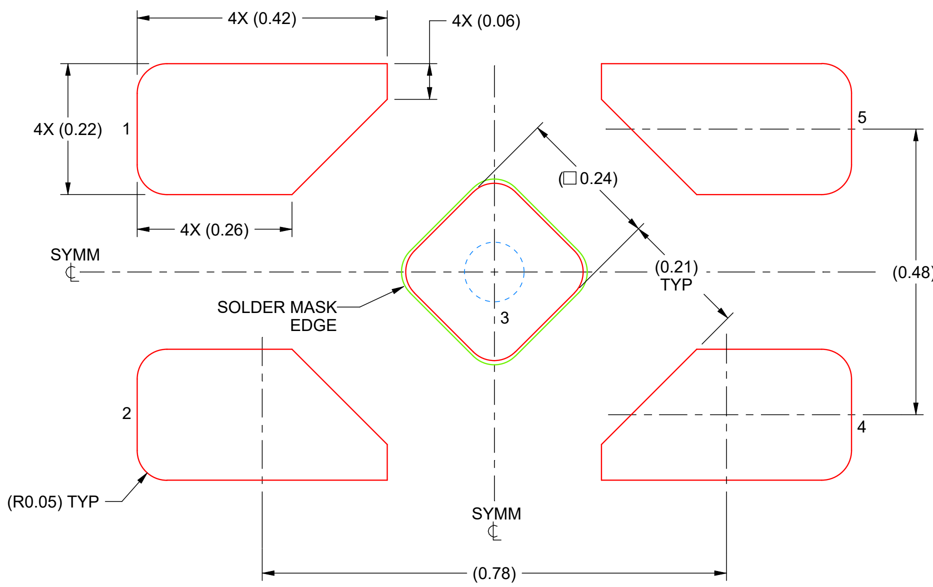
ADVANCE INFORMATION

ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

**DPW0005A** **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

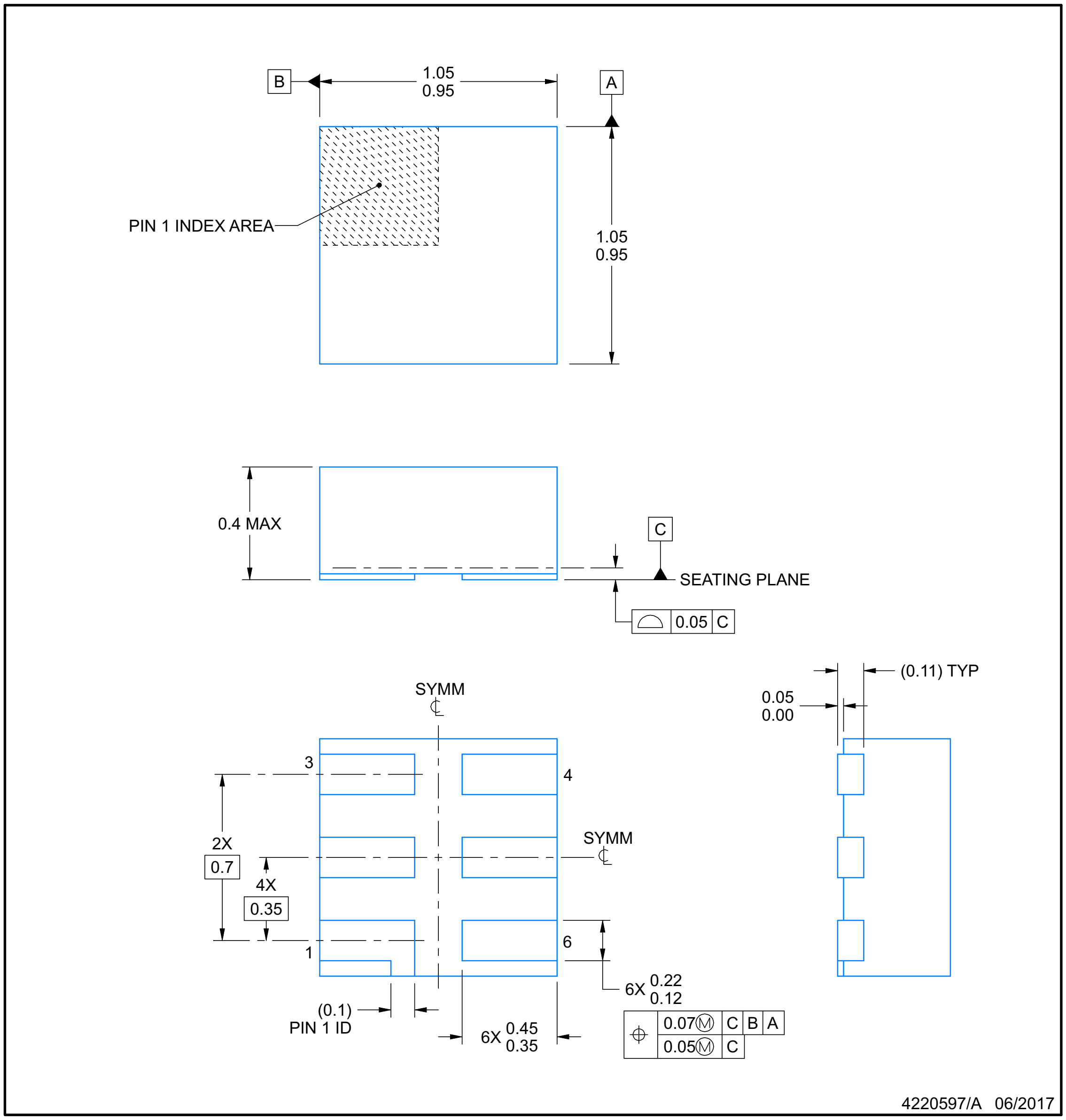
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

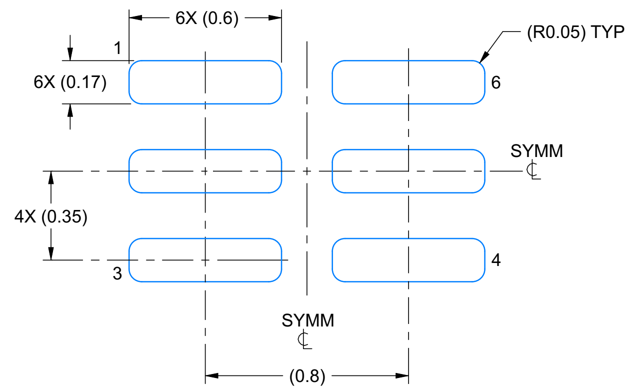
ADVANCE INFORMATION

ADVANCE INFORMATION

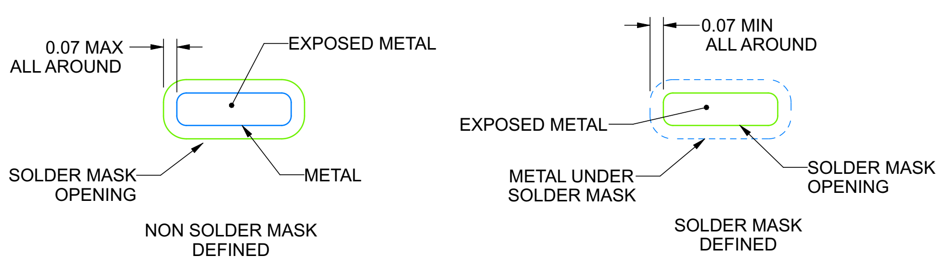
## EXAMPLE BOARD LAYOUT

**DSF0006A** **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

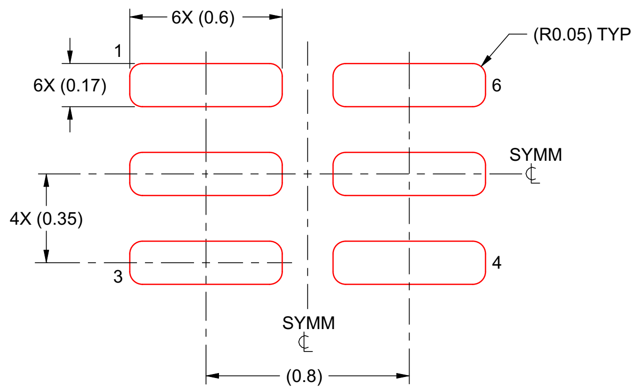
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

## EXAMPLE STENCIL DESIGN

## DSF0006A

**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

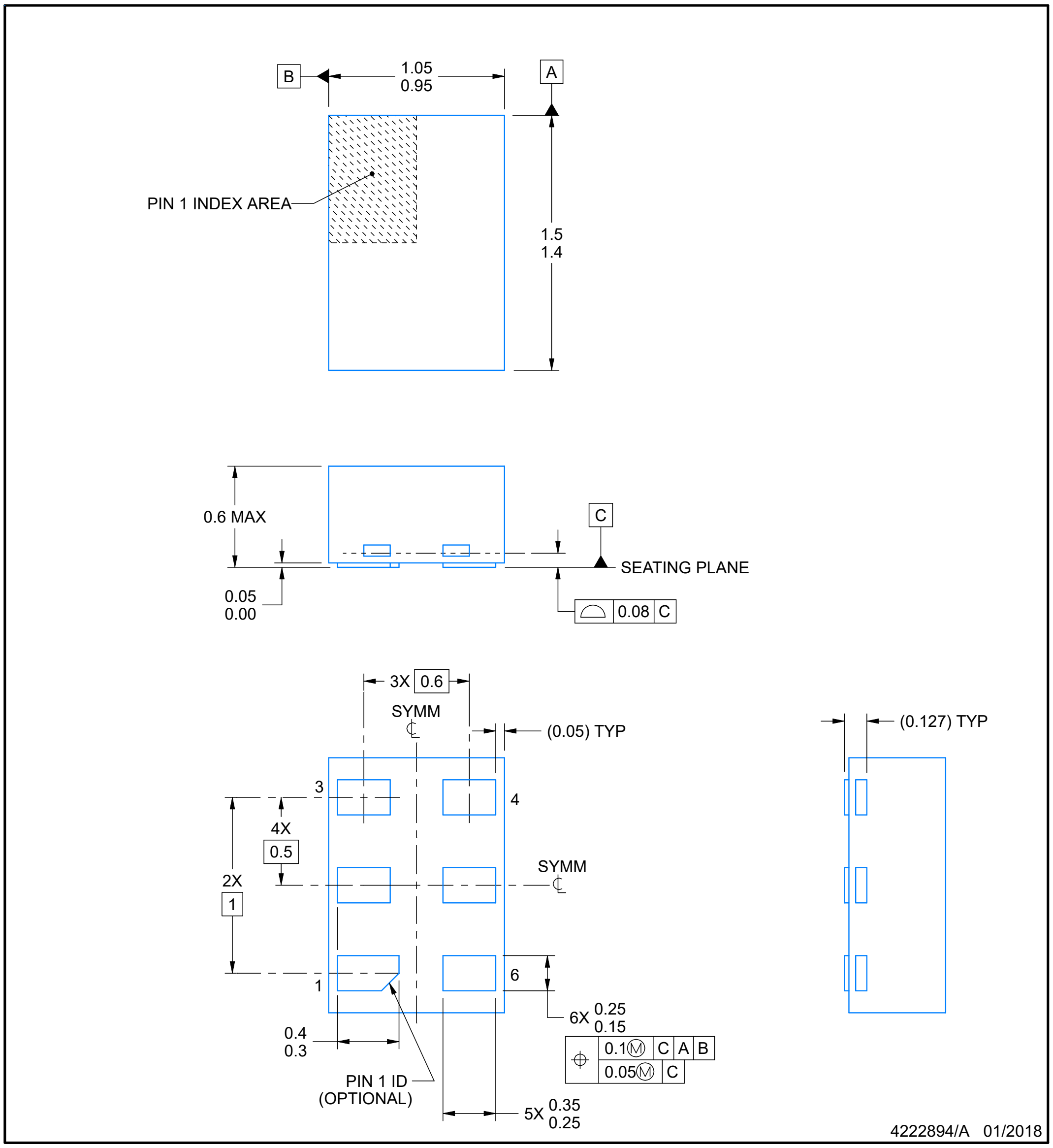
ADVANCE INFORMATION

# PACKAGE OUTLINE

## DRY0006A

### USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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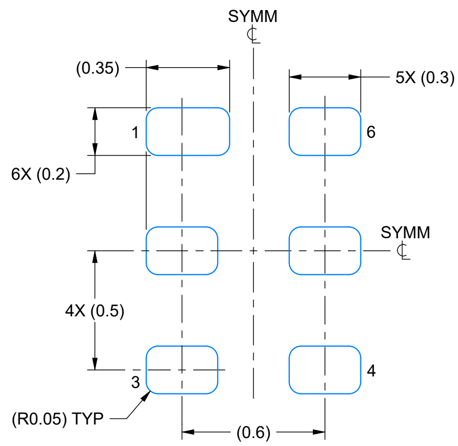
# EXAMPLE BOARD LAYOUT

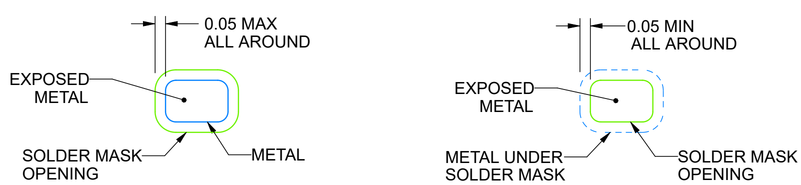
## DRY0006A

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X




NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

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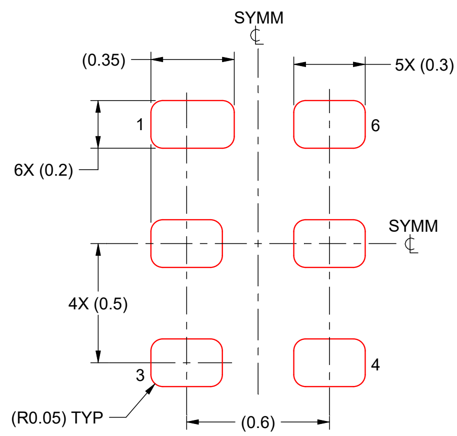
## EXAMPLE STENCIL DESIGN

**DRY0006A** **USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.