SN75172 Quadruple Differential Line Driver

1 Features

- Meets or exceeds the requirements of ANSI standards EIA/TIA-422-B and RS-485 and ITU recommendation V.11
- Designed for multipoint transmission on long bus lines in noisy environments
- 3-state outputs
- Common-mode output voltage range of: –7V to 12V
- Active-high and active-low enables
- Thermal shutdown protection
- Positive- and negative-current limiting
- Operates from single 5V supply
- Logically interchangeable with AM26LS31

2 Applications

- Chemical and gas sensors
- Field transmitters: temperature sensors and pressure sensors
- Motor drives: brushless DC and brushed DC
- Temperature sensors and controllers using modbus

3 Description

The SN75172 is a monolithic quadruple differential line driver with 3-state outputs. Dsigned to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges, making it suitable for party-line applications in noisy environments.

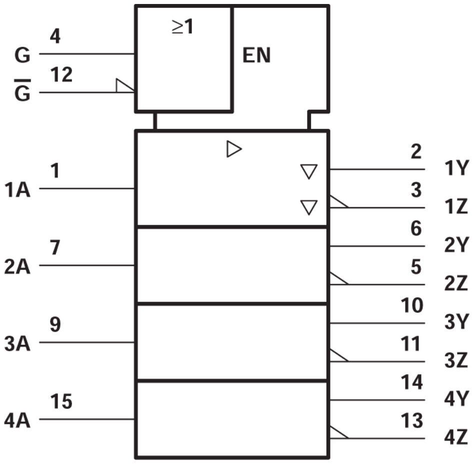
The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from 0°C to 70°C.

Package Information

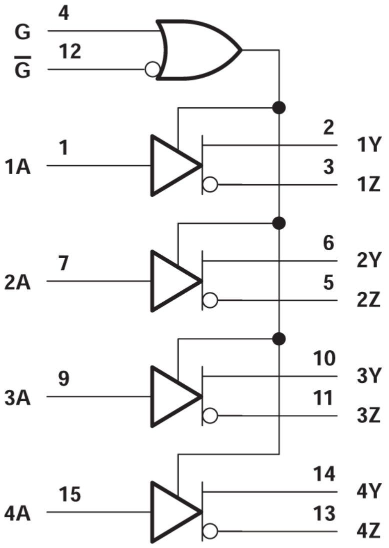
PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
SN75172	N (PDIP, 16)	19.3mm × 9.4mm
	DW (SOIC, 20)	12.8mm × 10.3mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



A. Pin numbers shown are for the N package.

Logic Symbol[1]



Logic Diagram (Positive Logic)

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[1] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Table of Contents

4 Pin Configuration and Functions

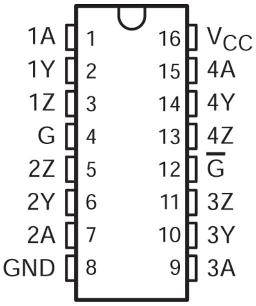
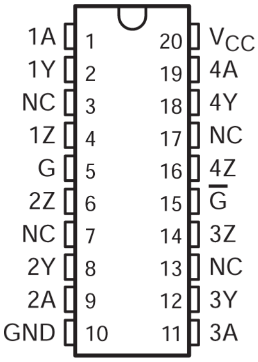


Figure 4-1. N Package (Top View)



NC – No internal connection

Figure 4-2. DW Package (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage, see [2]	-0.3	7	V
V_{BUS}	Voltage range at any bus terminal	–10	15	V
V_I	Input voltage	-0.3	5.5	V
P_D	Continuous total dissipation	See Dissipation Rating Table		
T_A	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	–65	150	°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal.

5.2 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
DW	1125mW	9mW/°C	720mW
N	1150mW	9.2mW/°C	736mW

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}	-7		12	V
High-level output current, I_{OH}			–60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

5.4 Thermal Information

THERMAL METRIC(1)		N (PDIP)	DW	UNIT
		16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	39.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.5	8.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.3	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = ±18mA					±1.5	V
V_O	Output voltage	I_O = 0			0		6	V
V_{OH}	High-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OH} = ±33mA		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2V,	V_{IL} = 0.8V,	I_{OH} = 33mA		1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0			1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100Ω,	See Figure 6-1		1/2 V_{OD1} or 2(2)			V
		R_I = 54Ω,	See Figure 6-1		1.5	1.5	5	V
V_{OD3}	Differential output voltage	See (5)			1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(3)						±0.2	V
V_{OC}	Common-mode output voltage(4)	R_L = 54Ω or 100Ω		See Figure 6-1	-1		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)						±0.2	V
I_O	Output current with power off	V_{CC} = 0	V_O = ±7V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = ±7V to 12V					±100	µA
I_{IH}	High-level input current	V_I = 1.7V					20	µA
I_{IL}	Low-level input current	V_I = 0.5V					±360	µA
I_{OS}	Short-circuit output current	V_O = ±7V					±180	mA
		V_O = V_{CC}					180	
		V_O = 12V					500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			38	60	mA
			Outputs disabled			18	40	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with a 100Ω load is either 1/2 V_{OD1} or 2V, whichever is greater.
(3) $\Delta_{|VOD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5) See Figure 6-3 of EIA Standard RS-485.

Table 5-1. Symbol Equivalents

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o	V_o
$\lvert V_{OD2}\rvert$	V_t (R_L = 100Ω)	V_t (R_L = 54Ω)
$\lvert V_{OD2}\rvert$		V_t (Test Termination Measurement(5))
$\Delta\lvert V_{OD}\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$
V_{OC}	$\lvert V_{os}\rvert$	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	$\lvert I_{sa}\rvert, \lvert I_{sb}\rvert$	
I_O	$\lvert I_{xa}\rvert, \lvert I_{xb}\rvert$	I_{ia}, I_{ib}

5.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54Ω,	See Figure 6-2		45	65	ns
$t_{t(OD)}$	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110Ω,	See Figure 6-3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110Ω,	See Figure 6-4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110Ω,	See Figure 6-3		78	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110Ω,	See Figure 6-4		18	30	ns

5.7 Typical Characteristics

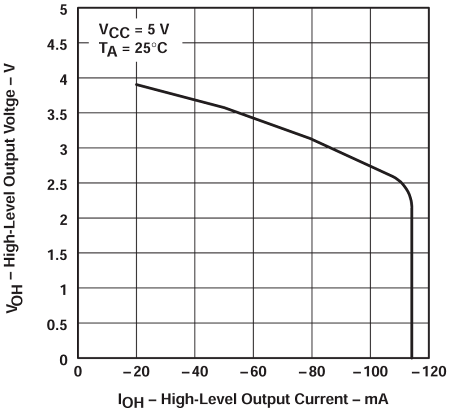


Figure 5-1. High-level Output Voltage vs High-level Output Current

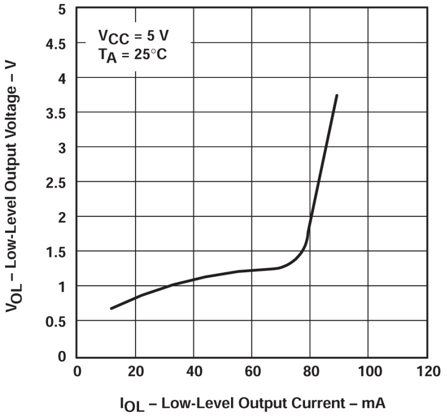


Figure 5-2. Low-level Output Voltage vs Low-level Output Current

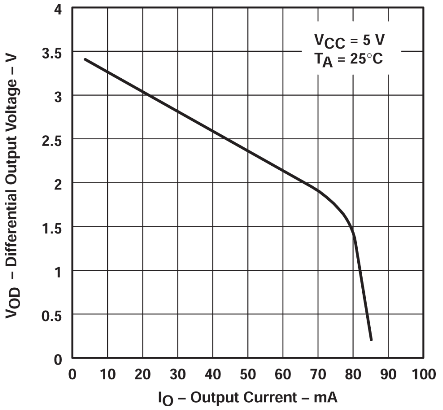


Figure 5-3. Differential Output Voltage vs Output Current

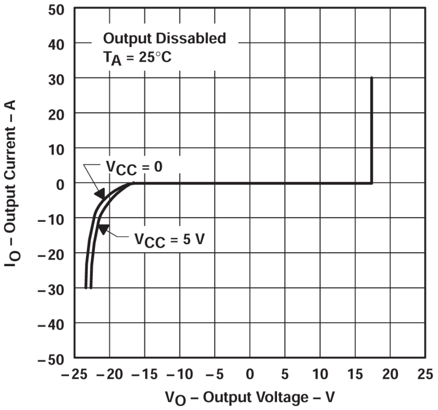


Figure 5-4. Output Current vs Output Voltage

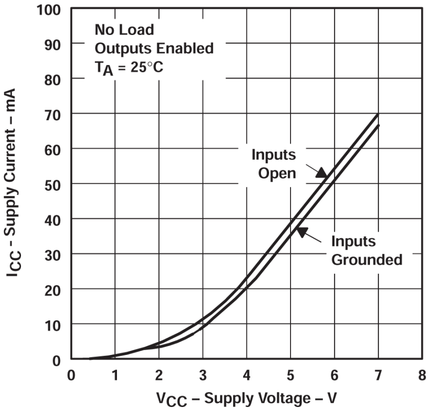


Figure 5-5. Supply Current vs Supply Voltage

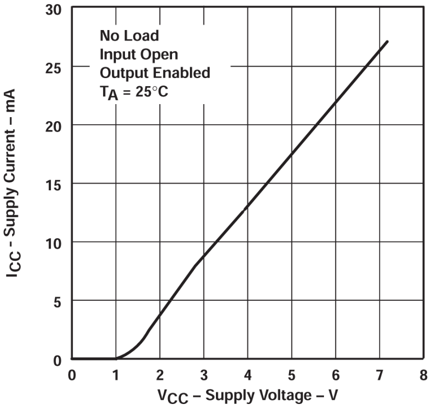


Figure 5-6. Supply Current vs Supply Voltage

6 Parameter Measurement Information

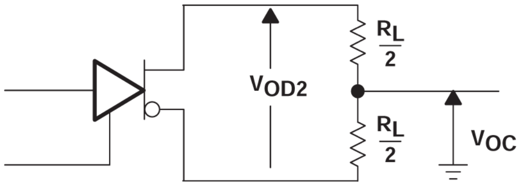
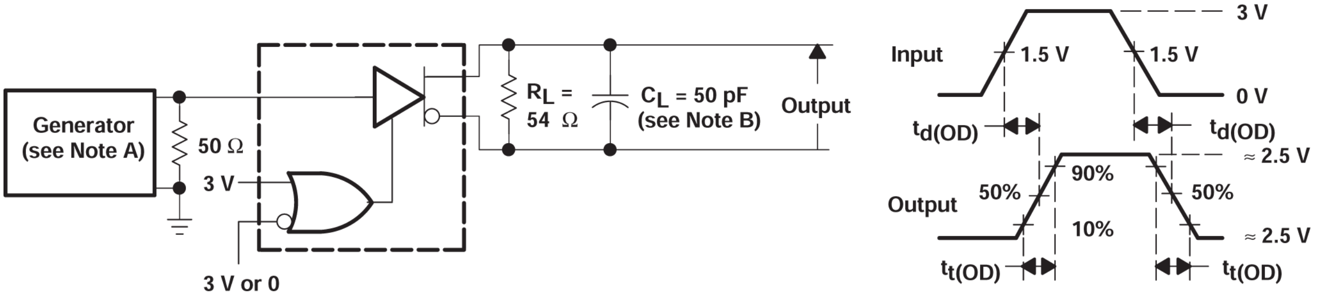


Figure 6-1. Differential and Common-Mode Output Voltages



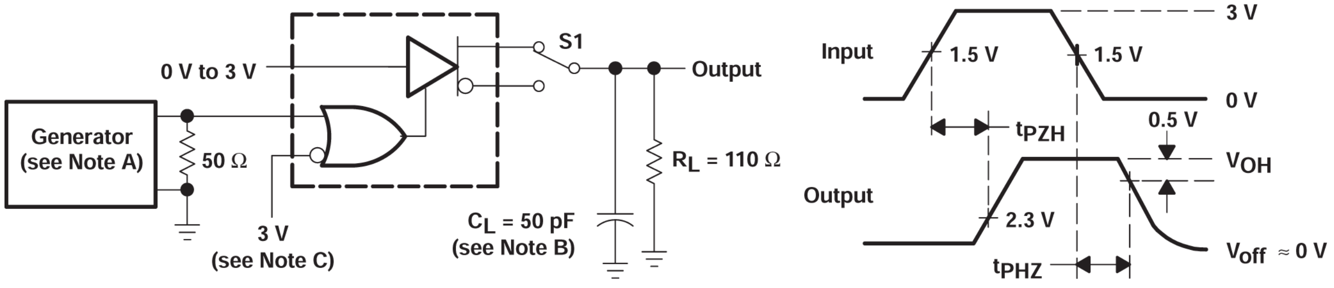
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 10ns, t_f ≤ 10ns, PRR ≤ 1MHz, duty cycle = 50%, Z_O = 50Ω.

B. C_L includes probe and stray capacitance.

Figure 6-2. Differential-Output Test Circuit and Voltage Waveforms



TEST CIRCUIT

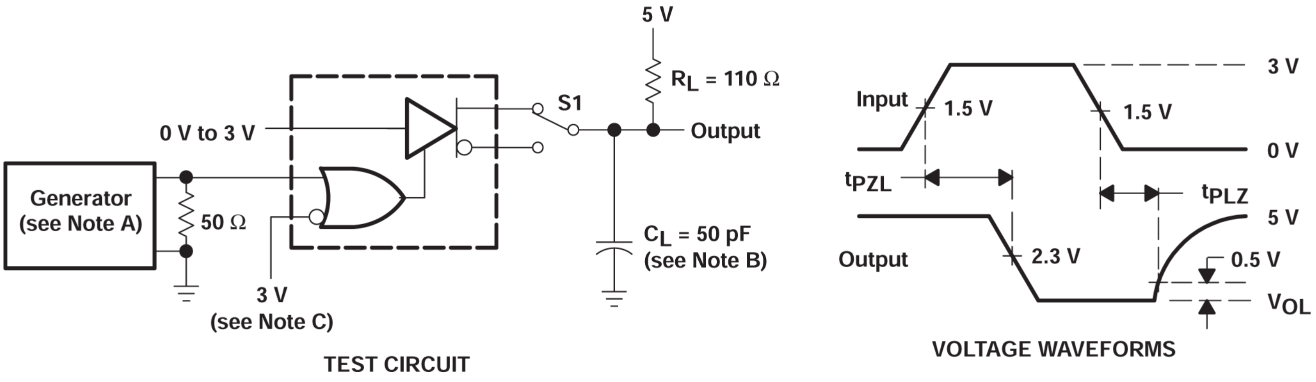
VOLTAGE WAVEFORMS

A. A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle = 50%, t_r ≤ 10ns, t_f ≤ 10ns, Z_O = 50Ω.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 6-3. Test Circuit and Voltage Waveforms



A. A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle = 50%, t_r ≤ 5ns, t_f ≤ 5ns, Z_O = 50Ω.

B. C_L includes probe and stray capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 6-4. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Device Functional Modes

Function Table (Each Driver)

INPUT A(1)	**ENABLES**		**OUTPUTS**	
	G	**$\overline{G}$**	**Y**	**Z**
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

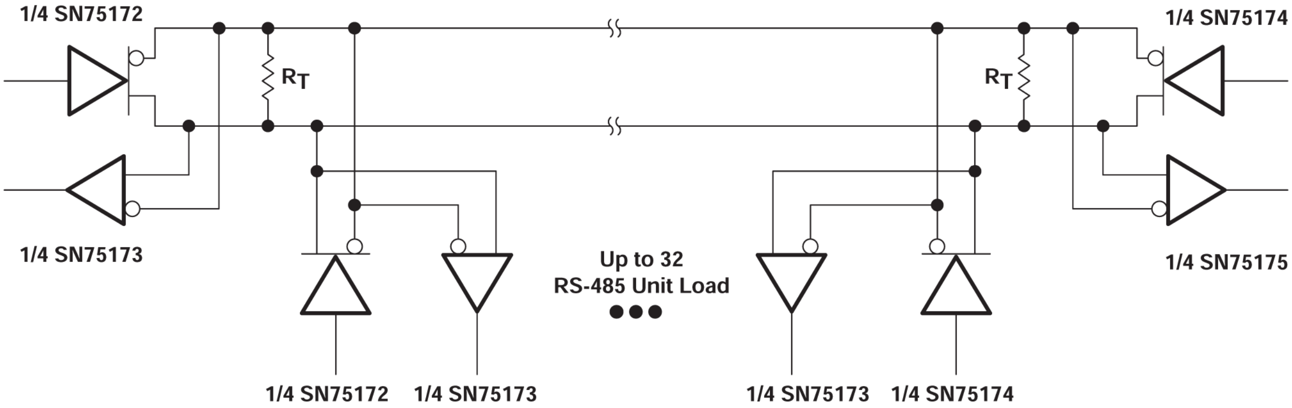
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information



A. The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 1995) to Revision C (April 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Thermal Information* table	5
• Changed Note A in Figure 6-2 and Figure 6-3	8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75172DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	SN75172
SN75172DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172
SN75172DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75172
SN75172N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75172N
SN75172N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75172N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

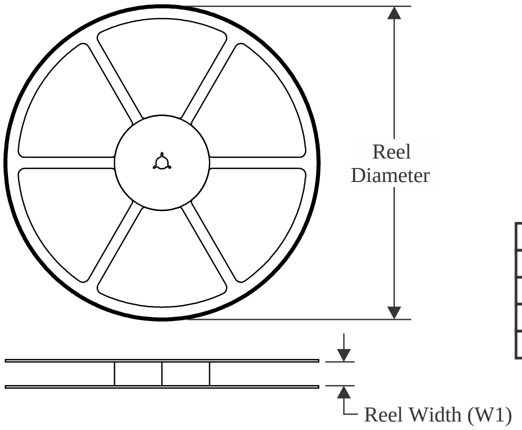
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

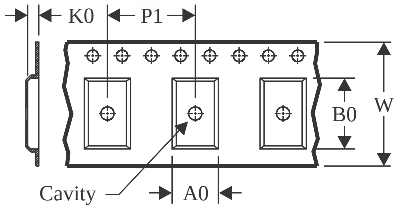
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

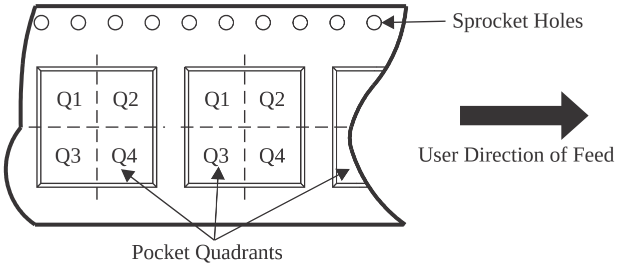


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

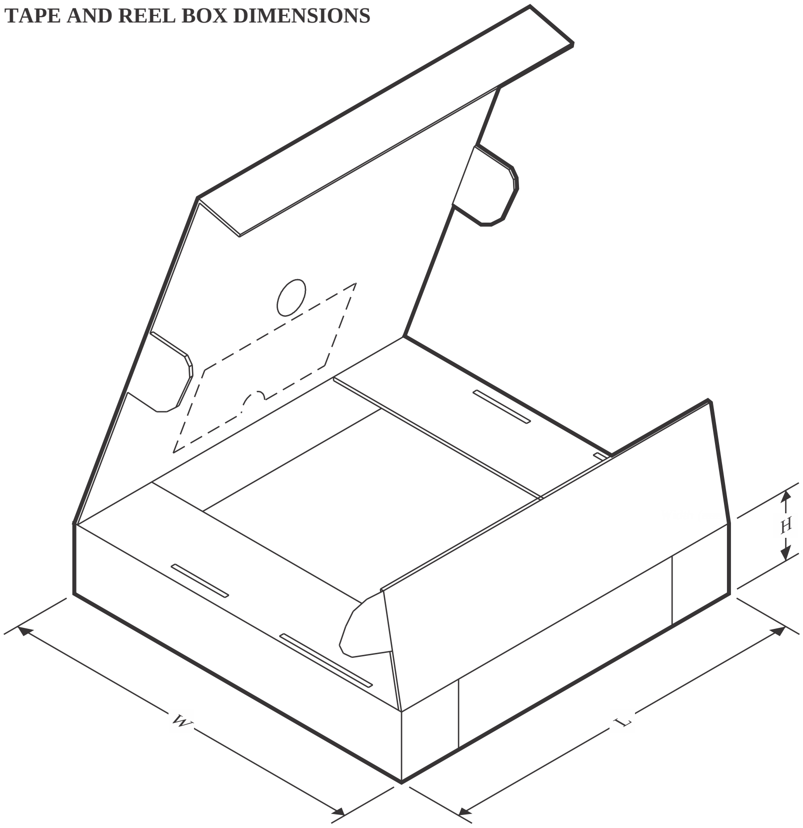
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

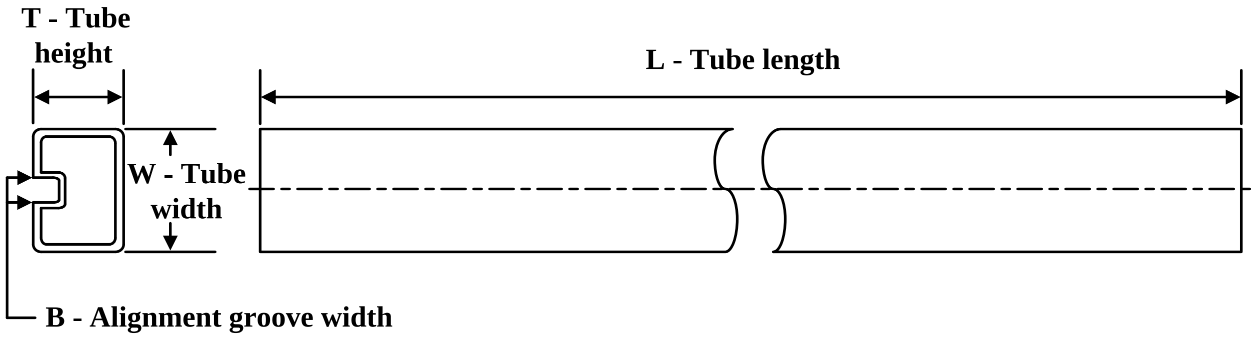
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75172DWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



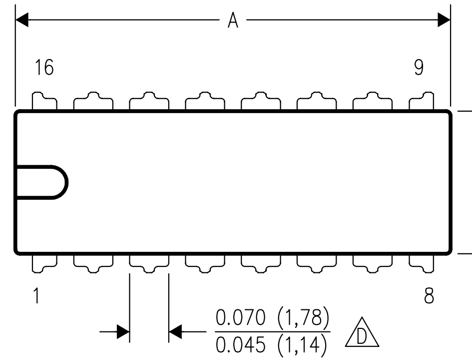
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75172N	N	PDIP	16	25	506	13.97	11230	4.32
SN75172N.A	N	PDIP	16	25	506	13.97	11230	4.32

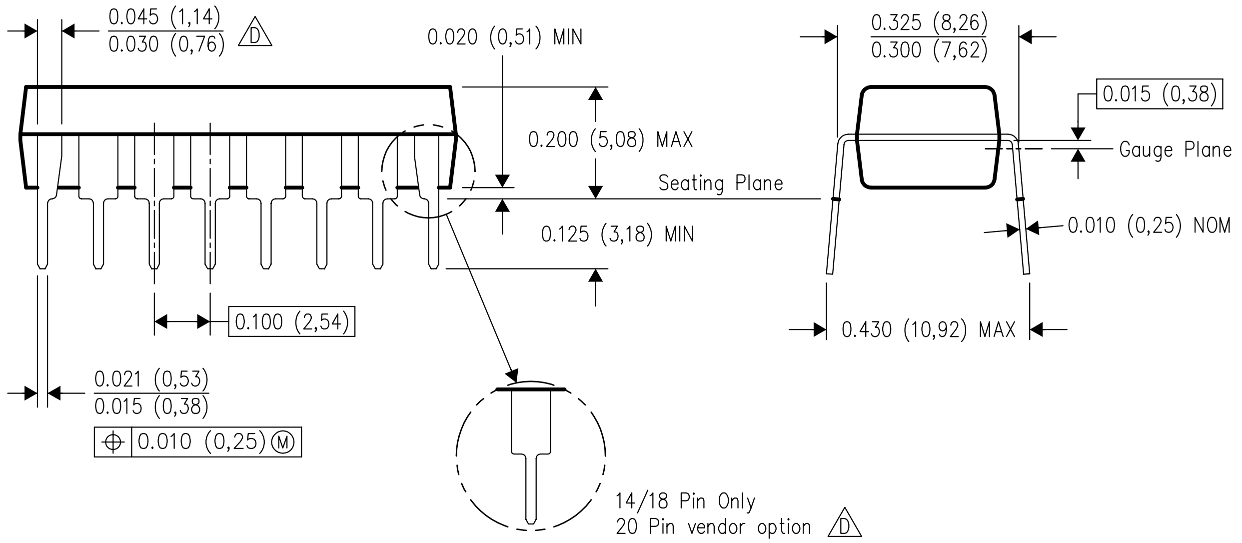
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
C MS–001 VARIATION	AA	BB	AC	AD



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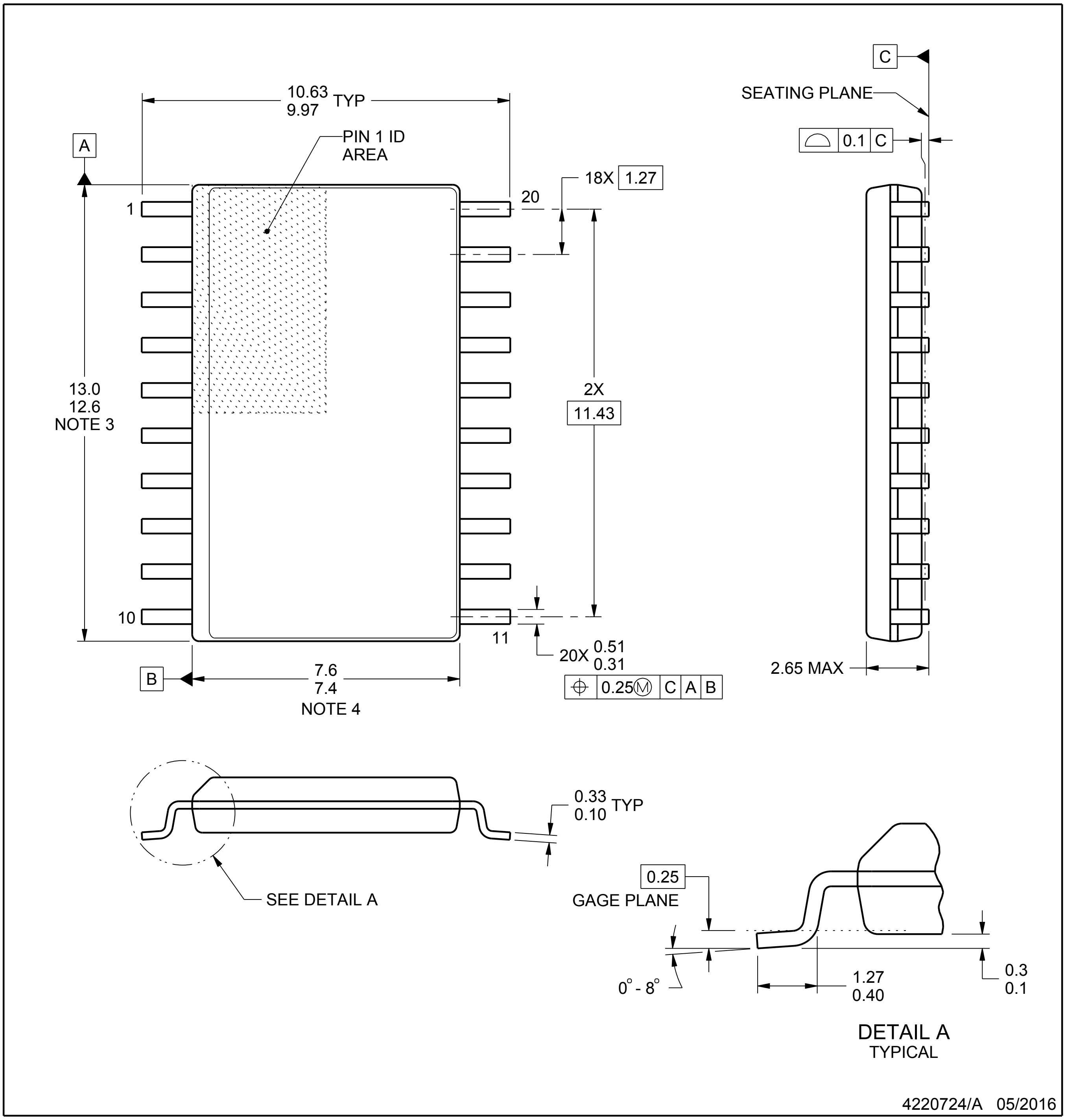
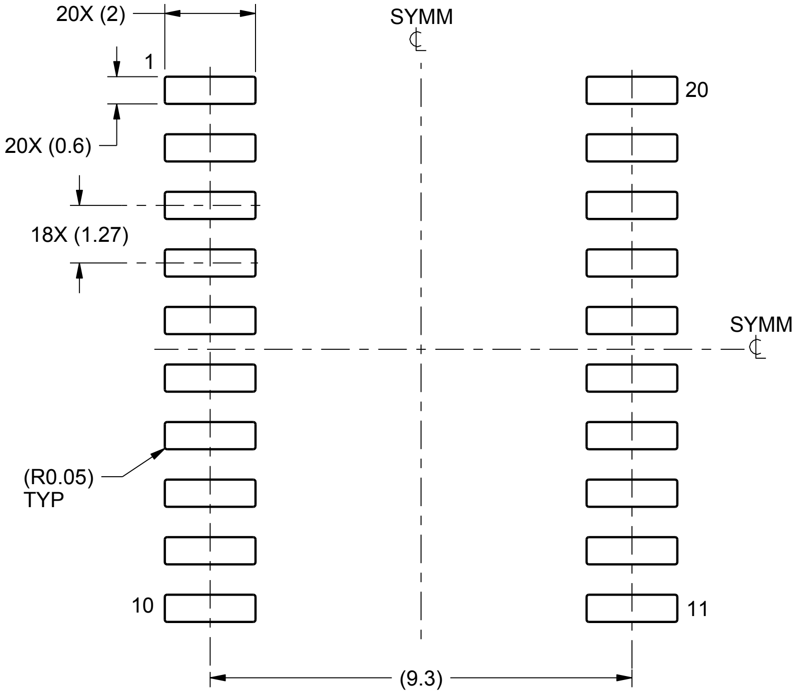
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

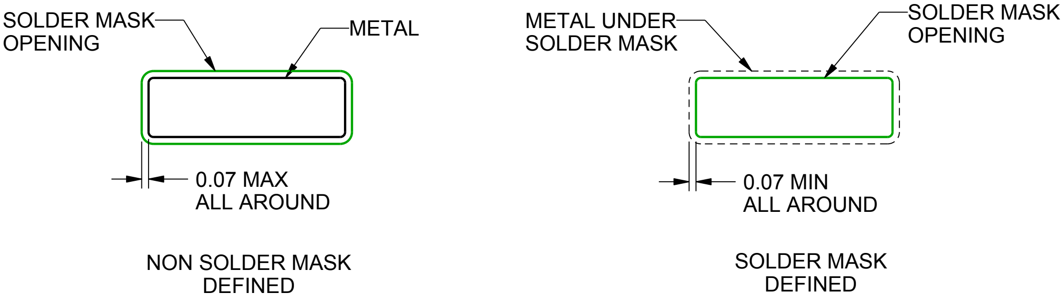


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

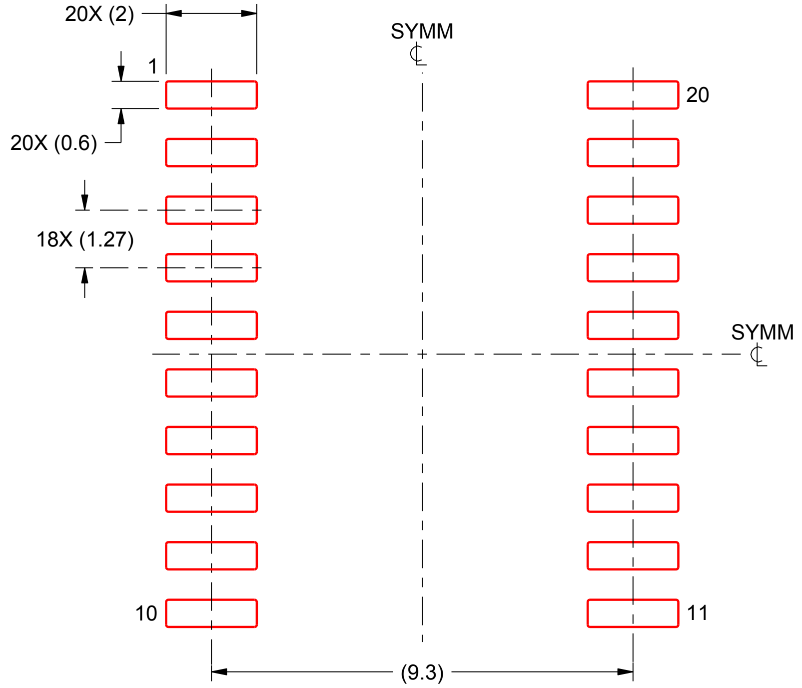


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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