SNx5ALS180 Differential Driver and Receiver Pairs

1 Features

- Meet or exceed the requirements of TIA/EIA-422-B, TIA/EIA-485-A[1] and ITU recommendation V.11
- High-speed advanced low-power Schottky circuitry
- Designed for 25-Mbaud operation in both serial and parallel applications
- Low skew between devices: 6 ns max
- Low supply-current requirements: 30 mA max
- Individual driver and receiver I/O pins with dual V_{CC} and dual GND
- Wide positive and negative input/output bus voltage ranges
- Driver output capacity: ±60 mA
- Thermal shutdown protection
- Driver positive- and negative-current limiting
- Receiver input impedance: 12 kΩ min
- Receiver input sensitivity: ±200 mV max
- Receiver input hysteresis: 60 mV typ
- Operate from a single 5-V supply
- Glitch-free power-up and power-down protection

2 Description

The SN65ALS180 and SN75ALS180 differential driver and receiver pairs are integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The devices are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11.

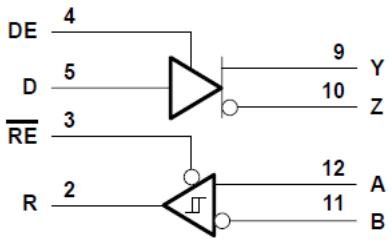
The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

These ports feature wide positive and negative common-mode voltage ranges, making the device an excellent choice for party-line applications.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SNx5ALS176	D (SOIC)	8.65 mm x 3.91 mm
	N (PDIP)	19.3 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

[1] Thes edevices meet or exceed the requirements of TIA/EIA-485-A, except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are –6 V to 8 V for the SN75ALS180 and –4 V to 8 V for the SN65ALS180.

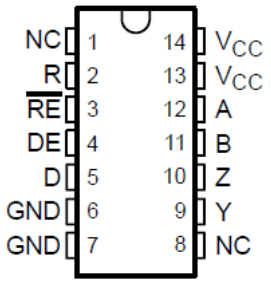
Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2003) to Revision H (January 2023)	Page
• Changed the document to the latest TI format	1
• Deleted the Package thermal impedance from the *Absolute Maximum Ratings*	4
• Added the *Thermal Information* table	4
• Changed the *Typical Characteristics* graphs	8

4 Pin Configuration and Functions



NC – No internal connection

Figure 4-1. SN65ALS180 D Package
SN75ALS180 D or N Package
(Top View)

Table 4-1. Pin Functions

NO	Name	Type	Description
1	NC	-	No Internal connection
2	R	O	Receive data output
3	$\overline{RE}$	I	Receiver enable, active low
4	DE	I	Driver enable, active high
5	D	I	Driver data input
6, 7	GND	GND	Device ground
8	NC	-	No Internal connection
9	Y	O	Digital bus output, Y (Complementary to Z)
10	Z	O	Digital bus output, Z (Complementary to Y)
11	A	I	Bus input, A (complementary to B)
12	B	I	Bus input, B (complementary to A)
13, 14	V_{CC}	SUPPLY	4.75V to 5.25V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	-10	15	V
V_I	Enable input voltage		5.5	V
T_J	Operating virtual junction temperature		150	℃
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	℃
T_{stg}	Storage temperature range	-65	150	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)				12	V
					–7	
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature	SN65ALS180	–40		85	°C
		SN75ALS180	0		70	

(1) Differential-input/output bus voltage is measured at the noninverting terminal, A/Y, with respect to the inverting terminal, B/Z.

5.3 Thermal Information

THERMAL METRIC(1)		N (PDIP)	D (SOIC) (SN65 Devices)	D (SOIC) (SN75 Devices)	UNIT
		14-Pins	14-Pins	14-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	93.2	83.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	40	47.5	39.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	49.4	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	11.2	7.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	48.9	39.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See Figure 6-1	$1/2V_{OD1}$ or 2[3]			V
		R_L = 54 Ω	See Figure 6-1	1.5	2.5	5	
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See Figure 6-2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage[4]	R_L = 54 Ω or 100 Ω	See Figure 6-1			±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω	See Figure 6-1			3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage[4]	R_L = 54 Ω or 100 Ω	See Figure 6-1			±0.2	V
I_O	Output current	Output disabled[6]	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current[5]	V_O = –6 V	SN75ALS180			–250	mA
		V_O = –4 V	SN65ALS180			–250	
		V_O = 0	All			–150	
		V_O = V_{CC}	All			250	
		V_O = 8 V	All			250	
I_{CC}	Supply current	No load	Driver outputs enabled, Receiver disabled		25	30	mA
			Outputs disabled		19	26	

(1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
(4) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(5) Duration of the short circuit should not exceed one second for this test.
(6) This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω	C_L = 50 pF,	See Figure 6-3	3	8	13	ns
	Pulse skew ($\|t_{d(ODH)} - t_{d(ODL)}\|$)	R_L = 54 Ω	C_L = 50 pF,	See Figure 6-3		1	6	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω	C_L = 50 pF,	See Figure 6-3	3	8	13	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω	See Figure 6-4			23	50	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω	See Figure 6-5			19	24	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω	See Figure 6-4			8	13	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω	See Figure 6-5			8	13	ns

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.6 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, Vo_b
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	$V_t(R_L = 100\ \Omega)$	$V_t(R_L = 54\ \Omega)$
$\|V_{OD3}\|$		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|V_t\|\|$	$\|\|V_t\| - \|V_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - V_{os}\|$	$\|V_{os} - V_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

5.7 Electrical Characteristics - Receivers

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+}– $V_{IT–}$)					60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –400 µA,	See Figure 6-6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA,	See Figure 6-6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	µA
I_I	Line input current	Other input = 0 V(3)	V_I = 12 V				1	mA
			V_I = –7 V				–0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	mA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					–100	mA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0		–15		–85	mA
I_{CC}	Supply current	No load	Receiver outputs enabled, Driver inputs disabled			19	30	mA
			Outputs disabled			19	26	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.8 Switching Characteristics - Receivers

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 6-7	C_L = 15 pF,	9	14	19	ns
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 6-7	C_L = 15 pF,	9	14	19	ns
	Skew ($\lvert t_{PHL} – t_{PLH} \rvert$)	V_{ID} = –1.5 V to 1.5 V, See Figure 6-7	C_L = 15 pF,		2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 6-8		7	14	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 6-8		7	14	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 6-8		20	35	ns
t_{PLZ}	Output disable time from low level	C_L= 15 pF,	See Figure 6-8		8	17	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.9 Typical Characteristics

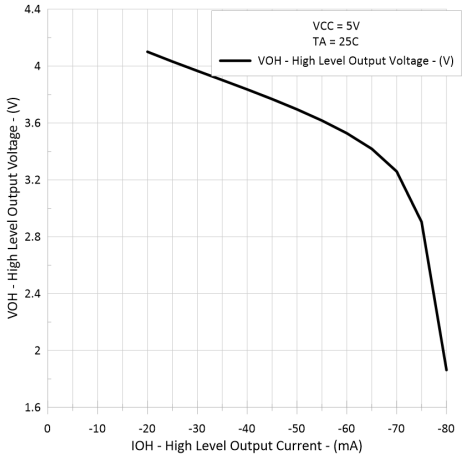


Figure 5-1. Drivers High-Level Output Voltage vs High-Level Output Voltage

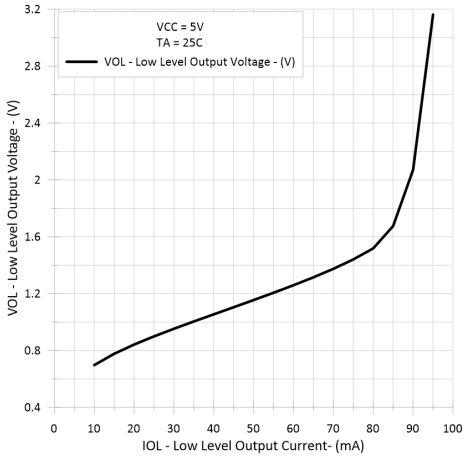


Figure 5-2. Drivers Low-Level Output Voltage vs Low-Level Output Current

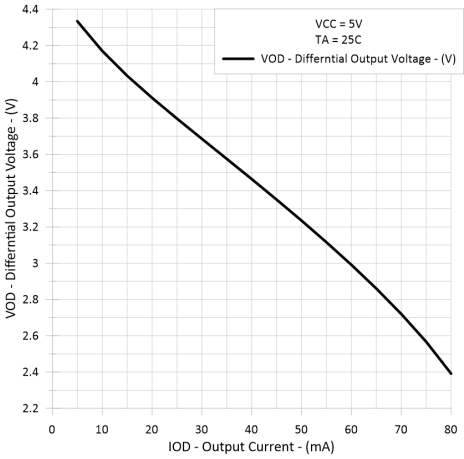


Figure 5-3. Drivers Differential Output Voltage vs Output Current

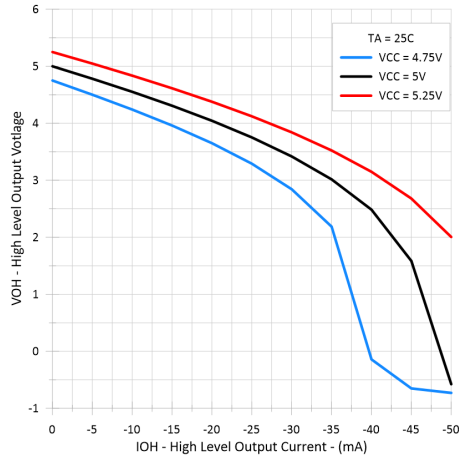


Figure 5-4. Receivers High-Level Output Voltage vs High-Level Output Current

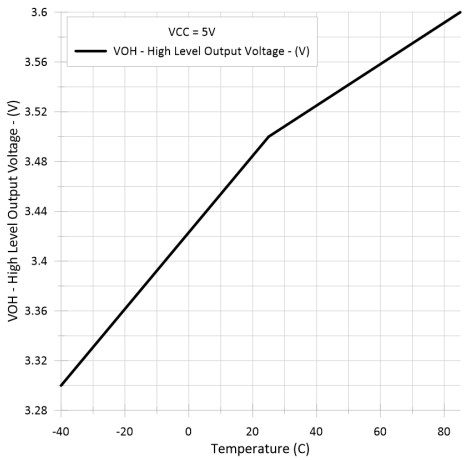


Figure 5-5. Receivers High-Level Output Voltage vs Free-Air Temperature

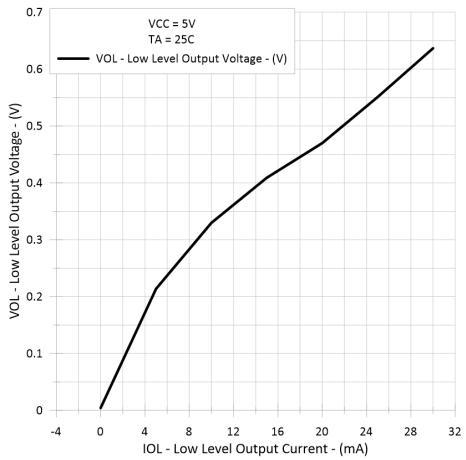


Figure 5-6. Receivers Low-Level Output Voltage vs Low-Level Output Current

5.9 Typical Characteristics (continued)

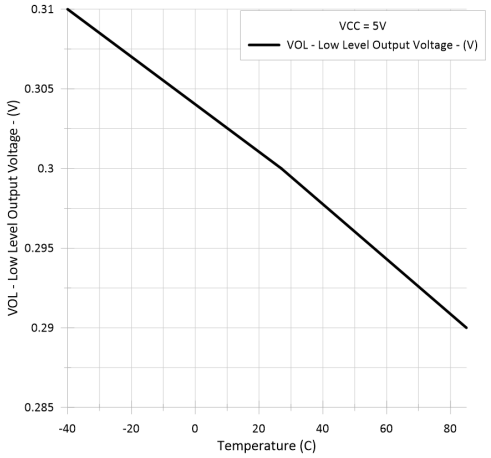


Figure 5-7. Receivers Low-Level Output Voltage vs Free-Air Temperature

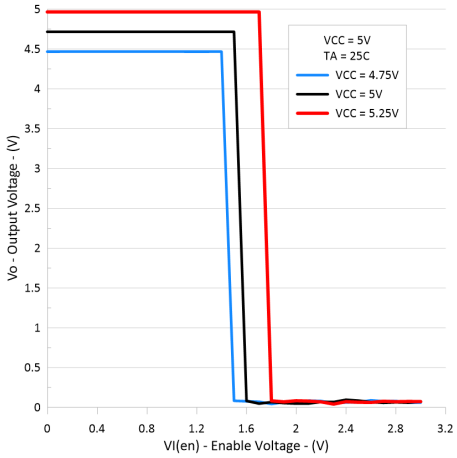


Figure 5-8. Receivers Output Voltage vs Enable Voltage

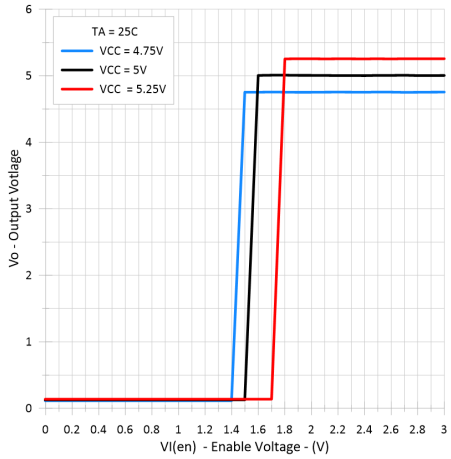


Figure 5-9. Receivers Output Voltage vs Enable Voltage

6 Parameter Measurement Information

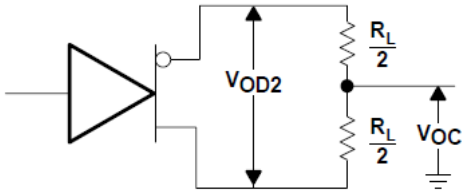


Figure 6-1. Driver V_{OD} and V_{OC}

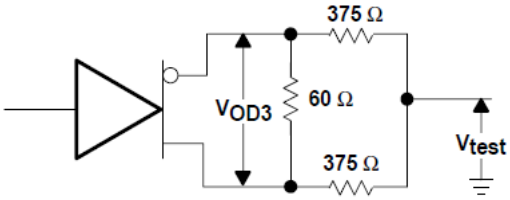
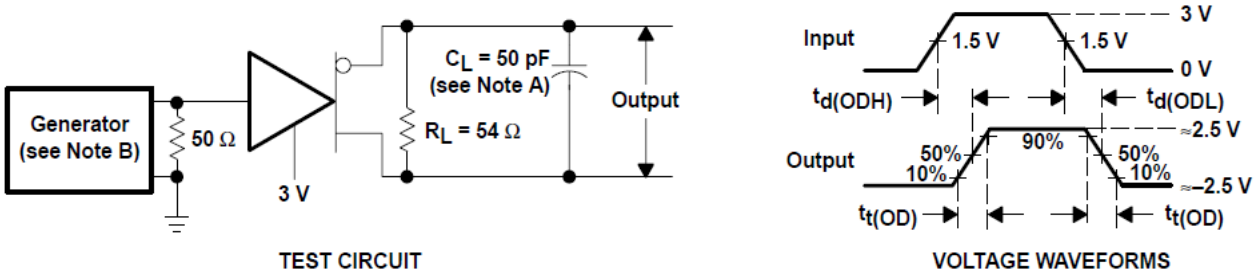
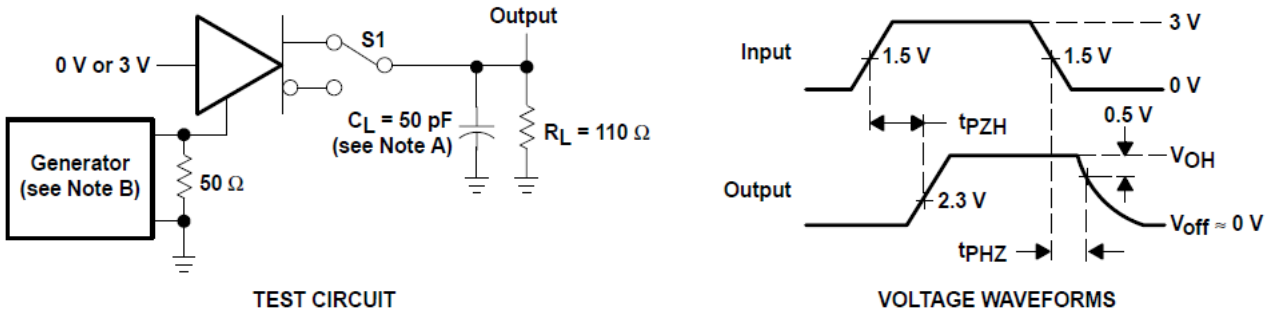


Figure 6-2. Driver V_{OD3}



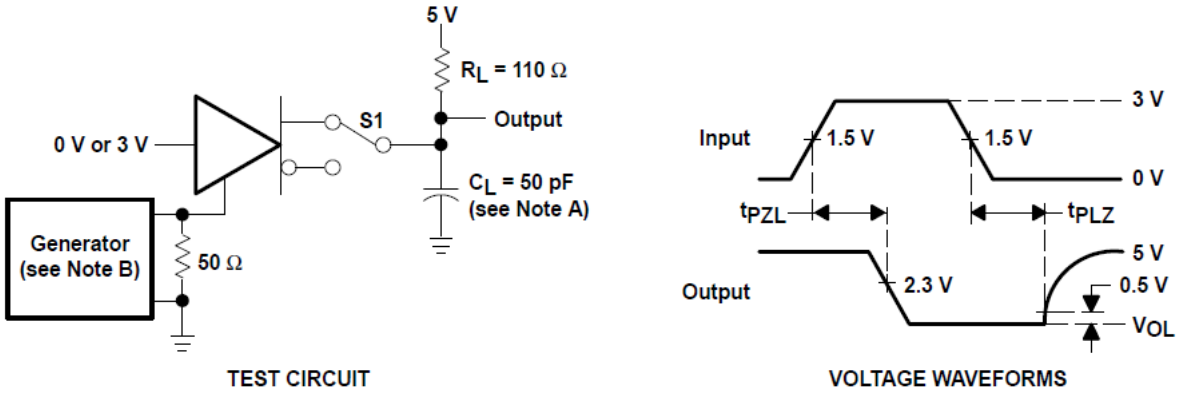
A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

Figure 6-3. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

Figure 6-4. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

Figure 6-5. Driver Test Circuit and Voltage Waveforms

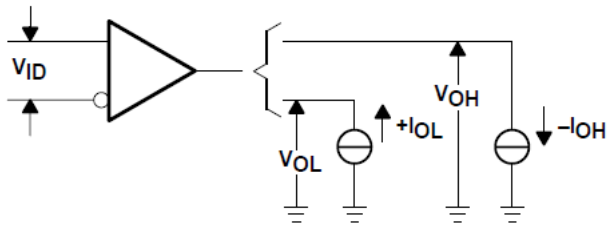
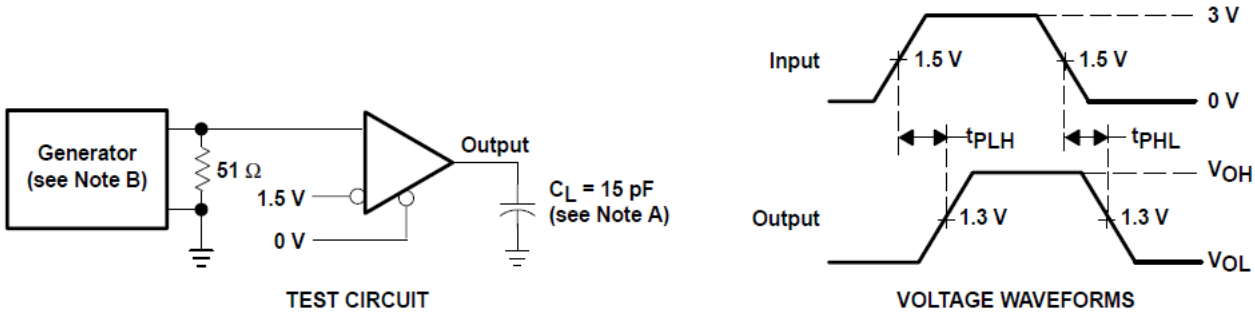
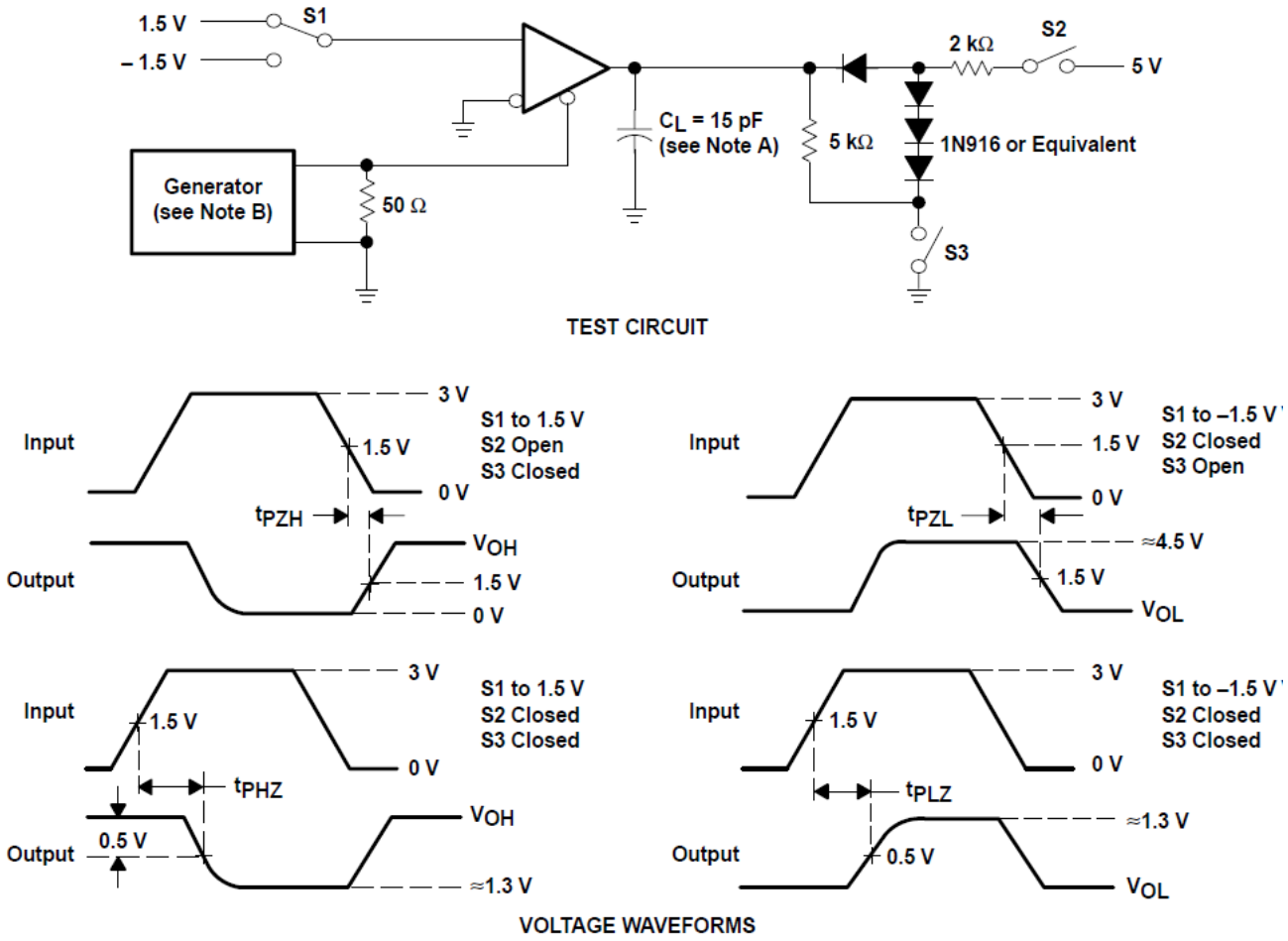


Figure 6-6. Receiver V_{OH} and V_{OL}



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

Figure 6-7. Receiver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r≤ 6 ns, t_f ≤ 6ns, Z_O = 50 Ω.

Figure 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

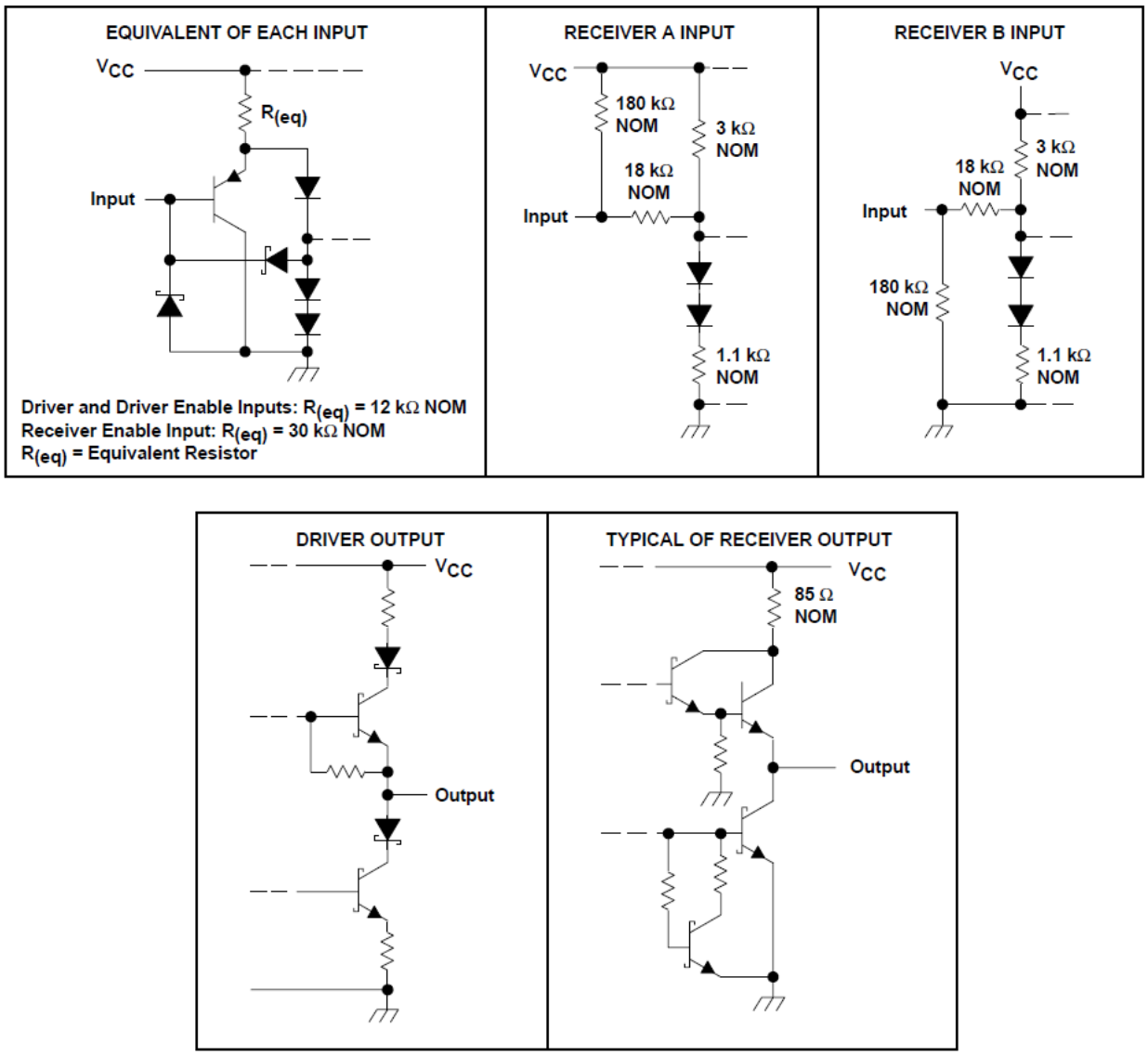


Figure 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

Table 7-1. Driver[1]

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

Table 7-2. Receiver[1]

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
–0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

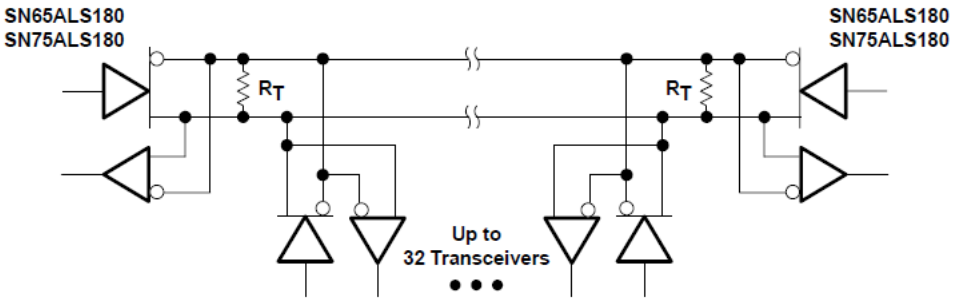
8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application



A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65ALS180DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180
SN65ALS180DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180
SN65ALS180DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180
SN75ALS180D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	75ALS180
SN75ALS180DR	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	75ALS180
SN75ALS180N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS180N
SN75ALS180N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS180N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

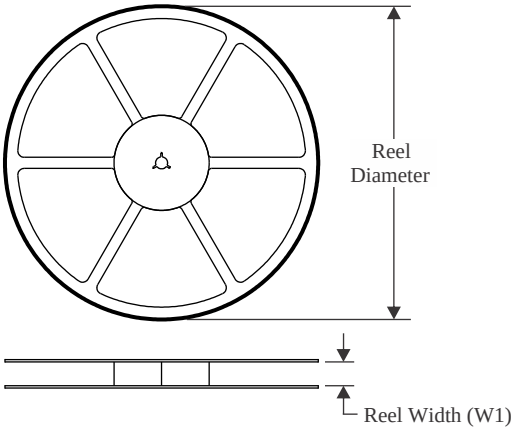
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

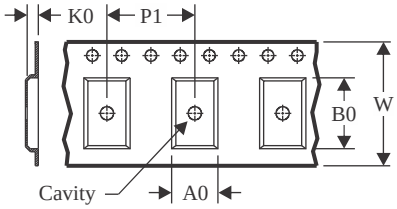
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

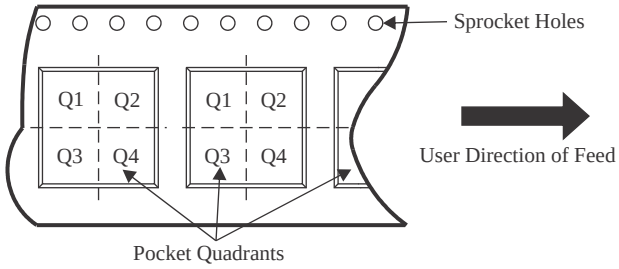


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

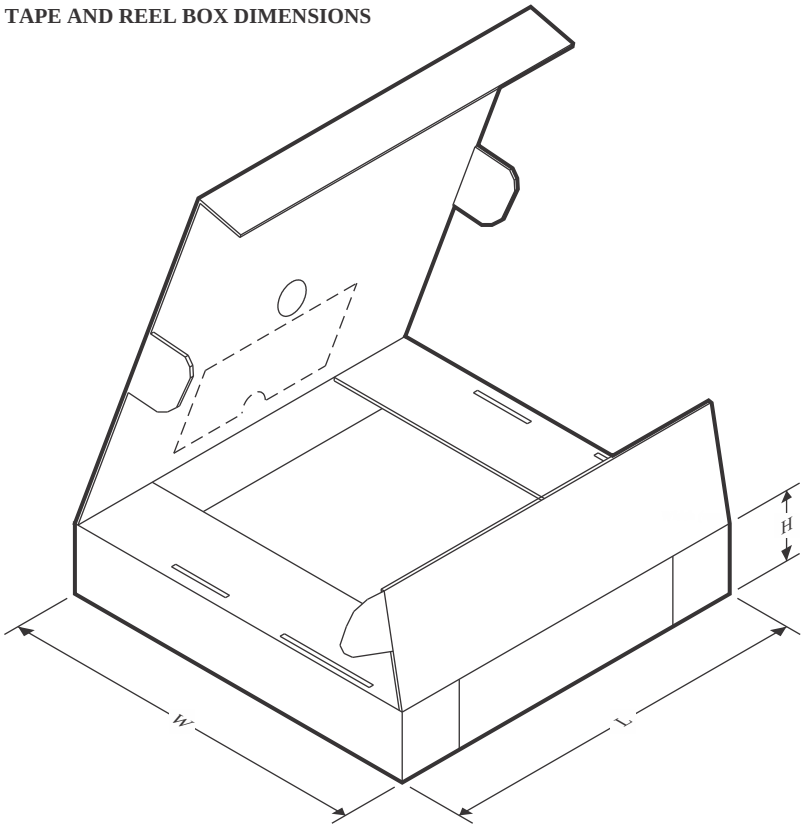
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

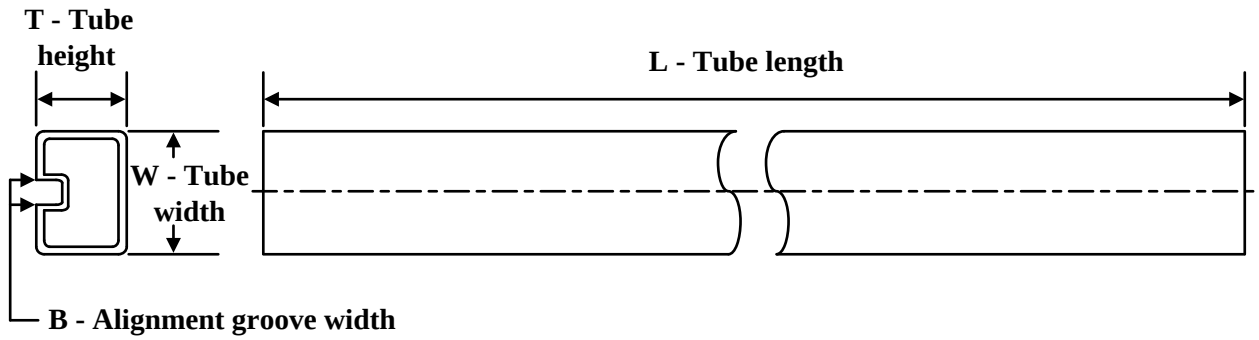
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

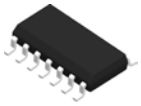
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS180DR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS180N	N	PDIP	14	25	506	13.97	11230	4.32
SN75ALS180N.A	N	PDIP	14	25	506	13.97	11230	4.32

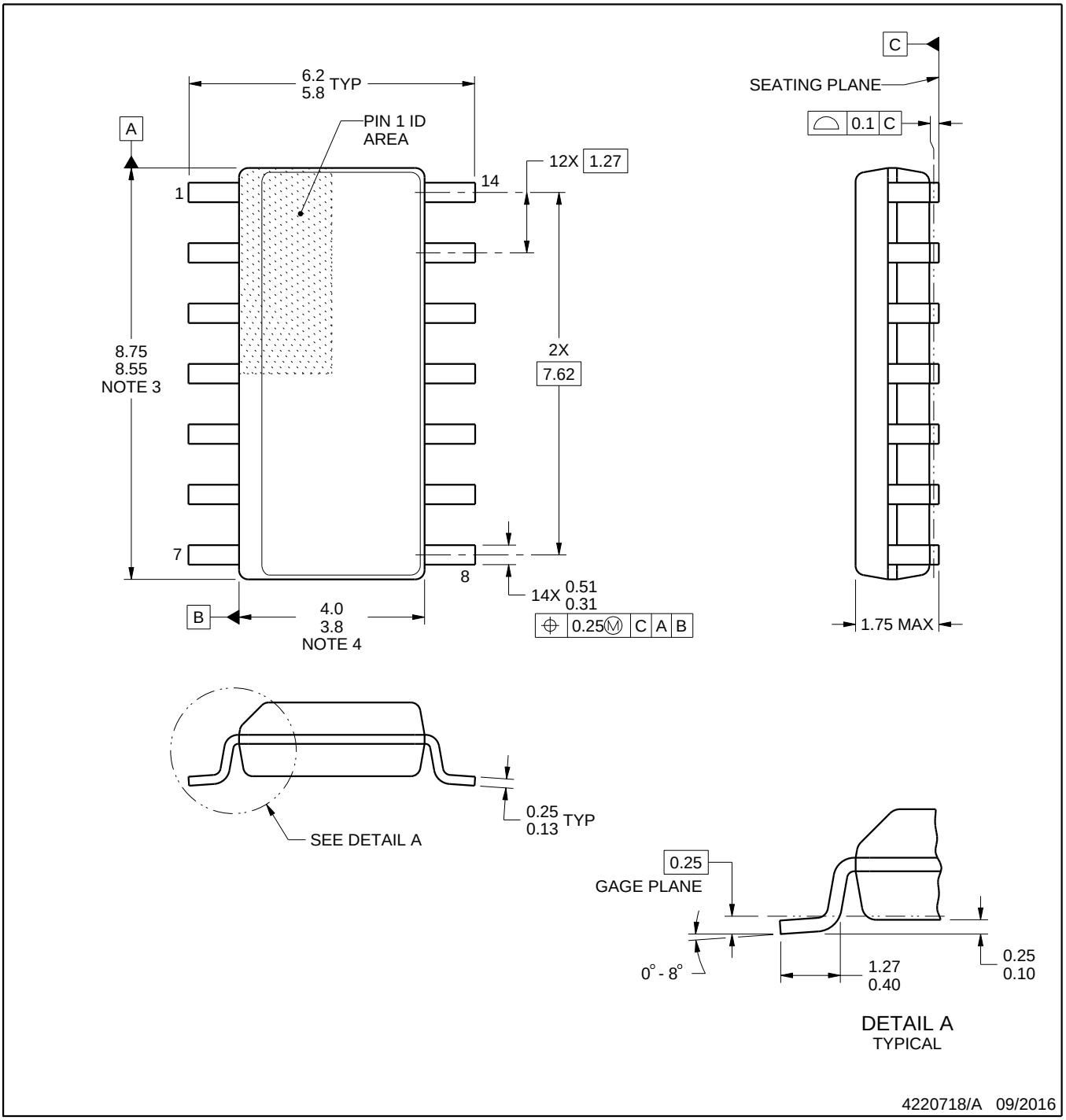


PACKAGE OUTLINE

D0014A

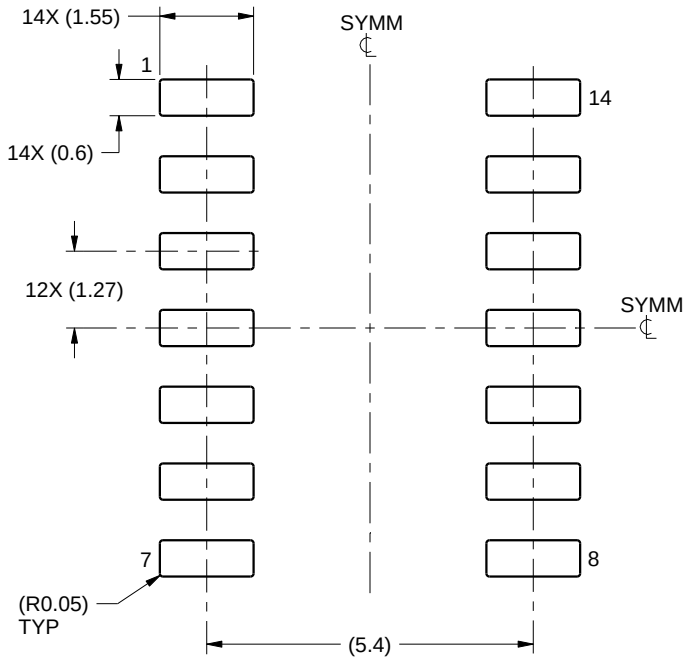
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

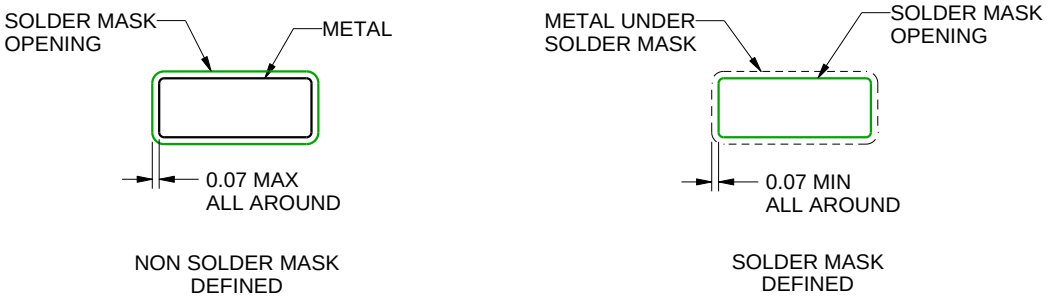


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

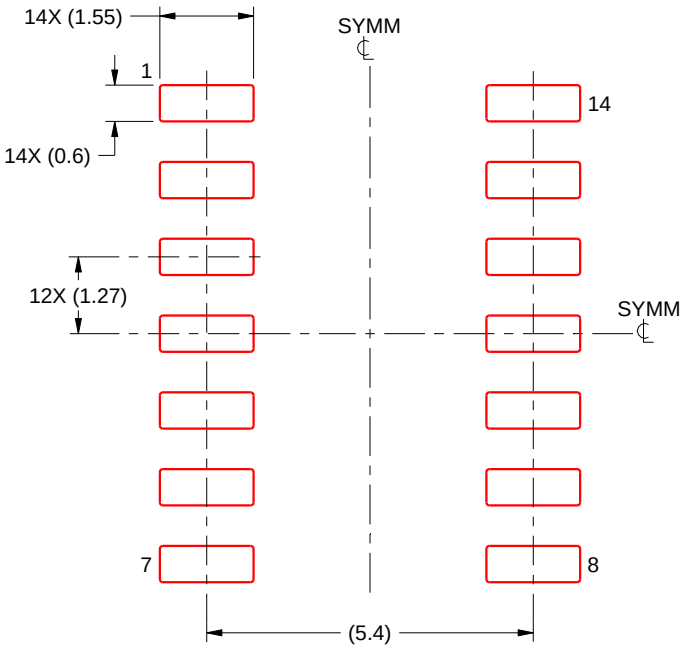
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

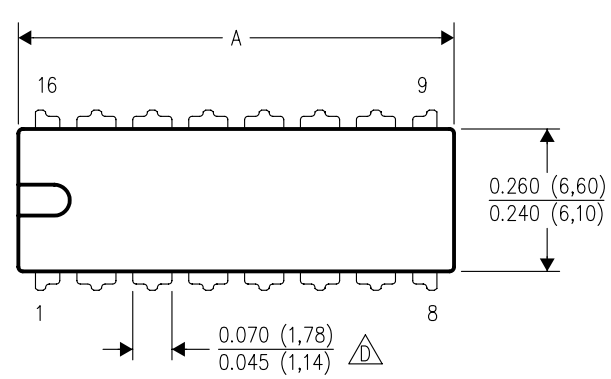
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

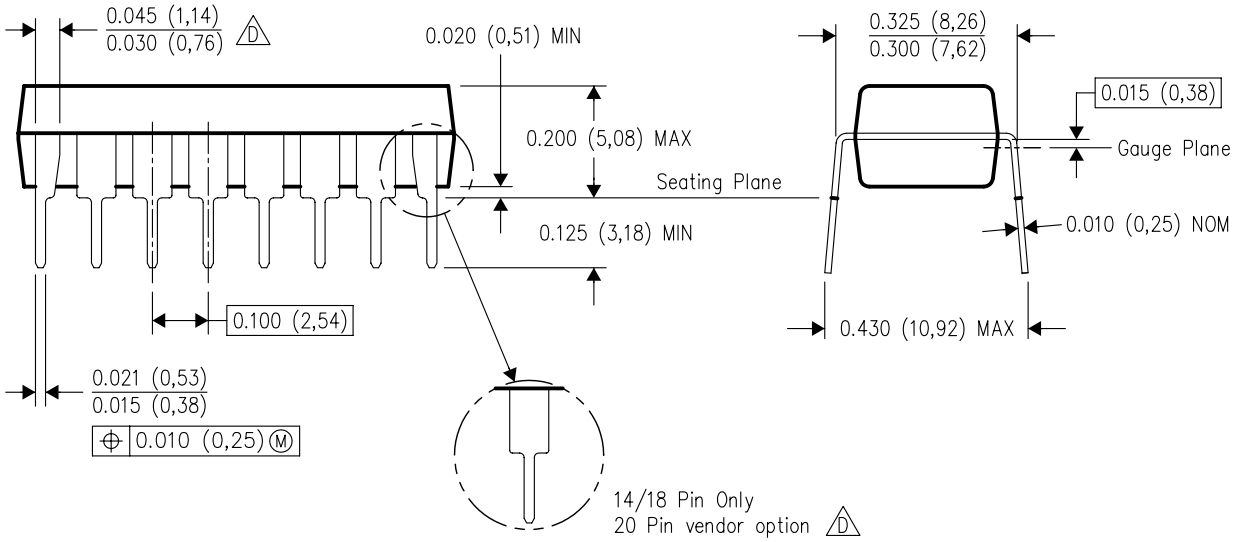
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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