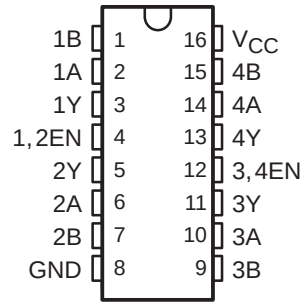
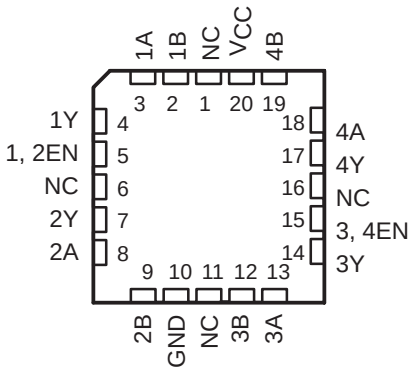
- **Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A**
- **Meet ITU Recommendations V.10 and V.11**
- **Designed to Operate Up to 20 Mbaud**
- **–7 V to 7 V Common-Mode Input Voltage Range With 200-mV Sensitivity**
- **3-State TTL-Compatible Outputs**
- **High Input Impedance . . . 12 kΩ Min**
- **Input Hysteresis . . . 120 mV Typ**
- **Single 5-V Supply Operation**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to MC3486**

SN55ALS195 . . . J OR W PACKAGE
SN75ALS195 . . . J OR N PACKAGE†
(TOP VIEW)



SN55ALS195 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
† For surface-mount package, see the SN75ALS199.

description

The SN55ALS195 and SN75ALS195 are four differential line receivers with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. The 3-state outputs permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The devices are optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 mV over a common-mode input voltage range of ±7 V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quadruple differential line drivers.

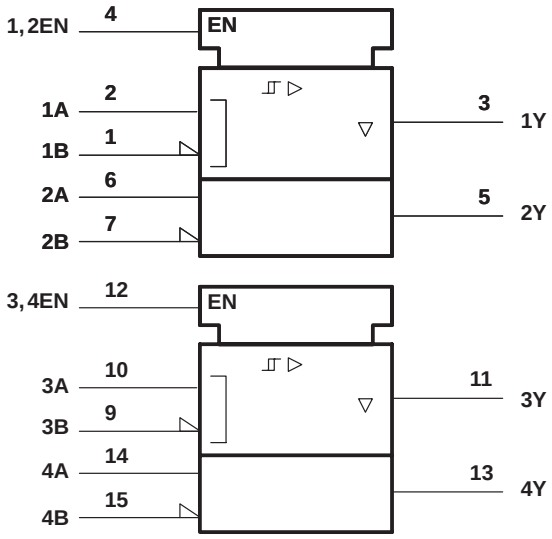
The SN55ALS195 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75ALS195 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant, ? = indeterminate,
Z = high impedance (off)

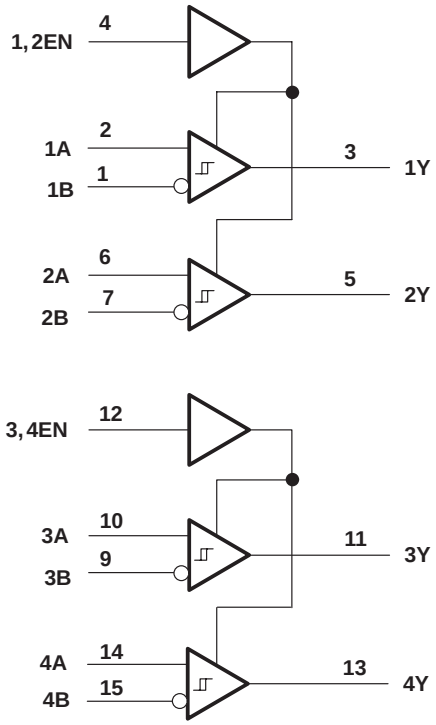
logic symbol†



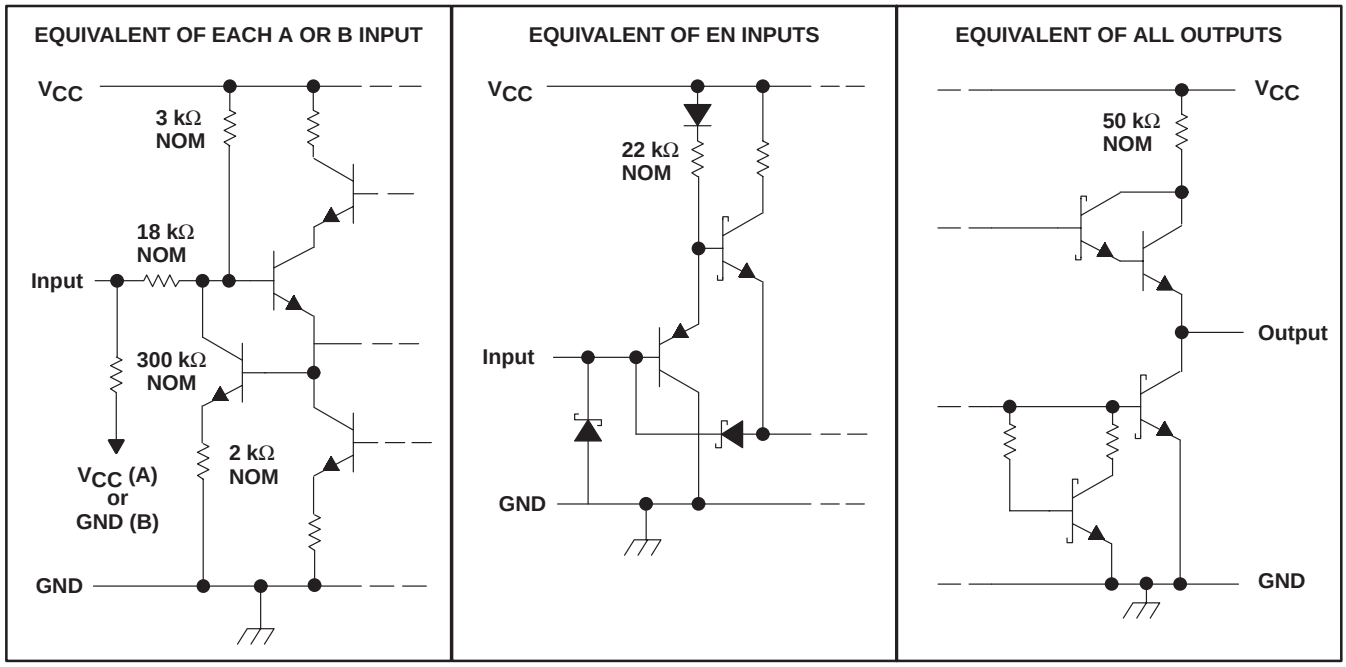
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J, N, and W packages.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs, V_I . . . . . ±15 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±15 V
Enable input voltage, V_I . . . . . 7 V
Low-level output current, I_{OL} . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55ALS195 . . . . . – 55°C to 125°C
SN75ALS195 . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Case temperature for 60 seconds, T_C: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, N, or W package . . . . . 300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditons is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS195)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS195)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

	SN55ALS195			SN75ALS195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±7	V
Differential input voltage, V_{ID}			±12			±12	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			–400			–400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage						200	mV
$V_{IT–}$	Negative-going input threshold voltage				–200§			mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)					120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = – 18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, See Figure 1	V_{ID} = 200 mV,	I_{OH} = – 400 μA,	2.5	3.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = – 200 mV, See Figure 1	I_{OL} = 8 mA				0.45	V
			I_{OL} = 16 mA				0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = MAX, V_O = 2.7 V	V_{IL} = 0.8 V,	V_{ID} = – 3 V,			20	μA
		V_{CC} = MAX, V_O = 0.5 V	V_{IL} = 0.8 V,	V_{ID} = 3 V,			–20	
I_I	Line input current	Other input at 0 V, See Note 3	V_{CC} = MIN,	V_I = 15 V		0.7	1.2	mA
			V_{CC} = MAX,	V_I = –15 V		–1	–1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V				20	μA
			V_{IH} = 5.25 V				100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V				–100	μA
r_i	Input resistance				12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, See Note 4	V_{ID} = 3 V,	V_O = 0,	–15	–78	–130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled			22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
NOTES: 3. Refer to ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, See Figure 2		15	22	ns
t_{PHL}	Propagation delay time, high- to low-level output			15	22	ns
t_{PZH}	Output enable time to high level	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level			10	25	
t_{PHZ}	Output disable time from high level	See Figure 3		19	25	ns
t_{PLZ}	Output disable time from low level			17	22	

PARAMETER MEASUREMENT INFORMATION

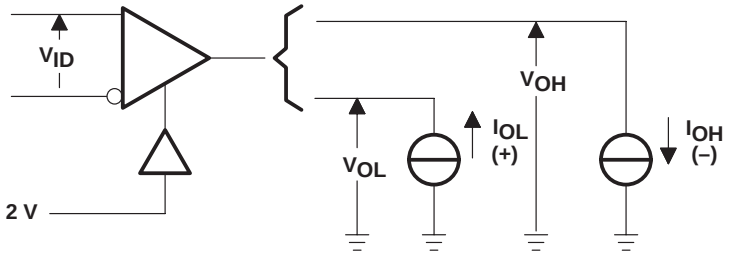
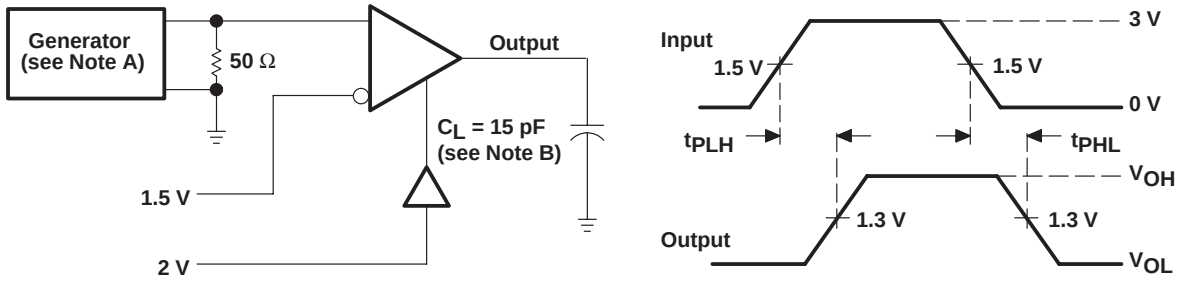


Figure 1. V_{OH}, V_{OL}

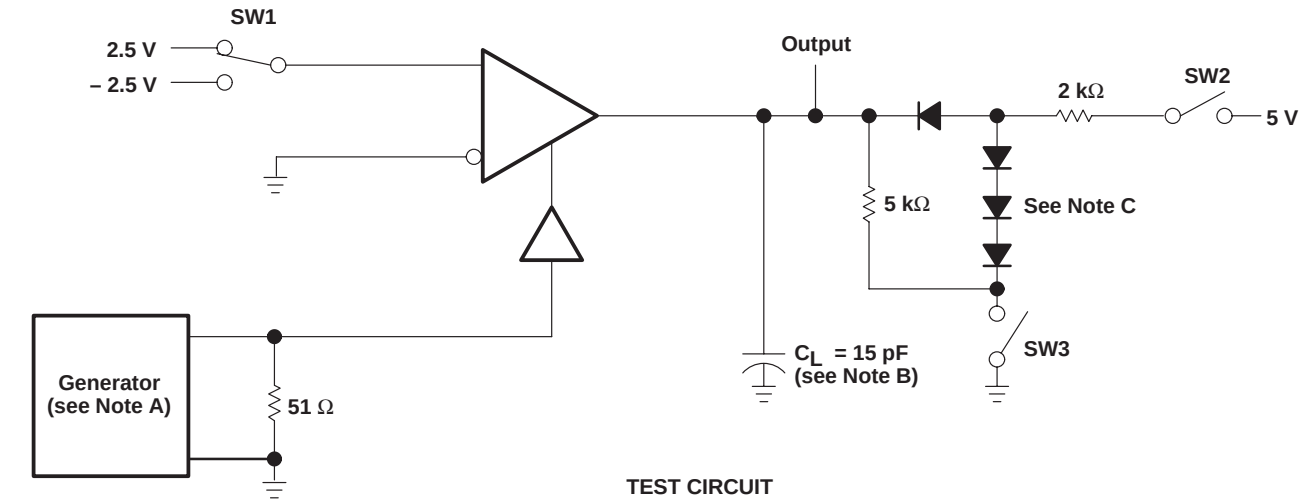


TEST CIRCUIT **VOLTAGE WAVEFORMS**

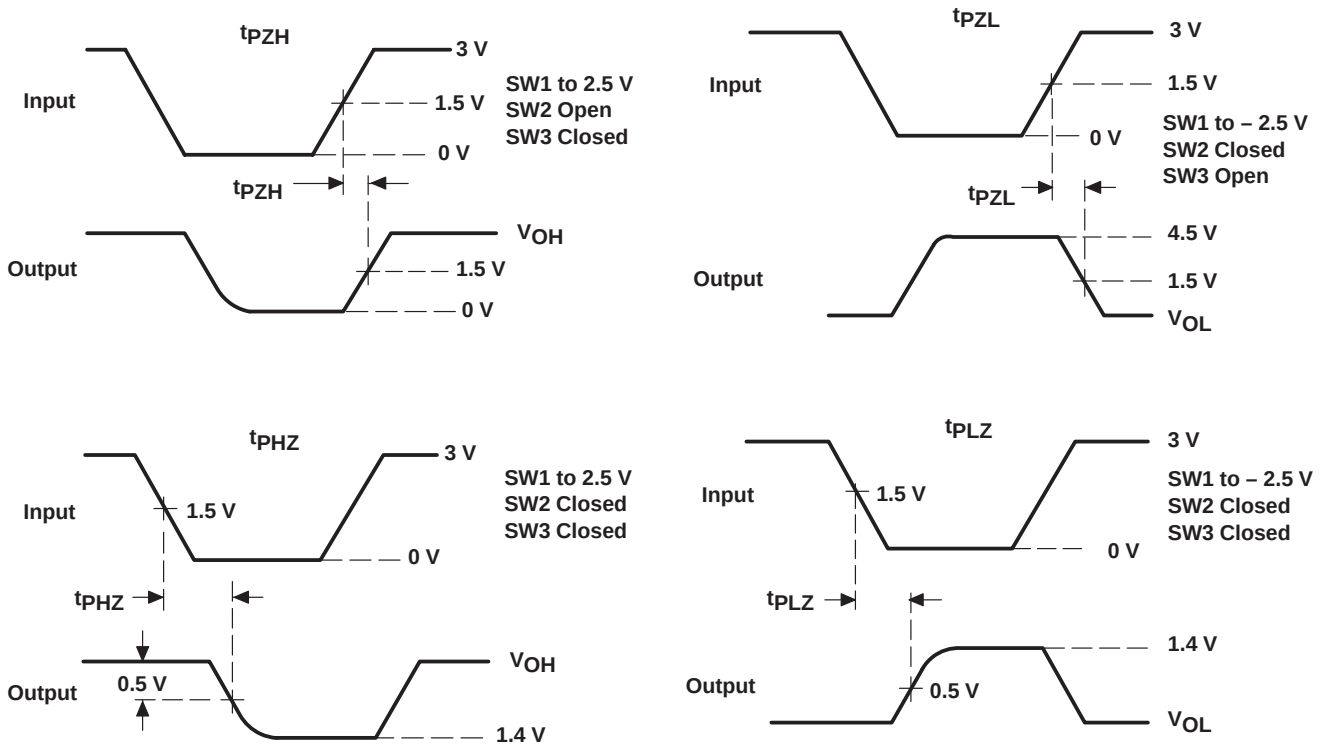
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test CIrcuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs ENABLE VOLTAGE

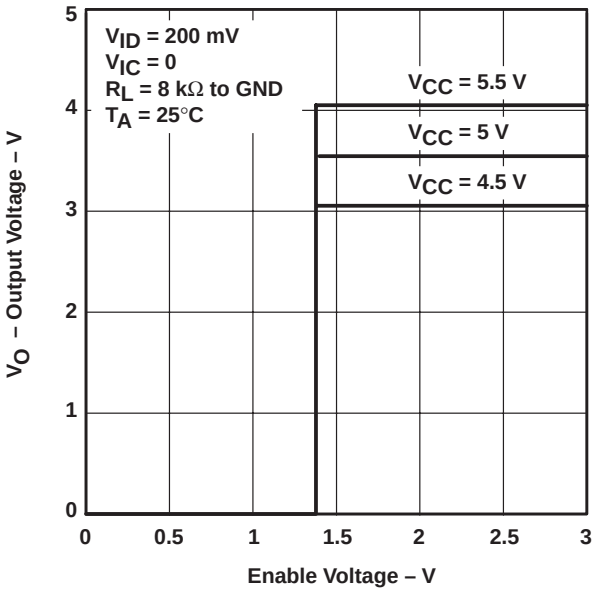


Figure 4

OUTPUT VOLTAGE vs ENABLE VOLTAGE

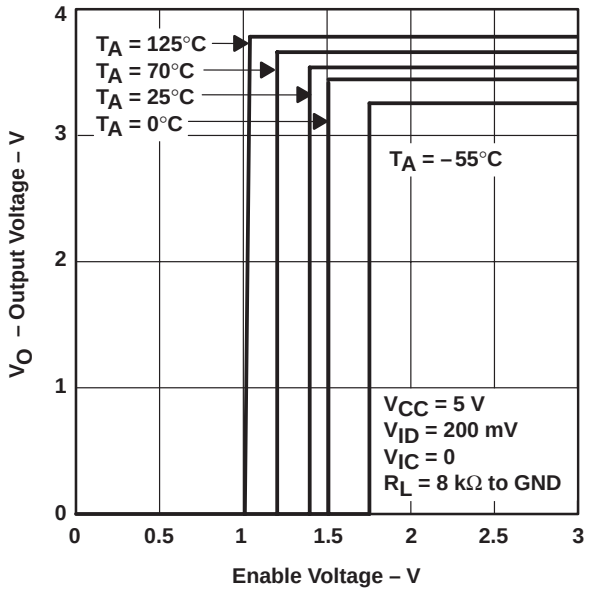


Figure 5

OUTPUT VOLTAGE vs ENABLE VOLTAGE

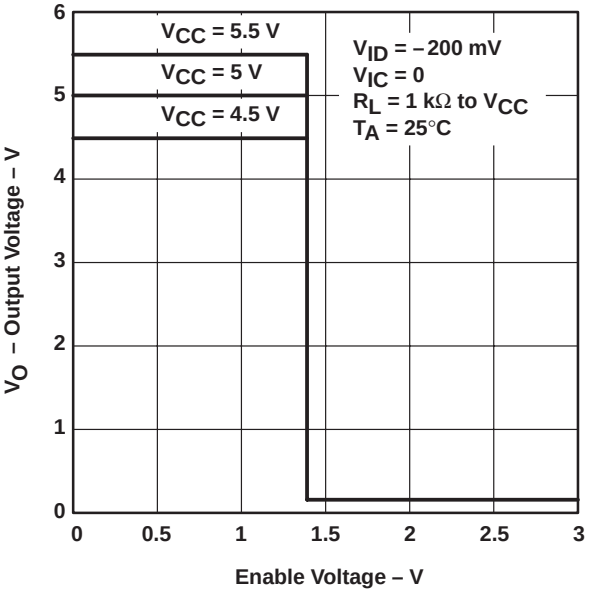


Figure 6

OUTPUT VOLTAGE vs ENABLE VOLTAGE

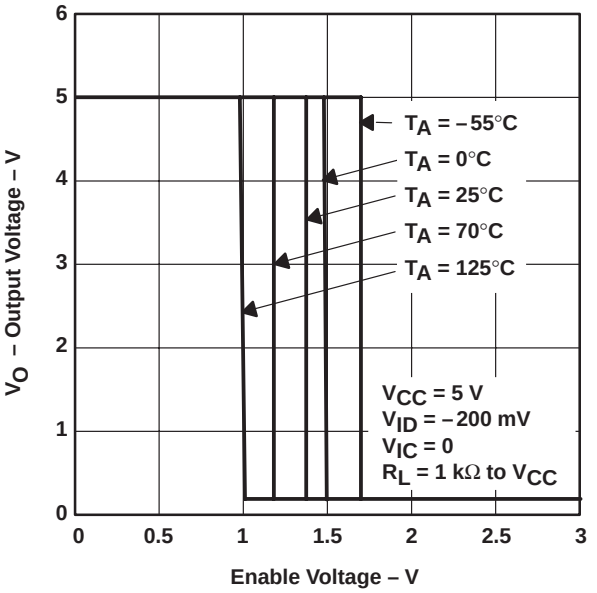


Figure 7

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

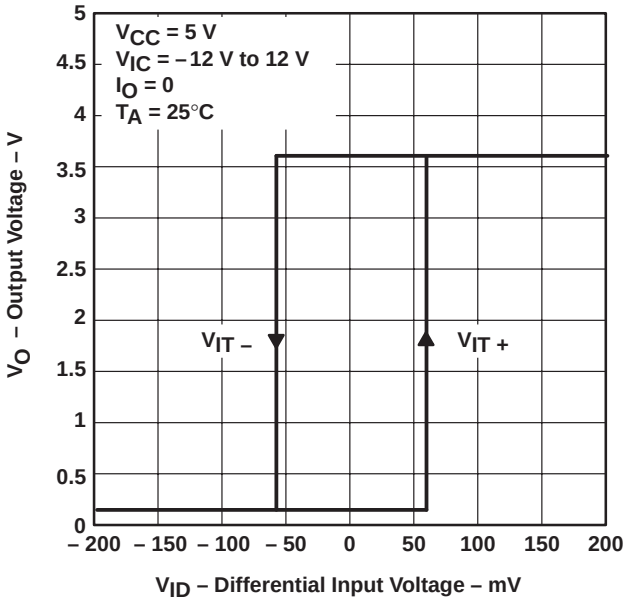


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

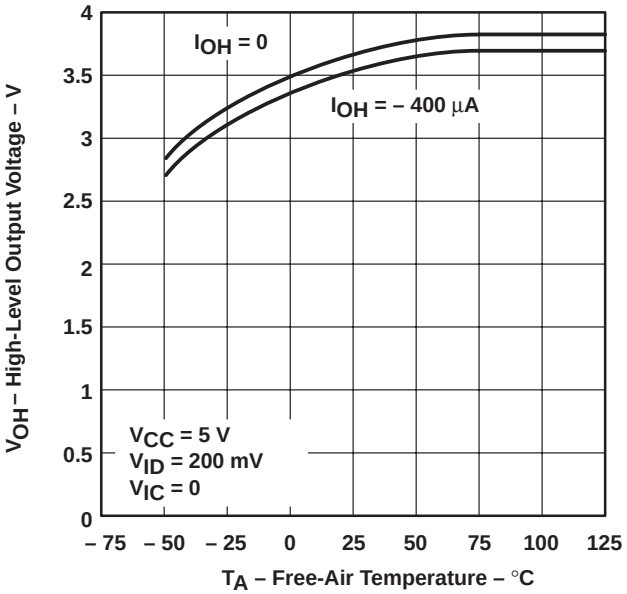


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

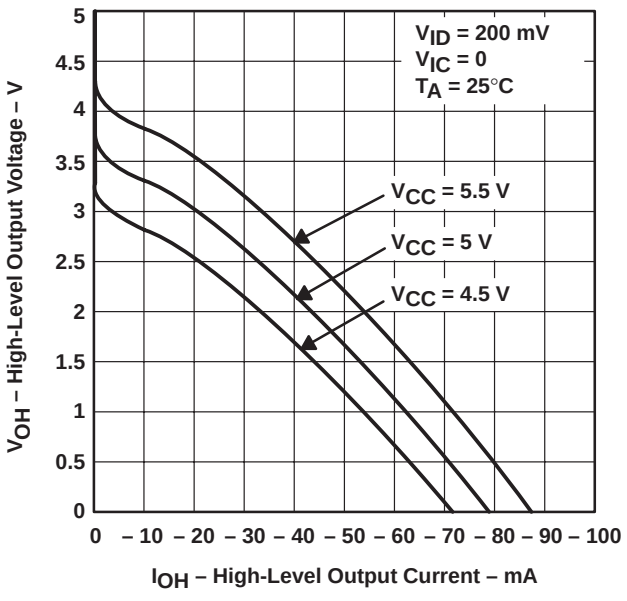


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

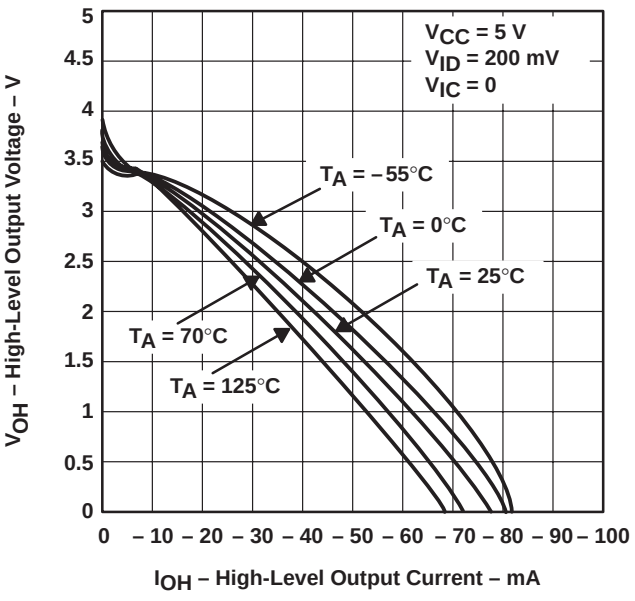


Figure 11

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

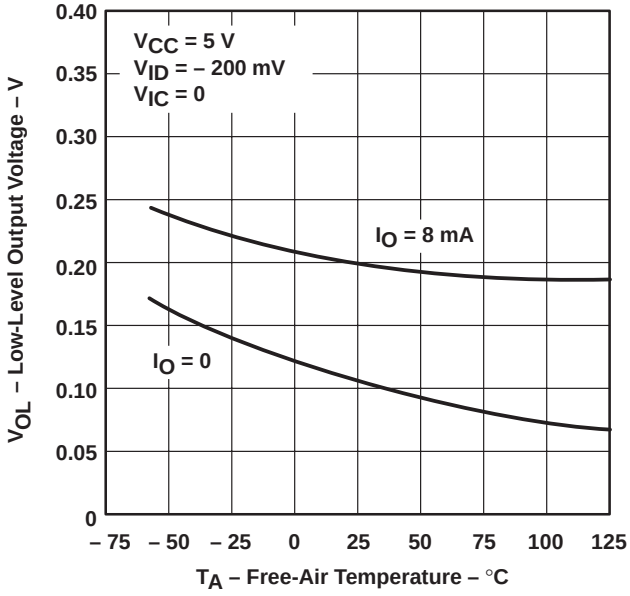


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

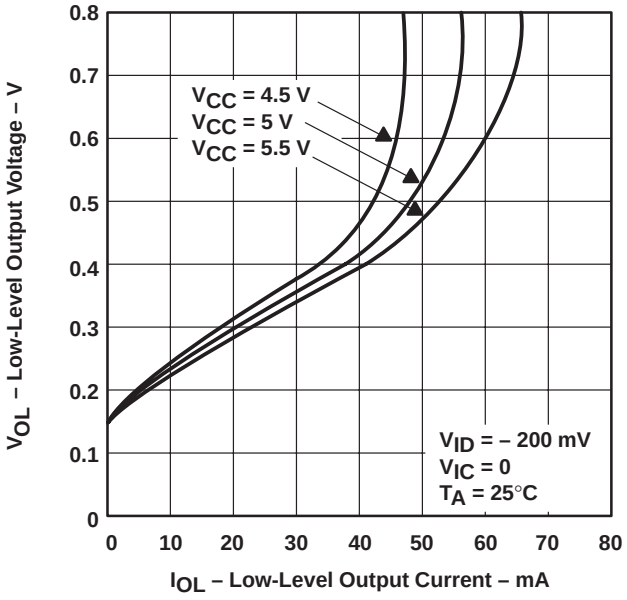


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

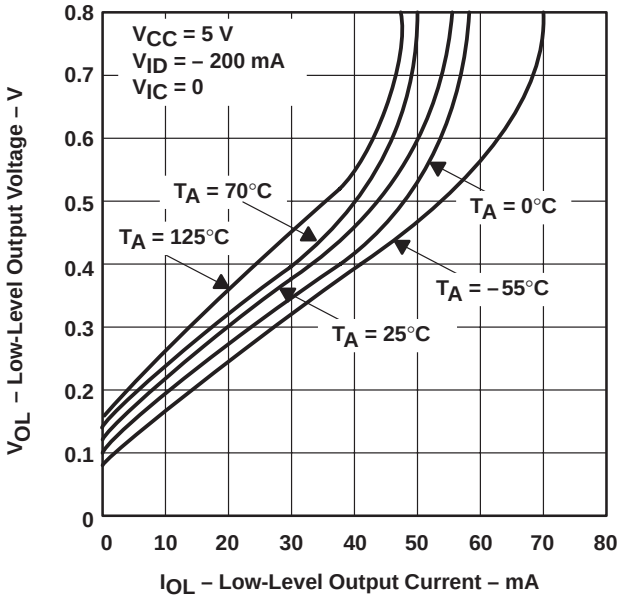


Figure 14

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT vs SUPPLY VOLTAGE

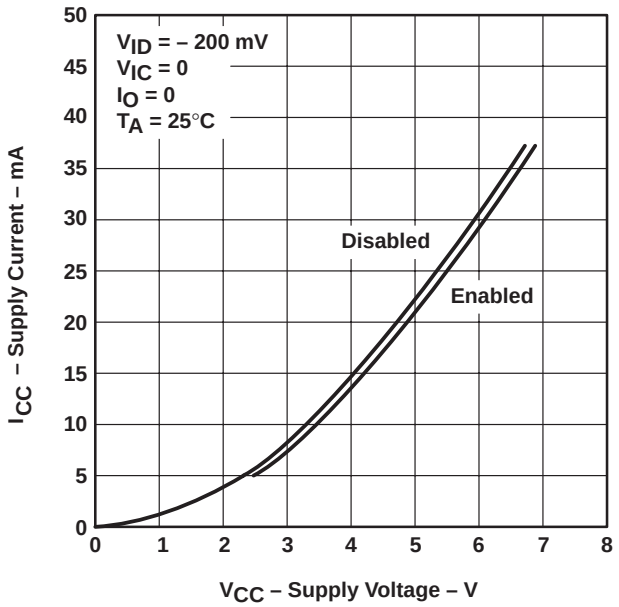


Figure 15

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

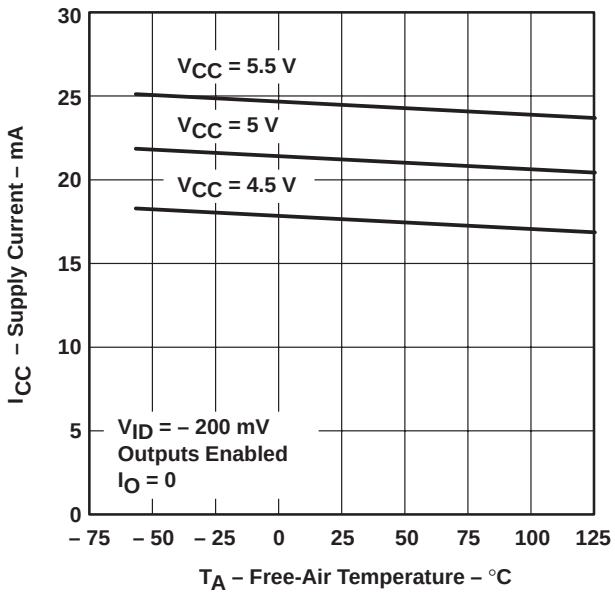


Figure 16

SUPPLY CURRENT vs DIFFERENTIAL INPUT VOLTAGE

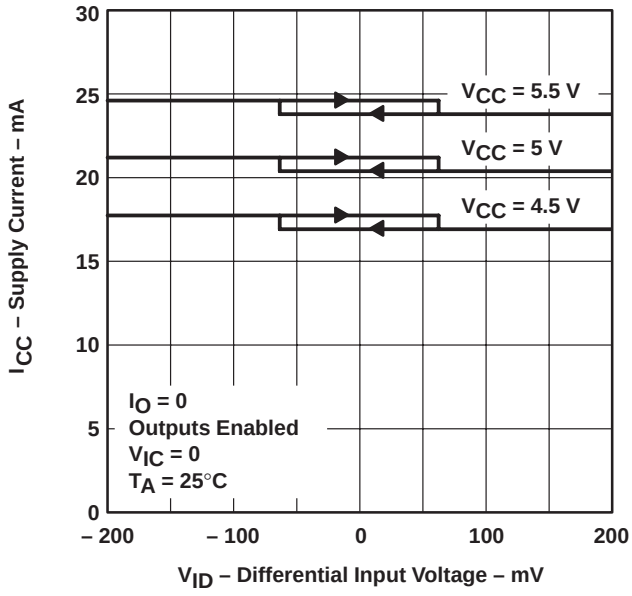


Figure 17

SUPPLY CURRENT vs FREQUENCY

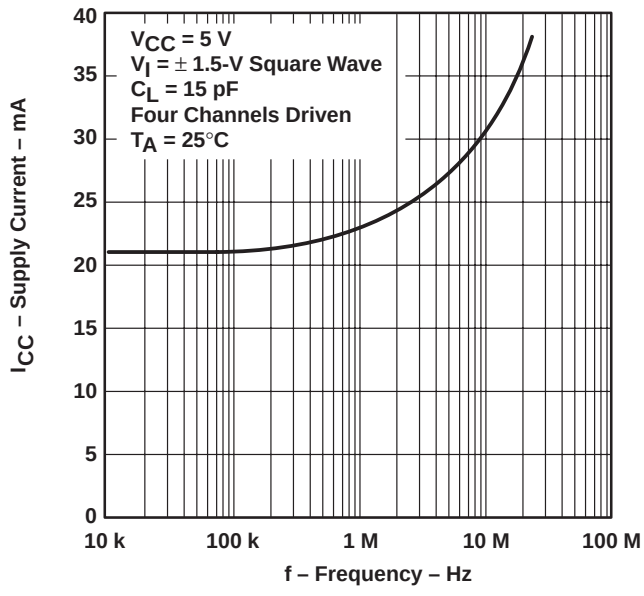


Figure 18

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

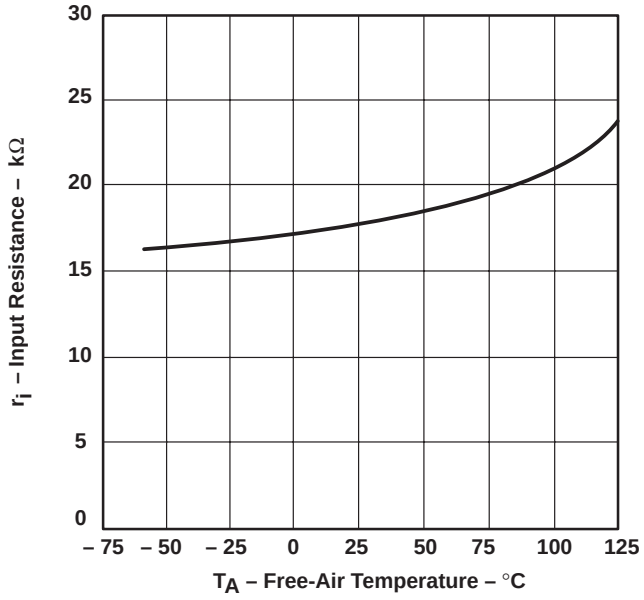


Figure 19

INPUT CURRENT vs INPUT VOLTAGE TO GND

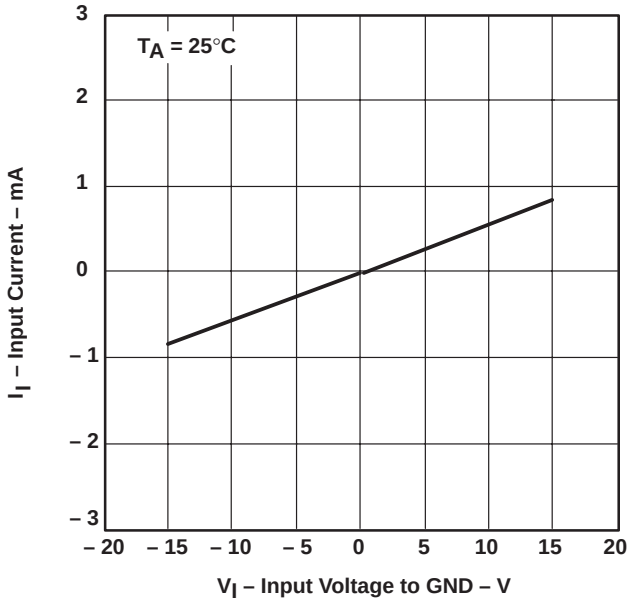


Figure 20

SWITCHING TIME vs FREE-AIR TEMPERATURE

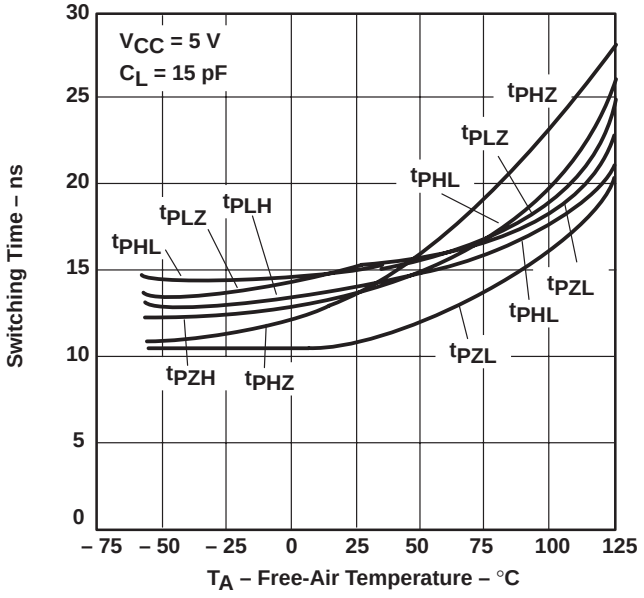


Figure 21

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

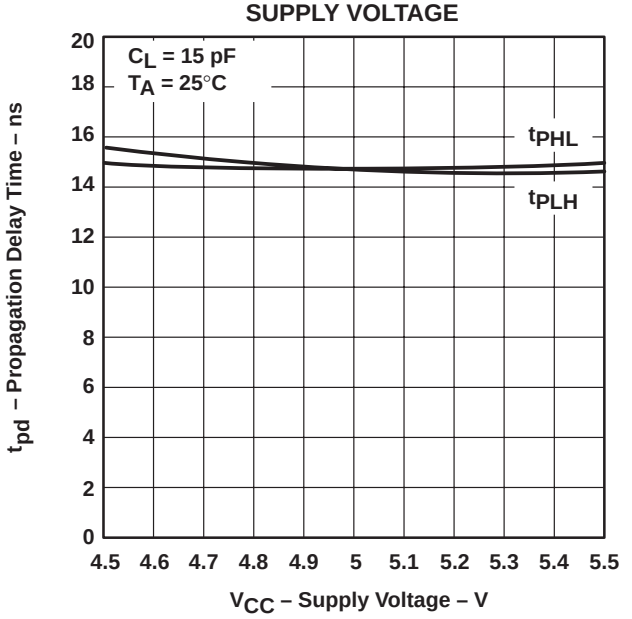


Figure 22

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS195N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS195N
SN75ALS195N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75ALS195N

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

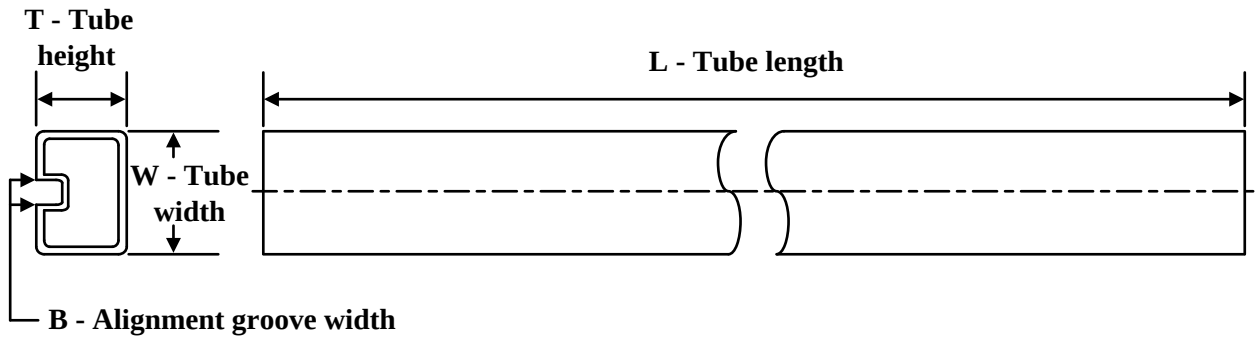
(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



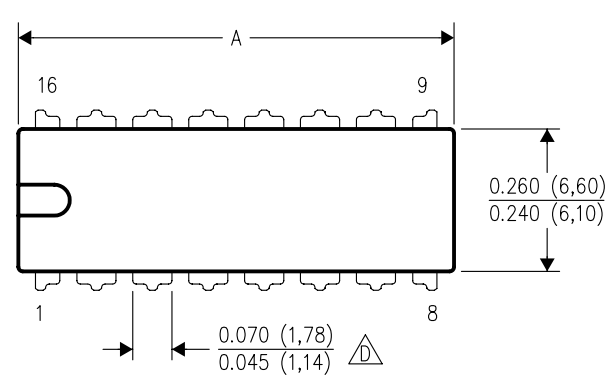
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS195N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS195N.A	N	PDIP	16	25	506	13.97	11230	4.32

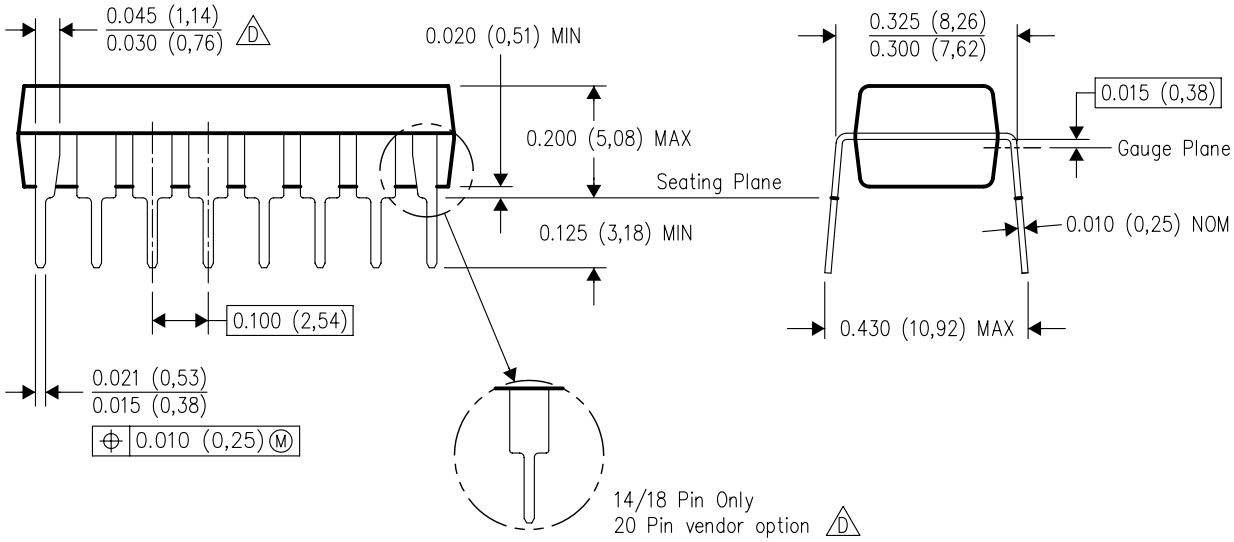
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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