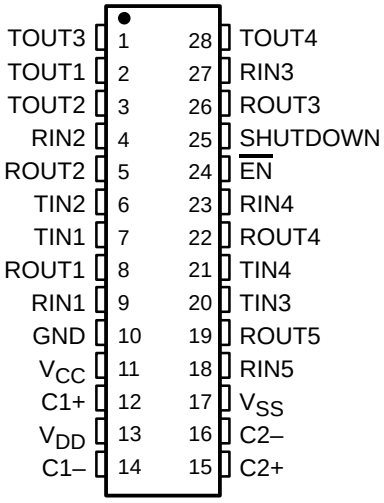
SLLS137F – MAY 1992 – REVISED FEBRUARY 2001

- **Operates With Single 5-V Power Supply**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Improved Performance Replacement for MAX241**
- **Operates at Data Rates up to 100 kbit/s Over a 3-m Cable**
- **Low-Power Shutdown Mode . . . ≤1 μA Typ**
- **LinBiCMOS™ Process Technology**
- **Four Drivers and Five Receivers**
- **±30-V Input Levels**
- **3-State TTL/CMOS Receiver Outputs**
- **±9-V Output Swing With a 5-V Supply**
- **Applications**
  - **TIA/EIA-232-F Interface**
  - **Battery-Powered Systems**
  - **Terminals**
  - **Modems**
  - **Computers**
- **Packaged in Plastic Small-Outline Package**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC241 is a low-power LinBiCMOS™ line-interface device containing four independent drivers and five receivers. It is designed as a plug-in replacement for the Maxim MAX241. The SN75LBC241 provides a capacitive-charge-pump voltage generator to produce RS-232 voltage levels from a 5-V supply. The charge-pump oscillator frequency is 20 kHz. Each receiver converts RS-232 inputs to 5-V TTL/CMOS levels. The receivers have a typical threshold of 1.2 V and a typical hysteresis of 0.5 V and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into RS-232 levels.

The SN75LBC241 includes a receiver, a 3-state control line, and a low-power shutdown control line. When the $\overline{EN}$ line is high, receiver outputs are placed in the high-impedance state. When $\overline{EN}$ is low, normal operation is enabled.

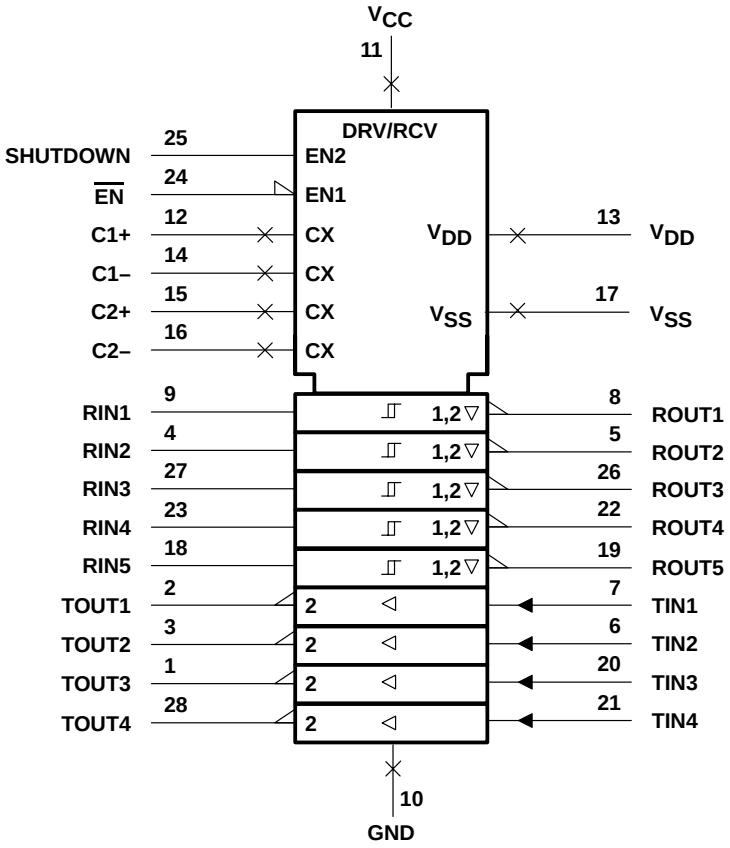
The shutdown mode reduces power dissipation to less than 5 μW, typically. In this mode, receiver outputs have high impedance, driver outputs are turned off, and the charge-pump circuit is turned off. When SHUTDOWN is high, the shutdown mode is enabled. When SHUTDOWN is low, normal operation is enabled.

This device has been designed to conform to TIA/EIA-232-F and ITU Recommendation V.28.

The SN75LBC241 has been designed using LinBiCMOS technology and cells contained in the Texas Instruments LinASIC™ library. Use of LinBiCMOS circuitry increases latch-up immunity in this device over an all-CMOS design.

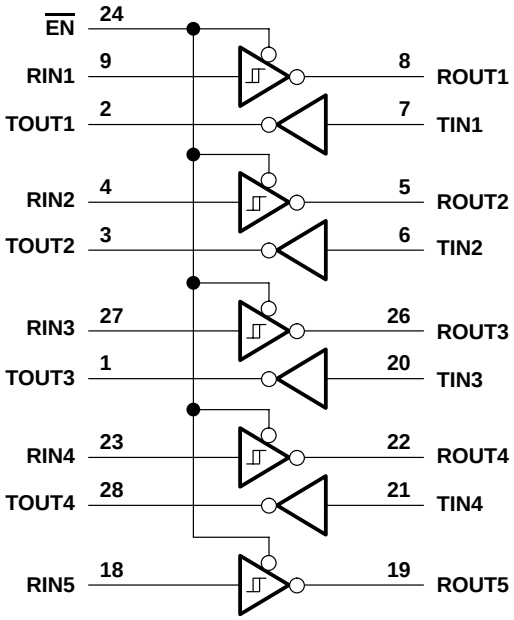
The SN75LBC241 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 6 V
Positive output supply voltage range, V_{DD} . . . . . V_{CC} –0.3 V to 15 V
Negative output supply voltage range, V_{SS} . . . . . 0.3 V to –15 V
Input voltage range, V_I: Driver . . . . . –0.3 V to V_{CC} + 0.3 V
Receiver . . . . . ±30 V
Output voltage range, V_O: TOUT . . . . . V_{SS} –0.3 V to V_{DD} + 0.3 V
ROUT . . . . . –0.3 V to V_{CC} + 0.3 V
Short-circuit duration: TOUT . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 46°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1603 mW	12.8 mW/°C	1026 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Supply voltage, V_{CC}	4.5	5	5.5	V
V_{IH}	High-level input voltage	TIN	2			V
		$\overline{EN}$, SHUTDOWN	2.4			
V_{IL}	Low-level input voltage	TIN, $\overline{EN}$, SHUTDOWN			0.8	V
	External charge-pump capacitor	C1–C4 (see Figure 5)	1			µF
	External charge-pump capacitor voltage rating	C1, C3 (see Figure 5)	6.3			V
		C2, C4 (see Figure 5)	16			
V_I	Receiver input voltage				±30	V
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

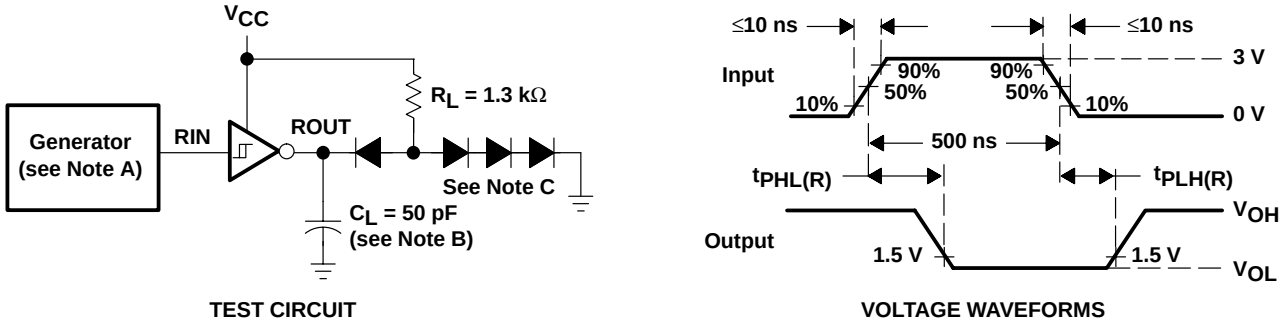
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TOUT	R_L = 3 kΩ to GND, See Note 3	5	9		V
		ROUT	I_{OH} = –1 mA	3.5			
V_{OL}	Low-level output voltage	TOUT	R_L = 3 kΩ to GND, See Note 4		–9‡	–5	V
		ROUT	I_{OL} = 3.2 mA			0.4	
V_{IT+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
$V_{IT–}$	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage ($V_{IT+} – V_{IT–}$)	RIN	V_{CC} = 5 V		0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ
r_o	Output resistance	TOUT	$V_{DD} = V_{SS} = V_{CC} = 0$, V_O = ±2 V	300			Ω
I_{OS}	Short-circuit output current§	TOUT	V_{CC} = 5.5 V, V_O = 0		±10		mA
I_{IS}	Short-circuit input current	TIN	V_I = 0			200	µA
I_{CC}	Supply current		V_{CC} = 5.5 V, T_A = 25°C, All outputs open		4	8	mA
			All outputs open, T_A = 25°C, SHUTDOWN high		1	10	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at one time.
NOTES: 3. Total I_{OH} drawn from TOUT1, TOUT2, TOUT3, TOUT4, and V_{DD} terminals should not exceed 12 mA.
4. Total I_{OL} drawn from TOUT1, TOUT2, TOUT3, TOUT4, and V_{SS} terminals should not exceed –12 mA.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Receiver propagation-delay time, low- to high-level output	See Figure 1		500		ns
$t_{PHL(R)}$	Receiver propagation-delay time, high- to low-level output	See Figure 1		500		ns
t_{PZH}	Receiver output-enable time to high level	See Figure 4		100		ns
t_{PZL}	Receiver output-enable time to low level	See Figure 4		100		ns
t_{PHZ}	Receiver output-disable time from high level	See Figure 4		50		ns
t_{PLZ}	Receiver output-disable time from low level	See Figure 4		50		ns
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3			30	V/µs
$SR_{(tr)}$	Driver transition-region slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3	4	6		V/µs

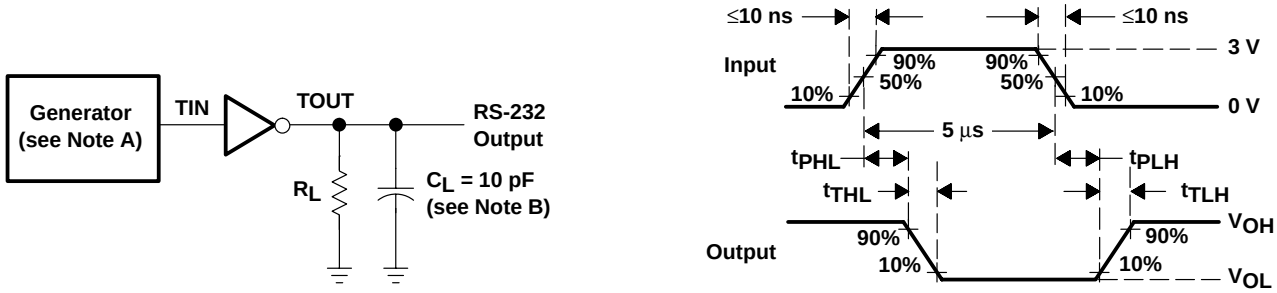
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

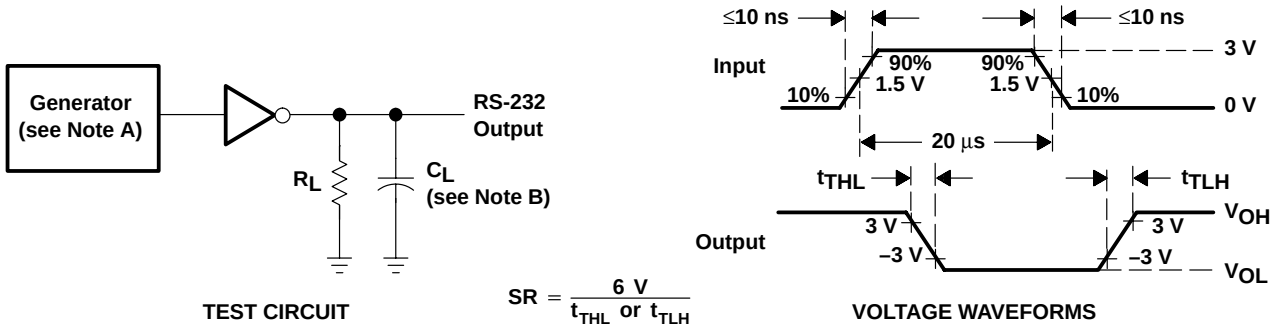
Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement (5-μs Input)



TEST CIRCUIT

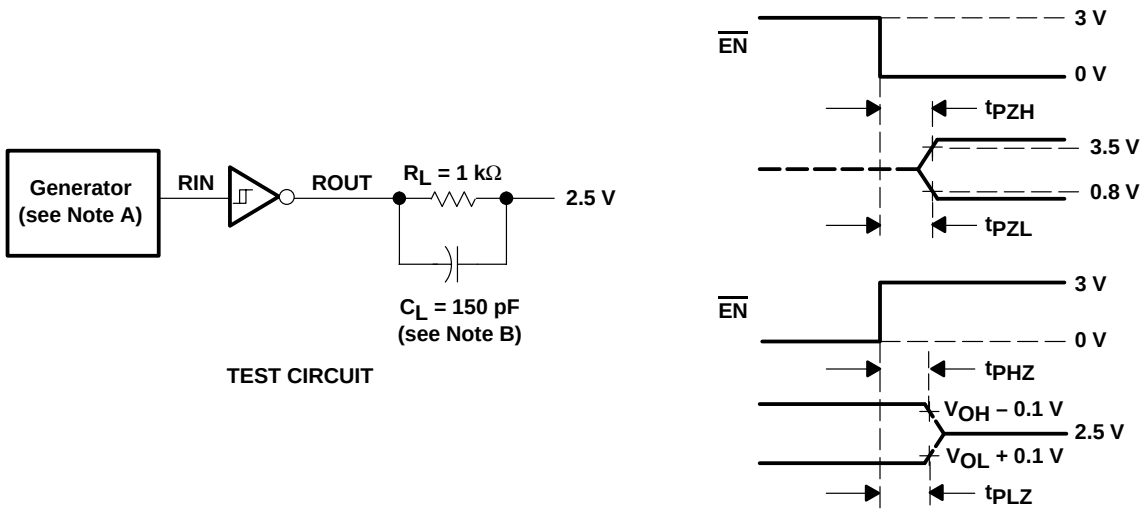
$$SR = \frac{6\ V}{t_{THL}\ \text{or}\ t_{TLH}}$$

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurement (20-μs Input)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 4. Receiver Output Enable and Disable Timing

APPLICATION INFORMATION

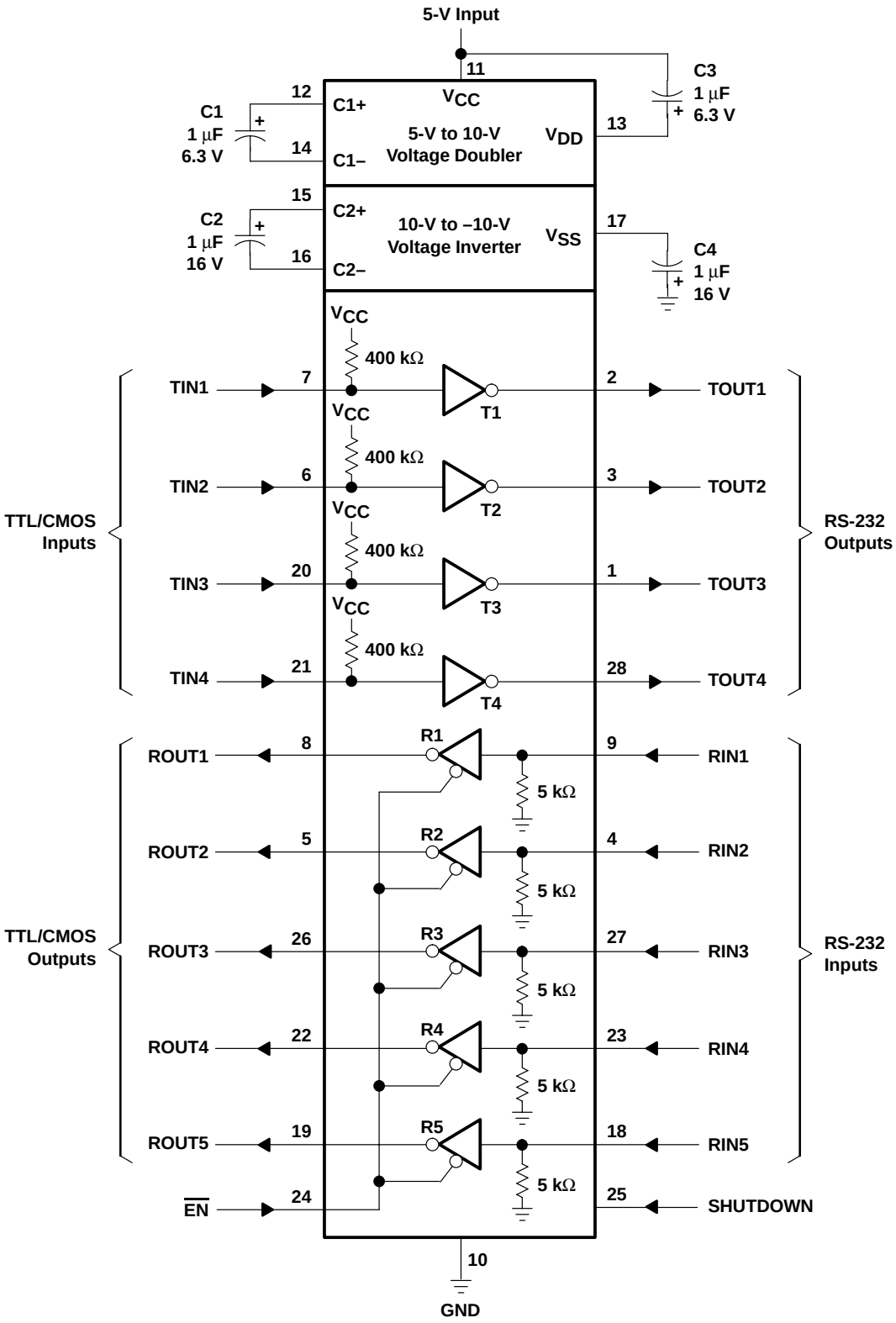


Figure 5. Typical Operating Circuit

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LBC241DW	Active	Production	SOIC (DW) | 28	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC241
SN75LBC241DW.A	Active	Production	SOIC (DW) | 28	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC241
SN75LBC241DWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC241
SN75LBC241DWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC241

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

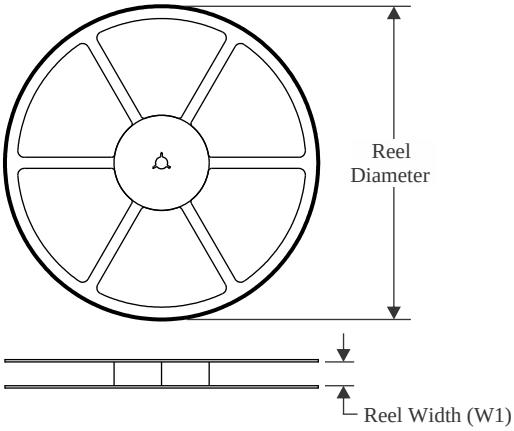
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

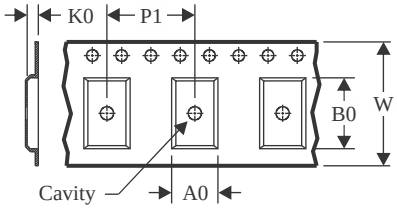
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

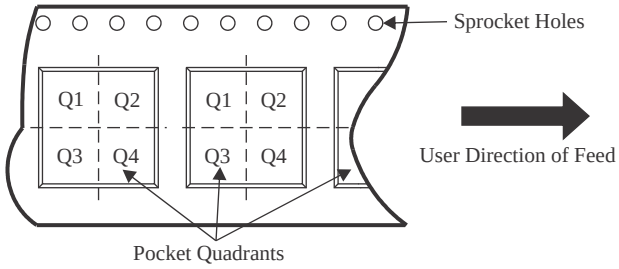


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

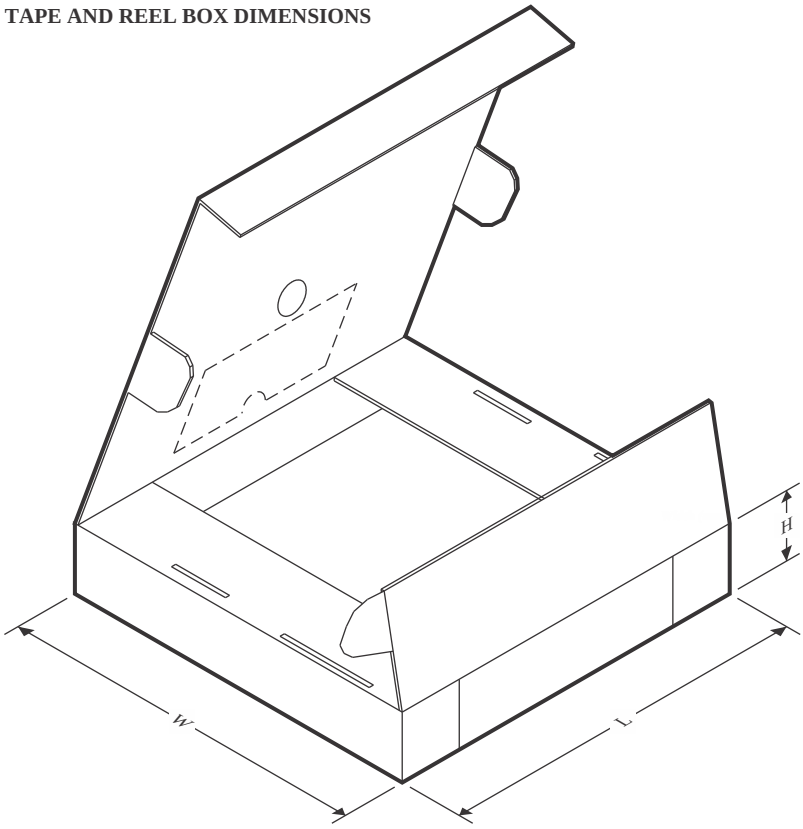
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC241DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

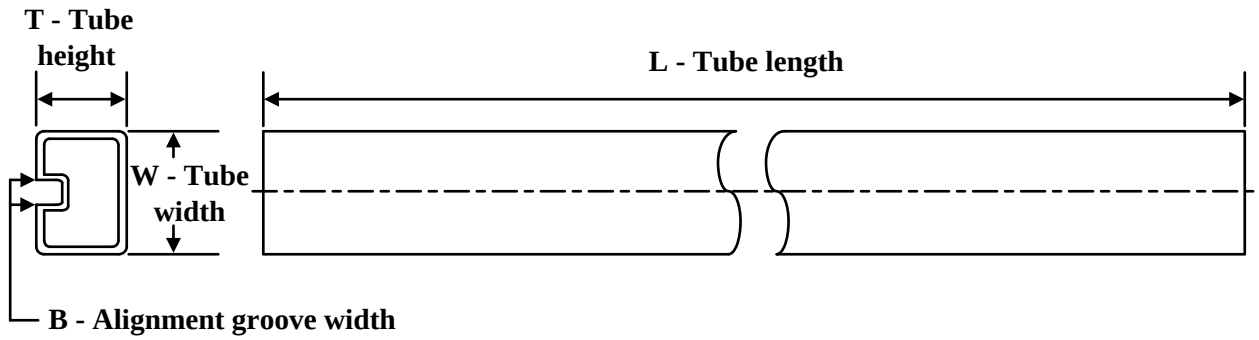
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC241DWR	SOIC	DW	28	1000	350.0	350.0	66.0

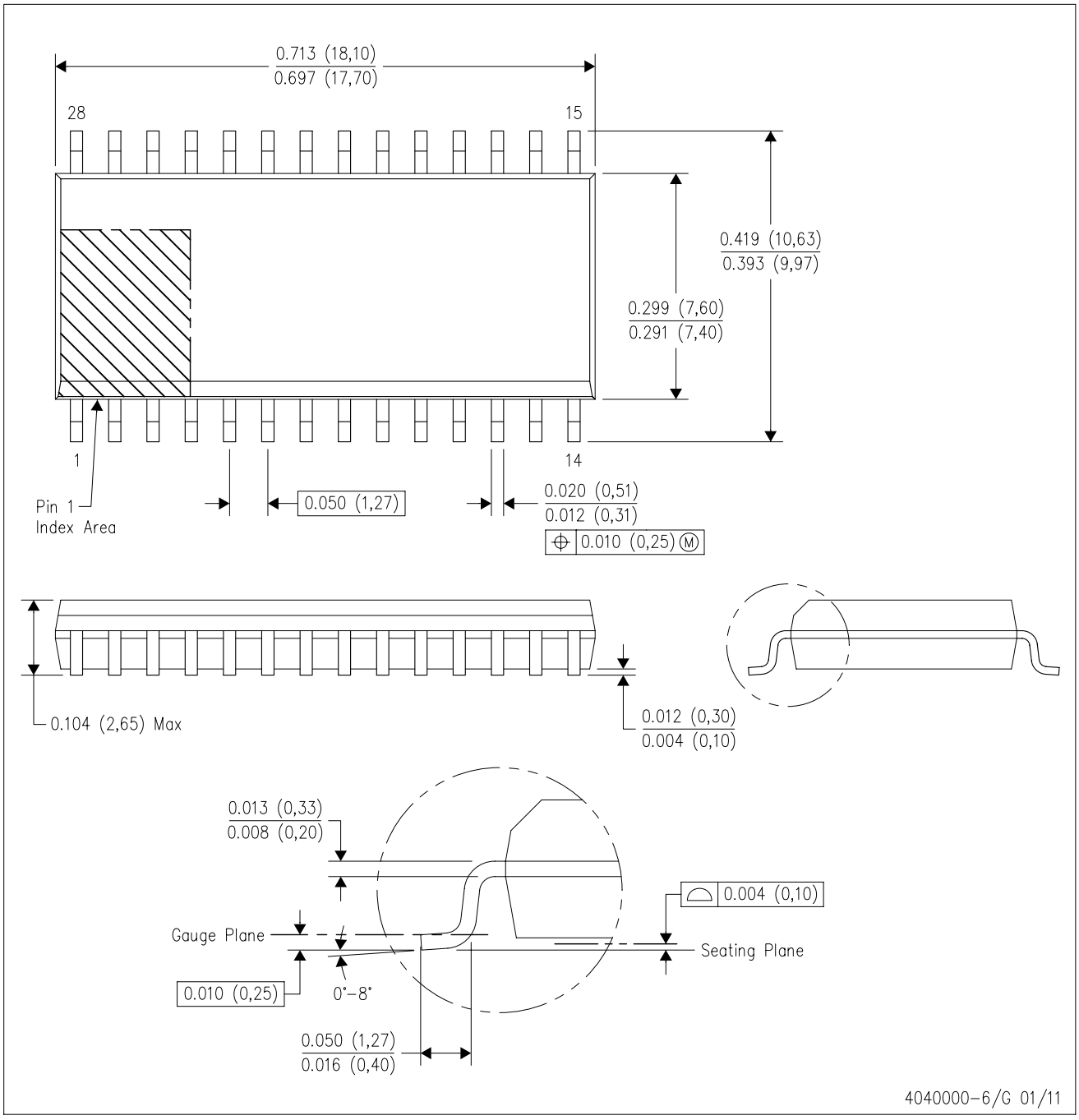
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LBC241DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN75LBC241DW.A	DW	SOIC	28	20	506.98	12.7	4826	6.6

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

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