

TAS2573 Boosted Class-D Audio Amplifier with Integrated DSP and IV Sense

1 Features

- Powerful class-D amplifier
 - 8.5W 1% THD+N (8Ω at 4.4V)
 - 8.8W 1% THD+N (4Ω at 4.4V)
 - 15V boost with 5.1A max current limit
- Best in class efficiency
 - Upto 89% efficiency at system level for 8Ω load
 - 19mW idle channel power in active mode
 - 5.5mW idle channel power in Noise gate mode
 - Integrated 1.8V Y-bridge and 33mV step class-H
- High performance audio channel
 - 4.2μV A-wt. idle channel noise
 - 114dB Dynamic Range
 - 90dB THDN
 - Low EMI performance with ERC and SSM
 - < 1μs chip to chip group delay matching
- Advanced integrated features
 - Speaker Protection and Advanced Battery Guard with integrated IV sense
 - Audio tuning with EQ, DRC, DEQ
 - Speaker Rattle Noise Suppression algorithm
 - Signal detection high efficiency modes
 - High accuracy voltage monitor & temp sensor
- Ease of use features
 - 1cell, 2cell and 3cell Li-ion battery support
 - Clock based power up/down
 - Auto clock rate detection: 16kHz to 192kHz
 - External 14V PVDD supply support
 - MCLK free operation
 - Thermal and over current protection
 - Programmable drive strength IO buffers
- Power Supplies and user interface
 - VBAT: 2.0V to 5.5V
 - VDD: 1.65V to 1.95V
 - IOVDD: 1.2V or 1.8V
 - VBAT_SNS: 2.0V to 10.0V
 - PVDD: 2.5V to 14V (Ext. PVDD mode)
 - I²S/TDM: 8 channels
 - I²C: 4 selectable addresses
- 48-Ball, 0.35mm Pitch, WCSP package

2 Applications

- Mobile phone, Tablets & Wearables
- Smart Speakers with Voice Assistance
- Bluetooth and Wireless speakers

3 Description

The TAS2573 is a digital input Class-D amplifier with an integrated Boost for higher power delivery in battery-operated systems. The device has integrated IV-Sense for real-time monitoring of the loudspeakers. An on-chip, low-latency DSP supports Texas Instruments SmartAmp speaker protection and audio tuning algorithms to enable high output SPL while keeping speakers in a safe operating region.

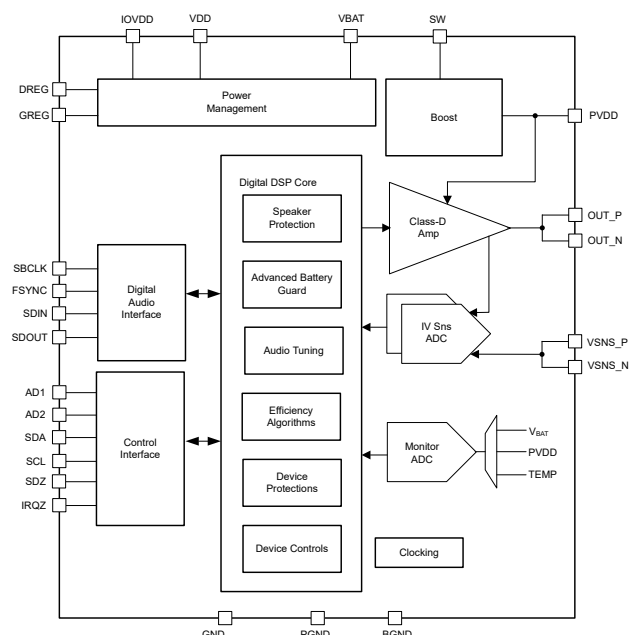
The device is optimized for delivering the best battery life with advanced efficiency optimization features like Class-H, Y-bridge and DSP algorithms. An advanced battery guard algorithm on the DSP manages peak output power delivery while avoiding any audio distortion when battery capacity is depleting. This algorithm is supported using a local battery voltage monitor ADC.

Up to four TAS2573 amps can share a common bus via I²S/TDM + I²C interfaces.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TAS2573	WCSP	3.15mm × 2.26mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



Functional block diagram

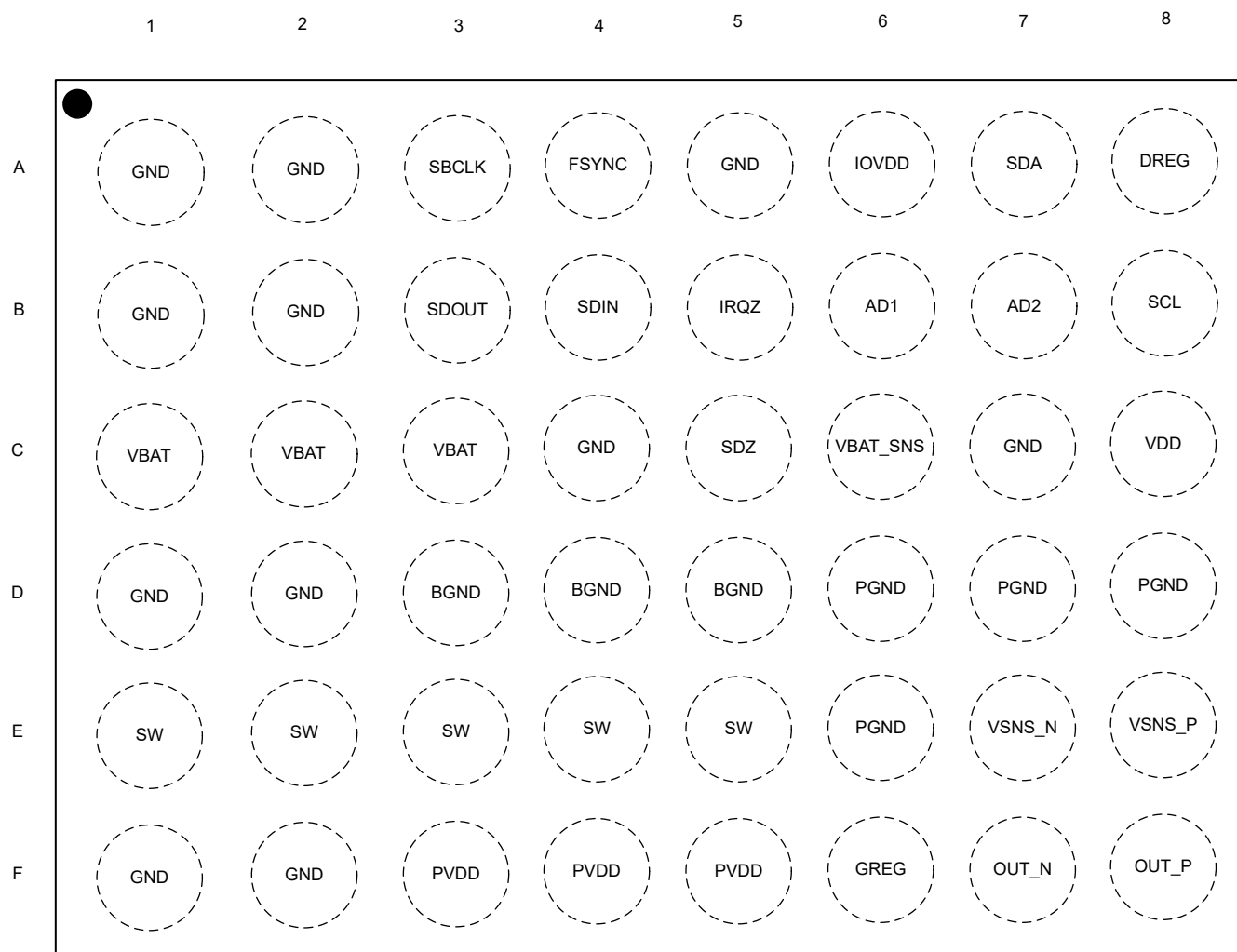


Table of Contents

1 Features	1	7.1 PAGE_0 Registers.....	53
2 Applications	1	7.2 PAGE_1 Registers.....	108
3 Description	1	8 Application and Implementation	124
4 Pin Configuration and Functions	3	8.1 Application Information.....	124
5 Specifications	6	8.2 Typical Application.....	124
5.1 Absolute Maximum Ratings.....	6	8.3 Power Supply Recommendations.....	132
5.2 ESD Ratings.....	6	8.4 Layout.....	132
5.3 Recommended Operating Conditions.....	6	9 Revision History	134
5.4 Thermal Information.....	7	10 Device and Documentation Support	135
5.5 Electrical Characteristics.....	7	10.1 Documentation Support.....	135
5.6 Timing Requirements.....	15	10.2 Receiving Notification of Documentation Updates.....	135
5.7 Timing Diagrams.....	17	10.3 Support Resources.....	135
5.8 Typical Characteristics.....	17	10.4 Trademarks.....	135
6 Detailed Description	23	10.5 Electrostatic Discharge Caution.....	135
6.1 Overview.....	23	10.6 Glossary.....	135
6.2 Functional Block Diagram.....	23	11 Mechanical, Packaging, and Orderable Information	136
6.3 Device Functional Modes.....	23	11.1 Package Option Addendum.....	137
6.4 Feature Description.....	31	11.2 Tape and Reel Information.....	138
6.5 Programming.....	48		
7 Register Maps	52		

4 Pin Configuration and Functions

Figure 4-1. Package Top Level View Pinout



ADVANCE INFORMATION

Pin Functions

PIN		Type ¹	DESCRIPTION
NAME	NO.		
AD1	B6	I	I ² C address pin LSB.
AD2	B7	I	I ² C address pin LSB+1.
BGND	D3	G	Boost ground. Connect to PCB GND plane strongly with multiple vias.
	D4		
	D5		
DREG	A8	P	Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to external load.
FSYNC	A4	I	I ² S word clock or TDM frame sync for Primary Audio Interface.
GREG	F6	P	High-side gate CP regulator output. Do not connect to external load.
GND	A1	G	Digital ground. Connect to PCB GND plane. Strong connection to ground plane required through multiple vias.
	A2		
	A5		
	B1		
	B2		
	C4		
	C7		
	D1		
	D2		
	F1		
	F2		
IOVDD	A6	P	1.2V or 1.8V Digital IO supply. Decouple to GND with capacitor.
IRQZ	B5	O	Open drain, active low interrupt pin. Pull up to IOVDD with resistor if optional internal pullup is not used.
OUT_N	F7	O	Class-D negative output.
OUT_P	F8	O	Class-D positive output.
PGND	D6	G	Class-D Power stage ground. Connect to PCB GND plane strongly through multiple vias.
	D7		
	D8		
	E6		
PVDD	F3	P	Integrated boost output and Class-D power stage supply.
	F4		
	F5		
SBCLK	A3	I	I ² S/TDM serial bit clock for Primary Audio Interface.
SCL	B8	I	I ² C Clock Pin. Pull up to IOVDD with a resistor.
SDA	A7	I/O	I ² C Data Pin. Pull up to IOVDD with a resistor.
SDIN	B4	I	I ² S or TDM serial data input for Primary Audio Interface.
SDOUT	B3	O	I ² S or TDM serial data output for Primary Audio Interface.
SDZ	C5	I	Active low hardware shutdown.
SW	E1	P	Boost converter switch input.
	E2		
	E3		
	E4		
	E5		

Pin Functions (continued)

PIN		Type ¹	DESCRIPTION
NAME	NO.		
VBAT	C1	P	Battery power supply input. Connect to 2.5V to 5.5V supply and decouple with a capacitor.
	C2		
	C3		
VBAT_SNS	C6	I	Battery sense terminal. Connect to 1S or 2S battery supply for remote battery sensing. Ground the pin if remote sensing is not used.
VDD	C8	P	Analog, digital power supply. Connect to 1.8V supply and decouple to GND with capacitor.
VSNS_N	E7	I	Voltage sense negative input. Connect to speaker negative terminal as close to speaker as possible. Add series resistor if EMI filter is used.
VSNS_P	E8	I	Voltage sense positive input. Connect to speaker positive terminal as close to speaker as possible. Add series resistor if EMI filter is used.

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply Voltage	PVDD	−0.3	19	V
Supply Voltage	VBAT	−0.3	6	V
Supply Voltage Sense	VBAT_SNS	−0.3	12	V
Supply Voltage	VDD, IOVDD	−0.3	2	V
Boost Switching Pin	SW	−0.7	19	V
Class-D Output	OUTP, OUTM	−0.7	19	V
Voltage Sense Pins	VSNSP, VSNSM	−0.3	30	V
High Side Drive Regulator	GREG	−0.3	PVDD + 6	V
Digital Supply Regulator	DREG	−0.3	1.65	V
Digital IO Pins	Digital pins referenced to IOVDD supply	−0.3	2	V
T _{stg}	Storage temperature	−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{BAT}	Battery Supply (1S mode and external PVDD mode of operation)	2.5	3.6	5.5	V
V _{BAT}	Battery Supply (2S mode of operation, Low volt battery mode of operation)	3	3.6	5.5	V
V _{BAT_SNS}	Battery Sense pin voltage	2.0		10	V
V _{BAT_LV}	Battery Voltage in Low volt battery mode of operation (connected to SW pin through inductor)	2.0	3.6	5.5	V
V _{BAT2S}	2Series Cell Battery Voltage (connected to SW pin through inductor)	4.7	7.2	10	V
V _{PVDD}	Amplifier supply - External PVDD Mode	V _{BAT}	12	14	V
V _{VDD}	Supply Voltage	1.65	1.8	1.95	V
V _{IOVDD}	IO Supply Voltage 1.8V	1.62	1.8	1.98	V
V _{IOVDD}	IO Supply Voltage 1.2V	1.08	1.2	1.32	V
R _{SPK}	Speaker resistance	3.2	8	38.4	Ω
L _{SPK}	Speaker inductance	5	33	100	μH
T _A	Ambient temperature	−40		85	°C
T _J	Junction temperature	−40		150	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		Standard JEDEC ⁽²⁾	EVM Board ⁽³⁾	UNIT
		YCG (DSBGA)	YCG (DSBGA)	
		36 PINS	36 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	61.9	28.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.3	-	°C/W
R _{θJB}	Junction-to-board thermal resistance	14.1	-	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.2	0.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	13.9	14	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
(2) JEDEC Standard 4 Layer PCB
(3) Measured using EVM Board

5.5 Electrical Characteristics

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AMPLIFIER PERFORMANCE - 15V INTERNAL BOOST 1S Mode						
P _{OUT}	Maximum Continuous Output Power - 1% THDN	R _L = 8 Ω + 33 μH		7.0		W
		R _L = 8 Ω + 33 μH, VBAT = 4.4V		8.5		W
		R _L = 6 Ω + 33 μH		7.3		W
		R _L = 4 Ω + 33 μH		7.2		W
		R _L = 4 Ω + 33 μH, VBAT = 4.4V		8.8		W
P _{OUT}	Maximum Continuous Output Power - 1% THDN, Low voltage battery mode	R _L = 8 Ω + 33 μH		7.0		W
		R _L = 8 Ω + 33 μH, VBAT = 4.4V		8.5		W
P _{OUT}	Maximum Continuous Output Power - 10% THDN	RL = 8 Ω + 33 μH, VBAT = 4.4V		10.7		W
		RL = 6 Ω + 33 μH, VBAT = 4.4V		10.6		W
		RL = 4 Ω + 33 μH, VBAT = 4.4V		10.6		W
η _{SYSTEM_0.5W}	System Efficiency at P _{OUT} = 0.5W	R _L = 8 Ω + 33 μH		86.6		%
		R _L = 8 Ω + 33 μH, VBAT = 4.4V		86.1		%
		R _L = 4 Ω + 33 μH		84.8		%
		R _L = 4 Ω + 33 μH, VBAT = 4.4V		84.5		%
η _{SYSTEM_1W}	System Efficiency at P _{OUT} = 1.0W	R _L = 8 Ω + 33 μH		85.5		%
		R _L = 8 Ω + 33 μH, VBAT = 4.4V		88.1		%
		R _L = 4 Ω + 33 μH		85.2		%
		R _L = 4 Ω + 33 μH, VBAT = 4.4V		86.7		%
η _{SYSTEM_1W}	System Efficiency at P _{OUT} = 1.0W, Low voltage battery mode.	R _L = 8 Ω + 33 μH		86.6		%
		R _L = 8 Ω + 33 μH, VBAT = 4.4V		87.7		%
η _{SYSTEM_MAX_POUT}	System Efficiency at 1% THD+N power Level	R _L = 8 Ω + 33 μH		79.4		%
η _{SYSTEM_MAX_POUT}	System Efficiency at 1% THD+N power Level	R _L = 4 Ω + 33 μH		76.3		%

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VN	Idle channel Noise	A-Weighted, Gain = 6dBV (Receiver Mode), DAC-Running		4.2		μV
		A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.2		μV
DNR	Dynamic Range	A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 μH, Gain = 6dBV (Receiver Mode)		114.0		dB
		A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 μH, Gain = 21dBV (Speaker Mode)		114.0		dB
THD+N	Total Harmonic distortion + Noise	POUT = 1 W, RL = 8 Ω + 33 μH		0.003		%
		POUT = 1 W, RL = 4 Ω + 33 μH		0.005		%
		POUT = 0.25 W, RL = 8 Ω + 33 μH, Gain = 6dBV (Receiver Mode)		0.003		%
KCP	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes in/out of mute, power up and power down, noise gate mode entry and exit. Measured as peak A-weighted voltage. RL = 8 Ω + 33 μH, Input = digital silence		-68		dBV
BW	Amplifier input signal Bandwidth	fs ≥ 96ksp/s, Gain error < Pass-Band Ripple		45		kHz
VFS	Full scale equivalent Voltage	Measured at -6dBFS Input		11.2		VRMS
		Measured at -6dBFS Input, Gain = 6dBV (Receiver Mode)		2.00		VRMS
AGAIN	Audio channel Gain programmability range	Gain programmability in steps of 0.5dB	0		21	dBV
AGAIN_ER	Amplifier Gain error	POUT = 1W		±0.1		dB
		POUT = 0.25W, Gain = 6dBV (Receiver Mode)		±0.1		dB
VOS	Output Offset Voltage	Idle channel	-1		1	mV
		Idle channel, Gain = 6dBV (Receiver Mode)	-1		1	mV
FPWM	Class-D PWM switching Frequency	Average clock frequency with SSM mode		384		kHz
PSRRVBAT	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mVpp, f_ripple = 217 Hz		115		dB
		VBAT = 3.6 V + 200 mVpp, f_ripple = 1 kHz		115		dB
		VBAT = 3.6 V + 200 mVpp, f_ripple = 20 kHz		85		dB
PSRRVD	VDD power-supply rejection ratio	VDD = 1.8 V + 200 mVpp, f_ripple = 217 Hz		110		dB
		VDD = 1.8 V + 200 mVpp, f_ripple = 1 kHz		110		dB
		VDD = 1.8 V + 200 mVpp, f_ripple = 20 kHz		90		dB
MUTE_ATT	Mute Attenuation	Device is MUTE mode. DAC modulator running		114		dB
AMPLIFIER PERFORMANCE - INTERNAL BOOST 2S Mode						
POUT_BOOST_2S	Maximum Continuous Output Power - 1% THDN	RL = 8 Ω + 33 μH		10.4		W
		RL = 8 Ω + 33 μH, VBAT2S = 8.4V		10.7		W
		RL = 6 Ω + 33 μH		12.1		W
		RL = 4 Ω + 33 μH		13.2		W
		RL = 4 Ω + 33 μH, VBAT2S = 8.4V		15.0		W

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\eta_{\text{SYSTEM_0.5W_2S}}$	System Efficiency at P _{OUT} = 0.5W	R _L = 8 Ω + 33 μH		85.1		%
		R _L = 8 Ω + 33 μH, VBAT2S= 8.4V		85.7		%
		R _L = 4 Ω + 33 μH		83.5		%
		R _L = 4 Ω + 33 μH, VBAT2S = 8.4V		82.7		%
$\eta_{\text{SYSTEM_1W_2S}}$	System Efficiency at P _{OUT} = 1.0W	R _L = 8 Ω + 33 μH		89.2		%
		R _L = 8 Ω + 33 μH, VBAT2S = 8.4V		89.5		%
		R _L = 4 Ω + 33 μH		86.2		%
		R _L = 4 Ω + 33 μH, VBAT2S = 8.4V		85.8		%
$\eta_{\text{SYSTEM_MAX_POUT_2S}}$	System Efficiency at 1% THD+N power Level	R _L = 8 Ω + 33 μH		87.5		%
		R _L = 8 Ω + 33 μH, VBAT2S= 8.4V		88.4		%
		R _L = 4 Ω + 33 μH		82.1		%
		R _L = 4 Ω + 33 μH, VBAT2S = 8.4V		82.9		%
V _{N_2S}	Idle channel Noise	A-Weighted, Gain = 6dBV (Receiver Mode), DAC-Running		4.2		μV
		A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.1		μV
DNR_2S	Dynamic Range	A-Weighted, -60 dBFS Method, Gain = 6dBV (Receiver Mode)		114.0		dB
		A-Weighted, -60 dBFS Method, Gain = 21dBV (Speaker Mode)		115.6		dB
THD+N_2S	Total Harmonic distortion + Noise	P _{OUT} = 1 W, R _L = 8 Ω + 33 μH, f _{in} = 1 kHz		0.003		%
		P _{OUT} = 1 W, R _L = 4 Ω + 33 μH, f _{in} = 1 kHz		0.003		%
		POUT = 0.25 W, RL = 8 Ω + 33 μH, fin = 1 kHz, Gain = 6dBV (Receiver Mode)		0.005		%
K _{CP_2S}	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes In/Out of Mute, Power Up and power Down, Noise Gate mode entry and Exit. Measured at Peak A-weighted Voltage. RL = 8 Ω + 33 μH, Input = Digital silence.		-68		dBV
PSRR _{VB AT2S}	VBAT2S power-supply rejection ratio	VBAT2S = 7.2 V + 200 mVpp, fripple = 217 Hz		115		dB
		VBAT2S = 7.2 V + 200 mVpp, fripple = 1 kHz		115		dB
		VBAT2S = 7.2 V + 200 mVpp, fripple = 20 kHz		90		dB
PSRR _{VB AT_2S}	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mVpp, f _{ripple} = 217 Hz		115		dB
		VBAT = 3.6 V + 200 mVpp, f _{ripple} = 1 kHz		115		dB
		VBAT = 3.6 V + 200 mVpp, f _{ripple} = 20 kHz		90		dB
PSRR _{VD D_2S}	VDD power-supply rejection ratio	VDD = 1.8 V + 200 mVpp, f _{ripple} = 217 Hz		110		dB
		VDD = 1.8 V + 200 mVpp, f _{ripple} = 1 kHz		110		dB
		VDD = 1.8 V + 200 mVpp, f _{ripple} = 20 kHz		90		dB

AMPLIFIER PERFORMANCE - EXTERNAL PVDD Mode

P _{OUT_EXT_PVDD}	Maximum Continuous Output Power - 1% THDN	R _L = 8 Ω + 33 μH		8.3		W
		R _L = 4 Ω + 33 μH		14.9		W

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _{OUT_EXT_PVDD}	Maximum Continuous Output Power - 10% THDN	RL = 8 Ω + 33 μH		10.3		W
		RL = 4 Ω + 33 μH		18.4		W
		RL = 4 Ω + 33 μH, PVDD=14V		24.5		W
η _{SYSTEM_EXT_0.5W}	System Efficiency at P _{OUT} = 0.5W	R _L = 8 Ω + 33 μH		83.9		%
		R _L = 4 Ω + 33 μH		80.0		%
η _{SYSTEM_EXT_1W}	System Efficiency at P _{OUT} = 1.0W	R _L = 8 Ω + 33 μH		88.1		%
		R _L = 4 Ω + 33 μH		84.2		%
η _{SYSTEM_EXT_MAX_POUT}	System Efficiency at 1% THD+N power Level	R _L = 8 Ω + 33 μH		93.2		%
		R _L = 4 Ω + 33 μH		88.5		%
V _{N_EXT}	Idle channel Noise	A-Weighted, Gain = 21dBV (Speaker Mode), DAC-Running		14.4		μV
DNR _{EXT}	Dynamic Range	A-Weighted, -60 dBFS Method, RL = 8 Ω + 33 μH		114.4		dB
THD+N _{EXT}	Total Harmonic distortion + Noise	P _{OUT} = 1 W, R _L = 8 Ω + 33 μH, f _{in} = 1 kHz		0.003		%
		P _{OUT} = 1 W, R _L = 4 Ω + 33 μH, f _{in} = 1 kHz		0.004		%
K _{CP_EXT}	Click and pop performance	All dynamic power up/downs of audio channel except for faults. Includes In/Out of Mute, Power Up and power Down, Noise Gate mode entry and Exit. Measured at Peak A-weighted Voltage. RL = 8 Ω + 33 μH, Input = Digital Silence		-68		dBV
V _{OS_EXT}	Output Offset Voltage	Idle channel	-1		1	mV
PSRR _{PVDD_EXT}	PVDD power-supply rejection ratio	PVDD = 12 V + 200 mV _{pp} , fripple = 217 Hz		115		dB
		PVDD = 12 V + 200 mV _{pp} , fripple = 1 kHz		115		dB
		PVDD = 12 V + 200 mV _{pp} , fripple = 20 kHz		95		dB
PSRR _{VBAT_EXT}	VBAT power-supply rejection ratio	VBAT = 3.6 V + 200 mV _{pp} , f _{ripple} = 217 Hz		115		dB
		VBAT = 3.6 V + 200 mV _{pp} , f _{ripple} = 1 kHz		115		dB
		VBAT = 3.6 V + 200 mV _{pp} , f _{ripple} = 20 kHz		90		dB
PSRR _{VDD_EXT}	VDD power-supply rejection ratio	VDD = 1.8 V + 200 mV _{pp} , f _{ripple} = 217 Hz		110		dB
		VDD = 1.8 V + 200 mV _{pp} , f _{ripple} = 1 kHz		110		dB
		VDD = 1.8 V + 200 mV _{pp} , f _{ripple} = 20 kHz		90		dB
Current and Voltage (I-V) Sense						
I _{SENSE_FS}	Current sense Full scale Input current	Default programmable setting, Measured at -6dBFS		2		A _{PK}
I _{SENSE_ACC}	Current-sense accuracy	f _{IN} = 1kHz, P _{OUT} = 1W		±1		%
		f _{IN} = 1kHz, P _{OUT} = 1W, 2S mode of operation		±1		%
		f _{IN} = 1kHz, P _{OUT} = 1W, External PVDD mode		±1		%
V _{SENSE_FS}	Full scale Voltage input	Default programmable setting, Measured at -6dBFS		13		V _{PK}

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{SENSE_A} CC	Voltage-sense accuracy	f _{IN} = 1kHz, P _{OUT} = 1W		±1		%
		f _{IN} = 1kHz, P _{OUT} = 1W, 2S mode of operation		±1		%
		f _{IN} = 1kHz, P _{OUT} = 1W, External PVDD mode		±1		%
V _{_BY_I} LI N	V/I sense gain relative Accuracy	f _{IN} = 20Hz - 20kHz, P _{OUT} ≥ 5mW to 0.1% THDN Power, , 0°C ≤ T _{AMB} ≤ +70°C, Calibrated wrt. Pilot = -40dBFS/16Hz (Single Tone)		±0.4		%
		f _{IN} = 20Hz - 20kHz, P _{OUT} ≥ 5mW to 0.1% THDN Power, 0°C ≤ T _{AMB} ≤ +70°C, Calibrated wrt. Pilot = -40dBFS/16Hz (Single Tone), 2S Mode of operation		±0.4		%
		f _{IN} = 20Hz - 20kHz, P _{OUT} ≥ 5mW to 0.1% THDN Power, 0°C ≤ T _{AMB} ≤ +70°C, RL = 4 Ω + 33 μH, 5A I-sense Full scale, External PVDD, Calibrated wrt. Pilot = -40dBFS/16Hz (Single Tone)		±0.4		%
Boost Converter						
V _{BOOST_} RANGE	Max Output Voltage programmability Range	Programmable in steps of 66mV	5.5		15	V
V _{BOOST_} STEP	Class-H Output Voltage Step Size			33		mV
V _{BOOST}	Output Boost Voltage	I _O = 0.1A. Average output value. V _{BOOST_MAX_CTRL} = max value		14.9		V
I _{BOOST_} CL	Peak Input Current Limit	BST_ILIM = Max Setting		5.1		A
I _{BOOST_} CL	Peak Input Current Limit	BST_ILIM = Min Setting		1.5		A
	Peak Input Current Limit Programmable step size			39.1		mA
Boost Converter 2S Mode of operation						
V _{BOOST_} RANGE	Output Voltage Range	Programmable in steps of 66mV	10		15	V
V _{BOOST_} STEP	Class-H Output Voltage Step Size			33		mV
I _{BOOST_} CL	Peak Input Current Limit	Max Setting		5.1		A
I _{BOOST_} CL	Peak Input Current Limit	Min Setting		1.5		A
TDM Serial Port						
	PCM Sample Rates and FSYNC Input Frequency		16		192	kHz
	SBCLK Input Frequency	I ² S/TDM Operation	0.512		24.57	MHz
	SBCLK Maximum Input Jitter	RMS Jitter below 40 kHz that can be tolerated without performance degradation			0.5	ns
		RMS Jitter above 40 kHz that can be tolerated without performance degradation			5	ns

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	SBCLK Cycles per FSYNC in I ² S and TDM Modes	Values: 64, 96, 128, 192, 256, 384 and 512	64		512	Cycles
PCM Playback Characteristics to fs ≤ 48 kHz						
fs	Sample Rates		16		48	kHz
	Audio Channel Passband LPF Corner	Ripple < pass-band ripple		0.454		fs
	Audio Channel Passband Ripple	20 Hz to LPF cutoff		± 0.1		dB
	Audio Channel Stop Band Attenuation	≥ 0.55 fs		60		dB
		≥ 1 fs		65		dB
	Audio Channel Group Delay	Fin = 1kHz, Class-H mode		31.5		1/fs
		Fin = 1kHz, Class-H bypassed		6.5		1/fs
		DC to 20kHz, HPF bypassed, Class-H bypassed		11.0		1/fs
		DC to 20kHz, HPF bypassed, Class-H mode		37.0		1/fs
	I-V Sense channel Low pass filter Cut-off frequency	Ripple < pass-band ripple		0.417		kHz
		IVSENSE_LPF_ENABLE = 1 , Ripple < pass-band ripple		0.125		kHz
	I-V Sense Channel Passband Ripple	20Hz to 20kHz		± 0.1		dB
	I-V Sense Channel Group Delay	Fin = 1kHz		4.8		fs
		DC to LPF Corner, HPF bypassed		13.7		fs
PCM Playback Characteristics to fs > 48 kHz						
fs	Sample Rates		88.2		192	kHz
	Audio Channel Passband LPF Corner	fs = 96 kHz		0.469		fs
		fs = 192 kHz		0.234		fs
	Audio Channel Passband Ripple	20 Hz to LPF cutoff		± 0.2		dB
	Audio Channel Stop Band Attenuation	fs = 96 kHz, fin ≥ 0.55 fs		60		dB
		fs = 96 kHz, fin ≥ 1 fs		65		dB
		fs = 192 kHz, 0.55 fs ≥ fin ≥ 0.275 fs		60		dB
	Audio Channel Group Delay	fin=1kHz, fs=96 kHz, Class-H mode		56.7		1/fs
		DC to 40kHz, fs=96 kHz, HPF Bypassed, Class-H bypassed		8.6		1/fs
		DC to 40kHz, fs=192 kHz, HPF Bypassed, Class-H Mode		117.8		1/fs
	I-V Sense channel Low pass filter Cut-off frequency	fs = 96kHz		0.208		kHz
		fs = 192kHz		0.104		kHz
		IVSENSE_LPF_ENABLE = 1, fs = 96kHz		0.125		kHz
		IVSENSE_LPF_ENABLE = 1, fs = 192kHz		0.063		kHz
	I-V Sense Channel Passband Ripple	20 Hz to 20kHz		±0.1		fs
	I-V Sense Channel Group Delay	Fin = 1kHz		6.3		fs
		DC to LPF Corner, HPF bypassed		8.7		fs
Sense Circuits						
	Temperature Measurement Range		−40		150	°C
	Temperature Measurement Resolution			2		°C

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Temperature Measurement Accuracy	Measured at 25C		±2.5		°C
	VBAT Measurement Range	VBAT pin			6	V
	VBAT Measurement Range	VBAT_SNS pin			12	V
	VBAT Measurement Resolution	VBAT pin		1.25		mV
	VBAT Measurement Resolution	VBAT_SNS pin		2.5		mV
	VBAT Measurement Accuracy	VBAT pin, measured at 3.6V		±25		mV
	VBAT Measurement Accuracy	VBAT_SNS pin, measured at 7.2V		±50		mV
	PVDD Measurement Range				18	V
	PVDD Measurement Resolution			3.75		mV
	PVDD Measurement Accuracy			±75		mV
Protection Circuits						
	Thermal shutdown temperature			140		°C
	Thermal shutdown retry time			1.5		s
	VBAT undervoltage lockout threshold (UVLO)	UVLO is asserted	1.9			V
		UVLO is released		2.3		V
	VDD undervoltage lockout threshold (UVLO)	UVLO is asserted	1.4			V
		UVLO is released		1.6		V
	PVDD undervoltage lockout threshold (UVLO)	UVLO is asserted, external PVDD mode only	2.6			V
		UVLO is released, external PVDD mode only		2.8		V
	PVDD overvoltage lockout threshold (OVLO)	OVLO is asserted, OVLO protection enabled.		16		V
	Output Short circuit protection	Output to Output, Output to GND, Output to PVDD, Output to VBAT, H-bridge mode		4.1		A
Power up/down Time						
T _{STDBY}	Turn ON time from SDZ Asserted to device ready for i2c Command				300	us
T _{ACTIVE}	Turn ON time from release of Software Shutdown to Amplifier output Active	Volume ramping disabled		1.6		ms
		Volume ramping enabled		3.9		ms
T _{TURNOFF}	Turn OFF time from assertion of Software Shutdown to Amplifier output Hi-Z	Volume ramping disabled		0.2		ms
		Volume ramping enabled		13.9		ms
Current Consumption - Internal Boost Mode						
I _{Q_HW_SD}	Current consumption in Hardware Shutdown	VBAT, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
I _{Q_SW_SD}	Current consumption in Software Shutdown	VBAT, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{Q_NG}	Current consumption in Idle channel	VBAT, P _{OUT} = 0, Noise Gate enabled		0.19		mA
		VDD, P _{OUT} = 0, Noise Gate enabled		2.6		mA
		IOVDD, P _{OUT} = 0, Noise Gate enabled		0.1		mA
		Total Power, P _{OUT} = 0, Noise Gate enabled		5.5		mW
I _{Q_IDLE}	Current consumption in Idle channel	VBAT, P _{OUT} = 0, Noise gate disabled		0.65		mA
		VDD, P _{OUT} = 0, Noise gate disabled		9.3		mA
		IOVDD, P _{OUT} = 0, Noise gate disabled		0.1		mA
		Total Power, P _{OUT} = 0, Noise gate disabled		19		mW
I _{Q_IDLE}	Current consumption in Idle channel, Low voltage battery mode of operation	VBAT, P _{OUT} = 0, Noise gate disabled		0.67		mA
		VBAT_LV (Current in SW + VBAT_SNS), P _{OUT} = 0, Noise gate disabled		0.3		mA
		VDD, P _{OUT} = 0, Noise gate disabled		9.3		mA
		IOVDD, P _{OUT} = 0, Noise gate disabled		0.1		mA
		Total Power, P _{OUT} = 0, Noise gate disabled		20		mW
Current Consumption - Internal Boost Mode 2S Mode						
I _{Q_HW_SD}	Current consumption in Hardware Shutdown	VBAT, SDZ=0		0.1		uA
		VBAT2S, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA
I _{Q_SW_SD}	Current consumption in Software Shutdown	VBAT, All clocks Stopped		0.1		uA
		VBAT2S, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I _{Q_NG}	Current consumption in Idle channel	VBAT, P _{OUT} = 0, Noise gate enabled		0.1		mA
		VBAT2S, P _{OUT} = 0, Noise gate enabled		0.1		mA
		VDD, P _{OUT} = 0, Noise gate enabled		2.7		mA
		IOVDD, P _{OUT} = 0, Noise gate enabled		0.1		mA
		Total Power, P _{OUT} = 0, Noise gate enabled		5.8		mW
I _{Q_IDLE}	Current consumption in Idle Channel	VBAT, P _{OUT} = 0, Noise gate disabled		0.5		mA
		VBAT2S, P _{OUT} = 0, Noise gate disabled		0.35		mA
		VDD, P _{OUT} = 0, Noise gate disabled		9.3		mA
		IOVDD, P _{OUT} = 0, Noise gate disabled		0.1		mA
		Total Power, P _{OUT} = 0, Noise gate disabled		21.2		mW
Current Consumption - External PVDD Mode						
I _{Q_HW_SD}	Current consumption in Hardware Shutdown	PVDD, SDZ=0		1		uA
		VBAT, SDZ=0		0.1		uA
		VDD, SDZ=0		0.2		uA
		IOVDD, SDZ=0		0.1		uA

TA = 25 °C, VBAT = 3.6 V, VBAT2S = 7.2V (2S mode enabled), PVDD = 12 V (External PVDD mode enabled), VDD = 1.8 V, IOVDD = 1.8V RL = 8Ω + 33μH, LBOOST = 1μH, fin = 1 kHz, fs = 48 kHz, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.1A, SDZ = 1, VBAT_BIAS_SEL2 = 10 for low voltage Battery mode, Noise Gate mode disabled, Measured filter free with an Audio Precision with a 22 Hz to 20 kHz un-weighted bandwidth (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{Q_SW_SD}	Current consumption in Software Shutdown	PVDD, All clocks Stopped		1		uA
		VBAT, All clocks Stopped		0.1		uA
		VDD, All clocks Stopped		12		uA
		IOVDD, All clocks Stopped		0.1		uA
I _{Q_NG}	Current consumption in Idle channel	PVDD, P _{OUT} = 0, Noise gate enabled		0.1		mA
		VBAT, P _{OUT} = 0, Noise gate enabled		0.12		mA
		VDD, P _{OUT} = 0, Noise gate enabled		2.6		mA
		IOVDD, P _{OUT} = 0, Noise gate enabled		0.1		mA
		Total Power, P _{OUT} = 0, Noise gate enabled		5.9		mW
I _{Q_IDLE}	Current consumption in Idle channel	PVDD, P _{OUT} = 0, Noise gate disabled		0.2		mA
		VBAT, P _{OUT} = 0, Noise gate disabled		0.5		mA
		VDD, P _{OUT} = 0, Noise gate disabled		9.2		mA
		IOVDD, P _{OUT} = 0, Noise gate disabled		0.1		mA
		Total Power, P _{OUT} = 0, Noise gate disabled		20.5		mW
DIGITAL IOS						
V _{IH}	High-level digital input logic voltage threshold	All digital pins	0.7 x IOVDD			V
V _{IL}	Low-level digital input logic voltage threshold	All digital pins	0.3 x IOVDD			V
V _{OH}	High-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I _{OH} = 100µA	IOVDD - 0.2 V			V
V _{OL}	Low-level digital output voltage	All digital pins except SDA, SCL and IRQZ; I _{OL} = -100µA	0.2			V
V _{OL(I2C)}	Low-level digital output voltage	SDA and SCL; I _{OL} = -1mA	0.2 x IOVDD			V
V _{OL(IRQZ)}	Low-level digital output voltage for open drain output	IRQZ pin; I _{OL} = -1mA	0.2			V
I _{IH}	Input logic-high leakage for digital inputs	All digital pins; Input = IOVDD.	-1		1	µA
I _{IL}	Input logic-low leakage for digital inputs	All digital pins; Input = GND	-1		1	µA
C _{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R _{PD}	Pull down resistance for digital input/IO pins when asserted on	All digital pins. Pull down resistance option enabled		18		kΩ

5.6 Timing Requirements

TA = 25 °C, VDD = IOVDD = 1.8 V (unless other wise noted)

		MIN	NOM	MAX	UNIT
I2C - Standard-Mode					
f _{SCL}	SCL clock frequency	0		100	kHz
t _{HD,STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			μs
t _{LOW}	LOW period of the SCL clock	4.7			μs
t _{HIGH}	HIGH period of the SCL clock	4			μs
t _{SU,STA}	Setup time for a repeated START condition	4.7			μs

TAS2573

SLASFM6 – OCTOBER 2026

 $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = I_{OVDD} = 1.8\text{ V}$ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{HD;DAT}$	Data hold time: For I ² C bus devices	0		3.45	μs
$t_{SU;DAT}$	Data set-up time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4			μs
t_{BUF}	Bus free time between a STOP and START condition	4.7			μs
C_b	Capacitive load for each bus line			400	pF
I2C - Fast-Mode					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			μs
t_{LOW}	LOW period of the SCL clock	1.3			μs
t_{HIGH}	HIGH period of the SCL clock	0.6			μs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6			μs
$t_{HD;DAT}$	Data hold time: For I ² C bus devices	0		0.9	μs
$t_{SU;DAT}$	Data set-up time	100			ns
t_r	SDA and SCL rise time	$20 + 0.1 \times C_b$		300	ns
t_f	SDA and SCL fall time	$20 + 0.1 \times C_b$		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6			μs
t_{BUF}	Bus free time between a STOP and START condition	1.3			μs
C_b	Capacitive load for each bus line			400	pF
I2C - Fast-Mode Plus					
f_{SCL}	SCL clock frequency	0		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26			μs
t_{LOW}	LOW period of the SCL clock	0.5			μs
t_{HIGH}	HIGH period of the SCL clock	0.26			μs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26			μs
$t_{HD;DAT}$	Data hold time: For I ² C bus devices	0			μs
$t_{SU;DAT}$	Data set-up time	50			ns
t_r	SDA and SCL Rise Time			120	ns
t_f	SDA and SCL Fall Time			120	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.26			μs
t_{BUF}	Bus free time between a STOP and START condition	0.5			μs
C_b	Capacitive load for each bus line			550	pF
TDM Port					
f_{sbclk}	SBCLK Frequency range	0.384		24.576	MHz
$t_H(SBCLK)$	SBCLK high period	$0.35/f_{sbclk}$			ns
$t_L(SBCLK)$	SBCLK low period	$0.35/f_{sbclk}$			ns
$t_{SU}(FSYNC)$	FSYNC setup time	8			ns
$t_{HLD}(FSYNC)$	FSYNC hold time	8			ns
$t_{SU}(SDIN)$	SDIN setup time	8			ns
$t_{HLD}(SDIN)$	SDIN hold time	8			ns
$t_d(SBCLK-SDOUT)$	SBCLK to SDOUT delay : 10% of SBCLK falling edge or 90% of SBCLK rising edge to 50% of SDOUT, $I_{OVDD}=1.8\text{V}$			13	ns

$T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = I_{OVDD} = 1.8\text{ V}$ (unless other wise noted)

		MIN	NOM	MAX	UNIT
$t_{d(SBCLK\text{-}SDOUT)}$	SBCLK to SDOUT delay : 10% of SBCLK falling edge or 90% of SBCLK rising edge to 50% of SDOUT, $I_{OVDD}=1.2\text{V}$			18	ns
$t_r(SBCLK)$	SBCLK rise time : 10 % - 90 %		$0.15 / f_{sbclk}$		ns
$t_f(SBCLK)$	SBCLK fall time : 90 % - 10 %		$0.15 / f_{sbclk}$		ns

5.7 Timing Diagrams

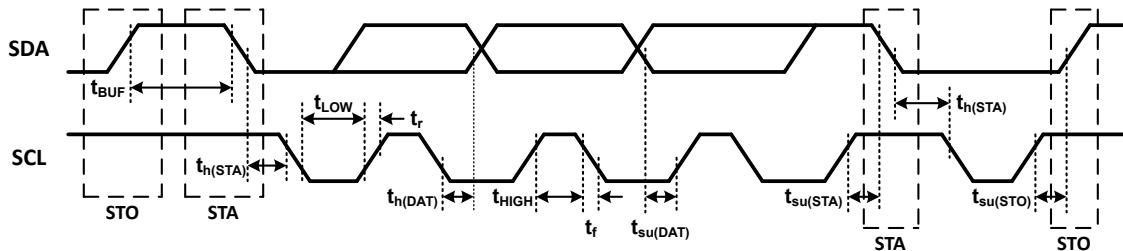


Figure 5-1. I²C timing diagram

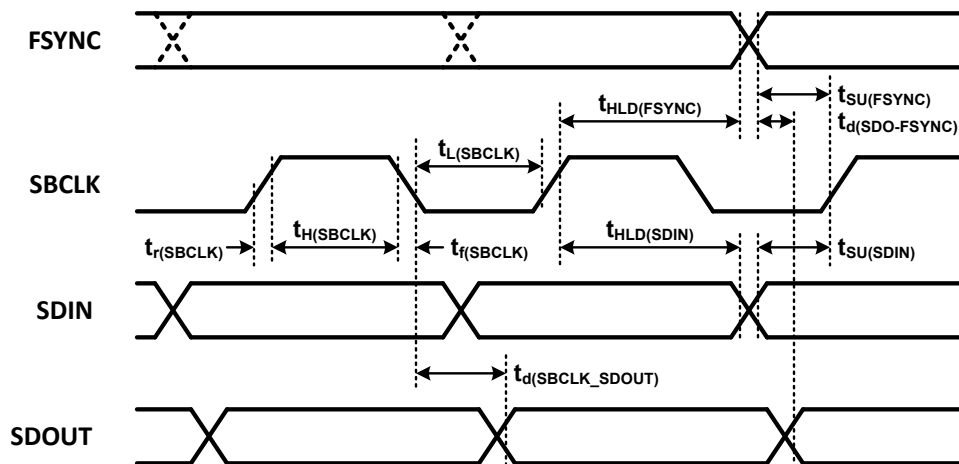


Figure 5-2. I²S/TDM timing diagram

5.8 Typical Characteristics

$T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 3.6\text{V}$, $V_{BAT2S} = 7.2\text{V}$ (2S mode enabled), $P_{VDD} = 12\text{V}$ (External P_{VDD} mode enabled), $V_{DD}=1.8\text{V}$, $I_{OVDD}=1.8\text{V}$, Load = $8\Omega + 33\mu\text{H}$, $L_{BOOST} = 1\mu\text{H}$, $F_{IN} = 1\text{kHz}$, $F_s = 48\text{ kHz}$, Gain = 21dBV, BST_ILIM (1S Boost mode) = 5.1A, BST_ILIM (2S Boost mode) = 5.0A $SDZ=1$, $V_{BAT_BIAS_SEL2} = 10$ for low voltage battery mode, Noise gate mode disabled, Measured filter free with an Audio Precision with a 22Hz to 20kHz un-weighted bandwidth, unless otherwise noted.

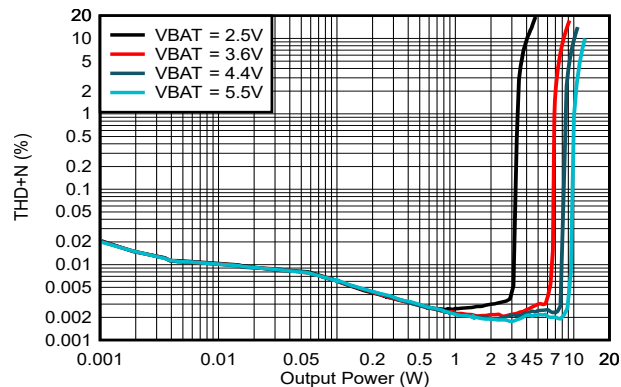
 $R_L = 8\Omega$

Figure 5-3. THD+N vs Output Power

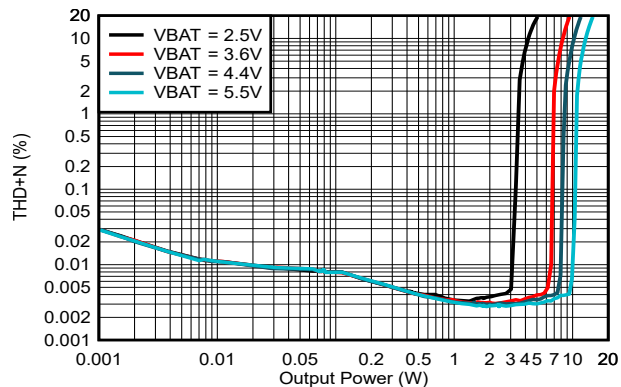
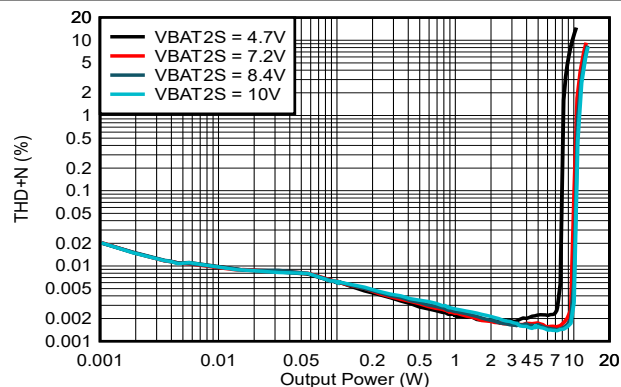
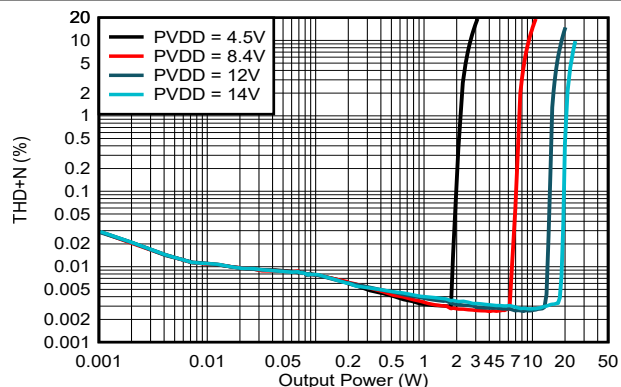
 $R_L = 4\Omega$

Figure 5-4. THD+N vs Output Power

 $R_L = 8\Omega$

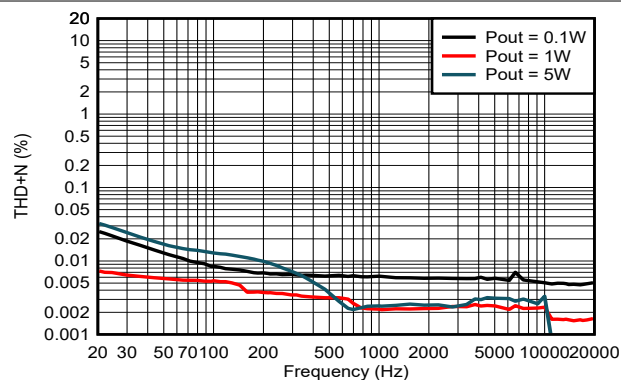
2S Battery Mode

Figure 5-5. THD+N vs Output Power

 $R_L = 4\Omega$

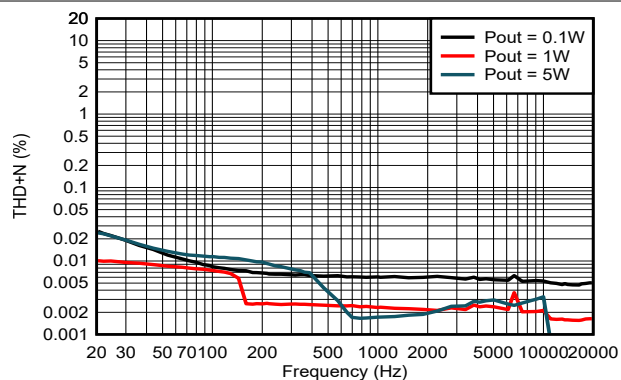
External PVDD mode

Figure 5-6. THD+N vs Output Power

 $R_L = 8\Omega$

VBAT = 4.4V

Figure 5-7. THD+N vs Frequency

 $R_L = 8\Omega$

VBAT2S = 8.4V

2S Battery mode

Figure 5-8. THD+N vs Frequency

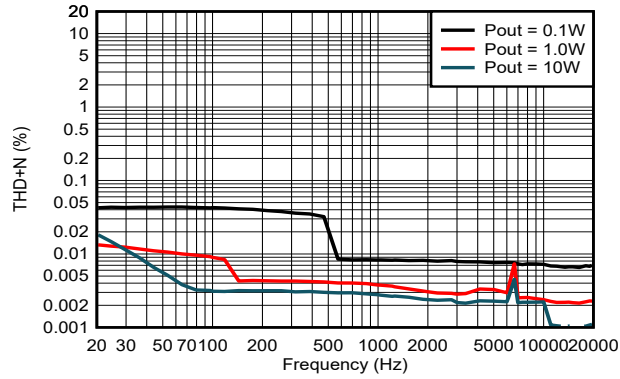


Figure 5-9. THD+N vs Frequency

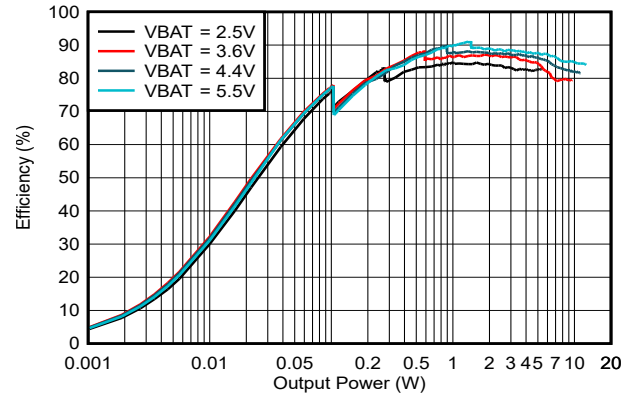


Figure 5-10. Efficiency vs Output Power

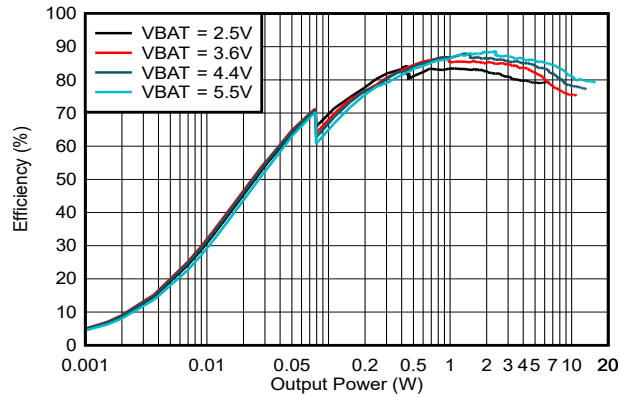


Figure 5-11. Efficiency vs Output Power

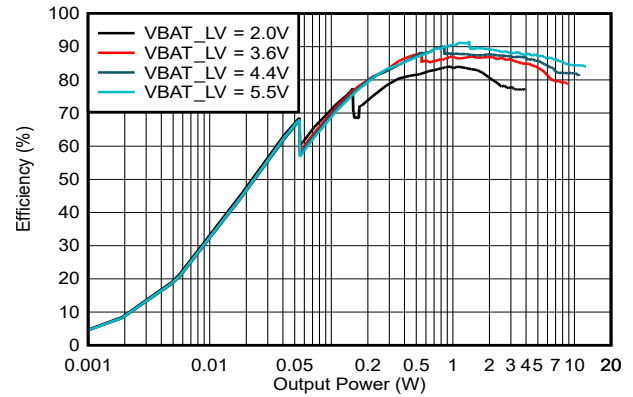


Figure 5-12. Efficiency vs Output power

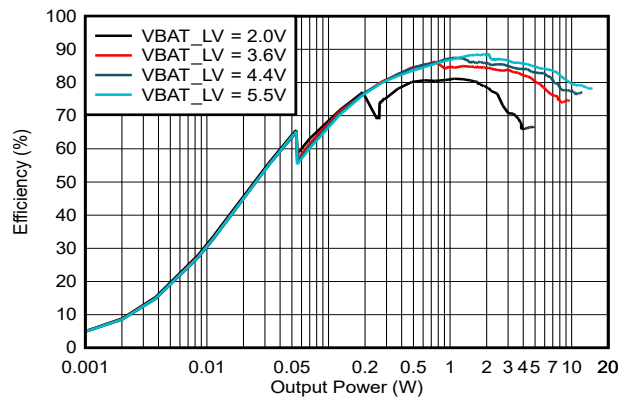


Figure 5-13. Efficiency vs Output power

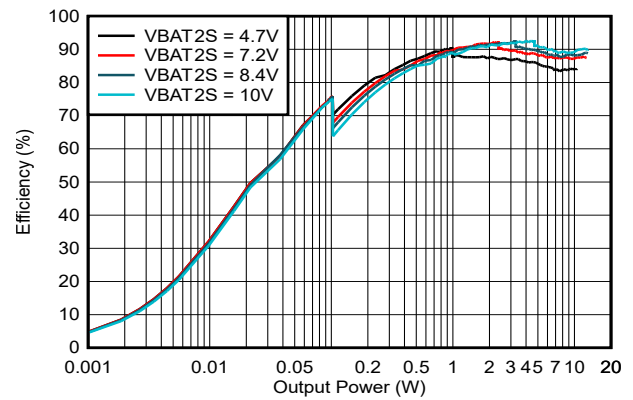


Figure 5-14. Efficiency vs Output power

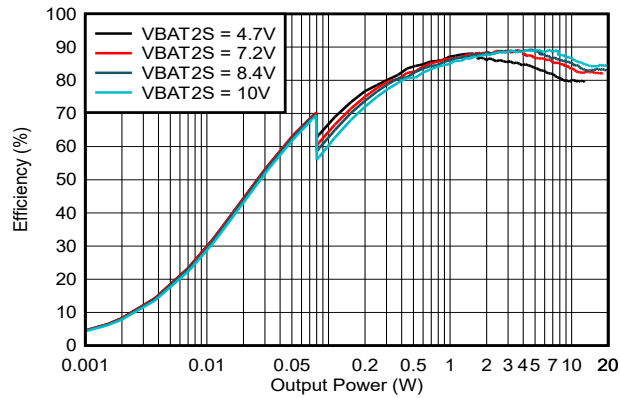

 $R_L = 4\Omega$ 2S Battery mode

Figure 5-15. Efficiency vs Output power

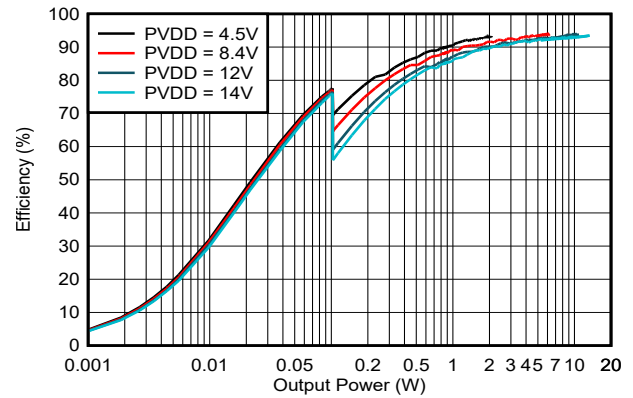

 $R_L = 8\Omega$ External PVDD mode

Figure 5-16. Efficiency vs Output Power

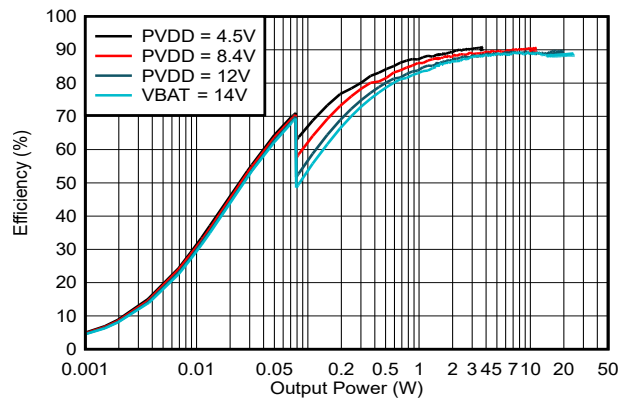

 $R_L = 4\Omega$ External PVDD mode

Figure 5-17. Efficiency vs Output Power

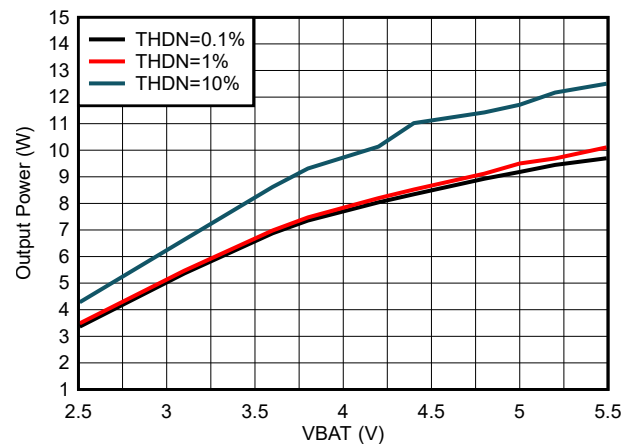

 $R_L = 8\Omega$

Figure 5-18. Output Power vs Battery voltage

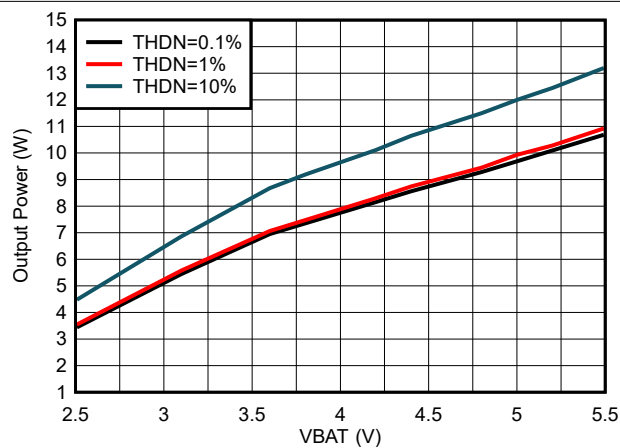

 $R_L = 4\Omega$

Figure 5-19. Output Power vs Battery voltage

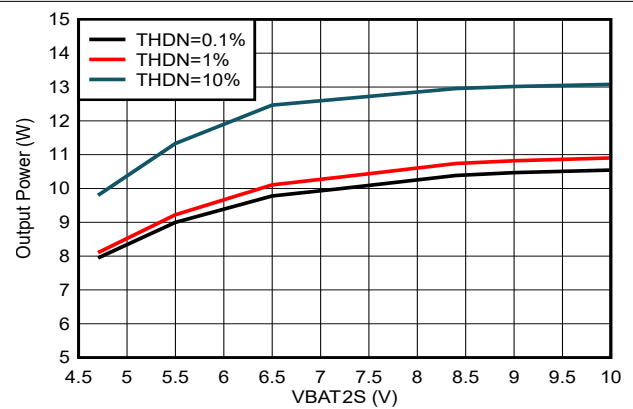
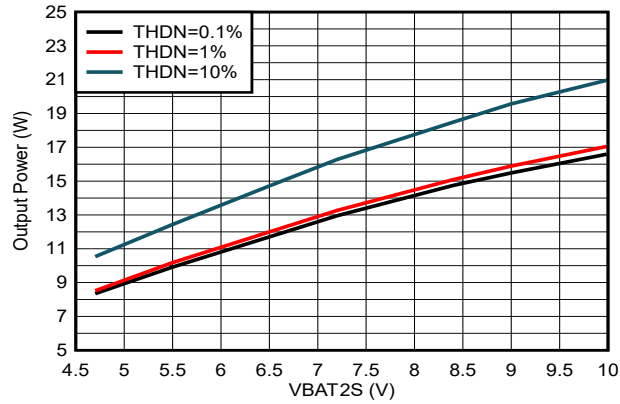
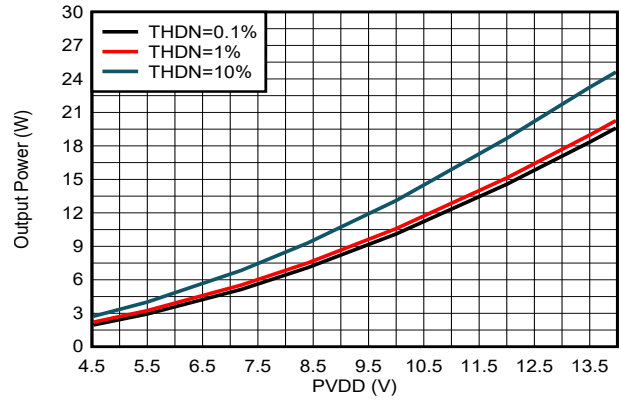

 $R_L = 8\Omega$ 2S Battery Mode

Figure 5-20. Output Power vs 2S Battery voltage



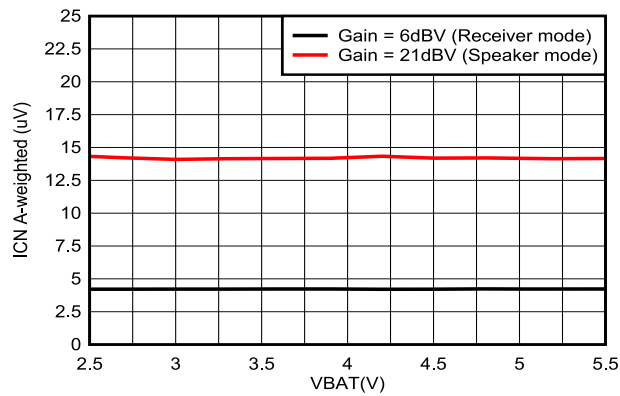
$R_L = 4\Omega$ 2S Battery Mode

Figure 5-21. Output Power vs 2S Battery voltage



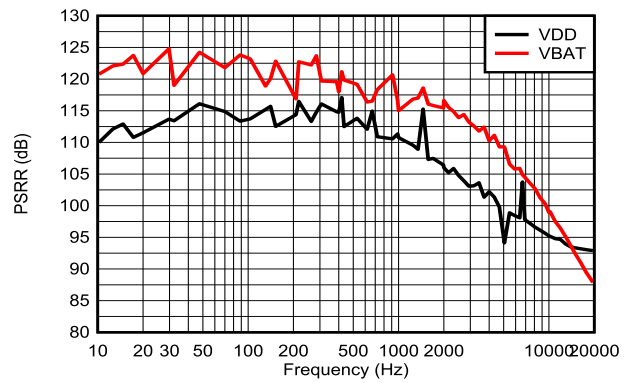
$R_L = 4\Omega$ External PVDD mode

Figure 5-22. Output Power vs external PVDD voltage



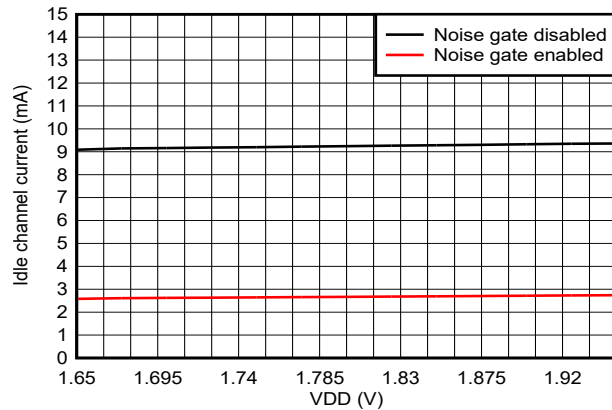
$R_L = 8\Omega$

Figure 5-23. Idle channel Noise vs VBAT voltage



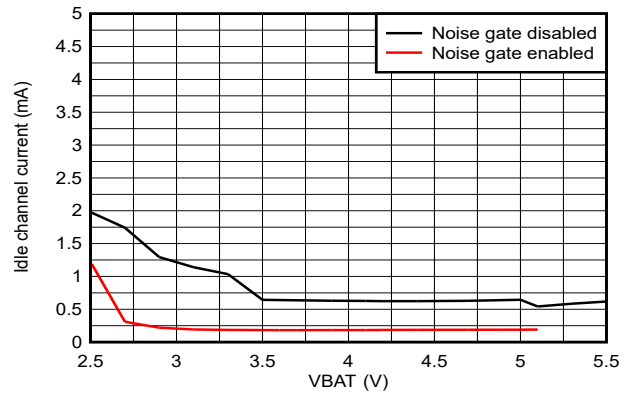
$R_L = 8\Omega$

Figure 5-24. PSRR vs Frequency



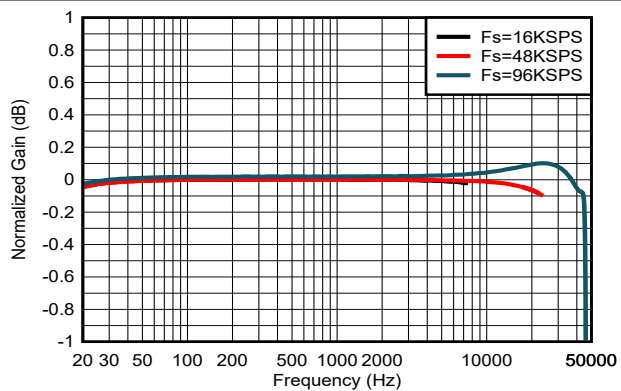
$R_L = 8\Omega$ DSP algorithms disabled

Figure 5-25. Idle channel current vs VDD voltage



$R_L = 8\Omega$

Figure 5-26. Idle channel current vs VBAT voltage

 $R_L = 8\Omega$ **Figure 5-27. Audio channel frequency response**

6 Detailed Description

6.1 Overview

The TAS2573 is a mono digital input Class-D amplifier optimized for delivering the highest efficiency across all powers for longer battery life operation. The device comes with a small design size for board space-constrained applications. The device integrates Class-H Boost with 33mV step size resolution for class-H control, highly accurate speaker voltage and current sensors, and battery/temperature sensors for system-level protection features. An on-chip, low-latency DSP supports speaker protection, audio enhancement and battery protection algorithms.

6.2 Functional Block Diagram

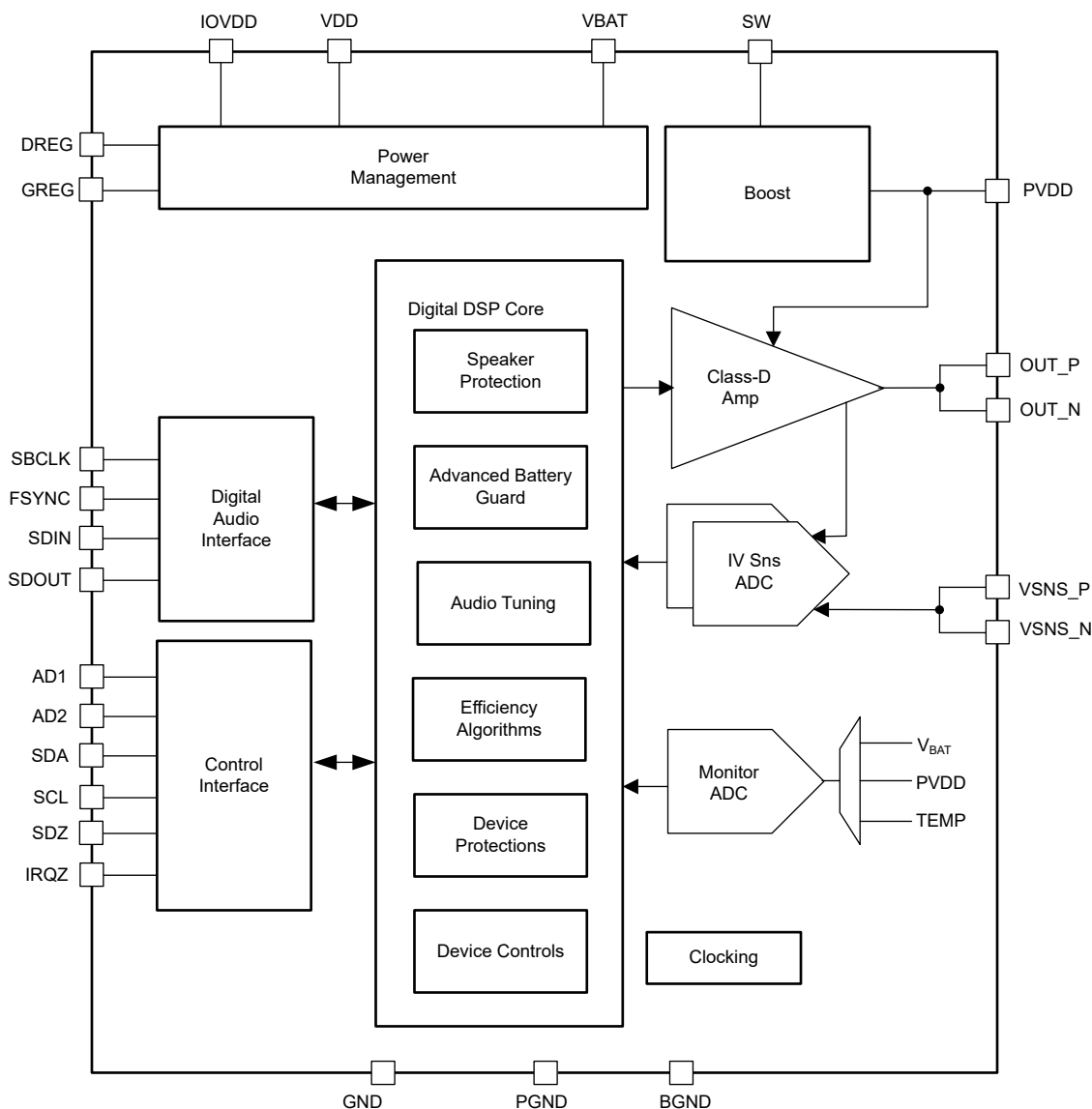


Figure 6-1. Top Level Functional block diagram

6.3 Device Functional Modes

6.3.1 Operational Modes

6.3.1.1 Hardware Shutdown

The device can be powered down by asserting SDZ pin low. The shutdown behavior of the device when SDZ pin is pulled low is controlled by SDZ_MODE register settings.

In Hardware Shutdown mode (SDZ_MODE[1:0] = 00 or 01) if the SDZ pin is asserted low, the device consumes the minimum quiescent current from VDD and VBAT supplies. All registers lose state in this mode and go back to default settings, and I²C communication is disabled.

If configured in SDZ_MODE[1:0] = 00, when the SDZ pin is asserted low while audio is playing, the device follows the normal power down sequencing like volume ramp down on the audio (if enabled), stop the Class-D switching, power down analog and digital blocks to maintain no power down pop and finally put the device into Hardware Shutdown mode. I²C communication is disabled while the SDZ pin is asserted low in this mode.

If configured in SDZ_MODE[1:0] = 01, when the SDZ pin is asserted low the device immediately enters the hardware shutdown and does not go through any power-down sequencing routine. TI recommends to maintain that the audio input signal is ramped down to the idle channel before asserting the SDZ pin low in this mode (device software mute mode can be used to realize this). I²C communication is disabled while the SDZ pin is asserted low in this mode.

Finally, the device can be configured to Software shutdown mode by setting SDZ_MODE[1:0] = 10. In this mode, when the SDZ pin is pulled low, the device follows normal power-down sequencing and enter software shutdown mode. All the device register configuration programmed is retained as is from the state the device is in before the SDZ pin is pulled low. I²C communication is still available while the SDZ pin is asserted low in this mode.

Table 6-1. Shutdown Control

SDZ_MODE[1:0]	Configuration
00 (default)	Hardware shutdown mode with power-down sequencing
01	Hardware shutdown mode - immediate
10	Software shutdown mode (All register values retained)
11	Reserved

When SDZ_MODE[1:0] is 00 or 10, the device goes through shutdown sequencing and the SDZ pin must be held low for the entire duration of the shutdown time. The shutdown time is specified in the Power up/down Time section of the Electrical Characteristics section. When SDZ is released, the device samples the AD1 and AD2 pins and enter the software shutdown mode.

6.3.1.2 Software Power Modes Control and Software Reset

The TAS2573 power state can be controlled using the register MODE[1:0]. Change in any of the MODE settings does not cause the device to lose any of the existing device configuration register settings.

Active state: When MODE[1:0] is configured as '00', the device enters an active mode of operation with the audio and the I-V sense channels powered up with proper power-up sequencing to minimize the click and pop. Speaker voltage and current sensing are operational if enabled.

Mute state: When MODE[1:0] is configured as '01', the device enters mute mode of operation. If the state of the device is software shutdown before the mute state is programmed, the audio and the I-V sense channels powers up with proper power-up sequencing to minimize the click and pop and then the channels enter into mute mode. If the audio channel is active when the mute state is asserted, the device volume ramps down the Class-D amplifier to a mute state. During mute the Class-D still switches, but transmits no audio content. If mute is de-asserted and the device is configured into an active state, the device volume ramps back to the programmed digital volume setting.

Software shutdown state: When MODE[1:0] is configured as '10', the device enters software shutdown mode. This mode powers down all analog blocks required to playback audio but does not cause the device to lose

register state. If audio is playing when Software Shutdown is asserted, the Class-D volume ramps down before shutting down. When de-asserted, the Class-D begins switching and volume ramp back to the programmed digital volume setting.

Clock based Active and shutdown state: When MODE[1:0] is configured as '11' the device toggles between Active and Shutdown state based on valid ASI clock signals applied on the ASI input pins, BCLK and FSYNC. When clocks are applied, the device automatically detects the clock signals and follow proper power-up sequencing to avoid any power-up click and pop. When the audio channels are powered up and the ASI clock is removed, the device automatically starts power-down sequencing and avoid any click and pop. TI recommends to do a volume ramp-down in the input data stream before stopping the clocks for the best pop & click experience (device software mute mode can be used to realize this).

Table 6-2. Software Mode Control

MODE[1:0]	Configuration
00	Device in active mode of operation
01	Reserved
10 (default)	Device in software shutdown mode
11	Device in Clock based Active and shutdown mode

TAS2573 can be reset to the default configuration by setting the SW_RESET register to '1'. If the device is powered up, when the SW_RESET bit is set high, all the channels are powered down immediately. All the registers are restored to the default state when SW_RESET is set high. This bit is self-clearing and goes back to '0' once the reset is complete.

The device can also signal to the host once the status of the device reaches Active mode of operation using the INT_LTCH0[1] bit (Section 6.3.2). This bit is a live device status bit and reflects the device status in real-time. This bit is set high when the device is in Active mode and set low when the device is in shutdown mode.

6.3.1.3 Efficiency and power saving modes

TAS2573 has multiple power-saving modes of operation designed to achieve the highest system level efficiency under all operating conditions. The device transitions from one mode to the next based on the configured mode and the signal condition. The transitions from one mode to another are automatic and designed to maintain high-performance audio levels during the transition of the modes.

EFFICIENCY_MODE[1:0] register allows for configuration of the Music efficiency and Noise gate modes of operation

Table 6-3. Efficiency Mode Control

EFFICIENCY_MODE[1:0]	Configuration
00	Music Efficiency & Noise gate mode disabled
01	Noise gate mode only
10	Music Efficiency mode only
11 (default)	Music Efficiency & Noise gate mode both enabled

6.3.1.3.1 Noise Gate

When the Noise gate feature is enabled, the device automatically detects periods of silence during active playback mode and reduces the idle channel power consumption significantly to extend the battery life. This feature is useful for signals playback having long periods of silence, eg voice calls, movie tracks, etc.

The device monitors the input audio signal level against the programmed Noise gate threshold configured by the `NG_TH_LVL[2:0]` register. When the audio signal falls below the threshold, an internal Hysteresis timer is enabled. If the signal level remains below the configured `NG_TH_LVL[2:0]` for the entire duration of the `NG_HYST_TIMER[1:0]`, the device enters into the Noise gate mode and reduces the idle channel power consumption. In the Noise gate mode of operation, the high switching blocks like class-D PWM output are turned OFF and outputs are pulled low. The output impedance of class-D can be controlled when the Noise gate mode is active using the `CLASSD_HIZ_MODE` register. While the Noise gate mode is active, class-D outputs are not switching and the device does not produce any audio output signal. When the device is in Noise gate mode, the `NG_STATUS` bit is set as high and when the device comes out of noise gate mode, the status bit is set to low.

When the signal level increases above the `NG_TH_LVL[1:0]`, the device automatically wakes up the blocks in low IQ mode and starts playing out the audio input signals. The wake up from Noise gate maintains the signal fidelity by buffering the input signal data during the transition time from noise gate mode to active playback mode. The device does not lose any audio input samples while transitioning from noise gate to active playback.

The transition into noise gate mode and recovery out of noise gate mode is designed to be click and pop-free by following the proper shutdown and power up sequencing.

Table 6-4. Noise gate threshold

<code>NG_TH_LVL[2:0]</code>	Configuration
000	-85 dBFs
001	-90 dBFs
010	-95 dBFs
011	-100 dBFs
100 (default)	-105 dBFs
101	-110 dBFs
110	-115 dBFs
111	-120 dBFs

Table 6-5. Noise gate hysteresis timer

<code>NG_HYST_TIMER[1:0]</code>	Configuration
00	10ms
01 (default)	50ms
10	100ms
11	1000ms

6.3.1.3.2 Music Efficiency Mode

When the Music efficiency mode feature is enabled, the device automatically detects low-power signal states during active playback mode and reduces the overall I_Q power consumption to extend the battery life. This feature is useful for dynamic audio signals with varying signal levels eg. Music tracks, voice calls movie tracks, and so forth.

The device monitors the input audio signal level against the programmed Music efficiency threshold configured by the `MUSIC_EFF_MODE_THR[23:0]` register. When the audio signal falls below the threshold, an internal hysteresis timer is enabled. If the signal level remains below the configured `MUSIC_EFF_MODE_THR[23:0]` for the entire duration of the `MUSIC_EFF_MODE_TIMER[23:0]`, the device enters into the Music efficiency mode. In Music efficiency mode, the device's internal blocks like I-sense and V-sense, etc enter into a low I_Q state to reduce the overall device I_Q power consumption. While the Music efficiency mode is active the I-V sense output data is held at '0' level. When the device is in Music efficiency mode, the `MUSIC_EFF_STATUS` bit is set as high and when the device comes out of music efficiency mode, the status bit is set low.

When the signal level increases above the *MUSIC_EFF_MODE_THR[23:0]*, the device automatically wakes up the blocks in low I_Q mode and continues playing out the audio input signals. The transition from Music efficiency mode to normal operation occurs with minimal click and pop. While the device is in Music efficiency mode, the audio channel performance is maintained and doesn't impact the output signal level or noise.

The *MUSIC_EFF_MODE_THR[23:0]* and *MUSIC_EFF_MODE_TIMER[23:0]* registers can be configured using the PPC3 Software [Section 6.4.1](#).

6.3.1.3.3 VDD Y-bridge

TAS2573 uses a Y-bridge output stage for switching the class-D output PWM voltage between the VDD and PVDD supply. When the feature is enabled using *EN_Y_BRIDGE_MODE* set to high, the device will automatically select the output voltage required to switch the output PWM. When the signal level is low, the output will switch at VDD to enable higher system-level efficiency by reducing the class-D output switching voltage. When the signal level is high, the output switches on the PVDD voltage rail set by the integrated Boost, or external PVDD in the external PVDD mode of operation.

The device monitors the input audio signal level against the programmed Y-bridge mode threshold configured by *VDD_MODE_THR_LVL[23:0]* register. When the audio signal falls below the threshold, an internal hysteresis timer is enabled. If the signal level remains below the configured *YBRIDGE_HYST_TIMER[1:0]* for the entire duration of the selected time, the device enters into the lower voltage VDD supply-based PWM switching mode.

When the signal level increases above the *VDD_MODE_THR_LVL[23:0]* plus *VDD_MODE_HYST[23:0]*, the device starts switching the output PWM signal on PVDD supply without introducing any signal clipping.

The *VDD_MODE_THR_LVL[23:0]* and *VDD_MODE_HYST[23:0]* registers can be configured using the PPC3 Software [Section 6.4.1](#).

Table 6-6. VDD Y-bridge hysteresis timer

<i>YBRIDGE_HYST_TIMER[1:0]</i>	Configuration
00	100 us
01 (default)	500 us
10	5ms
11	50ms

Table 6-7. VDD Y-bridge enable

<i>EN_Y_BRIDGE_MODE</i>	Configuration
0	Y-bridge mode is disabled
1 (default)	Y-bridge mode is enabled

6.3.1.3.4 Class-H Boost

TAS2573 has an advanced class-H algorithm to control the integrated Boost. The class-H algorithm enables Boost supply to closely track audio signal levels and achieve high system level efficiency for extending battery life. Class-H mode is enabled using the *BST_MODE[1:0]* register.

The class-H algorithm buffers the input signal to enable sufficient look-ahead time required to charge the Boost output capacitor and avoid any signal clipping. The algorithm monitors the input signal level and uses system-level parameters configured in PPC3 software like Boost output voltage, Boost output capacitor, channel gain, and so forth and computes the most optimum class-H tuning parameters. These tuning parameter registers are then calculated in the PPC3 software and configured in the corresponding *CLASSH_TUNING_x[23:0]* registers.

When the *BST_MODE[1:0]* is configured to use the device in Class-G mode or Boost always-ON mode, the max inrush current from the battery can be controlled by setting the Inrush current parameter in PPC3 software. The software generates the required coefficients in the *CLASSH_TUNING_x[23:0]* register based on the system level parameters configured like Boost output capacitor, Inrush current required, and so forth.

6.3.1.4 2S Battery Mode

TAS2573 can be configured to function for different battery systems like single series cell (1S) Li-ion battery (2.5V to 5.5V) or 2-series cell (2S) series cell battery (4.7V to 10V). When the 2S battery is selected for the device, the diagram below shows the conceptual connections in the system to connect the 2S battery. When selected for 2S battery operation, the VBAT pin of the device is used for biasing internal blocks and needs to be supplied from external power source between 3.0V to 5.5V.

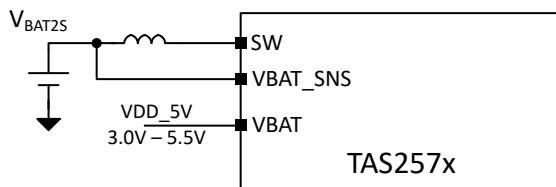


Figure 6-2. 2S Battery Mode System Configuration

The internal battery voltage monitor needs to be switched to sense the voltage on the VBAT_SNS pin instead of the default sensing done on the VBAT pin. *SEL_VBAT_MODE[1:0]* configures the internal voltage monitor and the device configuration between 1S or 2S battery systems.

When *SEL_VBAT_MODE[1:0]* is set as '10', for example 2S mode of operation, the device internal bias voltage needs to be configured based on *VBAT_BIAS_SELx* registers. If the VBAT pin voltage is available from the center tap or half of the 2S battery voltage, the *VBAT_BIAS_SEL1* needs to be set high. For other VBAT voltage configurations the *VBAT_BIAS_SEL1* must be set low and appropriate *VBAT_BIAS_SEL2* configuration must be selected.

Table 6-8. Battery Mode Selection

<i>SEL_VBAT_MODE[1:0]</i>	Configuration
00 (default)	Voltage monitor on VBAT pin. 1S mode of operation
01	Voltage monitor on VBAT_SNS pin. 1S mode of operation
10	Voltage monitor on VBAT_SNS pin. 2S mode of operation
11	Reserved

Table 6-9. VBAT Pin Bias Voltage Selector

<i>VBAT_BIAS_SEL1</i>	Configuration
0 (default)	VBAT pin biasing based on <i>VBAT_BIAS_SEL2</i> register
1	VBAT pin voltage is half of 2S battery voltage

Table 6-10. VBAT Pin Bias Voltage Selector

<i>VBAT_BIAS_SEL2[1:0]</i>	Configuration
00	Reserved
01(default)	Minimum VBAT pin voltage > 2.9V
10	Minimum VBAT pin voltage > 3.3V

**Table 6-10. VBAT Pin Bias Voltage Selector
(continued)**

VBAT_BIAS_SEL2[1:0]	Configuration
11	Minimum VBAT pin voltage > 3.7V

6.3.1.5 Low voltage battery mode

TAS2573 can be configured to function for different battery systems like single series cell (1S) Li-ion battery (2.5V to 5.5V) or other low voltage 1S batteries ($V_{BAT_LV} = 1.8\text{ V to }5.5\text{V}$). When the low voltage battery mode is selected for the device, the diagram below shows the conceptual connections in the system to connect the battery. When selected, the VBAT pin of the device is used for biasing internal blocks and needs to be supplied from external power source between 3.0V to 5.5V.

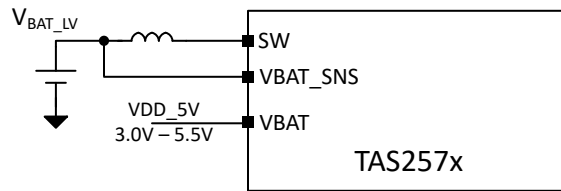


Figure 6-3. Low voltage battery mode system configuration

The internal battery voltage monitor needs to be switched to sense the voltage on the VBAT_SNS pin instead of the default sensing done on the VBAT pin. *SEL_VBAT_MODE[1:0]* configures the internal voltage monitor.

The *SEL_VBAT_MODE[1:0]* is set as '10', ie battery voltage sensed on VBAT_SNS pin, and the *VBAT_BIAS_SEL2* register needs to be configured based on the available VDD_5V voltage in the system. Configuring *VBAT_BIAS_SEL2 = '01'*, ie minimum VDD_5V voltage of 2.9V leads to lower power configuration of the boost due to limited bias voltage availability and reduces the max output power.

The selection for minimum voltage needs to be done using PPC3 software. Two options of V_{BAT_LV} minimum voltage support are available, ie min 1.8V mode and min 2.0V mode. There is tradeoff between minimum voltage support and efficiency. When V_{BAT_LV} is selected as 1.8V, the output power at which boost turns ON is lower compared to V_{BAT_LV} minimum 2.0V mode and the efficiency of device while boost is turned ON, is also lower in the V_{BAT_LV} min 1.8V mode vs min 2.0V mode.

6.3.1.6 External PVDD Mode

The internal Boost of TAS2573 can be disabled by setting *BST_EN* register low. When the external PVDD mode is used, the class-D amplifier is directly powered from the voltage source on PVDD pin. The device configurations needs to be updated using PPC3 software to configure the device in required performance configurations for external PVDD mode of operation.

6.3.2 Faults and Status

During power-up sequencing, the power-on-reset circuit (POR) monitors the VDD and IOVDD pins and holds device in reset (including all the configuration registers) until the supplies are valid. Any supply voltage dip on VDD or IOVDD below the UVLO voltage thresholds resets the device immediately along with all the register configurations.

During operation modes, the device monitors internal device status and fault conditions and can notify the host of error and status conditions using the IRQZ interrupt pin and internal I²C based interrupt registers. The interrupt generation in IRQZ pin can be masked by configuring the corresponding Interrupt mask register bit.

Table 6-11 lists the different faults and interrupts that the device monitors and the corresponding configuration bits to enable/disable the interrupt generation and reading the I2C interrupt status

Table 6-11. Faults and Interrupts

Category	Interrupt	Interrupt Mask register bit	Default Mask status	Interrupt Latched status bit
Limiter & Brown out protection Section 6.4.2.5	Brownout detected	<i>INT_MASK0[3]</i>	Not Masked	<i>INT_LTCH0[3]</i>
	BOP Active	<i>INT_MASK0[2]</i>	Not Masked	<i>INT_LTCH0[2]</i>
	BOP infinite hold	<i>INT_MASK0[7]</i>	Not Masked	<i>INT_LTCH0[7]</i>
	Limiter Active	<i>INT_MASK0[4]</i>	Not Masked	<i>INT_LTCH0[4]</i>
	Limiter attenuation	<i>INT_MASK0[6]</i>	Not Masked	<i>INT_LTCH0[6]</i>
	Supply below inflection point	<i>INT_MASK0[5]</i>	Not Masked	<i>INT_LTCH0[5]</i>
Supply Voltage Monitors Section 6.4.6	PVDD Over voltage	<i>INT_MASK3[2]</i>	Not Masked	<i>INT_LTCH3[2]</i>
	PVDD Under voltage	<i>INT_MASK1[7]</i>	Not Masked	<i>INT_LTCH1[7]</i>
	VBAT2S supply under voltage	<i>INT_MASK1[6]</i>	Not Masked	<i>INT_LTCH1[6]</i>
	VBAT supply under voltage	<i>INT_MASK4[7]</i>	Not Masked	<i>INT_LTCH4[7]</i>
Thermal protection Section 6.4.7	Thermal warning at 135C	<i>INT_MASK1[4]</i>	Masked	<i>INT_LTCH1[4]</i>
	Thermal warning at 125C	<i>INT_MASK1[3]</i>	Masked	<i>INT_LTCH1[3]</i>
	Thermal warning at 115C	<i>INT_MASK1[2]</i>	Masked	<i>INT_LTCH1[2]</i>
	Thermal warning at 105C	<i>INT_MASK1[1]</i>	Masked	<i>INT_LTCH1[1]</i>
	Over temperature error	<i>INT_MASK3[7]</i>	Not Masked	<i>INT_LTCH3[7]</i>
Clock protection Section 6.4.8.1	Clock error	<i>INT_MASK2[3]</i>	Not Masked	<i>INT_LTCH2[3]</i>
	Pre-Power-up Clock error	<i>INT_MASK4[2]</i>	Not Masked	<i>INT_LTCH4[2]</i>
	Clock ratio change error	<i>INT_MASK2[2]</i>	Not Masked	<i>INT_LTCH2[2]</i>
	Fs change error	<i>INT_MASK2[1]</i>	Not Masked	<i>INT_LTCH2[1]</i>
	Fs invalid error	<i>INT_MASK2[0]</i>	Not Masked	<i>INT_LTCH2[0]</i>
	Frame out of sync	<i>INT_MASK2[5]</i>	Not Masked	<i>INT_LTCH2[5]</i>
	Internal PLL Clock error	<i>INT_MASK2[4]</i>	Not Masked	<i>INT_LTCH2[4]</i>
	Digital watchdog	<i>INT_MASK2[7]</i>	Not Masked	<i>INT_LTCH2[7]</i>
	DSP watchdog	<i>INT_MASK6[6]</i>	Not Masked	<i>INT_LTCH6[6]</i>
DSP Events Section 6.4.2.1.3	Factory Calibration completed	<i>INT_MASK5[7]</i>	Not Masked	<i>INT_LTCH5[7]</i>
	Short Circuit detected	<i>INT_MASK5[4]</i>	Not Masked	<i>INT_LTCH5[4]</i>
	Open Circuit detected	<i>INT_MASK5[3]</i>	Not Masked	<i>INT_LTCH5[3]</i>
Other Protections & Status	Class-D Over current error	<i>INT_MASK3[3]</i>	Not Masked	<i>INT_LTCH3[3]</i>
	Device Active	<i>INT_MASK0[1]</i>	Masked	<i>INT_LTCH0[1]</i>

6.3.2.1 Interrupt generation and clearing

The IRQZ is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to IOVDD. An internal pull up resistor (18kΩ) is provided in the device and can be assessed by setting the *IRQZ_PU* register bit.

The interrupt generation on IRQZ pin can be configured using *IRQZ_PIN_CFG[1:0]* register. For the interrupts that have auto retry feature, the retry timer can be configured using *RETRY_WAIT_TIME* register. The interrupt pin polarity can be changed from the default case of Active Low to Active high by setting the *IRQZ_POL* register bit high.

Any latched interrupt can be cleared by setting *INT_CLR_LTCH* bit high. This is self clearing bit and automatically gets updated to low once the interrupt is cleared. Interrupts can also be cleared by hardware shutdown by pulling the SDZ pin low, or by software reset using *SW_RESET* bit.

Table 6-12. IRQZ pin configuration

IRQZ_PIN_CFG[1:0]	Configuration
00	Reserved
01(default)	Interrupt generated on any unmasked latched interrupt
10	Reserved
11	Interrupt generated for 2 to 4ms every 4ms on any unmasked latched interrupt

Table 6-13. Retry wait timer

RETRY_WAIT_TIME	Configuration
0 (default)	Retry every 1.5sec
1	Retry every 100ms

6.4 Feature Description

6.4.1 PurePath™ Console 3 Software

The TAS2573's advanced features, algorithms and device configuration can be performed using PurePath Console 3 (PPC3) software. The base software PPC3 is downloaded and installed from the TI website. Once installed the TAS2573 application can be downloaded from with-in PPC3. The PPC3 tool calculates necessary register coefficients for device configuration that are described in the following sections. The device performance is optimized using registers named *TUNING* based on the options for system configuration selected in the GUI. This is the recommended method to configure the device. Tuning of algorithms is done using specific GUI panels in the PPC3 software. The PPC3 tool calculates the necessary coefficients for algorithm and downloads them to the device. Once the TAS2573 application calculates and updates the device, the registers values can be read back using the PPC3 tool for final system integration.

6.4.2 Playback Signal Path

6.4.2.1 Digital Signal Processor

The TAS2573 has an on-chip, low-latency DSP supporting Texas Instruments' Smart Amp Audio Tuning, Speaker Protection and Advanced Battery Guard algorithms to maximize audio quality, bass and loudness while maintaining safe speaker conditions.

The Audio Tuning Algorithms supported in the TAS2573 are EQ (Equalizer Filters with 13-bands), DRC (Dynamic Range Compressor with 3-bands), DEQ (Dynamic Equalizer with 2-bands) and Rattle Suppressor.

The Speaker Protection Algorithm monitors the loudspeaker health real-time using integrated IV-Sense and controls the audio to maximize bass and loudness content while preventing any damage to the speaker due to excessive diaphragm movement (excursion protection) or due to over heating of the voice coil (thermal protection). The Advanced Battery Guard Algorithm manages peak output power delivery while avoiding any audio distortion when the battery capacity is depleting.

The TAS2573 has on-chip Factory Calibration routine to accurately determine the temperature of the loudspeaker while accounting for variations in the voice coil resistance. The Factory Calibration routine can also identify loudspeaker manufacturing defects by comparing loudspeaker parameters for pass/fail limits as well as determining open and shorted loudspeaker coils.

The Audio Tuning, Speaker Protection and Advanced Battery Guard algorithms can be enabled and tuned using the PPC3 Software [Section 6.4.1](#).

The Audio Tuning, Speaker Protection and Advanced Battery Guard algorithms are supported only for sample rate = 48KHz.

6.4.2.1.1 Algorithm Blocks

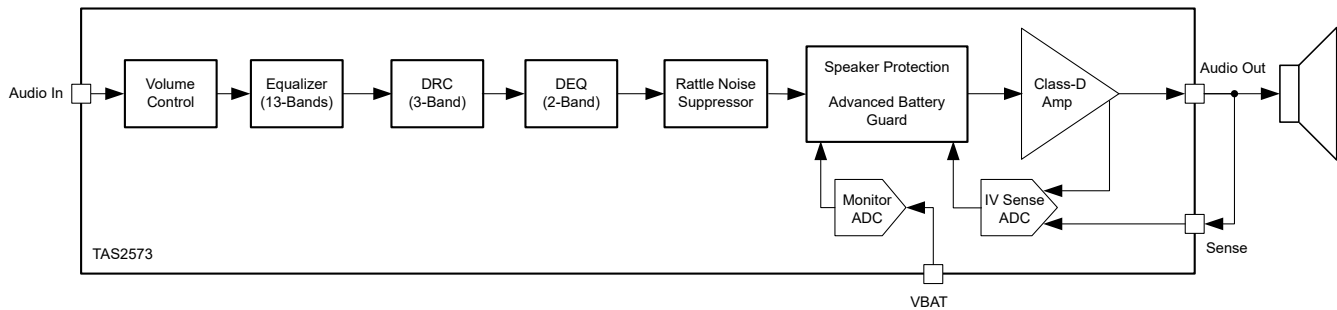


Figure 6-4. Algorithm Blocks

Audio samples are received over the I²S/TDM interface. The audio samples are processed through the Audio Tuning algorithms followed by the Speaker Protection and Advanced Battery Guard algorithms. The IV sense signals and the VBAT supply monitor signals are used by the Speaker Protection and Advanced Battery Guard algorithms to control the audio output to protect the loudspeaker, prevent clipping and brownout and maximize audio quality and loudness.

6.4.2.1.2 Algorithm Features

Algorithm Features

Speaker Protection - Thermal: This algorithm protects the speaker from temperature damage. The IV sense signals are monitored by the algorithm to estimate the temperature of the loudspeaker and control the output audio power so that the temperature is always regulated within the safety limit (T_{max}) of the loudspeaker.

Speaker Protection - Excursion: This algorithm protects the speaker from over excursion (excessive diaphragm movement). The algorithm monitors the loudspeaker properties (e.g. resonance frequency) based on the IV sense signals and dynamically adapts the output audio voltage to maintain the diaphragm excursion within the rated safety limit (X_{max}) of the loudspeaker.

Advanced Battery Guard: This algorithm prevents excessive droop of supply voltage which can cause output audio clipping and system level brownout. This issue is exacerbated at depleted battery levels where excessive current drawn from the battery can result in sagging of power rails (due to increased battery internal resistance) causing distorted audio and unforeseen system fault. Using VBAT sense, the algorithm can monitor the supply ripple and auto-regulate the output power to prevent clipping and brown out.

Integrated Factory Calibration: Factory calibration of loudspeakers is necessary to account for variations of voice coil resistance and compensate the effect for loudspeaker temperature measurement and protection. Additionally the factory calibration can be used for binning defective units e.g. open or shorted loudspeakers. The TAS2573 has integrated Factory Calibration feature triggered through a single I²C command facilitating ease-of-use for system integration.

Equalizer Filter (EQ): These are biquadratic filters (13 bands) which can be used to tune the output of loudspeaker drivers to provide flat and balanced response. The filters are used for loudspeaker frequency response compensation, extending the bass response, attenuate frequencies that produce high THD, remove dc or very low frequency signals that can cause speaker damage due to over excursion etc.

Dynamic Range Compressor (DRC): A Dynamic Range Compressor (DRC) is used to adjust the level of the audio signal to match the dynamic range of the loudspeaker. To maximize loudness, dynamic range compressors also amplifies soft signals to improve audibility. The DRC algorithm in TAS2573 employs multi-band compression (3 bands) to maintain balance between bass transients, vocal clarity and high frequency content.

Dynamic Equalizer (DEQ): Dynamic Equalization is used to compensate for any non-linear loudspeaker distortion such as rub-and-buzz, sibilance noise and rocking modes. These distortions are mostly observed at large signal levels at specific frequencies. The dynamic equalizer attenuates only the large signals while

keeping the small signals unchanged. Two distinct tunable frequency points (2 bands) are supported in TAS2573 for effective control of loudspeaker non-linearity.

Rattle Noise Suppressor: The rattle noise suppressor is a special purpose frequency sensitive compressor that reduces rattle noise which is caused when loudspeakers are driven hard near the resonance frequency resulting in air turbulence and mechanical artefacts. This algorithm automatically detects and regulates audio content that can potentially cause rattle noise while maintaining the loudness for audio content e.g. wideband that is not impacted by rattle.

6.4.2.1.3 Factory Calibration

The TAS2573 device has integrated Factory Calibration feature to compensate for the effect of unit-to-unit variation of voice coil resistance of the loudspeaker. The feature triggers a measurement of the voice coil resistance in factory floor for storing the resistance value in the end-system as well for screening defective units e.g. open or shorted loudspeaker. The completion of factory calibration is flagged on *INT_LTCH5[7]* bit, and corresponding interrupt can be generated on *IRQZ* pin based on status of *INT_MASK5[7]* bit. For defective speakers, open circuit is flagged using *INT_LTCH5[3]* bit with a corresponding interrupt generated based on *INT_MASK5[3]* bit while short circuit is flagged using *INT_LTCH5[4]* bit with a corresponding interrupt generated based on *INT_MASK5[4]* bit.

The Factory Calibration feature can be enabled and tuned using the PPC3 Software [Section 6.4.1](#).

6.4.2.2 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier's analog gain level (A_{AMP}), digital volume control (A_{DVC}) and user volume control (A_{USER}). [Equation 1](#) calculates the output voltage of the amplifier. Amplifier analog gain setting (A_{AMP}) must be set before powering up the playback channel and must not be changed while the channel is active. The user volume control (A_{USER}) can be modified while the channel is active and is used for changing the output level dynamically based on user input. The digital volume control (A_{DVC}) can be modified while the channel is active but only if the on chip DSP algorithms are disabled. When the on chip DSP algorithms are enabled, A_{DVC} must be set before powering up the playback channel and must not be changed while the channel is active. Both the A_{DVC} and A_{USER} allows for soft volume ramp up/down feature to allow for smooth transition of output voltage from one level to another.

$$V_{AMP} = \text{Input} + A_{USER} + A_{DVC} + A_{AMP} \text{ dBV} \quad (1)$$

where

- V_{AMP} is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0dBFS
- A_{USER} is the user volume control setting, 18dB to -105dB in 0.5dB steps
- A_{DVC} is the digital volume control setting, 6dB to -110dB in 0.5dB steps
- A_{AMP} is the amplifier output level setting, -0.071dBV to 21.0dBV in 0.5017dBV steps.

Amplifier output level settings are presented in dBV (dB relative to $1V_{rms}$) with a full scale digital audio input (0dBFS) and the digital volume control set to 0dB. Note that these levels are not achievable because of analog clipping in the amplifier, so the levels must be used to convey gain only.

[Table 6-14](#) shows gain settings that can be programmed via the *AMP_LVL* register for A_{AMP} . When *AMP_LVL* is set to less than 9dBV settings, the playback channel is automatically configured to low noise mode or receiver mode of operation.

Table 6-14. Amplifier Output Level Settings

<i>AMP_LVL[5:0]</i>	FULL SCALE OUTPUT	
	dBV	V_{PEAK} (V)
0x00	21.000	15.9
0x01	20.498	15.0
0x02	19.997	14.1
0x03	19.495	13.3

**Table 6-14. Amplifier Output Level Settings
(continued)**

AMP_LVL[5:0]	FULL SCALE OUTPUT	
	dBV	V _{PEAK} (V)
0x04	18.993	12.6
...	...	...
0x27	1.434	1.7
0x28	0.932	1.6
0x29	0.430	1.5
0x2A	-0.071	1.4
0x2B-0x3F	Reserved	Reserved

When a change in digital volume control (A_{DVC}) occurs, the device ramps the volume to the new setting based on the *DVC_SLEW_RATE* register bits. If *DVC_SLEW_RATE* is set to 0x7FFFFFFF, volume ramp is disabled. This can be used to speed up start up, shutdown and digital volume changes when volume ramp is handled by the system host. When volume ramp is disabled, the input audio data stream must be held at digital silence during shutdown and power up of the device to avoid any clicks and pops.

The device can be put in software based mute by setting *DVC_LEVEL* to 0x000000 setting.

The digital voltage control registers *DVC_LEVEL* and *DVC_SLEW_RATE* registers can be configured using the PPC3 Software [Section 6.4.1](#).

Table 6-15. Digital Volume Control

DVC_LEVEL[23:0]	VOLUME (dB)
0x000000	Software MUTE
0x00000D (MIN)	-110
...	...
0x400000	0 (default)
...	...
0x7FB261 (MAX)	6

Table 6-16. Digital Volume Ramp Rate

DVC_SLEW_RATE[23:0]	RAMP RATE @ 48kHz (s)
0x00036A	1000ms
...	...
0x034A51	4ms (default)
...	...
0x7FFFFFFF	0 - Ramp disabled

The A_{USER} settings can be tuned using the PPC3 Software [Section 6.4.1](#).

6.4.2.3 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The playback path employs a high-pass filter (HPF) to prevent this from occurring. The HPF is a 1st order filter and can be changed from the default 2Hz for 48ksp/s fs using the *AUDIO_HPF_N0*, *AUDIO_HPF_N1*, *AUDIO_HPF_D1* registers. The HPF filter frequency scales with change in the FSYNC clock and can be re-configured to achieve the required cutoff frequency for different FSYNC clock frequencies. The coefficients can also be changed to disable the HPF coefficients appropriately. These coefficients must be calculated and set using PPC3 Software [Section 6.4.1](#).

6.4.2.4 Class-D Amplifier

TAS2573 has integrated high performance class-D amplifier with low idle channel noise, low distortion and high PSRR. The Class-D amplifier switches on a clock frequency derived from the SBCLK frequency and is always synchronized to the input clock source. The *SAMP_RATE_CFG* register enables selection between input clock source based out of multiple of 44.1kHz vs 48kHz multiples.

Table 6-17. Sample rate configuration

<i>SAMP_RATE_CFG</i>	Configuration
0 (default)	Audio data rate is multiple/sub-multiple of 48ksps
1	Audio data rate is multiple/sub-multiple of 44.1ksps

For improvements in EMI performance the class-D amplifier supports programmable Edge rate control (ERC) and class-D clock spread spectrum modulation (SSM).

The edge rate of class-D can be controlled using *CLASSD_OUTPUT_EDGERATE_CTRL[1:0]* register. By default the class-D output edge rate is configured to fastest setting to enable high efficiency in the system. The class-D output edge rate can be slowed down using other configuration settings to reduce the EMI energy at high frequency with reduction in efficiency. The exact rate of change of output edge rate varies based on output load conditions, and the values mentioned in the tables below are approximate edge rate levels for default loading conditions.

Table 6-18. Class-D output edge rate control

<i>CLASSD_OUTPUT_EDGERATE_CTRL[1:0]</i>	Configuration
00	Class-D output edge rate of 0.5V/ns
01	Class-D output edge rate of 1.0V/ns
10	Reserved
11(default)	Class-D output edge rate of 2V/ns

The class-D amplifier has over current protection on each of the output power FETs, including the PVDD High side, VDD high side and the ground power FETs.

The class-D amplifier output impedance can be controlled when the outputs stop switching during Noise gate mode using *CLASSD_HIZ_MODE* control register.

Table 6-19. Class-D high-Z mode control

<i>CLASSD_HIZ_MODE</i>	Configuration
0 (default)	Output pulled down with 2.5kΩ
1	Output pulled down with >13kΩ

6.4.2.5 Supply Tracking Limiters with Brown Out Prevention

TAS2573 monitors class-D supply voltage (VBAT or PVDD) along with the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiter and brown out module calculates the signal attenuation required based on the condition of the signal level, channel gain and the selected supply voltage. Both these features are available irrespective of whether the on chip DSP algorithms are enabled or disabled. Additionally, when the on chip DSP algorithms are enabled, the Advanced Battery Protection algorithm (Section 6.4.2.1.2) can monitor supply voltage droop and provide precise control of audio while preventing clipping and brown out.

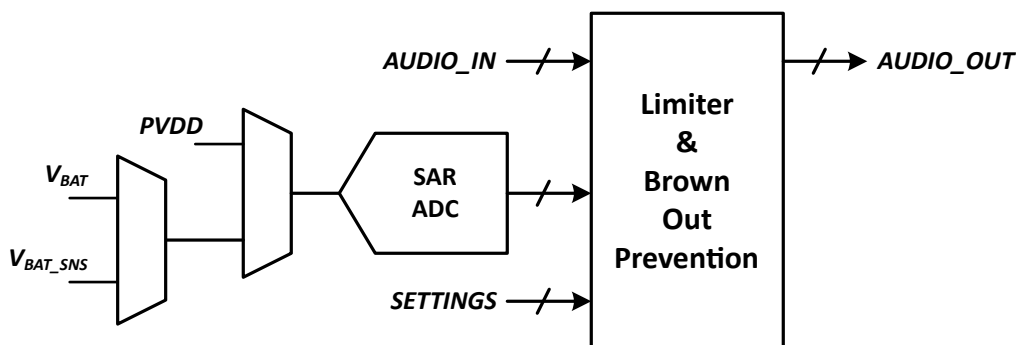


Figure 6-5. Limiter and Brown out protection module

The Brown Out Prevention (BOP) module provides a priority input to provide a fast response to transient dips in the battery supply. The BOP feature can be enabled by configuring the register bit *BOP_EN* high. The supply voltage that is tracked to determine Brown out conditions can be configured as V_{BAT}/V_{BAT_SNS} or $PVDD$ based on system configuration needs by using *BOP_SRC* register bit. When the selected supply dips below the brown-out threshold configured by setting register *BOP_THR_LVL[23:0]*, the BOP begins reducing gain. The rate of gain reduction (db/sample) can be configured by setting the *BOP_ATK_RATE[23:0]* registers. When the V_{BAT} supply rises above the brownout threshold, the BOP begins to release the gain after the programmed hold timer, *BOP_HLD_COUNT[23:0]*. The BOP feature uses the *LIM_RLS_RATE[23:0]* register setting to release after a brown out event. The release rate is rate of gain increase in db/sample ratio. During a BOP event the limiter updates is paused. This is to prevent a limiter from releasing during a BOP event.

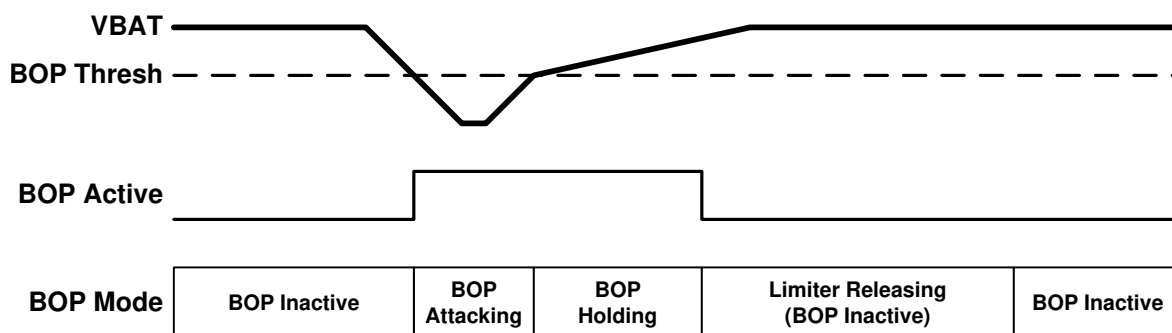


Figure 6-6. Brown Out Prevention Event

The device can be configured to hold the gain attenuation once a BOP event is detected by setting the register bit *BOP_INF_HLD* high. When the bit is programmed high, the Limiter and BOP module does not release the gain attenuation and holds the device in the programmed min gain attenuation level until the infinite hold is cleared by setting the register bit *BOP_HLD_CLR* high. The hold clearing bit is self clearing and automatically resets to low state once the hold is cleared.

A hard brownout level can be set to shutdown the device if the BOP gain attenuation cannot mitigate the drop in battery voltage. The brown out based shutdown of the device is enabled when *BOPSD_EN* bit is set high and shuts down when the battery voltage falls below the voltage threshold set by *BOSD_THR_LVL[23:0]* register bits.

A maximum level of attenuation applied by the limiters and brown out prevention feature is configurable via the *LIM_MAX_ATN* register. This attenuation limit is shared between the features. For instance, if the maximum attenuation is set to 6dB and the limiters have reduced gain by 4dB, the brown out prevention feature is only be able to reduce the gain further by another 2dB. If the limiter or brown out prevention feature is attacking and reaches the maximum attenuation, gain does not be reduced any further.

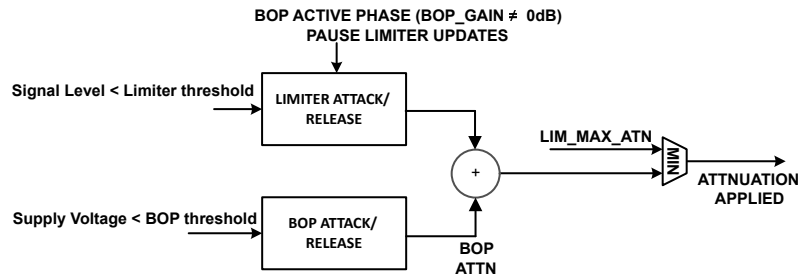


Figure 6-7. Limiter and Brown out gain attenuation

6.4.2.5.1 Voltage Limiter and Clipping protection

The supply tracking limiter can be configured using *LIM_MODE[1:0]* register. In the VBAT voltage mode, the limiter tracks the VBAT supply voltage for voltage limiter and in PVDD voltage mode, the limiter tracks the PVDD voltage for external PVDD mode of use case.

Table 6-20. Limiter mode selection

<i>LIM_MODE[1:0]</i>	Configuration
00 (default)	Disabled
01	VBAT voltage based limiter
10	PVDD voltage based limiter
11	Reserved

The limiter can be configured to reduce the output signal based on fixed signal threshold level, or it can attenuate signal based on a dynamic threshold which tracks the selected supply voltage. The register bit *SUPPLY_HEADROOM_LIM_MODE* enables the dynamic supply tracking and can be used to limit the clipping distortion when the supply voltage is varying in the system.

Table 6-21. Limiter dynamic supply headroom tracking mode

<i>SUPPLY_HEADROOM_LIM_MODE</i>	Configuration
0 (default)	Disabled
1	Enabled. Limiter threshold is dynamically changed based as a fixed percentage of monitored supply voltage.

When *SUPPLY_HEADROOM_LIM_MODE* is set high, the limiter sets the threshold as a fixed percentage of the monitored supply voltage. The limiter begins reducing gain when the output signal level is greater than the threshold configured. For eg, if voltage limiting is desired to be 10% below the supply voltage, then *LIM_SLOPE[23:0]* is configured as 0.9 and the threshold is calculated as monitored supply voltage multiplied by 1.1. Similarly if the *LIM_SLOPE[23:0]* is configured at > 1.0, the limiter threshold is set at higher than the supply voltage, and a small amount of controlled clipping occurs.

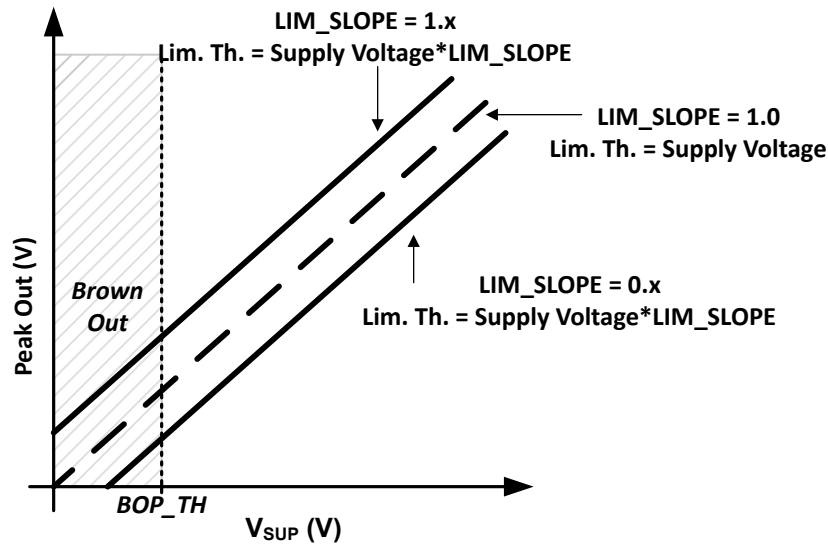


Figure 6-8. Limiter with dynamic supply headroom

When *SUPPLY_HEADROOM_LIM_MODE* is set low, the limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track selected supply below a programmable inflection point with a minimum threshold value. Figure 6-9 below shows the limiter configured to limit to a constant level regardless of the selected supply level. To achieve this behavior, set the limiter maximum threshold to the desired level using *LIM_TH_MAX[23:0]*. Set the limiter inflection point using *LIM_INF_PT[23:0]* below the minimum allowable supply setting. The limiter minimum threshold register *LIM_TH_MIN[23:0]* does not impact limiter behavior in this use case.

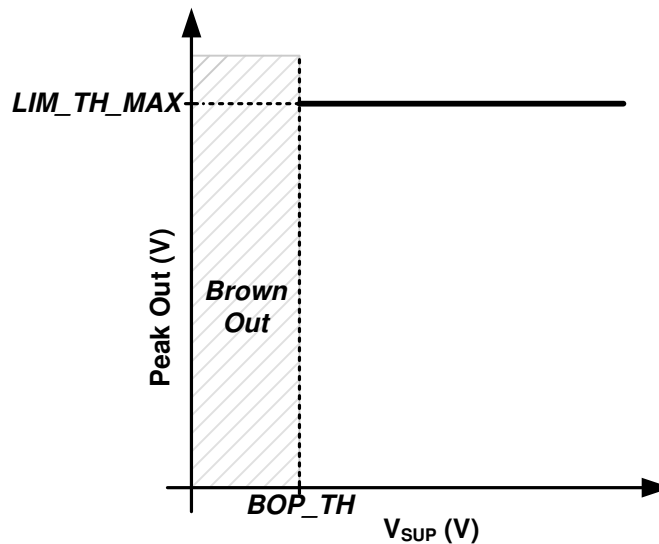


Figure 6-9. Limiter with Fixed Threshold

Figure 6-10 shows how to configure the limiter to track selected supply below a threshold without a minimum threshold. Set the *LIM_TH_MAX[23:0]* register to the desired threshold and *LIM_INF_PT[23:0]* register to the desired inflection point where the limiter begins to reduce the threshold with the selected supply. The *LIM_SLOPE[23:0]* register bits can be used to change the slope of the limiter tracking the supply voltage in V/V. For example, a slope value of 1V/V reduces the limiter threshold 1V for every 1V of drop in the supply voltage. Program the *LIM_TH_MIN[23:0]* below the minimum of the selected supply to prevent the limiter from having a minimum threshold reduction when tracking the selected supply.

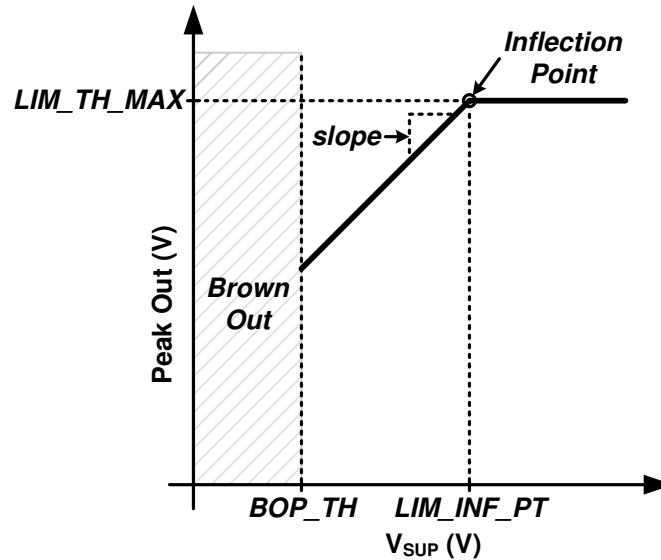


Figure 6-10. Limiter with Inflection Point

To achieve a limiter that tracks the selected supply below a threshold, configure the limiter as explained in the previous example, except program the `LIM_TH_MIN[23:0]` register to the desired minimum threshold. This is shown in Figure 6-11 below.

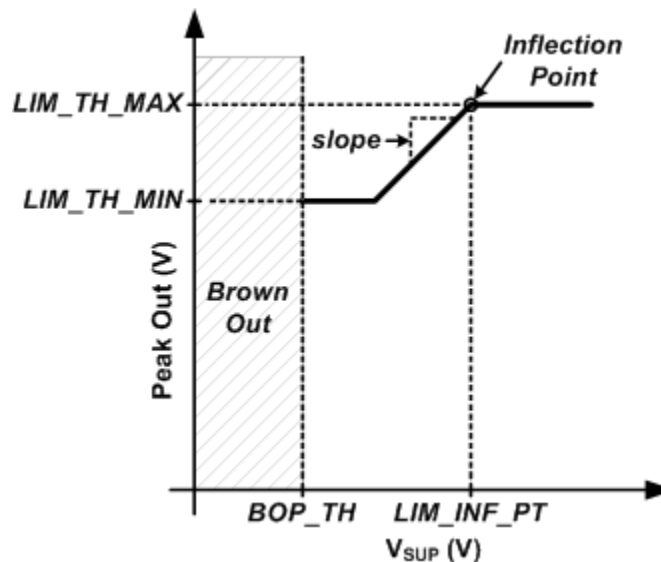


Figure 6-11. Limiter with Inflection Point and Minimum Threshold

The limiter has a configurable attack rate (dB/Sample), hold time (no of samples) and release rate (dB/Sample), which are available via the `LIM_ATK_RATE[23:0]`, `LIM_HLD_COUNT[23:0]`, `LIM_RLS_RATE[23:0]` register bits.

6.4.2.6 Tone Generator

TAS2573 can generate internally a sine tone using an integrated tone generator. This feature is available only when the on chip DSP algorithms are disabled. The tone generator can be enabled by configuring the register bit `INTERNAL_TONE_GEN_ENZ` to low. The tone signal starts playing back on the output by configuring the `INTERNAL_TONE_PLAYBACK_EN` bit high. When set high, the device starts generating a sine tone based on the programmed `TONE_GEN_CNTRL_xx` registers. The tone generator can generate any frequency from 16Hz to a maximum frequency of $0.45 \cdot F_s$, where F_s is the sampling rate of the input digital clocks. The amplitude of

the tone signal can also be controlled using the *TONE_GEN_CNTRL_xx* registers. TI recommends to program the tone frequency and amplitude using the PPC3 Software.

The internally generated tone can be mixed with incoming audio stream, or can replace the input audio stream and only tone signal is generated using *INTERNAL_TONE_MIXING_EN* register.

Table 6-22. Internal tone generator mixing options

<i>INTERNAL_TONE_MIXING_EN</i>	Configuration
0	Only internal tone is generated.
1 (default)	Internally generated tone is mixed with input audio data and played together.

The tone generator can use external clock source like BCLK, or the tone generator can be generated using internal oscillator to generate tone signals even with no external clock sources using *INTERNAL_TONE_CLK_SEL* register.

Table 6-23. Internal tone clock source selection

<i>INTERNAL_TONE_CLK_SEL</i>	Configuration
0 (default)	Tone generator uses external clocks
1	Tone generator uses internal oscillator

6.4.3 Digital Audio Serial Interface

The device provides a flexible Audio Serial Interface (ASI) port. The port can be configured to support a variety of formats including stereo I²S, Left Justified, and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit echo reference stream to enable echo cancellation algorithms in a host processor connected to the device.

The TDM serial audio port supports up to 16 32-bit time slots at 44.1/48kHz, 8 32-bit time slots at a 88.2/96kHz sample rate and 4 32-bit time slots at a 176.4/192kHz sample rate. The device automatically detects the number of time slots and this does not need to be programmed. PCM data sampling rate and SBCLK to FSYNC ratio detected on the TDM bus is reported back on the read-only register bits *FS_RATE_DETECTED[2:0]* and *FS_RATIO_DETECTED[3:0]* respectively.

Table 6-24. PCM Data Sample Rate Detected

<i>FS_RATE_DETECTED[2:0]</i> (Read Only)	Setting
000	Reserved
001	14.7kHz / 16kHz
010	22.05kHz / 24kHz
011	29.4kHz / 32kHz
100 (default)	44.1kHz / 48 kHz
101	88.2kHz / 96kHz
110	176.4kHz / 192kHz
111	Error condition

A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge set by the *RX_EDGE* register bit. The *RX_OFFSET[4:0]* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I²S format.

The *RX_SLEN[1:0]* register bits set the length of the RX time slot to 16, 24 or 32 (default) bits. The length of the audio sample word within the time slot is configured by the *RX_WLEN[1:0]* register bits. The RX port left justifies the audio sample within the time slot by default, but this can be changed to right justification via the *RX_JUSTIFY* register bit.

The device supports mono and stereo down mix playback ($(L+R)/2$). By default the device playback is mono from the time slot equal to the I²C base address offset (set by the AD1 and AD2 pins) for playback. The *RX_SCFG[3:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX_SLOT_L[3:0]* and *RX_SLOT_R[3:0]* register bits.

Table 6-25. RX channel selection

<i>RX_SCFG[3:0]</i>	RX Channel
0000	Channel with time slot equal to I2C address offset
0001	Left channel
0010	Right channel
0011	Stereo downmix (L+R)/2

If time slot selection places reception either partially or fully beyond the frame boundary, the receiver returns a null sample equivalent to a digitally muted sample.

The TDM port can transmit the echo reference streams on the SDOUT pin. This enables echo and noise cancellation algorithms in the host processor. The echo reference stream is transmitted on the SDOUT pin. Setup of the transmission path is done using PPC3 Software [Section 6.4.1](#).

6.4.4 Boost

The TAS2573 internal processing algorithm automatically enables the boost when needed. A look-ahead algorithm monitors the battery voltage and the digital audio stream. When the speaker output approaches the battery voltage the boost is enabled in-time to supply the required speaker output voltage. When the boost is no longer required the boost is disabled and bypassed to maximize efficiency. The boost can be configured in one of two modes. The first is low in-rush (Class-G) supporting only boost on-off and has the lowest in-rush current. The second is high-efficiency (Class-H) where the boost voltage level is adjusted to a value just above what is needed. This mode is more efficient but has a higher in-rush current to quickly transition the levels. This can be configured using *BST_MODE[1:0]* register bits.

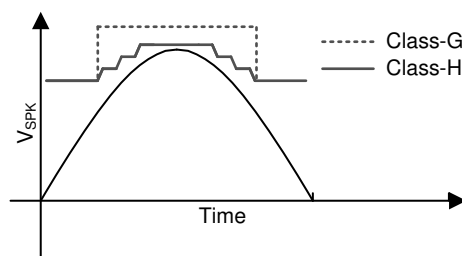


Figure 6-12. Boost Mode Signal Tracking Example

Table 6-26. Boost Mode

<i>BST_MODE[1:0]</i>	BOOST MODE
00	Class-H - High efficiency (default)
01	Class-G - Low in-rush
10	Always On
11	Always Off - Pass-through

The boost can be enabled and disabled using *BST_EN* register. When driving the Class-D amplifier using an external supply through the PVDD pin, the boost must be disabled and the SW pin must be left floating.

Table 6-27. Boost Enable

<i>BST_EN</i>	BOOST IS
0	Disabled (External PVDD mode)
1	Enabled (default)

The maximum boost voltage is set by *VBOOST_MAX_CTRL[7:0]*. When operating in class-G mode, the boost when needed is at this voltage. In class-H mode of operation the boost voltage is automatically selected based on the audio signal but does not exceed this set value. In class-H mode, the class-H controller controls the Boost with a minimum step size of 33mV to generate the required PVDD voltage. The max boost voltage that the device generates is controlled by *VBOOST_MAX_CTRL[7:0]* and the boost can be configured with a step size of 66mV.

Table 6-28. Boost Max Regulation Voltage

<i>VBOOST_MAX_CTRL[7:0]</i>	BOOST VOLTAGE (V)
0x00 - 0x53	Reserved
0x54	5.54V
0x55	5.61V
...	steps of 66mV per LSB step
0xA7	11.02V (default)
...	steps of 66mV per LSB step
0xE4	15.05V
0xE5	15.11V
0xE6 - 0xFF	Reserved

At light loads (for example, near zero cross of sine waves), the boost automatically enters PFM mode to improve the system efficiency. When the Boost is running in PFM mode, the minimum pulse frequency can be adjusted using *BST_MIN_FREQ_SEL*. Setting a higher PFM frequency maintains the Boost frequency is always above the set threshold at the cost of increasing the system power consumption.

Table 6-29. Active Mode PFM Lower Frequency Limit

<i>BST_MIN_FREQ_SEL[1:0]</i>	LOWER LIMIT
00	No lower limit (default)
01	25kHz
10	50kHz
11	RESERVED

The peak current drawn by the boost is controlled using *BST_ILIM[23:0]* register and the boost limits the current drawn from the VBAT supply. This setting allows flexibility in the inductor selection for various saturation currents. The system must always use inductors which have minimum saturation current (I_{SAT}) at least 5% higher than programmed *BST_ILIM* setting. The Boost circuit can go unstable if the inductor I_{SAT} is lower than the *BST_ILIM* setting. The current limit can be adjusted in 39.1mA steps with a range from 1.5A to 5.1A using PPC3 Software.

The change in boost configurations like *BST_ILIM*, *VBOOST_MAX_CTRL* etc requires re-tuning of device parameters such as *CLASSH_TUNING_xx[23:0]* registers to achieve best performance while maintaining no functionality failures. This configuration must be changed using PPC3 tool to enable automatic reconfiguration of all the associated device parameters.

For multiple channel systems, the boost phase can be shifted to maintain each device draws peak current from the battery at different instance of times and enable lower instantaneous peak current from the battery. The boost syncing among multiple devices is enabled using *BOOST_PHASE_SYNC_EN*. The individual device boost phase can be automatically configured to different values using the i2c target address device detected by using *BOOST_PHASE_FROM_ADDRESS_PIN* register, or device boost phase can be manually configured using *BOOST_PHASE* register. The Boost phase shift is done by each device using the FSYNC pulse to synchronize each device and all the devices which require the Boost phase synchronization must be connected to same FSYNC from the host in the system.

Table 6-30. Boost Sync

<i>BOOST_PHASE_SYNC_EN</i>	Status
0	Disabled
1	Enabled(default)

Table 6-31. Boost Phase Selection from i2c Target Address

<i>BOOST_PHASE_FROM_ADDRESS_PIN</i>	Status
0	Disabled
1	Enabled(default)

Table 6-32. Boost Phase Manual Selection (When *BOOST_PHASE_FORM_ADDRESS_PIN* = 0)

<i>BOOST_PHASE</i> [1:0]	Phase Delay
00	Phase shift is 0ns (default)
01	Phase shift is 65ns (~90° for max clock)
10	Phase shift is 130ns (~180° for max clock)
11	Phase shift is 195ns (~270° for max clock)

6.4.5 Speaker current and voltage (IV) sensing

TAS2573 has integrated current and voltage sense measurement circuitry for real time monitoring of output transducer behavior. The *VSNS_N* and *VSNS_P* pins must be connected close to the output load and after any ferrite bead filter to get highest accuracy from the voltage sensor. If *VSNS_N* and *VSNS_P* are connected after the EMI filters, then a series resistor is required to protect the device. If no EMI filter is used, then *VSNS_N* and *VSNS_P* can be directly connected to *OUT_P* and *OUT_N* connections.

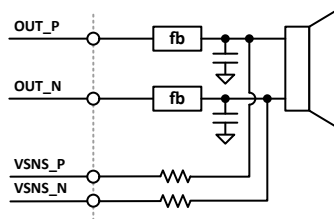


Figure 6-13. Voltage Sense connections

The current and voltage sense circuits are enabled by default and can be disabled by setting *ISNS_PD* and *VSNS_PD* register bits high. When powered down, the device returns null samples for the powered down block. For band-limited applications of current and voltage sense, the sensed signals can be low pass filtered using *IVSENSE_LPF_ENABLE* control bit. When enabled, the signals are filtered with a 4th order 6kHz filter at 48

ksps fs. The filter pole changes proportionately with the change in the FSYNC clock, for example, with 96ksps FSYNC, the filter pole becomes 12kHz.

Table 6-33. IV sense Low pass filter selection

<i>IVSENSE_LPF_ENABLE</i>	Configuration
0 (default)	Current & Voltage sense signal are not low pass filtered
1	Current & Voltage sense signal are low pass filtered by 6kHz filter

The full scale of sensed signal is programmable using *VSNS_GAIN_SEL* and *ISNS_GAIN_SEL* registers.

Table 6-34. Voltage Sense Gain selection

<i>VSENSE_GAIN_SEL</i>	Configuration
00	Voltage sense digital full scale (FS) is equal to 31.85Vpp
01 (default)	Voltage sense digital full scale (FS) is equal to 26Vpp
10	Voltage sense digital full scale (FS) is equal to 20.45Vpp
11	Voltage sense digital full scale (FS) is equal to 14.35Vpp

Table 6-35. Current Sense Gain selection

<i>ISENSE_GAIN_SEL</i>	Configuration
00	Current sense digital full scale (FS) is equal to 5.27 Apk
01	Current sense digital full scale (FS) is equal to 2.9 Apk
10 (default)	Current sense digital full scale (FS) is equal to 2 Apk
11	Current sense digital full scale (FS) is equal to 1.45 Apk

The IV-sense signals are high pass filtered (HPF) and the Bi-Quad filter coefficients can be changed from the default 2Hz using the PPC3 Software ([Section 6.4.1](#)) which configures the *IV_HPF_N0*, *IV_HPF_N1*, *IV_HPF_D1* coefficients. The same register bits are used to bypass the HPF if no filtering is desired. There are several registers configured for IV-sense performance based on system configurations. These IV sense performance tuning registers (*IV_TUNING_xx*) are configured using PPC3 Software.

6.4.6 Supply Voltage Monitors

TAS2573 has integrated SAR ADC to monitor the supply voltage pins VBAT or VBAT_SNS and PVDD. The sensed voltages are used for internal device features, protections and can also be streamed out over digital data bus or read through i2c registers.

The battery voltage can be sensed through either VBAT or VBAT_SNS pins based on the register *SEL_VBAT_MODE[1:0]*

Table 6-36. Battery mode selection

<i>SEL_VBAT_MODE[1:0]</i>	Configuration
00 (default)	Voltage monitor on VBAT pin. 1S mode of operation

Table 6-36. Battery mode selection (continued)

SEL_VBAT_MODE[1:0]	Configuration
01	Voltage monitor on VBAT_SNS pin. 1S mode of operation
10	Voltage monitor on VBAT_SNS pin. 2S mode of operation
11	Reserved

The monitor ADC samples the VBAT pin at higher rate compared to PVDD pin voltage. This sampling speed can be swapped to prioritize PVDD pin sampling rate over VBAT, for example in case of external PVDD mode of operation.

Table 6-37. Supply monitor sampling rate

SUPPLY_SAMPLING_RATE	Configuration
0(default)	VBAT Sampling rate is higher than PVDD
1	PVDD Sampling rate is higher than VBAT

The VBAT and PVDD monitored voltages are stored in the register *VBAT_CNV* and *PVDD_CNV* registers and can be read using i2c commands.

The supply monitors are also used for voltage protection like VBAT under voltage, PVDD over voltage and under voltage and VBAT2S under voltage. The voltage protection features monitors the supply voltages, and shuts down the device when the voltage crosses the protection threshold levels. The device also sets the corresponding fault register and can generate an interrupt on IRQZ pin based on configured interrupt Mask register as described in [Section 6.3.2](#). Once the device is shutdown, the device can be re-powered up using the *MODE[1:0]* register bits.

PVDD over voltage protection is based on the monitored PVDD voltage compared against a programmable threshold which can be controlled using *PVDD_OVLO_TH_SEL* in the internal boost mode, and *PVDD_OVLO_TH_SEL_EXT_BOOST* in the external PVDD mode of operation. The PVDD Over voltage protection is enabled by default and can be disabled by setting *PVDD_OV_DET_DIS* bit high.

Table 6-38. PVDD Over voltage protection threshold, internal Boost mode

PVDD_OVLO_TH_SEL[1:0]	Configuration
00	Over voltage threshold is 13.5V
01	Over voltage threshold is 14V
10	Over voltage threshold is 15V
11 (default)	Over voltage threshold is 16V

Table 6-39. PVDD Over voltage protection threshold, External PVDD mode

PVDD_OVLO_TH_SEL_EXT_BOOST[1:0]	Configuration
00	Over voltage threshold is 13.5V
01 (default)	Over voltage threshold is 14V
10	Over voltage threshold is 15V
11	Over voltage threshold is 16V

6.4.7 Thermal Protection

TAS2573 has internal device junction temperature monitor which protects the device against over temperature. When the internal temperature rises above the Over temperature threshold, the device automatically shuts down and sets the Over temperature flag in the corresponding Interrupt registers. The device can automatically retry to power up if *OTE_RETRY* bit is set high. When set high, the device attempts to re-power up after every *RETRY_WAIT_TIME* setting (default 1.5 seconds of retry)

Along with over temperature protection, the device has thermal warning thresholds to allow for system to raise interrupts or flags as the junction temperature is approaching the shutdown. There are four thermal warning flags available at the internal temperature of 105C, 115C, 125C and 135C. Each thermal warning flag can be independently set to control the Interrupt generation on the IRQZ pad. The minimum temperature and the step size of the temperature warning flag can be programmed using the registers *THERMAL_WARN_MIN_TEMP[23:0]* and *THERMAL_WARN_TEMP_STEP[23:0]*

The real time internal junction temperature is monitored are stored in the register *TMP_CNV* and can be read using i2c commands.

6.4.8 Clocks and PLL

In TDM/I²S Mode, the device operates from SBCLK. [Table 6-40](#) below shows the valid SBCLK frequencies for each sample rate and SBCLK to FSYNC ratio. For 44.1kHz based clocking, the same table is applicable with the associated ratio change between 48ksps to 44.1ksps.

While the sampling rate of 192kHz is supported, data is internally down-sampled to 96kHz. Therefore audio content greater than 40kHz must not be applied to prevent aliasing. This additionally affects all processing blocks like BOP and limiter which must use 96kHz fs when accepting 192kHz audio.

If the sample rate is properly configured via the *SAMPLE_RATE_CFG* bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device automatically detects the input PCM FSYNC and BCLK frequency and auto configures to playback audio signal. The detected clock rates can be read using the read only registers *FS_RATIO_DETECTED* and *FS_RATE_DETECTED*. The device detects improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts.

Table 6-40. Supported SBCLK Frequencies (MHz) (48kHz Based Sample Rates)

Sample Rate (kHz)	SBCLK to FSYNC Ratio													
	16	24	32	48	64	96	128	192	256	384	512	125	250	500
16kHz	NA	0.384	0.512	0.768	1.024	1.536	2.048	3.072	4.096	6.144	8.192	2	4	8
24kHz	0.384	0.576	0.768	1.152	1.536	2.304	3.072	4.608	6.144	9.216	12.288	3	6	12
32kHz	0.512	0.768	1.024	1.536	2.048	3.072	4.096	6.144	8.192	12.288	16.384	4	8	16
48kHz	0.768	1.152	1.536	2.304	3.072	4.608	6.144	9.216	12.288	18.432	24.576	6	12	24
96kHz	1.536	2.304	3.072	4.608	6.144	9.216	12.288	18.432	24.576	NA	NA	12	24	NA
192kHz	3.027	4.608	6.144	9.216	12.288	18.432	24.576	NA	NA	NA	NA	24	NA	NA

6.4.8.1 Auto clock based wakeup and clock errors

TAS2573 supports flexible operating mode transition from active to shutdown and vice-verse using ASI clock auto detection feature. When *MODE[1:0]* is configured as '11' the device toggles between Active and Software shutdown state based on valid ASI clock signals applied on the ASI input pins, for example BCLK and FSYNC. If no ASI clocks are detected in this mode, the device remains in software shutdown, with software shutdown mode *I_Q* on VDD pin, until a valid BCLK and FSYNC clock is detected. Once a valid clock is detected, the device is powered up in active state until the clocks are valid or device is shutdown using software or hardware shutdown commands.

The device can detect and raise interrupt flags on detection of incorrect clock configurations based on status of *CLK_ERR_PWR_EN*. When this bit is set high, the device monitors for activity on the clock pins and flags any

error using the latched interrupts status register. The device can also raise interrupts using IRQZ pin based on status of the corresponding interrupt MASK registers. When the error protection bit is enabled, if a clock error is detected, the device automatically shuts-down with proper shutdown sequencing and minimize any clicks and pops due to invalid clocks.

When the device is in shutdown state, the clock error detection can be delayed to provide system with time required to settle the input clocks. This power up delay in clock error detection is controlled using an internal pre-power up clock error detection timer configured by *CLK_HALT_TIMER*. If device does not detect a valid clock at the end of the *CLK_HALT_TIMER* expiry, the Pre-Power-up Clock error is flagged on *INT_LTCH4[2]* bit, and corresponding interrupt can be generated on IRQZ pin based on status of *INT_MASK4[2]* bit. When *MODE[1:0]* is configured as '11' (Wake-up on ASI mode), *CLK_HALT_TIMER* of '000' is not recommended and the device is stopped from entering the software shutdown and increases the VDD I_Q while the device is shutdown.

Once the device is powered up, the external and internally generated clocks are constantly monitored based on status of *CLK_ERR_PWR_EN* bit. If enabled, any error in external or internal clock is flagged using the clock error status register *INT_LTCH2[3]* bit, and corresponding interrupt can be generated on IRQZ pin based on status of *INT_MASK2[3]*.

For system flexibility, the device also sets the error status for the type of detected clock error. The device can also be configured to raise an interrupt on IRQZ pin for any specific type of clock error, instead of using the generic clock error interrupt generation. [Table 6-43](#) below explains the different type of clock errors and corresponding status bits and interrupt MASK register bits. One or more register bits in the table below can be set based on the type of clock error detected.

If the device shuts down due to any type of clock error, the device can attempt to re-power automatically when *MODE[1:0]* is set to '11'.

Table 6-41. Clock Error Detection Control

CLK_ERR_PWR_EN	Setting
0	Disabled
1	Enabled (default)

Table 6-42. Clock Halt Timer

CLK_HALT_TIMER[2:0]	Setting
000	Disabled (infinite time).
001	0.8ms (default)
010	3.2ms
011	34.1ms
100	68.3ms
101	256ms
110	768ms
111	1.3s

Table 6-43. Clock error type description

Clock error type	Description	Status flag register bit	IRQZ generation Mask bit
Clock error	Clock error for any internal or external clocking configuration errors. This bit is set along with specific clock errors detected in the rest of the table below except for Pre-Power-up Clock errors.	<i>INT_LTCH2[3]</i>	<i>INT_MASK2[3]</i>
Pre-Power-up Clock error	Clock error detected during shutdown mode after clock error is detected at end of <i>CLK_HALT_TIMER</i> .	<i>INT_LTCH4[2]</i>	<i>INT_MASK4[2]</i>
Clock ratio change error	Clock error detected due to easily change in FSYNC to SBCLK ratio.	<i>INT_LTCH2[2]</i>	<i>INT_MASK2[2]</i>

Table 6-43. Clock error type description (continued)

Clock error type	Description	Status flag register bit	IRQZ generation Mask bit
Fs change error	Clock error detected due to easily change in FSYNC clock frequency	INT_LTCH2[1]	INT_MASK2[1]
Fs invalid error	Clock error detected due to incorrect FSYNC clock frequency	INT_LTCH2[0]	INT_MASK2[0]
Frame out of sync	Clock error detected due to Frame out of sync	INT_LTCH2[5]	INT_MASK2[5]
Internal PLL Clock error	Clock error detected due to internally generated clock frequency error.	INT_LTCH2[4]	INT_MASK2[4]

The device also has a digital watchdog timer which monitors for errors in the internal digital state machine and shuts down the device on detection of such errors. This error can also raise an interrupt on IRQZ pin and flag to the host device of the error state.

6.4.9 Digital IO pins

TAS2573 supports 1.2V and 1.8V IO voltage supply based on the voltage applied on the IOVDD pin. The digital output pins, SDOUT, IRQZ and SDA have programmable output drive strength which can be configured using *SDO_DRIVE_SEL*, *IRQZ_DRIVE_SEL* and *SDA_DRIVE_SEL* registers respectively. Reducing drive strength affects the max data rate supported depending on the total capacitive load on the output pin.

Each digital input pin has an optional weak pull down to prevent the pin from floating. Pull downs are not enabled during HW shutdown. The pull downs are disabled by default and can be enabled by setting the corresponding Pull down enable bit high.

Table 6-44. Digital pin weak pull down

Pin Name	Pull down control register name
AD1	AD1_PD_EN
AD2	AD2_PD_EN
SDOUT	SDOUT_PD_EN
SDIN	SDIN_PD_EN
FSYNC	FSYNC_PD_EN
SBCLK	SBCLK_PD_EN

6.5 Programming

The device contains configuration registers and programming coefficients that can be set to the desired values for a specific system and application use. These registers are called device control registers and are each eight bits in width, mapped using a page scheme.

Each page contains 128 configuration registers. All key device configuration registers are stored in page 0, which is the default page setting at power up and after a software reset. All programmable coefficient registers are located in page 2, page 3 and later pages. The current page of the device can be switched to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

6.5.1 I²C Control Interface

The device supports the I²C control protocol as a target device, and is capable of operating in standard mode, fast mode, and fast mode plus. Device configuration and status are provided via the SDA and SCL pins using the I²C protocol.

6.5.2 I²C Address Selection

The TAS2573 can operate using one of four selectable device addresses. I²C target addresses is defined as the 7MSBs followed by read/write bit. [Table 6-45](#) below illustrates how to select the device I²C address and the address corresponds to R/W bit set to 0 (for example, ADDR[6:0], 1b'0). The I²C address is detected by sampling the address pins when SDZ pin is released or when device is reset using software reset bit.

Table 6-45. I²C Mode Address Selection

I ² C TARGET ADDRESS	AD2 PIN	AD1 PIN
0x80 (global address)	NA	NA
0x98	GND	GND
0x9A	GND	IOVDD
0x9C	IOVDD	GND
0x9E	IOVDD	IOVDD

The TAS2573 has a global 7-bit I²C address 0x40 (0x80 in 8-bit format with R/W bit set to 0). When enabled the device additionally responds to I²C commands at this address regardless of the address pins selected. This is used to speed up device configuration when using multiple TAS2573 devices and programming similar settings across all devices. The I²C ACK / NACK cannot be used during the multi-device writes since multiple devices are responding to the I²C command. The I²C CRC function must be used to maintain each device properly received the I²C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C_CKSUM* register must be checked on each device using the local address for a proper value. The global I²C address can be disabled using *I2C_GBL_EN* register.

Table 6-46. I²C Global Address Enable

<i>I2C_GBL_EN</i>	SETTING
0	Disabled
1	Enabled (default)

6.5.3 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred MSB first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

The controller device drives a start condition followed by the 7-bit target address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledgment condition. The target device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the controller device transmits the next byte of the sequence. Each target device is addressed by a unique 7-bit target address plus the R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the controller device generates a stop condition to release the bus. Figure 6-14 shows a generic data transfer sequence.

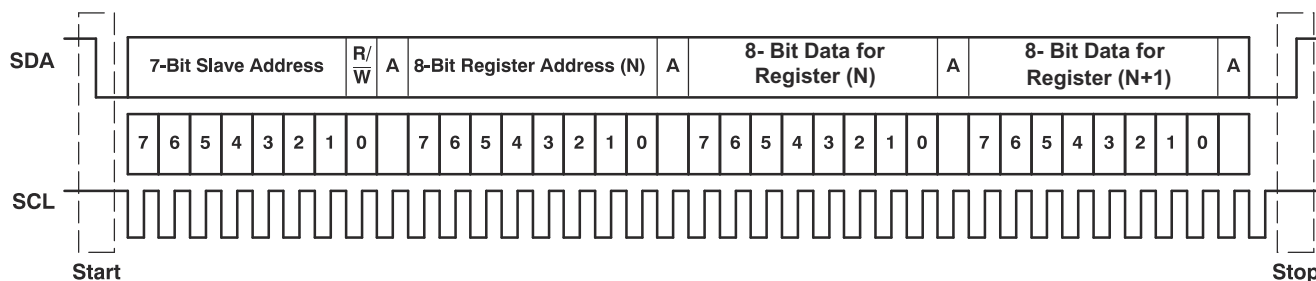


Figure 6-14. Typical I²C Sequence

In the system, use external pullup resistors for the SDA and SCL signals to set the logic high level for the bus. The SDA and SCL voltages must not exceed the device supply voltage, IOVDD.

6.5.4 I²C Single-Byte and Multiple-Byte Transfers

The device I²C interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the device responds with data, a byte at a time, starting at the register assigned, as long as the controller device continues to respond with acknowledges.

The device supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction takes place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many registers are written.

6.5.5 I²C Single-Byte Write

As shown in Figure 6-15, a single-byte data write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C target address and the read/write bit, the device responds with an acknowledge bit (ACK). Next, the controller device transmits the register byte corresponding to the device internal register address being accessed. After receiving the register byte, the device again responds with an acknowledge bit (ACK). Then, the controller device transmits the byte of data to be written to the specified register. When finished, the target device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition to complete the single-byte data write transfer.

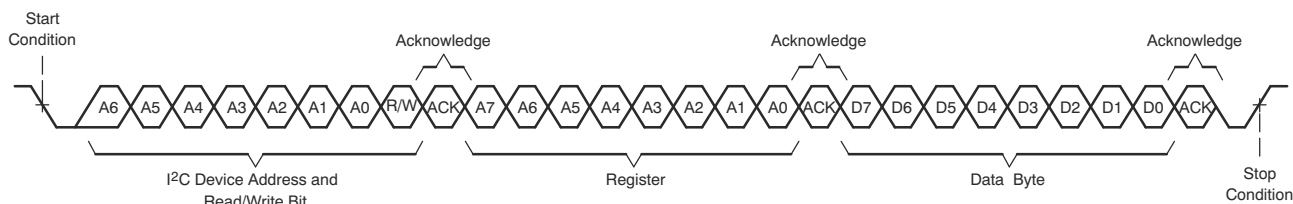


Figure 6-15. I²C Single-Byte Write Transfer

6.5.6 I²C Multiple-Byte Write

As shown in Figure 6-16, a multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the controller device to the target device. After receiving each data byte, the device responds with an acknowledge bit (ACK). Finally, the controller device transmits a stop condition after the last data-byte write transfer.

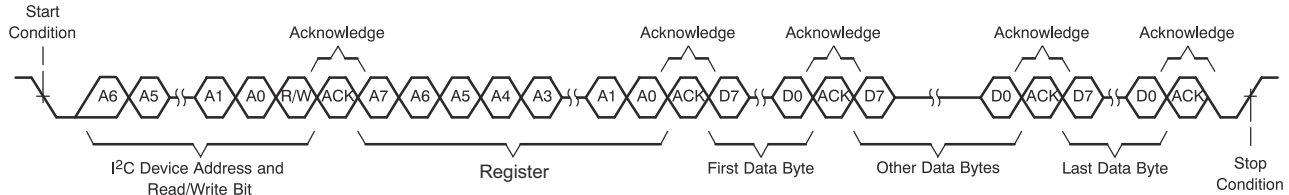


Figure 6-16. I²C Multiple-Byte Write Transfer

6.5.7 I²C Single-Byte Read

As shown in Figure 6-17, a single-byte data read transfer begins with the controller device transmitting a start condition followed by the I²C target address and the read/write bit. For the data read transfer, both a write followed by a read are done. Initially, a write is done to transfer the address byte of the internal register address to be read. As a result, the read/write bit is set to 0.

After receiving the target address and the read/write bit, the device responds with an acknowledge bit (ACK). The controller device then sends the internal register address byte, after which the device issues an acknowledge bit (ACK). The controller device transmits another start condition followed by the target address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the device transmits the data byte from the register address being read. After receiving the data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the single-byte data read transfer.

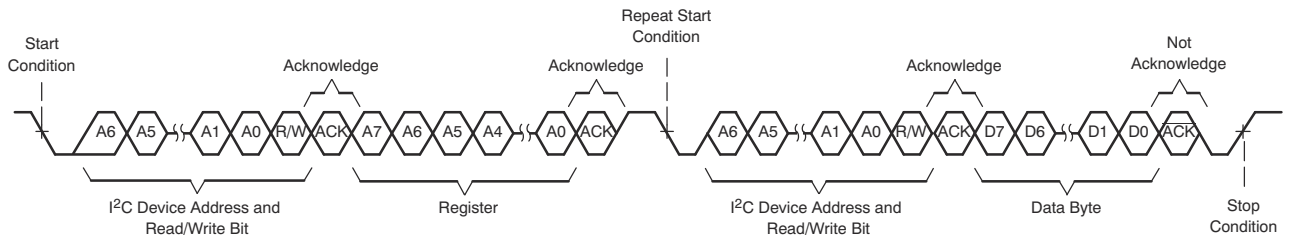


Figure 6-17. I²C Single-Byte Read Transfer

6.5.8 I²C Multiple-Byte Read

As shown in Figure 6-18, a multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the device to the controller device. With the exception of the last data byte, the controller device responds with an acknowledge bit after receiving each data byte. After receiving the last data byte, the controller device transmits a not-acknowledge (NACK) followed by a stop condition to complete the data read transfer.

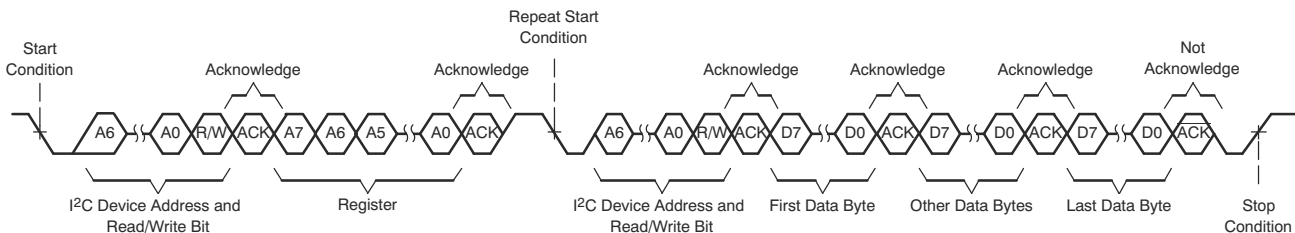


Figure 6-18. I²C Multiple-Byte Read Transfer

7 Register Maps

The device registers are organized into pages and books. The registers from Page 0 to Page 8 are all in Book 0, while the registers in Page 9 are in Book 100. The register map book number can be changed by programming the *BOOK[7:0]* register bit, and page number can be changed by programming *PAGE[7:0]* register bits.

7.1 PAGE_0 Registers

Table 7-1 lists the memory-mapped registers for the PAGE_0 registers. All register offset addresses not listed in Table 7-1 must be considered as reserved locations and the register contents must not be modified.

Table 7-1. PAGE_0 Registers

Offset	Acronym	Register Name	Section
0h	Page	Device Page	Section 7.1.1
1h	SW_RESET	Software Reset	Section 7.1.2
2h	PWR_CTL	Power Control	Section 7.1.3
3h	DEVICE_CFG_01	Device configuration registers	Section 7.1.4
4h	DEVICE_CFG_02	Device configuration registers	Section 7.1.5
5h	DEVICE_CFG_03	Device configuration registers	Section 7.1.6
6h	DEVICE_CFG_04	Device configuration registers	Section 7.1.7
7h	DEVICE_CFG_05	Device configuration registers	Section 7.1.8
8h	TDM_CFG1	TDM Configuration registers	Section 7.1.9
9h	TDM_CFG2	TDM Configuration registers	Section 7.1.10
Ah	TDM_CFG3	TDM Configuration registers	Section 7.1.11
Ch	TDM_CFG5	TDM Configuration registers	Section 7.1.12
Dh	TDM_CFG6	TDM Configuration registers	Section 7.1.13
Eh	TDM_CFG7	TDM Configuration registers	Section 7.1.14
Fh	TDM_CFG8	TDM Configuration registers	Section 7.1.15
10h	TDM_CFG9	TDM Configuration registers	Section 7.1.16
11h	TDM_CFG10	TDM Configuration registers	Section 7.1.17
12h	TDM_CFG11	TDM Configuration registers	Section 7.1.18
13h	TDM_CFG12	TDM Configuration registers	Section 7.1.19
14h	TDM_DET	TDM Clock detection monitor	Section 7.1.20
15h	MONITOR_CFG_01	Monitoring Configuration	Section 7.1.21
16h	MONITOR_CFG_02	Monitoring Configuration	Section 7.1.22
17h	LIM_CFG_0	Limiter configuration	Section 7.1.23
18h	BOP_CFG_0	Brown out protection configuration	Section 7.1.24
19h	TONE_GEN_01	Internal tone generator	Section 7.1.25
1Ah	TONE_GEN_02	Internal tone generator	Section 7.1.26
1Bh	IO_CFG_01	IO Configuration	Section 7.1.27
1Ch	IO_CFG_02	IO Configuration	Section 7.1.28
1Dh	IO_CFG_03	IO Configuration	Section 7.1.29
1Eh	NG_CFG0	Noise Gate Controls	Section 7.1.30
21h	BST_CFG_01	Boost Configuration	Section 7.1.31
22h	BST_CFG_02	Boost Configuration	Section 7.1.32
25h	INTERRUPT_CFG1	IRQZ clear	Section 7.1.33
2Ch	TDM_CFG13	TDM Configuration registers	Section 7.1.34
2Eh	TDM_CFG15	TDM Configuration registers	Section 7.1.35
31h	CLASSD_CFG_01	Class	Section 7.1.36
32h	CLASSD_CFG_02	Class	Section 7.1.37
3Bh	BST_CFG_05	Boost Configuration	Section 7.1.38
3Ch	THERM_CFG	Thermal warning configuration	Section 7.1.39
5Bh	INT_MASK_0	Interrupt Masks	Section 7.1.40
5Ch	INT_MASK_1	Interrupt Masks	Section 7.1.41

Table 7-1. PAGE_0 Registers (continued)

Offset	Acronym	Register Name	Section
5Dh	INT_MASK_2	Interrupt Masks	Section 7.1.42
5Fh	INT_MASK_3	Interrupt Masks	Section 7.1.43
60h	INT_LATCH_0	Latched interrupt readback	Section 7.1.44
61h	INT_LATCH_1	Latched interrupt readback	Section 7.1.45
62h	INT_LATCH_2	Latched interrupt readback	Section 7.1.46
63h	INT_LATCH_3	Latched interrupt readback	Section 7.1.47
64h	INT_LATCH_4	Latched interrupt readback	Section 7.1.48
65h	NG_IDLE_STATUS	Latched interrupt readback	Section 7.1.49
66h	INT_MASK_5	Interrupt Masks	Section 7.1.50
67h	INT_LATCH_5	Latched interrupt readback	Section 7.1.51
78h	REV_ID	Revision and PG ID	Section 7.1.52
7Fh	BOOK	Device Book	Section 7.1.53

7.1.1 Page Register (Offset = 0h) [Reset = 00h]

Page is shown in [Table 7-2](#).

Return to the [Summary Table](#).

The device's memory map is divided into pages and books. This register sets the page.

Table 7-2. Page Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE	R/W	0h	Sets the device page. 00h = Page 0 01h = Page 1 FFh = Page 255

7.1.2 SW_RESET Register (Offset = 1h) [Reset = 00h]

SW_RESET is shown in [Table 7-3](#).

Return to the [Summary Table](#).

Asserting Software Reset places all register values in the default POR (Power on Reset) state.

Table 7-3. SW_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	RESERVED
0	SW_RESET	R/W	0h	Software reset. Bit is self clearing. 0h = Don't reset 1h = Reset

7.1.3 PWR_CTL Register (Offset = 2h) [Reset = 02h]

PWR_CTL is shown in [Table 7-4](#).

Return to the [Summary Table](#).

Sets device's mode of operation and Power Configuration

Table 7-4. PWR_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	RESERVED
1-0	MODE	R/W	2h	Device operational mode. 0h = Active 1h = Mute 2h = Software Shutdown 3h = Wake-up and Shutdown on ASI Clock

7.1.4 DEVICE_CFG_01 Register (Offset = 3h) [Reset = C0h]

DEVICE_CFG_01 is shown in [Table 7-5](#).

Return to the [Summary Table](#).

This register configures the various device modes.

Table 7-5. DEVICE_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EFFICIENCY_MODE	R/W	3h	Device operational mode. 0h = Music Efficiency and Noise Gate mode disabled 1h = Noise Gate Mode Only 2h = Music Efficiency Only 3h = Music Efficiency + Noise Gate mode
5-2	RESERVED	R	0h	RESERVED
1-0	SDZ_MODE	R/W	0h	SDZ Mode configuration. 0h = Soft shutdown and device reset 1h = Immediate shutdown and device reset 2h = Soft shutdown only (registers settings are not cleared) 3h = Reserved

7.1.5 DEVICE_CFG_02 Register (Offset = 4h) [Reset = 8Ch]

DEVICE_CFG_02 is shown in [Table 7-6](#).

Return to the [Summary Table](#).

This register configures the various device modes.

Table 7-6. DEVICE_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_GBL_EN	R/W	1h	I2C global address is 0h = Disabled 1h = Enabled
6	RESERVED	R	0h	Reserved
5-3	CLK_HALT_TIME	R/W	1h	Device aborts the clock check after the time out defined by this register 0h = Perpetual checking mode. ASI CLK check is never aborted 1h = 800 us 2h = 3.2ms 3h = 34.1ms 4h = 68.3ms 5h = 256ms 6h = 768ms 7h = 1.3s
2	CLK_BASED_PWR_UP	R/W	1h	Power up/down based on valid ASI clocks is 0h = Disable 1h = Enabled.
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.6 DEVICE_CFG_03 Register (Offset = 5h) [Reset = 00h]

DEVICE_CFG_03 is shown in [Table 7-7](#).

Return to the [Summary Table](#).

This register configures the various device modes.

Table 7-7. DEVICE_CFG_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	OCE_RETRY	R/W	0h	Retry after over current event. 0h = Do not retry 1h = Retry after "RETRY_WAIT_TIME"
4	OTE_RETRY	R/W	0h	Retry after over temperature event. 0h = Do not retry 1h = Retry after "RETRY_WAIT_TIME"
3	RESERVED	R	0h	Reserved
2	CLKE_RETRY	R/W	0h	Retry after Internal Clock Error event. 0h = Do not retry 1h = Retry after "RETRY_WAIT_TIME"
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.7 DEVICE_CFG_04 Register (Offset = 6h) [Reset = 04h]

DEVICE_CFG_04 is shown in [Table 7-8](#).

Return to the [Summary Table](#).

This register configures the various device modes.

Table 7-8. DEVICE_CFG_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	RESERVED
5-4	SEL_VBAT_MODE	R/W	0h	Selects VBAT mode of operation 0h = VBAT 1S mode, VBAT pin voltage monitored 1h = VBAT 1S mode, VBAT_SNS pin voltage monitored Ah = VBAT 2S mode, VBAT_SNS pin voltage monitored Bh = RESERVED
3-2	IRQZ_PIN_CFG	R/W	1h	IRQZ interrupt configuration. IRQZ asserts 0h = on any unmasked live interrupts 1h = on any unmasked latched interrupts 2h = for 2-4ms one time on any unmasked live interrupt event 3h = for 2-4ms every 4ms on any unmasked latched interrupts
1	RESERVED	R	0h	RESERVED
0	RETRY_WAIT_TIME	R/W	0h	Retry wait time after device detects error (Valid only for errors with retry options available) 0h = 1.5 sec 1h = 100ms

7.1.8 DEVICE_CFG_05 Register (Offset = 7h) [Reset = 00h]

DEVICE_CFG_05 is shown in [Table 7-9](#).

Return to the [Summary Table](#).

This register configures the various device modes.

Table 7-9. DEVICE_CFG_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	SAMPLE_RATE_CFG	R/W	0h	Sampling Rate selection 0h = Audio data rate is multiple/sub-multiple of 48Ksps 1h = Audio data rate is multiple/sub-multiple of 44.1Ksps
5-0	AMP_LVL	R/W	0h	Device Channel Gain setting 0h = 21.000dB 1h = 20.498dB 2h = 19.997dB 3h = 19.495dB 4h = 18.993dB 26h = 1.935dB 27h = 1.434dB 28h = 0.932dB 29h = 0.430dB 2Ah = -0.071dB

7.1.9 TDM_CFG1 Register (Offset = 8h) [Reset = 82h]

TDM_CFG1 is shown in [Table 7-10](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-10. TDM_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FRAME_START	R/W	1h	TDM frame start polarity. 0h = Low to High on FSYNC 1h = High to Low on FSYNC
6	RX_JUSTIFY	R/W	0h	TDM RX sample justification within the time slot. 0h = Left 1h = Right
5-1	RX_OFFSET	R/W	1h	TDM RX start of frame to time slot 0 offset (SBCLK cycles).
0	RX_EDGE	R/W	0h	TDM RX capture clock polarity. 0h = Rising edge of SBCLK 1h = Falling edge of SBCLK

7.1.10 TDM_CFG2 Register (Offset = 9h) [Reset = 0Ah]

TDM_CFG2 is shown in [Table 7-11](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-11. TDM_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	IVMON_SLEN	R/W	0h	Sets the current and voltage data to length of 0h = 16 bits 1h = 12 bits 2h = 8 bits 3h = RESERVED
5-4	RESERVED	R	0h	RESERVED
3-2	RX_WLEN	R/W	2h	TDM RX word length. 0h = 16-bits 1h = 20-bits 2h = 24-bits 3h = 32-bits
1-0	RX_SLEN	R/W	2h	TDM RX time slot length. 0h = 16-bits 1h = 24-bits 2h = 32-bits 3h = RESERVED

7.1.11 TDM_CFG3 Register (Offset = Ah) [Reset = 10h]

TDM_CFG3 is shown in [Table 7-12](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-12. TDM_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RX_SLOT_R	R/W	1h	TDM RX Right Audio Channel Time Slot.
3-0	RX_SLOT_L	R/W	0h	TDM RX Left Audio Channel Time Slot.

7.1.12 TDM_CFG5 Register (Offset = Ch) [Reset = 13h]

TDM_CFG5 is shown in [Table 7-13](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-13. TDM_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_KEEPCY	R/W	0h	TDM TX SDOUT LSB data is driven for 0h = full-cycle 1h = half-cycle
6	TX_KEEPLN	R/W	0h	TDM TX SDOUT holds the bus for the following when TX_KEEPEN is enabled 0h = 1LSB cycle 1h = always
5	TX_KEEPEN	R/W	0h	TDM TX SDOUT bus keeper enable. 0h = Disable bus keeper 1h = Enable bus keeper
4	TX_FILL	R/W	1h	TDM TX SDOUT unused bitfield fill. 0h = Transmit 0 1h = Transmit Hi-Z
3-1	TX_OFFSET	R/W	1h	TDM TX start of frame to time slot 0 offset.
0	TX_EDGE	R/W	1h	TDM TX launch clock polarity. 0h = Rising edge of SBCLK 1h = Falling edge of SBCLK

7.1.13 TDM_CFG6 Register (Offset = Dh) [Reset = 02h]

TDM_CFG6 is shown in [Table 7-14](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-14. TDM_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	VSNS_TX	R/W	0h	TDM TX voltage sense transmit enable. 0h = Disabled 1h = Enabled
5-0	VSNS_SLOT	R/W	2h	TDM TX voltage sense time slot.

7.1.14 TDM_CFG7 Register (Offset = Eh) [Reset = 00h]

TDM_CFG7 is shown in [Table 7-15](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-15. TDM_CFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	ISNS_TX	R/W	0h	TDM TX current sense transmit enable. 0h = Disabled 1h = Enabled
5-0	ISNS_SLOT	R/W	0h	TDM TX current sense time slot.

7.1.15 TDM_CFG8 Register (Offset = Fh) [Reset = 04h]

TDM_CFG8 is shown in [Table 7-16](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-16. TDM_CFG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VBAT_SLEN	R/W	0h	TDM TX VBAT time slot length. 0h = Truncate to 8-bits 1h = Left justify to 16-bits
6	VBAT_TX	R/W	0h	TDM TX VBAT transmit enable. 0h = Disabled 1h = Enabled
5-0	VBAT_SLOT	R/W	4h	TDM TX VBAT time slot.

7.1.16 TDM_CFG9 Register (Offset = 10h) [Reset = 05h]

TDM_CFG9 is shown in [Table 7-17](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-17. TDM_CFG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	TEMP_TX	R/W	0h	TDM TX temp sensor transmit enable. 0h = Disabled 1h = Enabled
5-0	TEMP_SLOT	R/W	5h	TDM TX temp sensor time slot.

7.1.17 TDM_CFG10 Register (Offset = 11h) [Reset = 07h]

TDM_CFG10 is shown in [Table 7-18](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-18. TDM_CFG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	STATUS_TX	R/W	0h	TDM TX status bits transmit enable. 0h = Disabled 1h = Enabled
5-0	STATUS_SLOT	R/W	7h	TDM TX status bits time slot.

7.1.18 TDM_CFG11 Register (Offset = 12h) [Reset = 06h]

TDM_CFG11 is shown in [Table 7-19](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-19. TDM_CFG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PVDD_SLEN	R/W	0h	TDM TX PVDD time slot length. 0h = Truncate to 8-bits 1h = Left justify to 16-bits
6	PVDD_TX	R/W	0h	TDM TX PVDD transmit enable. 0h = Disabled 1h = Enabled
5-0	PVDD_SLOT	R/W	6h	TDM TX PVDD time slot.

7.1.19 TDM_CFG12 Register (Offset = 13h) [Reset = 12h]

TDM_CFG12 is shown in [Table 7-20](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-20. TDM_CFG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AUDIO_SLEN	R/W	0h	TDM audio slot length 0h = 16-bits 1h = 24-bits
6	AUDIO_TX	R/W	0h	TDM audio output transmit enable 0h = Disabled 1h = Enabled
5-0	AUDIO_SLOT	R/W	12h	TDM TX status time slot.

7.1.20 TDM_DET Register (Offset = 14h) [Reset = 7Fh]

TDM_DET is shown in [Table 7-21](#).

Return to the [Summary Table](#).

Readback of internal auto-rate detection.

Table 7-21. TDM_DET Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6-3	FS_RATIO_DETECTED	R	Fh	Detected SBCLK to FSYNC ratio. 00h = 16 01h = 24 02h = 32 03h = 48 04h = 64 05h = 96 06h = 128 07h = 192 08h = 256 09h = 384 0Ah = 512 0Bh = 125 0Dh = 500 0Eh = RESERVED 0Fh = Invalid ratio
2-0	FS_RATE_DETECTED	R	7h	Detected sample rate of TDM bus. 0h = RESERVED 1h = 14.7/16KHz 2h = 22.05/24KHz 3h = 29.4/32KHz 4h = 44.1/48KHz 5h = 88.2/96kHz 6h = 176.4/192kHz 7h = Error condition

7.1.21 MONITOR_CFG_01 Register (Offset = 15h) [Reset = 00h]

MONITOR_CFG_01 is shown in [Table 7-22](#).

Return to the [Summary Table](#).

This register configures the Monitor channels of the device

Table 7-22. MONITOR_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SUPPLY_SAMPLING_RATE	R/W	0h	Configure VBAT and PVDD sampling rates 0h = VBAT Sampling rate is higher than PVDD 1h = PVDD Sampling rate is higher than VBAT
6-0	RESERVED	R	0h	RESERVED

7.1.22 MONITOR_CFG_02 Register (Offset = 16h) [Reset = 30h]

MONITOR_CFG_02 is shown in [Table 7-23](#).

Return to the [Summary Table](#).

This register configures the Monitor channels of the device

Table 7-23. MONITOR_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IVSENSE_LPF_ENABLE	R/W	0h	Control for 6kHz LPF on the IV sense channel 0h = IV Sense LPF disabled 1h = IV sense LPF enabled
6-5	VSENSE_GAIN_SEL	R/W	1h	VSNS Full-scale (FS) programming
4-3	ISENSE_GAIN_SEL	R/W	2h	ISNS Full-scale (FS) programming
2-0	RESERVED	R	0h	RESERVED

7.1.23 LIM_CFG_0 Register (Offset = 17h) [Reset = 00h]

LIM_CFG_0 is shown in [Table 7-24](#).

Return to the [Summary Table](#).

This register configures the voltage limiter module

Table 7-24. LIM_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIM_MODE	R/W	0h	Limiter enable. 0h = Disabled 1h = VBAT voltage based limiter mode 2h = PVDD voltage based limiter mode 3h = ClassH Boost voltage based voltage limiter
5	SUPPLY_HEADROOM_LIM_MODE	R/W	0h	Select Limiter threshold based on supply headroom 0h = Disabled 1h = Enabled
4-0	RESERVED	R	0h	RESERVED

7.1.24 BOP_CFG_0 Register (Offset = 18h) [Reset = 00h]

BOP_CFG_0 is shown in [Table 7-25](#).

Return to the [Summary Table](#).

This register configures brown out protection module

Table 7-25. BOP_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	RESERVED
4	BOP_SRC	R/W	0h	Brown out prevention Source control 0h = VBAT 1h = PVDD
3	BOPSD_EN	R/W	0h	Brown out prevention shutdown enable. 0h = Disabled 1h = Enabled. Device shuts down when VBAT voltage is lower than programmed BOPD_THR_LVL[24:0]
2	BOP_HLD_CLR	R/W	0h	BOP infinite hold clear (self clearing). Available when BOP_INF_HLD = 1 0h = Don't clear 1h = Clear.
1	BOP_INF_HLD	R/W	0h	Infinite hold on brown out event. 0h = Use BOP_HLD_TM after brown out event 1h = Don't release until BOP_HLD_CLR is asserted high
0	BOP_EN	R/W	0h	Brown out prevention (BOP) enable. 0h = Disabled 1h = Enabled

7.1.25 TONE_GEN_01 Register (Offset = 19h) [Reset = 40h]

TONE_GEN_01 is shown in [Table 7-26](#).

Return to the [Summary Table](#).

Configurations for internal tone generator

Table 7-26. TONE_GEN_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INTERNAL_TONE_PLAYBACK_EN	R/W	0h	Pilot Tone signal playback control 0h = Pilot tone is not generated 1h = Pilot tone is generated (chirp_en must be set 0)
6	INTERNAL_TONE_MIXING_EN	R/W	1h	Internal tone mixing control 0h = Only tone is played(Audio data from ASI is ignored by FW) 1h = Tone signal is mixed with Audio data and played together
5	INTERNAL_TONE_CLK_SEL	R/W	0h	Clock source for tone generator 0h = External clocks 1h = Internal Oscillator
4	RESERVED	R	0h	Reserved
3-0	RESERVED	R	0h	RESERVED

7.1.26 TONE_GEN_02 Register (Offset = 1Ah) [Reset = 96h]

TONE_GEN_02 is shown in [Table 7-27](#).

Return to the [Summary Table](#).

Configurations for internal tone generator

Table 7-27. TONE_GEN_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CHIRP_FREQ_CYCLES	R/W	9h	No of cycles of each frequency in the chirp. Next frequency is always at zero cross of previous frequency cycle. 0h = 1 Cycle 1h = 2 Cycles Fh = 16 Cycles
3	CHIRP_EN	R/W	0h	Chirp Tone playback Control (Dynamic reg) (Note: ASI must be active with valid clock and fsync. Audio data can be Zero) 0h = Chirp tone is not generated 1h = Chirp tone is generated (pilot_tone_en must be set 0)
2	INTERNAL_TONE_GEN_ENZ	R/W	1h	Disables internal tone generation feature (Need to reset this bit to use tone feature) 0h = Tone Generator enabled 1h = Tone Generator disabled
1	CHIRP_RAMP_EN	R/W	1h	Chirp Ramp Control 0h = Ramp up/down disabled 1h = Ramp up/down enabled
0	RESERVED	R	0h	RESERVED

7.1.27 IO_CFG_01 Register (Offset = 1Bh) [Reset = 01h]

IO_CFG_01 is shown in [Table 7-28](#).

Return to the [Summary Table](#).

This register configures the IO buffers

Table 7-28. IO_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SDO_DRIVE_SEL	R/W	0h	Drive strength control register for SDO pad 0h = 2mA drive setting 1h = 4mA drive setting 2h = 6mA drive setting 3h = 8mA drive setting
5-4	IRQZ_DRIVE_SEL	R/W	0h	Drive strength control register for IRQZ pad 0h = 2mA drive setting 1h = 4mA drive setting 2h = 6mA drive setting 3h = 8mA drive setting
3-2	SDA_DRIVE_SEL	R/W	0h	Drive strength control register for SDA pad 0h = 2mA drive setting 1h = 4mA drive setting 2h = 6mA drive setting 3h = 8mA drive setting
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.28 IO_CFG_02 Register (Offset = 1Ch) [Reset = 3Ch]

IO_CFG_02 is shown in [Table 7-29](#).

Return to the [Summary Table](#).

This register configures the IO buffers

Table 7-29. IO_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IRQZ_POL	R/W	0h	IRQZ pin polarity for interrupt. 0h = Active low 1h = Active High
6	IRQZ_PU	R/W	0h	IRQZ internal pull/dn up enable. 0h = pull-up/dn disabled 1h = pull-up/dn enabled as per irqz_pol
5	EN_SDO_OUTPUT	R/W	1h	SDO (ASI) O/P Stage Enable 0h = SDO O/P Stage is disabled during function mode (Tristated) 1h = Enabled during function mode
4	EN_ASI2_SDO_OUTPUT	R/W	1h	SDO (ASI) O/P Stage Enable 0h = SDO O/P Stage is disabled during function mode (Tristated) 1h = Enabled during function mode
3	EN_ASI2_SBCLK_OUTP UT	R/W	1h	SDO (ASI) O/P Stage Enable 0h = SDO O/P Stage is disabled during function mode (Tristated) 1h = Enabled during function mode
2	EN_ASI2_FSYNC_OUTP UT	R/W	1h	SDO (ASI) O/P Stage Enable 0h = SDO O/P Stage is disabled during function mode (Tristated) 1h = Enabled during function mode
1-0	ICC_DS	R/W	0h	Drive strength control register for ICC pad 0h = 2mA drive setting 1h = 4mA drive setting 2h = 6mA drive setting 3h = 8mA drive setting

7.1.29 IO_CFG_03 Register (Offset = 1Dh) [Reset = 00h]

IO_CFG_03 is shown in [Table 7-30](#).

Return to the [Summary Table](#).

This register configures the IO buffers

Table 7-30. IO_CFG_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	RESERVED
6	WPD_EN_SDZ	R/W	0h	Weak pull down enable - SDZ 0h = pull-dn disabled 1h = pull-dn enabled
5	AD1_PD_EN	R/W	0h	Weak pull down enable - AD1 0h = pull-dn disabled 1h = pull-dn enabled
4	AD2_PD_EN	R/W	0h	Weak pull down enable - AD2 0h = pull-dn disabled 1h = pull-dn enabled
3	SDOUT_PD_EN	R/W	0h	Weak pull down for SDOUT. 0h = Disabled 1h = Enabled
2	SDIN_PD_EN	R/W	0h	Weak pull down for SDIN. 0h = Disabled 1h = Enabled
1	FSYNC_PD_EN	R/W	0h	Weak pull down for FSYNC. 0h = Disabled 1h = Enabled
0	SBCLK_PD_EN	R/W	0h	Weak pull down for SBCLK. 0h = Disabled 1h = Enabled

7.1.30 NG_CFG0 Register (Offset = 1Eh) [Reset = 60h]

NG_CFG0 is shown in [Table 7-31](#).

Return to the [Summary Table](#).

Noise gate hysteresis, threshold level, and enable.

Table 7-31. NG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	NG_HYST_TIMER	R/W	1h	Noise Gate Entry hysteresis timer 0h = 10ms 1h = 50ms 2h = 100ms 3h = 1000ms
5-3	NG_TH_LVL	R/W	4h	Noise-gate audio threshold level 0h = -85dBFS 1h = -90dBFS 2h = -95dBFS 3h = -100dBFS 4h = -105dBFS 5h = -110dBFS 6h = -115dBFS 7h = -120dBFS
2-0	RESERVED	R	0h	RESERVED

7.1.31 BST_CFG_01 Register (Offset = 21h) [Reset = 12h]

BST_CFG_01 is shown in [Table 7-32](#).

Return to the [Summary Table](#).

This register configures internal Boost controller

Table 7-32. BST_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	RESERVED
4	BOOST_PHASE_SYNC_EN	R/W	1h	Boost Phase sync enable 0h = Disabled 1h = Enabled
3-2	BOOST_PHASE	R/W	0h	Boost Phase sync delay control, applicable only when BOOST_PHASE_SYNC_EN = 1 0h = Phase shift is 0ns 1h = Phase shift is 65ns 2h = Phase shift is 130ns 3h = Phase shift is 195ns
1	BOOST_PHASE_FROM_ADDRESS_PIN	R/W	1h	Boost Phase shift sync control selected automatically based on i2c slave address detected from Address pin. Applicable only when BOOST_PHASE_SYNC_EN = 1 0h = Disabled 1h = Enabled
0	RESERVED	R	0h	Reserved

7.1.32 BST_CFG_02 Register (Offset = 22h) [Reset = 23h]

BST_CFG_02 is shown in [Table 7-33](#).

Return to the [Summary Table](#).

This register configures internal Boost controller

Table 7-33. BST_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BST_MODE	R/W	0h	Boost Mode 0h = Class-H 1h = Class-G 2h = Always ON 3h = Always OFF (Passthrough)
5	BOOST_EN	R/W	1h	Boost enable 0h = Disabled (External PVDD mode) 1h = Enabled
4-3	BOOST_MIN_FREQ_SEL	R/W	0h	Boost active mode PFM lower limit 0h = No Limit 1h = 25kHz 2h = 50kHz 3h = RESERVED
2-1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.33 INTERRUPT_CFG1 Register (Offset = 25h) [Reset = 00h]

INTERRUPT_CFG1 is shown in [Table 7-34](#).

Return to the [Summary Table](#).

This register clears all the latched interrupt registers

Table 7-34. INTERRUPT_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5-2	RESERVED	R	0h	RESERVED
1	INT_CLR_LTCH	R/W	0h	Clear INT_LTCH registers 0h = Don't clear 1h = Clear (self clearing bit)
0	RESERVED	R	0h	RESERVED

7.1.34 TDM_CFG13 Register (Offset = 2Ch) [Reset = 00h]

TDM_CFG13 is shown in [Table 7-35](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-35. TDM_CFG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ECHOREF1_SLEN	R/W	0h	TDM TX Echo Reference Channel 1 time slot length. 0h = Truncate to 8-bits 1h = Left justify to 16-bits
6	ECHOREF1_TX	R/W	0h	TDM TX Echo Reference Channel 1 transmit enable. 0h = Disabled 1h = Enabled
5-0	ECHOREF1_SLOT	R/W	0h	TDM TX Echo Reference Channel 1 time slot.

7.1.35 TDM_CFG15 Register (Offset = 2Eh) [Reset = 00h]

TDM_CFG15 is shown in [Table 7-36](#).

Return to the [Summary Table](#).

This register configures device TDM modes

Table 7-36. TDM_CFG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Sets the current and voltage data to length of 0h = 16 bits 1h = 12 bits 2h = 8 bits 3h = RESERVED
3-0	RX_CFG	R/W	0h	TDM RX time slot select config. 0h = Channel with time slot equal to I2C address offset 1h = Left channel 2h = Right channel 3h = Stereo downmix (L+R)/2 4h = RESERVED 5h = RESERVED 6h = RESERVED 7h = RESERVED 8h = RESERVED 9h = RESERVED Ah = RESERVED Bh = RESERVED Ch = RESERVED

7.1.36 CLASSD_CFG_01 Register (Offset = 31h) [Reset = 34h]

CLASSD_CFG_01 is shown in [Table 7-37](#).

Return to the [Summary Table](#).

D amp configurations - This register configures the class-D amplifier

Table 7-37. CLASSD_CFG_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	CLASSD_OUTPUT_EDGE_RATE_CTRL	R/W	3h	Edgerate programmability control 0h = Class-D output edge rate of approximately 0.5V/ns 1h = Class-D output edge rate of approximately 1V/ns 2h = Reserved Class-D output edge rate of approximately 2V/ns
3	CLASSD_HIZ_MODE	R/W	0h	Amp output state in Noise gate mode 0h = Not Hi-Z 1h = Enabled
2	RESERVED	R	0h	Reserved
1-0	RESERVED	R	0h	RESERVED

7.1.37 CLASSD_CFG_02 Register (Offset = 32h) [Reset = 94h]

CLASSD_CFG_02 is shown in [Table 7-38](#).

Return to the [Summary Table](#).

D amp configurations - This register configures the class-D amplifier

Table 7-38. CLASSD_CFG_02 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_Y_BRIDGE_MODE	R/W	1h	Enable/Disable VDD Bridge mode during device operation 0h = VDD Bridge mode disabled 1h = VDD Bridge mode enabled
6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-2	Y_BRIDGE_HYST_TIME R	R/W	1h	Time hysteresis programmability 0h = 100 us 1h = 500 us 2h = 5ms 3h = 50ms
1-0	RESERVED	R	0h	RESERVED

7.1.38 BST_CFG_05 Register (Offset = 3Bh) [Reset = A7h]

BST_CFG_05 is shown in [Table 7-39](#).

Return to the [Summary Table](#).

This register configures internal Boost controller

Table 7-39. BST_CFG_05 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VBOOST_MAX_CTRL	R/W	A7h	Boost VMAX setting in class-H mode. 54h = 5.54V (Min setting) E5h = 15.11V (Max setting)

7.1.39 THERM_CFG Register (Offset = 3Ch) [Reset = 00h]

THERM_CFG is shown in [Table 7-40](#).

Return to the [Summary Table](#).

This register configures thermal warning detection

Table 7-40. THERM_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	RESERVED
0	EN_THERM_WARN_DET	R/W	0h	Enable control for thermal warning detection feature 0h = Disabled 1h = Enabled

7.1.40 INT_MASK_0 Register (Offset = 5Bh) [Reset = 01h]

INT_MASK_0 is shown in [Table 7-41](#).

Return to the [Summary Table](#).

This register configures Masks for Interrupt flags

Table 7-41. INT_MASK_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK0[7]	R/W	0h	Mask for Interrupt due to BOP Inf Hold flag 0h = Don't Mask 1h = Mask
6	INT_MASK0[6]	R/W	0h	Mask for Interrupt due to limiter attenuation flag 0h = Don't Mask 1h = Mask
5	INT_MASK0[5]	R/W	0h	Mask for Interrupt due to supply less than inf pt flag 0h = Don't Mask 1h = Mask
4	INT_MASK0[4]	R/W	0h	Mask for Interrupt due to limiter active flag 0h = Don't Mask 1h = Mask
3	INT_MASK0[3]	R/W	0h	Mask for Interrupt due to brownout detected flag 0h = Don't Mask 1h = Mask
2	INT_MASK0[2]	R/W	0h	Mask for Interrupt due to bop active flag 0h = Don't Mask 1h = Mask
1	INT_MASK0[1]	R/W	0h	Mask for Interrupt due to device active flag 0h = Don't Mask 1h = Mask
0	RESERVED	R	0h	Reserved

7.1.41 INT_MASK_1 Register (Offset = 5Ch) [Reset = 1Fh]

INT_MASK_1 is shown in [Table 7-42](#).

Return to the [Summary Table](#).

This register configures Masks for Interrupt flags

Table 7-42. INT_MASK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK1[7]	R/W	0h	Mask for Interrupt due to PVDD Under voltage 0h = Don't Mask 1h = Mask
6	INT_MASK1[6]	R/W	0h	Mask for Interrupt due to VBAT 2S supply under voltage 0h = Don't Mask 1h = Mask
5	INT_MASK1[5]	R/W	0h	Mask for Interrupt due to DacMod overflow 0h = Don't Mask 1h = Mask
4	INT_MASK1[4]	R/W	1h	Mask for Interrupt due to Thermal Warning 135C 0h = Don't Mask 1h = Mask
3	INT_MASK1[3]	R/W	1h	Mask for Interrupt due to Thermal Warning 125C 0h = Don't Mask 1h = Mask
2	INT_MASK1[2]	R/W	1h	Mask for Interrupt due to Thermal Warning 115C 0h = Don't Mask 1h = Mask
1	INT_MASK1[1]	R/W	1h	Mask for Interrupt due to Thermal Warning 105C 0h = Don't Mask 1h = Mask
0	INT_MASK1[0]	R/W	1h	Mask for Interrupt due to DSP Mask for Interrupt output 0h = Don't Mask 1h = Mask

7.1.42 INT_MASK_2 Register (Offset = 5Dh) [Reset = 00h]

INT_MASK_2 is shown in [Table 7-43](#).

Return to the [Summary Table](#).

This register configures Masks for Interrupt flags

Table 7-43. INT_MASK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK2[7]	R/W	0h	Mask for Interrupt due to watchdog expiry 0h = Don't Mask 1h = Mask
6	RESERVED	R	0h	Reserved
5	INT_MASK2[5]	R/W	0h	Mask for Interrupt due to frame out of sync 0h = Don't Mask 1h = Mask
4	INT_MASK2[4]	R/W	0h	Mask for Interrupt due to PLL clock error 0h = Don't Mask 1h = Mask
3	INT_MASK2[3]	R/W	0h	Mask for Interrupt due to tdm error 0h = Don't Mask 1h = Mask
2	INT_MASK2[2]	R/W	0h	Mask for Interrupt due to ratio change error flag 0h = Don't Mask 1h = Mask
1	INT_MASK2[1]	R/W	0h	Mask for Interrupt due to fs change error flag 0h = Don't Mask 1h = Mask
0	INT_MASK2[0]	R/W	0h	Mask for Interrupt due to invalid ratio fs flag 0h = Don't Mask 1h = Mask

7.1.43 INT_MASK_3 Register (Offset = 5Fh) [Reset = 1Ah]

INT_MASK_3 is shown in [Table 7-44](#).

Return to the [Summary Table](#).

This register configures Masks for Interrupt flags

Table 7-44. INT_MASK_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK4[7]	R/W	0h	Mask for Interrupt due to vbat_por 0h = Don't Mask 1h = Mask
7	INT_MASK3[7]	R/W	0h	Mask for Interrupt due to over temperature detected 0h = Don't Mask 1h = Mask
6	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	INT_MASK3[3]	R/W	1h	Mask for Interrupt due to Class-D Over current protection 0h = Don't Mask 1h = Mask
3	RESERVED	R	0h	Reserved
2	INT_MASK4[2]	R/W	0h	Mask for Interrupt due to clock halt flag. This interrupt also flags errors due to Pre-power-up clock error while using Wake-up-on-ASI feature 0h = Don't Mask 1h = Mask
2	INT_MASK3[2]	R/W	0h	Mask for Interrupt due to pvdd_ov_flag 0h = Don't Mask 1h = Mask
1	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.44 INT_LATCH_0 Register (Offset = 60h) [Reset = 00h]

INT_LATCH_0 is shown in [Table 7-45](#).

Return to the [Summary Table](#).

This register provides the status of latched interrupts

Table 7-45. INT_LATCH_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0[7]	R	0h	Interrupt due to BOP Inf Hold flag 0h = No interrupt 1h = Interrupt
6	INT_LTCH0[6]	R	0h	Interrupt due to limiter attenuation flag 0h = No interrupt 1h = Interrupt
5	INT_LTCH0[5]	R	0h	Interrupt due to supply less than inf pt flag 0h = No interrupt 1h = Interrupt
4	INT_LTCH0[4]	R	0h	Interrupt due to limiter active flag 0h = No interrupt 1h = Interrupt
3	INT_LTCH0[3]	R	0h	Interrupt due to brownout detected flag 0h = No interrupt 1h = Interrupt
2	INT_LTCH0[2]	R	0h	Interrupt due to bop active flag 0h = No interrupt 1h = Interrupt
1	INT_LTCH0[1]	R	0h	Live Interrupt due to device active flag 0h = No interrupt 1h = Interrupt
0	RESERVED	R	0h	Reserved

7.1.45 INT_LATCH_1 Register (Offset = 61h) [Reset = 00h]

INT_LATCH_1 is shown in [Table 7-46](#).

Return to the [Summary Table](#).

This register provides the status of latched interrupts

Table 7-46. INT_LATCH_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH1[7]	R	0h	Interrupt due to PVDD under voltage detection 0h = No interrupt 1h = Interrupt
6	INT_LTCH1[6]	R	0h	Interrupt due to VBAT2S under voltage detection 0h = No interrupt 1h = Interrupt
5	INT_LTCH1[5]	R	0h	Interrupt due to DacMod overflow 0h = No interrupt 1h = Interrupt
4	INT_LTCH1[4]	R	0h	Interrupt due to Thermal Warning 135C 0h = No interrupt 1h = Interrupt
3	INT_LTCH1[3]	R	0h	Interrupt due to Thermal Warning 125C 0h = No interrupt 1h = Interrupt
2	INT_LTCH1[2]	R	0h	Interrupt due to Thermal Warning 115C 0h = No interrupt 1h = Interrupt
1	INT_LTCH1[1]	R	0h	Interrupt due to Thermal Warning 105C 0h = No interrupt 1h = Interrupt
0	INT_LTCH1[0]	R	0h	Interrupt due to DSP Mask for Interrupt output 0h = No interrupt 1h = Interrupt

7.1.46 INT_LATCH_2 Register (Offset = 62h) [Reset = 00h]

INT_LATCH_2 is shown in [Table 7-47](#).

Return to the [Summary Table](#).

This register provides the status of latched interrupts

Table 7-47. INT_LATCH_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH2[7]	R	0h	Interrupt due to watchdog expiry 0h = No interrupt 1h = Interrupt
6	RESERVED	R	0h	Reserved
5	INT_LTCH2[5]	R	0h	Interrupt due to frame out of sync 0h = No interrupt 1h = Interrupt
4	INT_LTCH2[4]	R	0h	Interrupt due to PLL clock error 0h = No interrupt 1h = Interrupt
3	INT_LTCH2[3]	R	0h	Interrupt due to tdm error 0h = No interrupt 1h = Interrupt
2	INT_LTCH2[2]	R	0h	Interrupt due to ratio change error flag 0h = No interrupt 1h = Interrupt
1	INT_LTCH2[1]	R	0h	Interrupt due to fs change error flag 0h = No interrupt 1h = Interrupt
0	INT_LTCH2[0]	R	0h	Interrupt due to invalid ratio fs flag 0h = No interrupt 1h = Interrupt

7.1.47 INT_LATCH_3 Register (Offset = 63h) [Reset = 00h]

INT_LATCH_3 is shown in [Table 7-48](#).

Return to the [Summary Table](#).

This register provides the status of latched interrupts

Table 7-48. INT_LATCH_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH3[7]	R	0h	Interrupt due to over temperature detected 0h = No interrupt 1h = Interrupt
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	INT_LTCH3[3]	R	0h	Interrupt due to Class-D Over current protection 0h = No interrupt 1h = Interrupt
2	INT_LTCH3[2]	R	0h	Interrupt due to Over voltage on PVDD supply. 0h = No interrupt 1h = Interrupt
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.48 INT_LATCH_4 Register (Offset = 64h) [Reset = 00h]

INT_LATCH_4 is shown in [Table 7-49](#).

Return to the [Summary Table](#).

This register provides the status of latched interrupts

Table 7-49. INT_LATCH_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH4[7]	R	0h	Interrupt due to VBAT under voltage detection 0h = No interrupt 1h = Interrupt
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	INT_LTCH4[2]	R	0h	Interrupt due to clock halt flag 0h = No interrupt 1h = Interrupt
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.1.49 NG_IDLE_STATUS Register (Offset = 65h) [Reset = 00h]

NG_IDLE_STATUS is shown in [Table 7-50](#).

Return to the [Summary Table](#).

This register provides the status of latched interrupts

Table 7-50. NG_IDLE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	NG_STATUS	R	0h	Noise mode status bit 0h = Device not in Noise gate mode 1h = Device in Noise gate mode
6	MUSIC_EFF_STATUS	R	0h	Music efficiency mode status bit 0h = Device not in music efficiency mode 1h = Device in music efficiency mode
5-0	RESERVED	R	0h	RESERVED

7.1.50 INT_MASK_5 Register (Offset = 66h) [Reset = 00h]

INT_MASK_5 is shown in [Table 7-51](#).

Return to the [Summary Table](#).

This register configures Masks for Interrupt flags

Table 7-51. INT_MASK_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK5[7]	R/W	0h	Mask for Interrupt due to completion of factory calibration 0h = Don't Mask 1h = Mask
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	INT_MASK5[4]	R/W	0h	Mask for Interrupt due to detection of short circuit 0h = Don't Mask 1h = Mask
3	INT_MASK5[3]	R/W	0h	Mask for Interrupt due to detection of open circuit 0h = Don't Mask 1h = Mask
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	
0	RESERVED	R	0h	

7.1.51 INT_LATCH_5 Register (Offset = 67h) [Reset = 00h]

INT_LATCH_5 is shown in [Table 7-52](#).

Return to the [Summary Table](#).

This register provides the status of latched interrupts of fct

Table 7-52. INT_LATCH_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH5[7]	R	0h	Interrupt due to completion of factory calibration 0h = No interrupt 1h = Interrupt
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	INT_LTCH5[4]	R	0h	Interrupt due to detection of short circuit 0h = No interrupt 1h = Interrupt
3	INT_LTCH5[3]	R	0h	Interrupt due to detection of open circuit 0h = No interrupt 1h = Interrupt
2	INT_LTCH5[2]	R	0h	Interrupt due to detection of silence in input audio 0h = No interrupt 1h = Interrupt
1	RESERVED	R	0h	
0	RESERVED	R	0h	

7.1.52 REV_ID Register (Offset = 78h) [Reset = 00h]

REV_ID is shown in [Table 7-53](#).

Return to the [Summary Table](#).

Returns REV and PG ID.

Table 7-53. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REV_ID	R	0h	Returns the revision ID.

7.1.53 BOOK Register (Offset = 7Fh) [Reset = 00h]

BOOK is shown in [Table 7-54](#).

Return to the [Summary Table](#).

Device's memory map is divided into pages and books. This register sets the book.

Table 7-54. BOOK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BOOK	R/W	0h	Sets the device book.

7.2 PAGE_1 Registers

Table 7-55 lists the memory-mapped registers for the PAGE_1 registers. All register offset addresses not listed in Table 7-55 must be considered as reserved locations and the register contents must not be modified.

Table 7-55. PAGE_1 Registers

Offset	Acronym	Register Name	Section
0h	PAGE	Device Page	Section 7.2.1
Ah	BOOST_TUNING_12	Boost configuration Register	Section 7.2.2
Bh	MISC_01	Misc Configuration	Section 7.2.3
Eh	DEV_PERF_TUNING_07	Device Performance Tuning Register	Section 7.2.4
10h	FAULT_DET_DIS	Fault Register	Section 7.2.5
17h	DEVICE_CFG_06	IV Sense performance Tuning register	Section 7.2.6
18h	PVDD_OVLO1	PVDD Over voltage	Section 7.2.7
19h	DEVICE_CFG_07	Device configuration	Section 7.2.8
1Ah	PVDD_OVLO2	PVDD Over voltage	Section 7.2.9
1Fh	DEV_PERF_TUNING_20	Device performance tuning register	Section 7.2.10
21h	DEVICE_CFG_08	Power Control	Section 7.2.11
23h	DEV_PERF_TUNING_11	Device performance tuning register	Section 7.2.12
29h	DEVICE_CFG_09	Device configuration	Section 7.2.13
2Bh	DEV_PERF_TUNING_04	Device performance Tuning register	Section 7.2.14
64h	I2C_CKSUM	I2C Checksum	Section 7.2.15

7.2.1 PAGE Register (Offset = 0h) [Reset = 00h]

PAGE is shown in [Table 7-56](#).

Return to the [Summary Table](#).

The device's memory map is divided into pages and books. This register sets the page.

Table 7-56. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE	R/W	0h	Sets the device page. 00h = Page 0 01h = Page 1 FFh = Page 255

7.2.2 BOOST_TUNING_12 Register (Offset = Ah) [Reset = 98h]

BOOST_TUNING_12 is shown in [Table 7-57](#).

Return to the [Summary Table](#).

Boost Configuration

Table 7-57. BOOST_TUNING_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-2	BOOST_TUNING_12	R/W	6h	Boost tuning register. Can be configured using the PPC3 software
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.2.3 MISC_01 Register (Offset = Bh) [Reset = 00h]

MISC_01 is shown in [Table 7-58](#).

Return to the [Summary Table](#).

This register is for loopbacks for debug purpose

Table 7-58. MISC_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	TDM_LOOPBACK	R/W	0h	SDIN to SDOUT pin loopback option 0h = Disabled 1h = Loop back enabled
4	TDM_DESER_LOOPBACK	R/W	0h	SDIN to SDOUT loopback after ASI protocol deserializer 0h = Disabled 1h = Loop back enabled
3-2	RESERVED	R	0h	Reserved
1-0	RESERVED	R	0h	Reserved

7.2.4 DEV_PERF_TUNING_07 Register (Offset = Eh) [Reset = 0Bh]

DEV_PERF_TUNING_07 is shown in [Table 7-59](#).

Return to the [Summary Table](#).

Device Performance Tuning

Table 7-59. DEV_PERF_TUNING_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-0	DEV_PERF_TUNING_07	R/W	Bh	Device performance tuning register 0h = External PVDD mode tuning Bh = 1S mode tuning

7.2.5 FAULT_DET_DIS Register (Offset = 10h) [Reset = 00h]

FAULT_DET_DIS is shown in [Table 7-60](#).

Return to the [Summary Table](#).

Control for fault reaction to device

Table 7-60. FAULT_DET_DIS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	PVDD_OV_DET_DIS	R/W	0h	Device Shutdown in the event of PVDD OV event.
0	DEV_PERF_TUNING_22	R/W	0h	Device performance tuning. PPC3 software generates the correct configuration required

7.2.6 DEVICE_CFG_06 Register (Offset = 17h) [Reset = 29h]

DEVICE_CFG_06 is shown in [Table 7-61](#).

Return to the [Summary Table](#).

IV Sense performance Tuning

Table 7-61. DEVICE_CFG_06 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-2	CLASSH_TUNING_06	R/W	Ah	Eh = Tuning Register
1-0	IV_TUNING_06	R/W	1h	IV Sense performance Tuning register 0h = Reserved 1h = Reserved 2h = Performance Tuning 3h = Reserved

7.2.7 PVDD_OVLO1 Register (Offset = 18h) [Reset = 6Bh]

PVDD_OVLO1 is shown in [Table 7-62](#).

Return to the [Summary Table](#).

Configures PVDD OVLO voltage in external PVDD mode

Table 7-62. PVDD_OVLO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PVDD_OVLO_TH_SEL_E XT_BOOST	R/W	1h	PVDD ovlo threshold selection during external PVDD mode 0h = 13.5V 1h = 14V 2h = 15V 3h = 16V
5-4	RESERVED	R	0h	Reserved
3-2	BOOST_TUNING_13	R/W	2h	Boost tuning register 0h = Reserved 1h = 2S mode of operation 2h = 1S mode of operation 3h = Reserved
1-0	RESERVED	R	0h	Reserved

7.2.8 DEVICE_CFG_07 Register (Offset = 19h) [Reset = 23h]

DEVICE_CFG_07 is shown in [Table 7-63](#).

Return to the [Summary Table](#).

This register is to get boost performance to meet the device specification

Table 7-63. DEVICE_CFG_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	DEV_PERF_TUNING_03	R/W	1h	Device performance tuning register 0h = Device performance configuration 1h = Reserved
4	DEV_PERF_TUNING_23	R/W	0h	Device performance tuning register
3-0	RESERVED	R	0h	Reserved

7.2.9 PVDD_OVLO2 Register (Offset = 1Ah) [Reset = C4h]

PVDD_OVLO2 is shown in [Table 7-64](#).

Return to the [Summary Table](#).

Configures PVDD OVLO voltage in Internal boost mode

Table 7-64. PVDD_OVLO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PVDD_OVLO_TH_SEL	R/W	3h	Pvdd ovlo threshold selection - Internal boost mode 0h = 13.5V 1h = 14V 2h = 15V 3h = 16V
5-3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.2.10 DEV_PERF_TUNING_20 Register (Offset = 1Fh) [Reset = 00h]

DEV_PERF_TUNING_20 is shown in [Table 7-65](#).

Return to the [Summary Table](#).

Device performance tuning

Table 7-65. DEV_PERF_TUNING_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	dig_spare_01	R/W	0h	Device performance tuning. PPC3 software generates the correct configuration required
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.2.11 DEVICE_CFG_08 Register (Offset = 21h) [Reset = 00h]

DEVICE_CFG_08 is shown in [Table 7-66](#).

Return to the [Summary Table](#).

Controls Power state of blocks

Table 7-66. DEVICE_CFG_08 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	isns_pd	R/W	0h	Current sense power down. 0h = Current sense active 1h = Current sense is powered down
2	vsns_pd	R/W	0h	Voltage sense power down. 0h = Voltage sense is active 1h = Voltage sense is powered down
1-0	RESERVED	R	0h	Reserved

7.2.12 DEV_PERF_TUNING_11 Register (Offset = 23h) [Reset = 00h]

DEV_PERF_TUNING_11 is shown in [Table 7-67](#).

Return to the [Summary Table](#).

Device performance tuning

Table 7-67. DEV_PERF_TUNING_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	DEV_PERF_TUNING_11	R/W	0h	Device performance tuning. PPC3 software generates the correct configuration required 0h = Device performance tuning. PPC3 software generates the correct configuration required 1h = Device performance tuning. PPC3 software generates the correct configuration required
3-0	RESERVED	R	0h	Reserved

7.2.13 DEVICE_CFG_09 Register (Offset = 29h) [Reset = 64h]

DEVICE_CFG_09 is shown in [Table 7-68](#).

Return to the [Summary Table](#).

This register is to select device internal bias voltage requirements

Table 7-68. DEVICE_CFG_09 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	DEVICE_CFG_1	R/W	3h	Configures internal Bias voltage 0h = Device performance configuration 1h = Reserved 2h = Reserved 3h = Reserved 4h = Reserved 5h = Reserved 6h = Reserved 7h = Reserved
4	VBAT_BIAS_SEL1	R/W	0h	Configures internal Bias voltages based on VBAT pin voltage 0h = based on VBAT_BIAS_SEL2 register 1h = interpolated as VBAT_2S/2
3-2	VBAT_BIAS_SEL2	R/W	1h	Configures internal Bias voltages when VBAT_BIAS_SEL1=0 0h = Reserved 1h = Minimum VBAT pin voltage > 2.9V 2h = Minimum VBAT pin voltage >3.3V 3h = Minimum VBAT pin voltage >3.7V
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.2.14 DEV_PERF_TUNING_04 Register (Offset = 2Bh) [Reset = 00h]

DEV_PERF_TUNING_04 is shown in [Table 7-69](#).

Return to the [Summary Table](#).

Device performance Tuning

Table 7-69. DEV_PERF_TUNING_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	DEV_PERF_TUNING_04	R/W	0h	Device performance tuning. PPC3 software generates the correct configuration required
0	DEV_PERF_TUNING_05	R/W	0h	Device performance tuning. PPC3 software generates the correct configuration required

7.2.15 I2C_CKSUM Register (Offset = 64h) [Reset = 00h]

I2C_CKSUM is shown in [Table 7-70](#).

Return to the [Summary Table](#).

Returns I2C checksum.

Table 7-70. I2C_CKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM	R/W	0h	Returns I2C checksum. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all books and pages.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TAS2573 is a mono channel digital-in class-D amplifier with integrated Boost, I-V sense, battery voltage and temperature monitoring capabilities. The on-chip DSP supports Smart Amp Audio Tuning, Speaker Protection and Advanced Battery Guard algorithms. I²S audio data is supplied by host processor via SDIN data port along with the bit clock and frame sync signals and the device sends echo reference stream back through the SDOUT data port. I²C bus is used for configuration and control.

The device needs external power supply voltages: VBAT - 2.5V to 5.5V, VDD - 1.65V to 1.95V and supports the 1.2V or 1.8V IOVDD rail.

PurePath™ Console 3 (PPC3) software is the recommended tool to configure the device, and PPC3 enables optimization of device and algorithm performance parameters depending on different application scenarios.

8.2 Typical Application

Diagrams below shows the typical application connections for 1S, low voltage 1S battery and 2S Li-Ion battery and for the external PVDD or 3S Battery connection. VBAT_SNS pin connection is optional for 1S mode and if not used, VBAT_SNS pin must be grounded. AD1 and AD2 are used for address detection and can be tied to IOVDD or ground to support up to four I²C target addresses as described in I²C Mode Address selection section ([Section 6.5.2](#)).

System can use same 1.8V supply source to power the IOVDD and VDD if required. The decoupling caps C2 and C3 must still be placed close to the device pins.

VDD signal to supply is critical for device performance and wide trace must be used from the source PMIC to the VDD pin to minimize the parasitic inductance. VDD supply ripple must be kept at minimum and the trace must be connected to common supply plane.

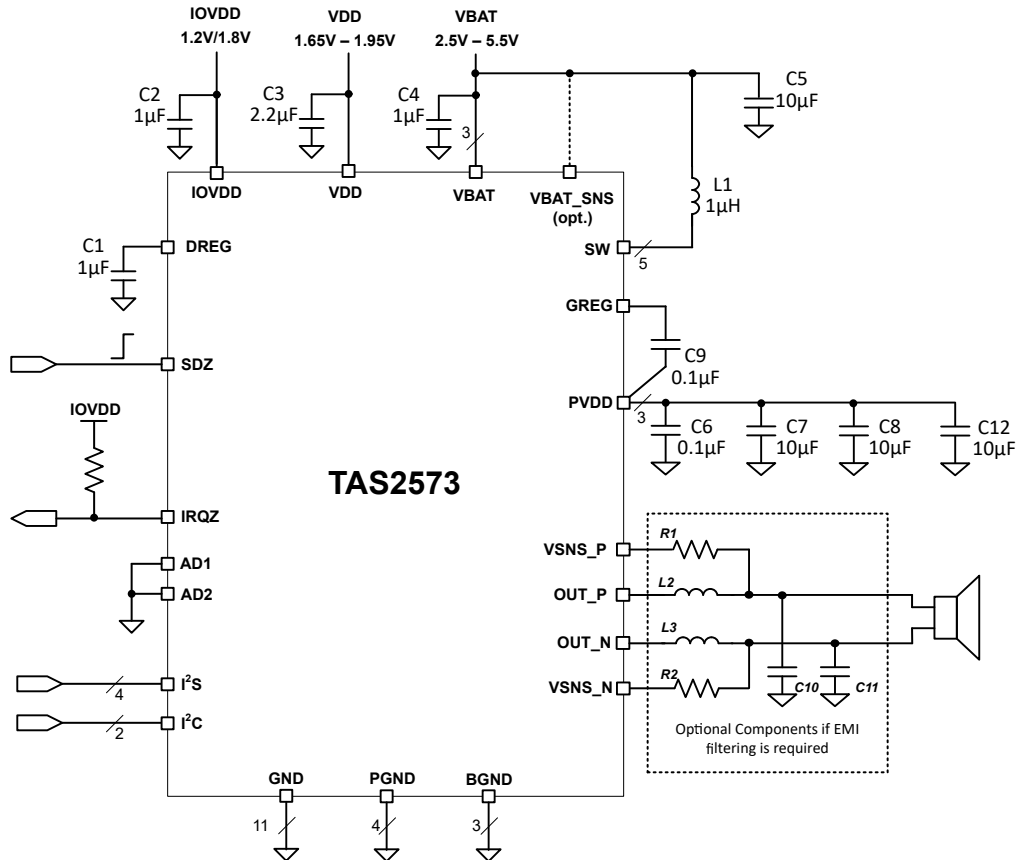


Figure 8-1. Application Diagram for 1S system

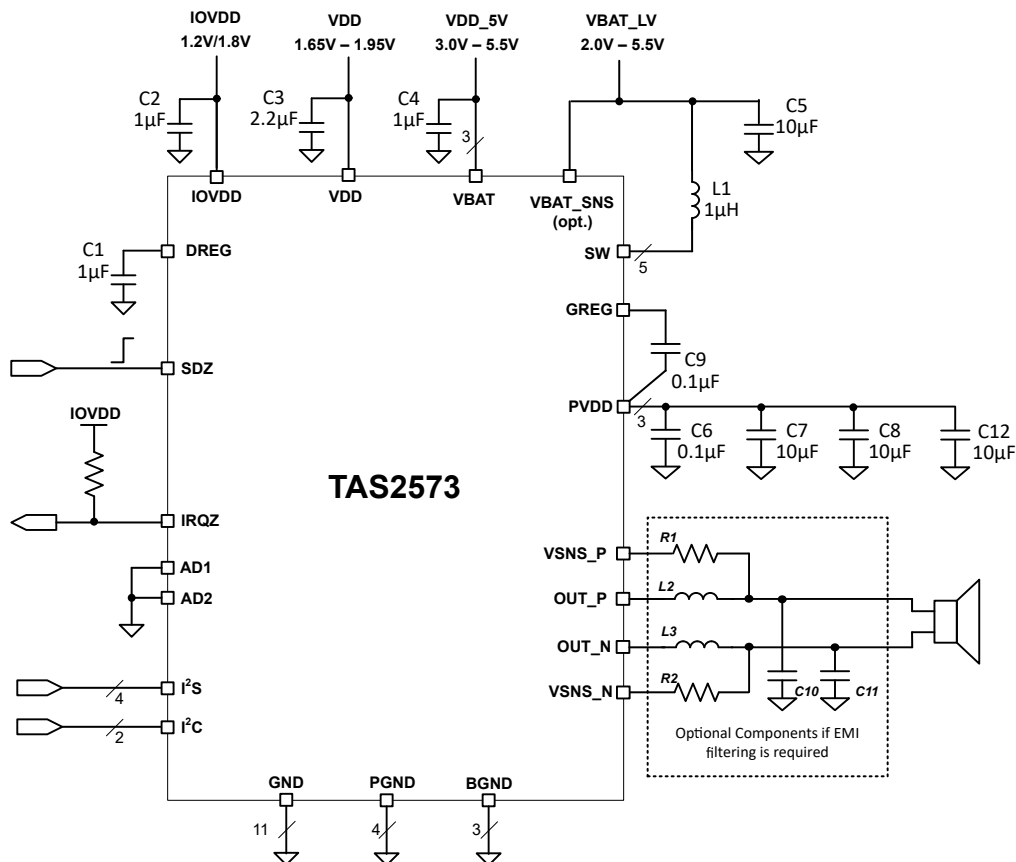


Figure 8-2. Application Diagram for low voltage 1S Battery system

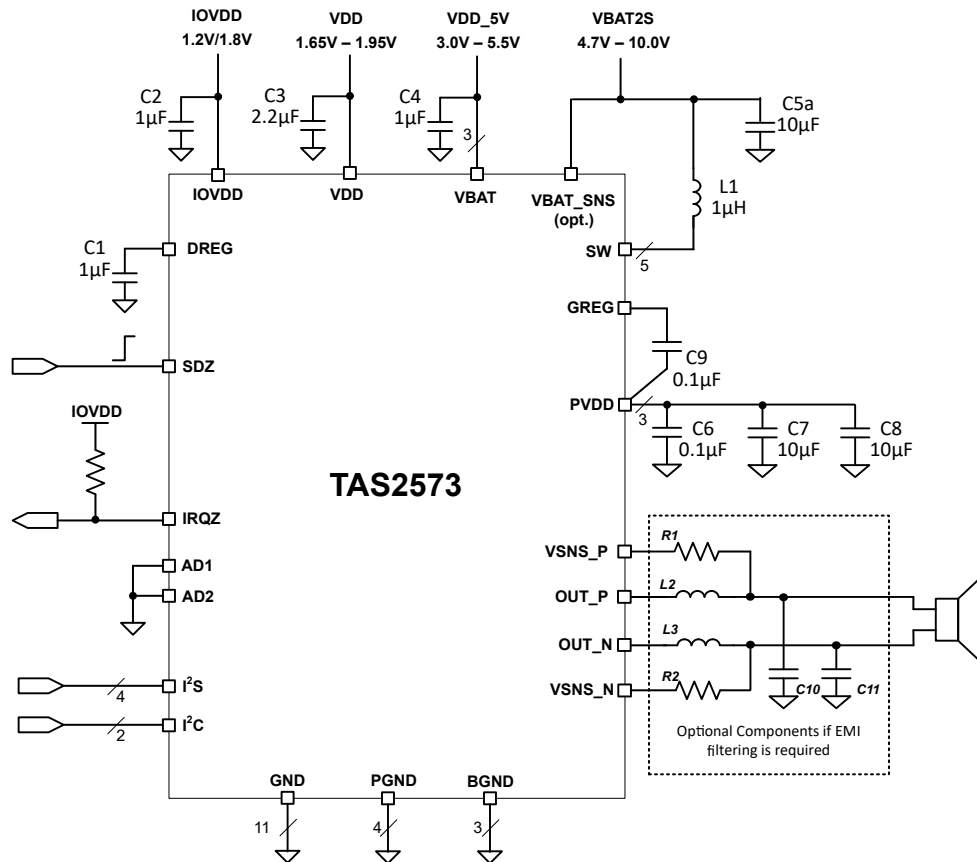


Figure 8-3. Application Diagram for 2S Battery system

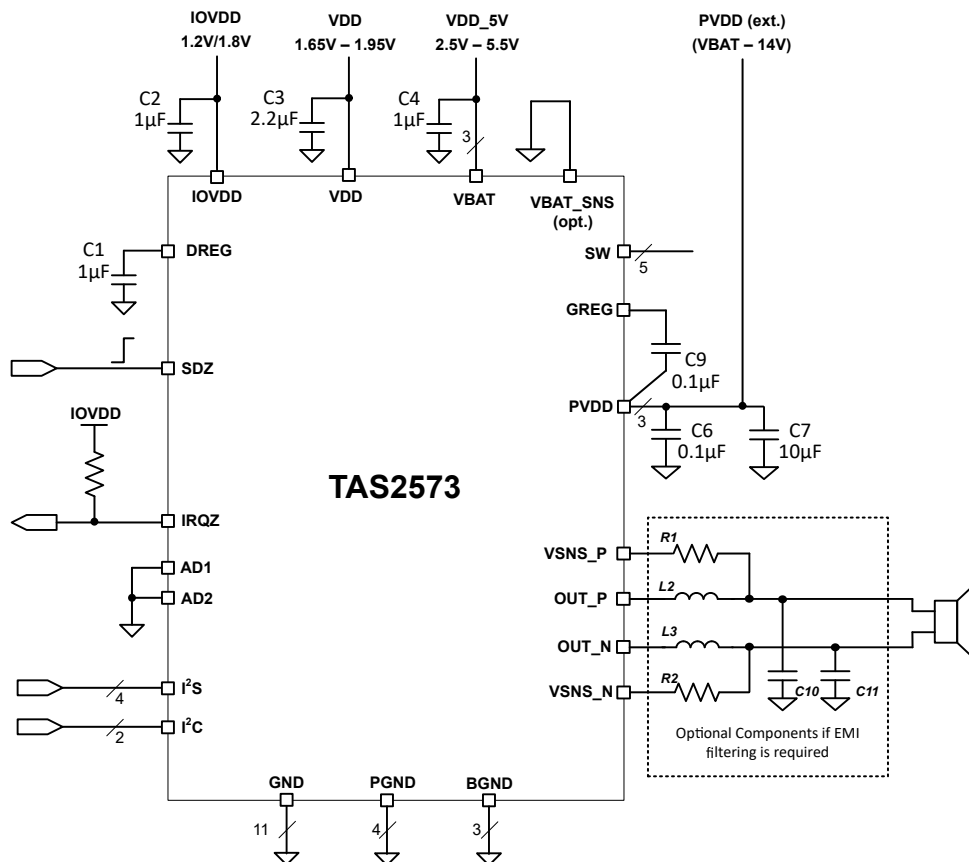


Figure 8-4. Application Diagram for External PVDD or 3S Battery system

Table 8-1. Recommended External Components

Component	Description	Specification	Min	Typ	Max	Unit
L1	Boost Convertor Inductor	Inductance, 20% Tolerance	0.47	1		μH
		Saturation current		5.3		A
L2, L3	Optional EMI Filter Inductors (must use R1, R2 if L2, L3 are used)	DC Current	2			A
C1, C2	DREG, IOVDD decaps	Capacitance, 20% tolerance		1		μF
		Voltage rating	2	6.3		V
C3	VDD decap	Capacitance, 20% tolerance		2.2		μF
		Voltage rating	2	6.3		V
C4	VBAT decap	Capacitance, 20% tolerance		1		μF
		Voltage rating	6.3	10		V
C5	VBAT Power decap	Capacitance, 20% tolerance		10		μF
		Voltage rating	6.3	10		V
C5a	VBAT 2S Power decap	Capacitance, 20% tolerance		10		μF
		Voltage rating	10	16		V
C6	PVDD Low ESL decap	Capacitance, 20% tolerance		0.1		μF
		Voltage rating	16	25		V
C7, C8, C12 ⁽¹⁾	PVDD Power decap	Capacitance, 20% tolerance		10		μF
		Voltage rating	16	25		V
		Effective total PVDD Capacitance at 13V DC after deratings for 1S battery system	3			μF
		Effective total PVDD Capacitance at 13V DC after deratings for 2S battery system <i>Note: C12 is not required for 2S system to meet the derating spec.</i>	2			μF
C9	GREG decap	Capacitance, 20% tolerance		0.1		μF
		Voltage rating	6.3	10		V
C10, C11	Optional EMI Filter capacitors (must use L2, L3 if C10, C11 are used)	Voltage rating	2xPVDD			V
R1, R2	Optional Voltage sense resistors (Must be used if L2, L3 are used)	Resistance, 5% tolerance	1	2.2	4.7	kΩ
		Temp Coefficient			300	ppm/C
		Power		0.01		W

(1) Number of capacitors can be reduced by replacing the 10μF with higher value capacitors which meet the cap derating requirement. For example Two GRM188C61E206ME01 cap meets the spec for 1S battery system and save the board space by reducing one 0603 package size capacitor.

8.2.1 Design Requirements

Table 8-1 lists the BOM components required for the application. Table 8-2 lists other requirements for the application.

Table 8-2. Design Parameters

PARAMETER	CONDITION	SPECIFICATION
VDD supply current ⁽¹⁾	VDD Y-bridge disabled, 48 ksps mode, all blocks enabled	< 15mA
	VDD Y-bridge disabled, 96 ksps mode, all blocks enabled	< 20mA

Table 8-2. Design Parameters (continued)

PARAMETER	CONDITION	SPECIFICATION
IOVDD supply current	1.2V mode	< 1mA
	1.8V mode	< 1mA
VBAT supply current	1S or 2S mode of operation. <i>Note: Current only through device VBAT pin, and not battery current taken through Boost inductor/SW pin.</i>	< 10mA

- (1) When VDD Y-bridge is enabled, additional power taken from VDD supply based on the selected switchover threshold voltage and the output load impedance.

8.2.2 Detailed Design Procedure

8.2.2.1 Mono/Stereo Configuration

In this application, the device is assumed to be operating in mono mode. See [Section 6.5.2](#) for information on changing the I²C address of the TAS2573 to support stereo or multi-channel operation. Mono or stereo configuration does not impact the device performance.

8.2.2.2 Boost Converter Passive Devices

The boost converter requires multiple passive devices that are labeled L1, C7, C8, C12 in [Section 8.2](#) and whose specifications are provided in [Table 8-1](#). These specifications are based on the design of the TAS2573 and are necessary to meet the performance targets of the device. In particular, L1 must not be allowed to enter in the current saturation region. The saturation current (I_{SAT}) for L1 must be $> (I_{LIM} + 5\%)$ to deliver Class-D peak power. I_{SAT} and I_{LIM} values must be selected based on peak output power required in the application.

Additionally, the ratio of L1/C (the derated value of C7,C8,C12) has to be less than 1/3 for boost stability. This ratio is relaxed to 1/2 in 2S battery mode of operation. This ratio must be maintained including the worst case variation of boost inductor and output capacitors.

To satisfy sufficient energy transfer, L1 needs to be $\geq 0.47\mu\text{H}$ at the boost switching frequency (100kHz to 4MHz). Using a $0.47\mu\text{H}$ helps in reducing the capacitor requirements and save board space, but comes at the cost of increased voltage ripple on VBAT and reduces average input current and hence max P_{OUT} of the device. High PSRR of TAS2573 can minimize the effect from the additional ripple on VBAT supply.

The L1 inductor series resistance (ESR) is another critical parameter to be selected in the application. Lower ESR reduces power loss and helps in improving overall system efficiency. Based on available board space, smallest ESR inductors which meet the application needs gives better efficiency performance.

8.2.2.3 EMI Passive Devices

The TAS2573 supports edge-rate control to minimize EMI, but the system designer can want to include passive devices on the Class-D output for further reduction in EMI. These passive devices that are labeled L2, L3, C10 and C11 in [Section 8.2](#). If C10 and C11 are used, L2 and L3 must also be installed, and C10 and C11 must be placed after L2 and L3 respectively to maintain the stability of the output stage. If the EMI filters are used, the additional series resistors R1 and R2 are required to be added in the Vsense (VSNS_P/N) pins.

The component value selection for the EMI filters depends on the application need on the frequency band that needs to be suppressed using these filters. Higher cutoff frequency helps in reducing the BOM size and reduces the switching power loss associated with the filters. Application selects the highest cutoff frequency filter which meets the system's frequency suppression target to get better efficiency performance.

The DC resistance of the inductors or ferrite beads used in the EMI filters also plays a critical role in system efficiency. Lower resistance reduces power loss and helps in improving overall system efficiency. Based on available board space, smallest DC resistance components which meet the application needs gives better efficiency performance.

8.2.2.4 Miscellaneous Passive Devices

The GREG Capacitor requires 100nF to meet boost and Class-D power delivery and efficiency specs. For device functionality, the GREG capacitor must be kelvin/star connected to PVDD pin of the device.

To maintain the device performance and keep the supply ripple within the device specification, minimizing the parasitic inductance on supply/ground paths for decoupling capacitors is required. All supply decapacitors must be selected as smallest package footprint to minimize the ESL of the capacitors. The layout placement and routing of the capacitors is critical for minimizing the trace parasitic inductance. Refer to Layout section ([Section 8.4.1](#)) to get detailed recommendations.

8.2.3 Application Performance Plots

$T_A = 25^\circ\text{C}$, $V_{BAT} = 3.6\text{V}$, $V_{DD} = 1.8\text{V}$, $IOV_{DD} = 1.8\text{V}$, Load = $8\Omega + 33\mu\text{H}$, $L_{BOOST} = 1\mu\text{H}$, $F_{IN} = 1\text{kHz}$, $F_s = 48\text{kHz}$, Gain = 21dBV, $BST_{ILIM} = 5.1\text{A}$, $SDZ = 1$, Noise gate mode disabled, Measured on EVM with

typical application use case (Section 8.2). Measured filter free with an Audio Precision with a 22Hz to 20kHz un-weighted bandwidth, unless otherwise noted.

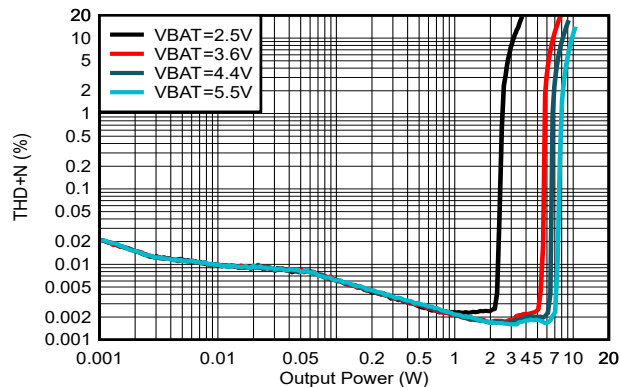


Figure 8-5. THD+N vs Output Power

8.2.4 What to Do and What Not to Do

- If the device is used for Ultrasonic signal generation with no in-band audio signal, and VDD Y-bridge is enabled with time hysteresis of < 50ms, the in-band a-weighted noise can be high and not desirable. It is recommended to keep the Y-bridge hysteresis time at 50ms or higher, or disable the Y-bridge feature to achieve low in-band noise with ultrasonic signal use-cases.
- The device's i2c configuration script should be generated using PPC3 software to ensure that all the device performance tuning registers are configured correctly.

8.3 Power Supply Recommendations

TAS2573 supports supply voltages to ramp up/down in any order of sequence for the externally supplied voltages on VDD, IOVDD, VBAT and PVDD(for external PVDD mode).

SDZ pin must be held low when supplies are not in stable operating condition. Once all the supplies are stable, SDZ pin can be asserted high for device to start operating. SDZ pin must be pulled low before any supply is ramped down below the recommended operating voltage.

If using the device in external PVDD mode, the SW pad must be kept floating.

Once all the supplies are valid and SDZ pin is released to high, the digital core voltage regulator powers up, and starts the internal initialization sequence. After a hardware or software reset, additional i2c commands to the device must be delayed by at-least 300us to allow the device internal blocks to be initialized.

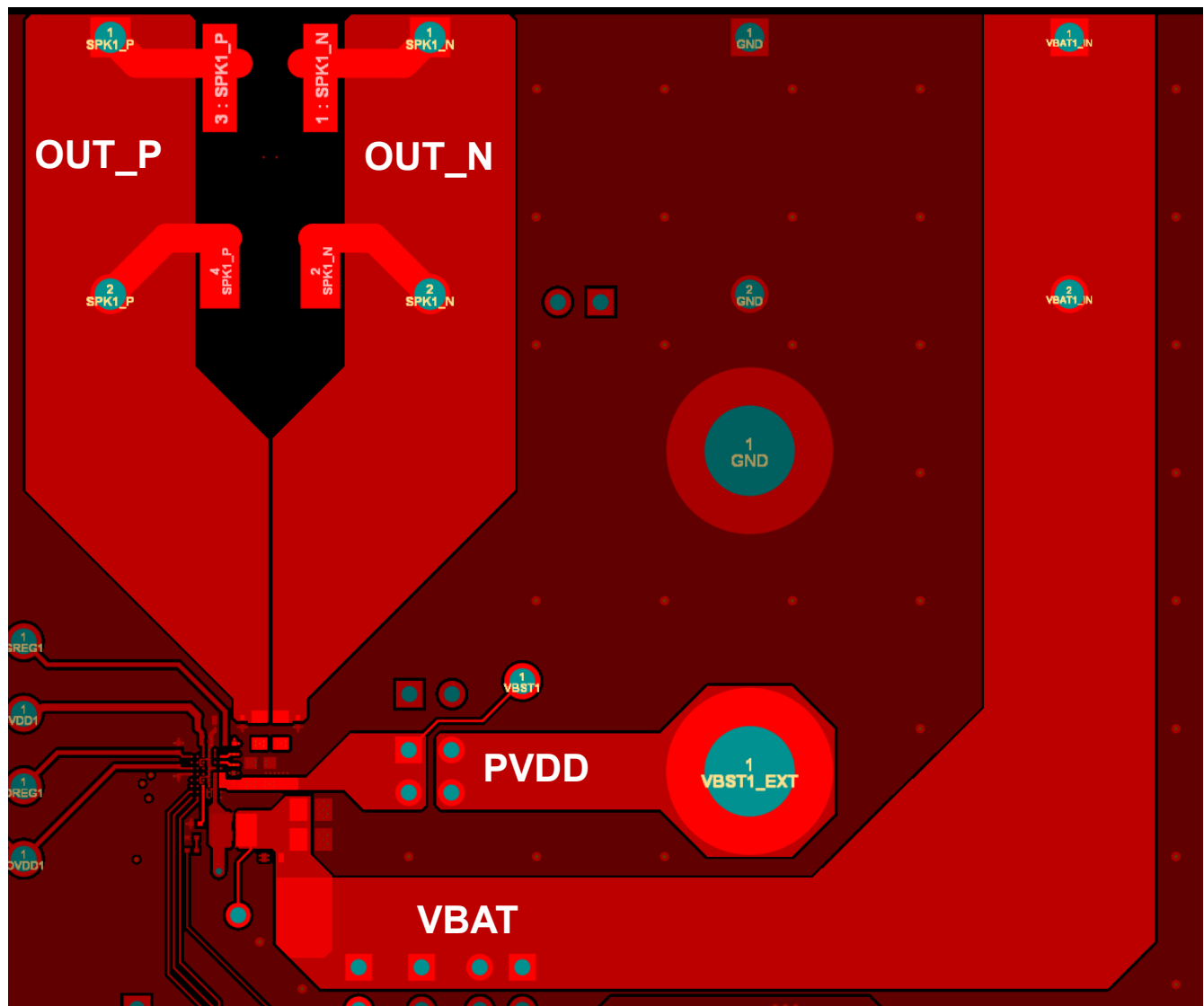
8.4 Layout

8.4.1 Layout Guidelines

- Use wide traces for signals that carry high current and avoid VIAs wherever possible. If VIAs can't be avoided, multiple VIAs must be added to enable low parasitic inductance and high current capability. These include traces for PVDD, VBAT, VDD, PGND, BGND, GND, OUT_P and OUT_N.
- PGND and BGND signals must be directly connected and shorted to the ground plane of board to minimize parasitic inductance. Common inductance between ground pins (for example GND and PGND or GND and BGND common routing) before connecting to ground plane must be avoided.
- The coupling between high switching signal traces like OUT_P, OUT_N, SW, VSNS_P and VSNS_N must be avoided from sensitive low voltage signals.
- Minimize capacitance between high switching lines like OUT_P, OUT_N, SW, VSNS_P and VSNS_N to ground/static nodes. Larger capacitance results in efficiency drop. Coupling between OUT_P and OUT_N also causes degraded efficiency.

- VBAT routing to the boost inductor and the device VBAT pin must be star connected to the common VBAT supply plane. Maintain the decoupling capacitor C4 is placed close to the device and decoupling capacitor C5 is placed close to the inductor.
 - If VBAT_SNS pin is used, connection must be star connected to the supply plane or as close to the battery as possible. Avoid connecting VBAT_SNS pin close to boost inductor VBAT connection.
- Place the boost inductor between VBAT and SW close to the device terminal with no VIAs between device terminal and the inductor. VBAT routing to the boost inductor must be routed with minimal routing resistance to achieve best performance from device.
- Decoupling capacitors must be placed close to the device. Smallest possible package size is recommended for the decaps to achieve best performance from device. DREG, VDD, IOVDD, VBAT (C4 cap), PVDD low ESL (C6 cap) are recommended to be 0201 case size or lower. VIAs between decapitators and device pins must be avoided, or multiple VIAs added to minimize parasitic inductance.
- All decoupling capacitor's ground terminal must be strongly connected to the ground plane with multiple ground VIAs. The ground routing loop between the cap ground and the device ground pins must be minimized.
- For VDD Y-bridge functionality, the routing from the host PMIC to the device VDD must be wide supply plane trace with minimal routing parasitic inductance.
- For the capacitor between GREG-PVDD (C9 cap), PVDD side of capacitor must not be connected directly to the PVDD decoupling capacitors (C6, C7 and C8), and must be connected as close as possible to the device PVDD pin.
- In external PVDD mode of operation, SW pin must be left floating and not connected to any supply or ground signals.

ADVANCE INFORMATION



DATE	REVISION	NOTES
October 2026	*	Initial Release

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documents see the following

- Texas Instruments, [Purepath Console 3 \(PPC3\) Software](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Package Option Addendum

Packaging Information

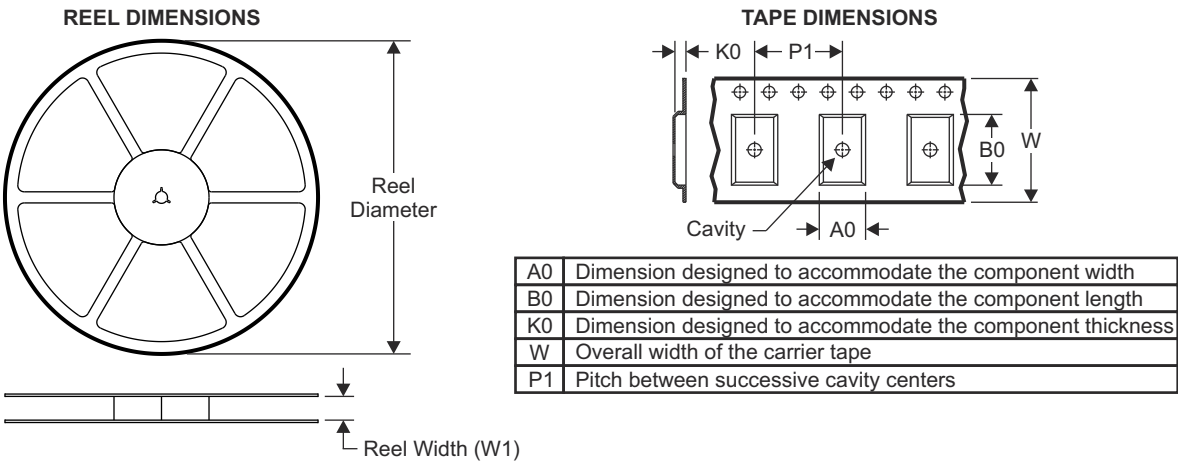
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ⁽⁴⁾⁽⁵⁾
PTAS2573YCFR	ACTIVE	WCSP	YCF	48	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	PRW138

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

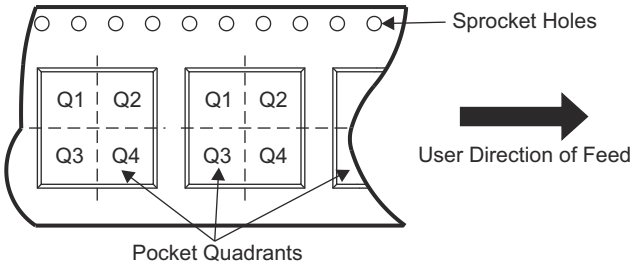
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

11.2 Tape and Reel Information

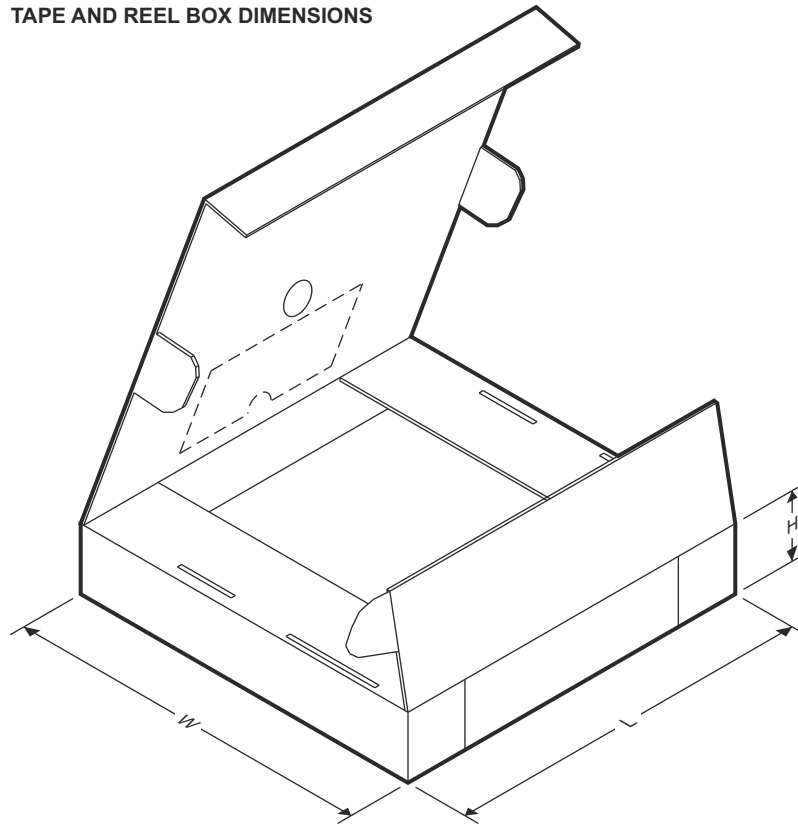


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



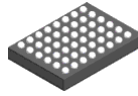
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTAS2573YCFR	WCSP	YCF	48	12000	330	12.4	2.36	3.30	0.60	4	12	Q2

TAPE AND REEL BOX DIMENSIONS



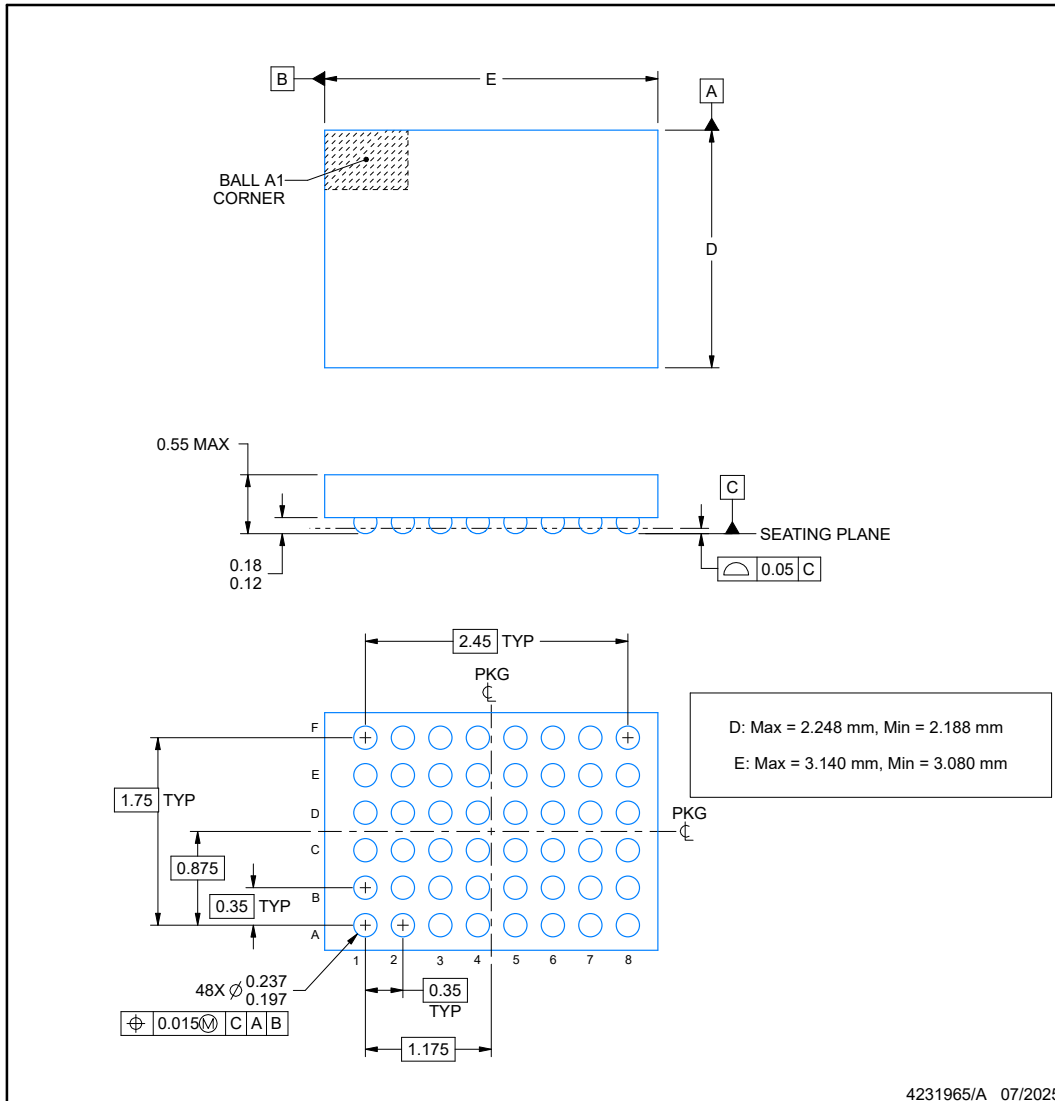
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTAS2573YCFR	WCSP	YCF	48	12000	360	360	36

ADVANCE INFORMATION

**YCF0048-C01****PACKAGE OUTLINE****DSBGA - 0.55 mm max height**

DIE SIZE BALL GRID ARRAY

ADVANCE INFORMATION

**NOTES:**

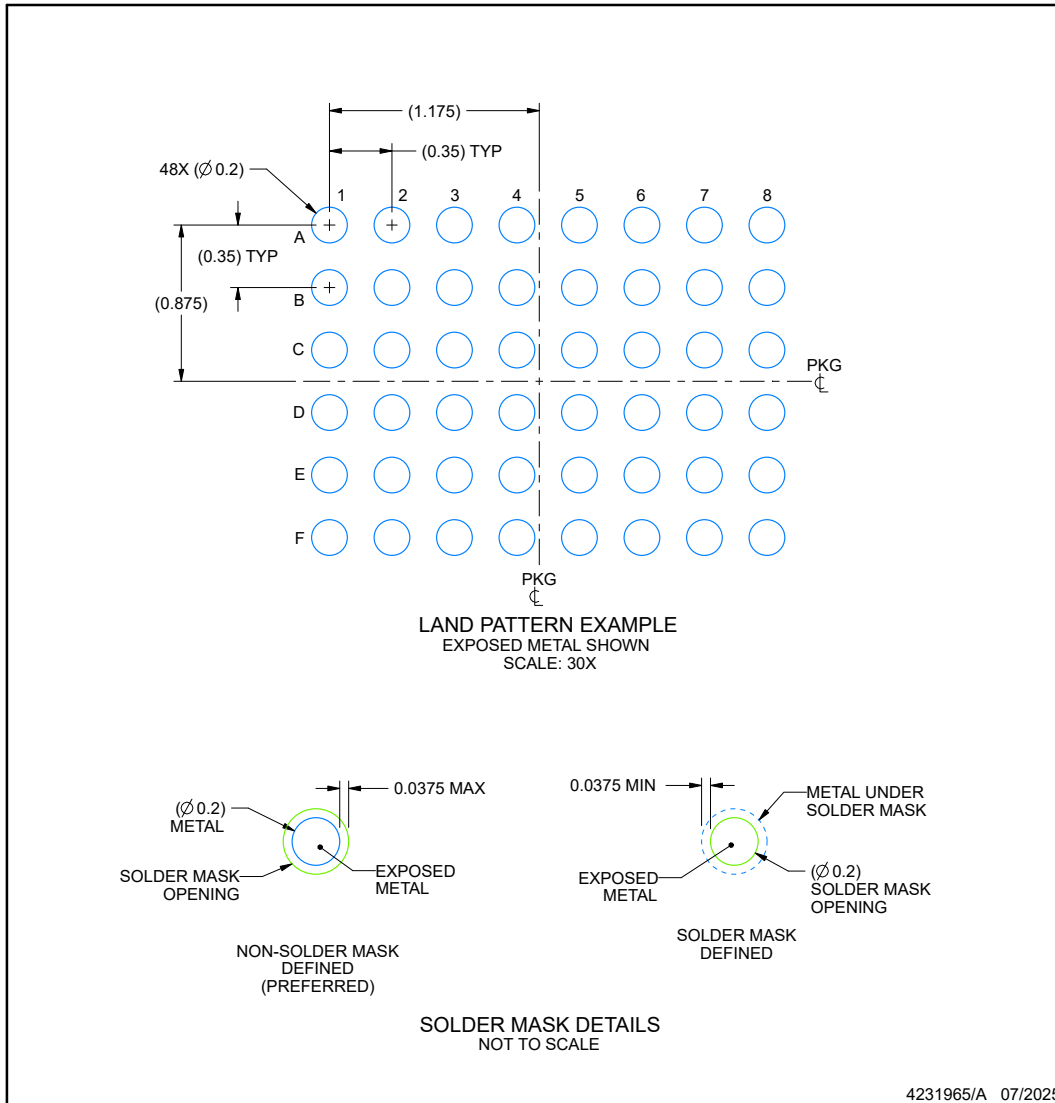
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YCF0048-C01

DSBGA - 0.55 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

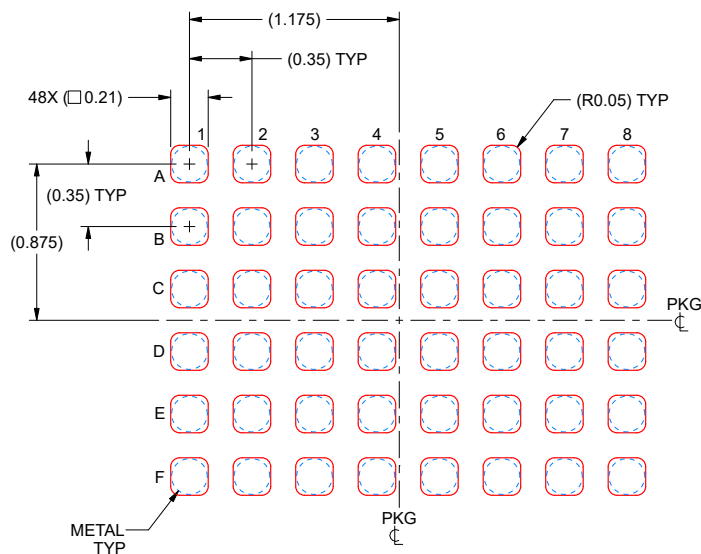
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCF0048-C01

DSBGA - 0.55 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 30X

4231965/A 07/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTAS2573YCFR	Active	Preproduction	DSBGA (YCF) 48	3000 LARGE T&R	-	Call TI	Call TI	-	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025