TCAN29xx-Q1 Automotive, Functional Safety-Compliant CAN FD and LIN System Basis Chip (SBC) Family With Integrated LDOs and Enhanced Diagnostics

ADVANCE INFORMATION

1 Features

- AEC-Q100: Qualified for automotive applications
- Meets the requirements for CAN FD ISO 11898-2:2024
- Meets the CAN FD SIC requirements per ISO 11898-2:2024 Annex A (TCAN295x-Q1)
- Local interconnect network (LIN) physical layer specification ISO/DIS 17987–4:2023 compliant and conforms to SAE J2602 recommended practice for LIN
- CAN FD and LIN transceiver higher data rates
  - CAN FD supports up to 8Mbps
  - LIN transceiver supports fast mode of 200kbps
- Classic CAN backwards compatible
- Functional Safety-Compliant targeted
  - Documentation to aid ISO 26262 system design will be available upon production release
  - Systematic capability up to ASIL B targeted
  - Developed per ISO 26262
  - Analog built-in self test (ABIST) for voltage monitoring circuits
  - Second badgap circuit to cross-monitor the primary bandgap circuit
  - Timeout, window and Q&A watchdog support
  - Undervoltage, overvoltage and short-circuit monitoring on regulator outputs
- Multiple methods to wake from sleep mode
  - CAN and LIN bus wake up pattern (WUP)
  - Local wake up (LWU) via WAKE pins
    - Using a high side switch, cyclic sensing wake up is supported
  - Digital wake up using the SW pin
  - Long duration timer (LDT)
- Low drop out (LDO) regulator supporting 250mA at 3.3V or 5V to power MCUs (VCC1)
- 5V LDO regulator supports up to 100mA (VCC2)
- Control of an external PNP transistor supporting up to 350mA at 1.8V, 2.5V, 3.3V or 5V (VEXCC)
- CAN and LIN support ±40V bus fault protection
- CAN bus fault (short to battery or ground) detection
- QFN (32) package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Infotainment and cluster
- Hybrid, electric and power train systems
- Industrial transportation

3 Description

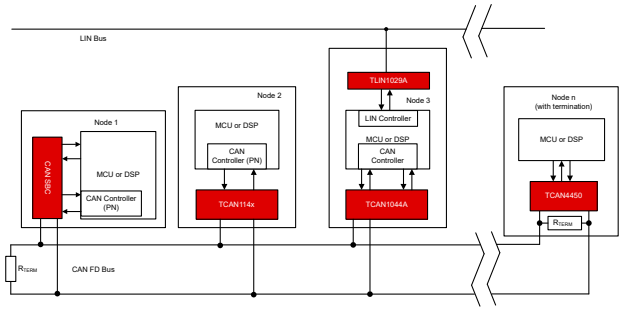
The TCAN29xx-Q1 is a family of system basis chips (SBC) that provide a control area network flexible data rate capable (CAN FD) transceiver. The TCAN2955-Q1 and TCAN2957-Q1 includes a local interconnect network (LIN) transceiver. The CAN FD transceiver supports data rates up to 8Mbps while the LIN transceiver supports fast mode data rates up to 200kbps. The VCC1 LDO provides 3.3V or 5V ±2% with up to 250mA of current and determines the digital IO logic values. If more current is needed an external PNP transistor can be used to support up to 350mA and voltages of 1.8V, 2.5V, 3.3V or 5V. VCC2 LDO provides 5V up to 100mA.

The TCAN29xx-Q1 includes features such as LIMP, upto five local wake inputs (four high-voltage inputs and one digital input) and four high side switches. The high side switch can be on/off, 10-bit PWM or timer controlled. Using the GFO pin it is possible to control an external CAN FD, LIN transceiver, CAN SBC or LIN SBC. The WAKE pins can be configured for static sensing or cyclic sensing . WAKE1 and WAKE2 can be alternatively configured to have an internal switch between the pins to enable external V_{BAT} monitoring. WAKE3 can be configured as a direct drive control pin for any combinations of high-side switches.

Device Information

PART NUMBER(3)	PACKAGE(1)	PACKAGE SIZE(2)
TCAN29xx-Q1	RHB (VQFN, 32)	5mm × 5mm

(1) For more information, see Section 13.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.



Simplified Schematics

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4 Device Comparison Table

Device Number	CAN FD Transceiver	CAN FD SIC Transceiver	LIN Transceiver	3.3V LDO	5V LDO	Functional Safety Rating
TCAN29453MRHBQ1	X			X		QM
TCAN29455MRHBQ1	X				X	QM
TCAN29473MRHBQ1	X		X	X		QM
TCAN29475MRHBQ1	X		X		X	QM
TCAN29453BRHBQ1	X			X		ASIL-B
TCAN29455BRHBQ1	X				X	ASIL-B
TCAN29473BRHBQ1	X		X	X		ASIL-B
TCAN29475BRHBQ1	X		X		X	ASIL-B
TCAN29553MRHBQ1		X		X		QM
TCAN29555MRHBQ1		X			X	QM
TCAN29573MRHBQ1		X	X	X		QM
TCAN29575MRHBQ1		X	X		X	QM
TCAN29553BRHBQ1		X		X		ASIL-B
TCAN29555BRHBQ1		X			X	ASIL-B
TCAN29573BRHBQ1		X	X	X		ASIL-B
TCAN29575BRHBQ1		X	X		X	ASIL-B

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5 Pin Configuration and Functions

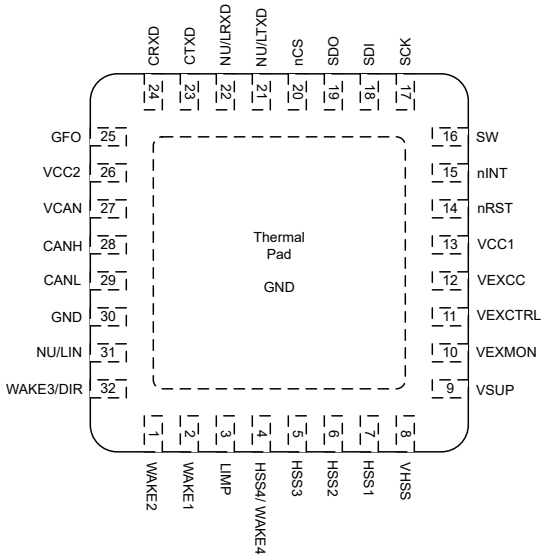

Figure 5-1. RHB Package, 32 Pin (QFN)
Top View

Table 5-1. Pin Functions RHB Package

PIN			TYPE	DESCRIPTION
NO.	TCAN2945 TCAN2955	TCAN2947 TCAN2957		
1	WAKE2	WAKE2	high voltage	Local wake input terminal, high voltage capable
2	WAKE1	WAKE1	high voltage	Local wake input terminal, high voltage capable
3	LIMP	LIMP	high voltage	Limp home output (Active low; open-drain output)
4	HSS4/ WAKE4	HSS4/ WAKE4	high voltage	Can be configured as either High side switch 4 or WAKE4
5	HSS3	HSS3	high voltage	High side switch
6	HSS2	HSS2	high voltage	High side switch
7	HSS1	HSS1	high voltage	High side switch
8	VHSS	VHSS	power	High side switch power
9	VSUP	VSUP	high voltage power	High voltage supply from the battery
10	VEXMON	VEXMON	power	External PNP emitter connection, shunt connection
11	VEXCTRL	VEXCTRL	power	External PNP base control
12	VEXCC	VEXCC	power	External PNP collector connection feedback
13	VCC1	VCC1	power	LDO supply output: 3.3V or 5V
14	nRST	nRST	digital	VCC output monitor pin (active low) and device reset input
15	nINT	nINT	digital	Interrupt output (active low)
16	SW	SW	digital	Programming mode input pin (SPI configurable active high or active low)
17	SCK	SCK	digital	SPI clock input
18	SDI	SDI	digital	SPI data input
19	SDO	SDO	digital	SPI data output
20	nCS	nCS	digital	Chip select input (active low)
21	NU	LTXD	digital	LIN transmit data input (low for dominant and high for recessive bus states) NU is not used and should not be connected to anything
22	NU	LRXD	digital	LIN receive data output (low for dominant and high for recessive bus states) NU is not used and should not be connected to anything
23	CTXD	CTXD	digital	CAN transmit data input (low for dominant and high for recessive bus states)
24	CRXD	CRXD	digital	CAN receive data output (low for dominant and high for recessive bus states)
25	GFO	GFO	digital	Function output pin (SPI configurable)
26	VCC2	VCC2	power	5V LDO output
27	VCAN	VCAN	power	CAN FD transceiver 5V power supply input
28	CANH	CANH	bus I/O	High level CAN bus I/O line

Table 5-1. Pin Functions RHB Package (continued)

PIN			TYPE	DESCRIPTION
NO.	TCAN2945 TCAN2955	TCAN2947 TCAN2957		
29	CANL	CANL	bus I/O	Low level CAN bus I/O line
30	GND	GND	power	Ground connection: Must be soldered to ground
31	NU	LIN	high voltage I/O	LIN bus input/output pin: NU is not used and should not be connected to anything
32	WAKE3/DIR	WAKE3/DIR	high voltage	Local wake input terminal, high voltage capable. Direct drive to control any HSSx when configured
PAD(1)	GND	GND	power	Ground connection: Must be soldered to ground

(1) The thermal pad, PAD, is a device ground pin must be soldered to GND

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6 Specifications

6.1 Absolute Maximum Ratings

Over recommended operating range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VSUP	Supply voltage (2)	–0.3	40	V
VHSS	High-side switches supply voltage (2)	–0.3	40	V
VEXMON	External PNP emitter monitor voltage	V_{SUP}–0.5	40 and $V_O \le V_{SUP}$+0.3	V
VEXCC	External PNP collector feedback voltage(2)	-0.3	40 and $V_O \le V_{SUP}$+0.3	V
VEXCTRL	External PNP base control voltage	–0.3	40 and $V_O \le V_{SUP}$+0.3	V
VCC1	Regulated 3.3 V and 5 V output supply	–0.3	6	V
V_{nRST}	Reset output voltage	-0.3	V_{CC} + 0.3	V
VCAN	CAN transceiver supply voltage	–0.3	6	V
VCC2	5 V output supply(2)	–0.3	6	V
V_{BUSCAN}	CAN bus I/O voltage (CANH, CANL)	–40	40	V
$V_{BUSCAN-DIFF}$	CAN bus maximum differential voltage	-42	42	V
V_{BUSLIN}	LIN bus I/O voltage	–40	40	V
$V_{WAKE1-3}$	WAKE input voltage	–0.3	40	V
V_{WAKE4}	WAKE4 pin input voltage range	–0.3	40 and $V_O \le$ VHSS+0.3	V
V_{HSSx}	High-side switch pin output voltage range	–0.3	40 and $V_O \le$ VHSS+0.3	V
V_{LIMP}	LIMP pin output voltage range	–0.3	40 and $V_O \le V_{SUP}$+0.3	V
V_{LOGIC_IN}	Logic pin input voltage range (SW, SDI, SCK, nCS, nRST, LTXD, CTXD)	–0.3	VCC1+0.3	V
V_{LOGIC_OUT}	Logic pin output voltage range (SDO, nRST, LRXD, CRXD, GFO)	–0.3	VCC1+0.3	V
$I_{O(LOGIC)}$	Logic pin output current (SDO, LRXD, CRXD, GFO)		8	mA
$I_{(WAKE)}$	WAKE pin input current		3	mA
$I_{(LIMP)}$	LIMP pin input current		20	mA
$I_{O(nRST)}$	Reset output current	–5	5	mA
T_J	Junction temperature	–55	165	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Able to support load dumps of up to 40 V for 300ms

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) CANL/H, LIN, per AEC Q100-002[1]		±8000	V
		Human body model (HBM), all other pins, per AEC Q100-002[1]		±2000	
		Charged device model (CDM) Classification Level C5, per AEC Q100-011	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 IEC ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge according to IEC 62228-2 for LIN and IEC 62228-3 for CAN[1]	contact discharge, LIN, CANH, CANL, VSUP[5], VHSS[5], HSSx [6], WAKE [7] and VEXCC	±8000	V
$V_{(ESD)}$	Electrostatic discharge according to IEC 62228-2 for LIN	Indirect ESD, LIN	±15000	V
$V_{(ESD)}$	Electrostatic discharge according to SAE J2962-1 for LIN and J2962-2 for CAN[2]	contact discharge (LIN, CANH, CANL)	±8000	V
		air-gap discharge (CANH, CANL)	±15000	
		air-gap discharge (LIN)	±25000	
ISO7637-2 and IEC 62215-3 Transients, LIN, CANH/L, VSUP, VHSS and WAKE[3]		Pulse 1	-100	V
		Pulse 2	75	
		Pulse 3a	-150	
		Pulse 3b	100	
IS07637-3 Slow Transient Pulse CAN and LIN bus terminals to GND[4]		Direct coupling capacitor "slow transient pulse" with 100 nF coupling capacitor - powered	±30	V

(1) IEC 62228-2 and IEC 62228-3 ESD performed by a third party. Different system-level configurations may lead to different results. See compliance report for circuit configuration.
(2) SAE J2962-1 and SAE J2962-2 testing performed at 3 rd party US3 approved EMC test facility.
(3) ISO 7637-2 according to IEC 62228-2 and IEC 62228-3 are system-level transient tests. Different system-level configurations may lead to different results. See compliance report for circuit configuration.
(4) ISO 7637-3 is a system-level transient test. Different system-level configurations may lead to different results.
(5) VSUP and VHSS are connected together on board and not tested separately
(6) HSSx pins have capacitor connected per the recommendation in the application diagram
(7) WAKEx pins are protected with the recommended series resistance and capacitor at the pins per the application diagram

6.4 Recommended Operating Conditions

Over recommended operating range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VSUP	Supply voltage [1] [2]	5.5		28	V
VHSS	High-side switches supply voltage	5		28	V
VCAN	CAN Transceiver supply voltage	4.75	5	5.25	V
V_{CM_CAN}	CAN bus common mode voltage range	-12		12	V
V_{LIN}	LIN bus input voltage	0		28	V
$I_{OH(DO)}$	Digital output high level current	–2			mA
$I_{OL(DO)}$	Digital output low level current			2	mA
$I_{O(LIMP)}$	LIMP pin current when configured as LIMP			6	mA
$I_{O(HSSx)}$	High side switch pin current		60	100	mA
$C_{(VHSS)}$	VHSS supply pin capacitance	100			nF
$C_{(VSUP)}$	V_{SUP} supply pin capacitance	100			nF
$C_{(VEXCC)}$	VEXCC supply capacitance;	4.7			µF

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6.4 Recommended Operating Conditions (continued)

Over recommended operating range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
ESR_C	VEXCC ESR capacitance requirements	1		150	mΩ
$C_{(VCC1/2)}$	VCC1 and VCC2 effective supply capacitance required for LDO stability; no load to full load	1			µF
ESR_{CO}	VCC1 and VCC2 output ESR capacitance requirements	0.001		1	Ω
TSDWR	Thermal shut down warning	145		165	°C
TSDWF	Thermal shut down warning release	130		150	°C
TSDWHYS	Thermal shut down warning hysteresis		15		°C
TSDR	Thermal shut down	165		200	°C
TSDF	Thermal shut down release	155		190	°C
TSDHYS	Thermal shut down hysteresis		10.0		°C
T_J	Operating junction temperature range	–40		150	°C

(1) When VCC1 is 3.3 V output, VCC1 will work with a VSUP of 4.5 V but other LDOs will be in pass thru mode and output voltage will not be at regulated value. For all LDOs to be in regulation VSUP needs to be at or above 5.5 V.
(2) When VCC1 is 3.3 V output and VSUP is above 4.5V, the LIN transceiver will function but may not meet the electrical or timing parameters.

6.5 Thermal Information

THERMAL METRIC(1)		RHB (QFN) 32-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Supply Characteristics

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Battery Supply Input (VSUP)						
$ISUP_{norm}$	Battery supply current device in SBC normal mode	SBC in Normal mode, No load on VCC1, VCC2 ON with no load, VEXCC = off, CAN and LIN transceivers off, all HSS are off, wake pins are disabled		1	2	mA
$ISUP_{stby-85c}$	Battery supply current, low power standby mode	Standby mode; VEXCC, VCC2 = off and VCC1 = On with no load; 6.5V ≤ VSUP ≤ 18V; CAN and LIN transceivers are off; All HSS and WAKE pins are off, Watchdog is off; Long Window has expired, -40°C ≤ T_J ≤ 85°C,			70	µA
$ISUP_{slp-85c}$	Battery supply current, sleep mode; LDO's and transceivers off	Sleep mode;VEXCC, VCC1 and VCC2 = off; 6.5V ≤ VSUP ≤ 18V; transceivers are off; All HSSx are off; one WAKE pin enabled and grounded or floating; -40°C ≤ T_J ≤ 85°C		20	35	µA

6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VSUP_{(PU)R}$	Supply on detection	VSUP rising; see Figure 7-17	2.9	3.4	3.7	V
$VSUP_{(PU)F}$	Supply off detection	VSUP falling; see Figure 10-2 and Figure 10-3	2.6	2.9	3.2	V
$VSUP_{(PU)HYS}$	Supply off detection hysteresis		300	430	800	mV
$UVSUP_{5R}$	Supply undervoltage recovery	VSUP rising; see Figure 7-17, Figure 10-2 and Figure 10-3	4.9		5.5	V
$UVSUP_{5F}$	Supply undervoltage detection	VSUP falling; see Figure 10-2 and Figure 10-3	4.5		5.1	V
$UVSUP_{5HYS}$	Supply undervoltage detection hysteresis		200		600	mV
$UVSUP_{33R}$	Supply undervoltage recovery	VSUP rising; see Figure 7-17, Figure 10-2 and Figure 10-3	3.7		4.4	V
$UVSUP_{33F}$	Supply undervoltage detection	VSUP falling; see Figure 10-2 and Figure 10-3	3.55		4.25	V
$UVSUP_{33HYS}$	Supply undervoltage detection hysteresis		50		300	mV
Current Consumption for additional features when enabled						
$ISUP_{VCC2-85C}$	Additional supply current when VCC2 LDO is enabled	Sleep or Standby mode; additional current when VCC2 is enabled and no load. VSUP = 6.5 V to 12 V; T_J : - 40 ℃ to 85 ℃		25	35	µA
$ISUP_{VCC2-150C}$	Additional supply current when VCC2 LDO is enabled	Sleep or Standby mode; additional current when VCC2 is enabled and no load. VSUP = 6.5 V to 28 V; T_J : - 40 ℃ to 150 ℃		25	40	µA
$ISUP_{HSSNOLOAD-LP}$	Incremental battery supply current for each HSS in low power mode.	For each HSSx turned ON (low power mode of HSS; HSSx_LP_EN =1b) but no load, $T_J \leq 85℃$		5	8	µA
$ISUP_{HSSNOLOAD}$	Incremental battery supply current for each HSS.	For each HSSx turned ON but no load, $T_J \leq 85℃$		25	35	µA
$ISUP_{WD}$	Incremental battery supply current when watchdog is enabled for Window or Q&A	Standby mode; VEXCC, VCC2 = off and VCC1 = On with no load; VSUP 14 V; CAN and LIN transceivers are wake capable and buses - recessive; All HSS and WAKE pins are off, Watchdog is enabled (Window, Q&A), $T_J \leq 85℃$		45	55	µA
$ISUP_{WDTO}$	Incremental battery supply current when Timeout watchdog is enabled.	Standby mode; VEXCC, VCC2 = off and VCC1 = On with no load; VSUP 14 V; CAN and LIN transceivers are wake capable and buses - recessive; All HSS and WAKE pins are off, Watchdog is enabled (Timeout), $T_J \leq 85℃$		2	2.5	µA
$ISUP_{CANBIAS}$	Additional current consumption when CAN outputs are in automatic bias (before tSILENCE expires)	Sleep or Standby mode before $t_{SILENCE}$ expires. VSUP =14V; $T_J \leq 85℃$		55	65	µA
$ISUP_{wake}$	Incremental battery supply current for each WAKEx pin when enabled	WAKEx pin enabled, VSUP=14V, $T_J \leq 85℃$		1	2	µA
$ISUP_{CS-WK}$	Incremental battery current when cyclic sensing wake is enabled in Sleep mode	Sleep mode; cyclic sensing wake enabled, VSUP=14V, $T_J \leq 85℃$, TIMERx with ON width = 1ms, period = 100ms		5	8	µA

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6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ISUP_{stdbyswodr}$	Battery supply current in sleep mode due to HSSx direct drive	Standby mode; VEXCC and VCC2 = off; VCC1 = On with no load; 6.5 V ≤ VSUP ≤ 18 V; CAN and LIN transceivers are wake capable; One HSSx turned on for 120 µs every 50 ms by WAKE3/DIR pin; All other HSSx and WAKEx are off; -40°C ≤ T_J ≤ 85°C(2)		60	75	µA
$ISUP_{stdbywodr}$	Battery supply current, sleep mode with HSS4 direct drive	Standby mode; VEXCC and VCC2 = off; VCC1 = On with no load; 6.5 V ≤ VSUP ≤ 18 V; CAN and LIN transceivers are wake capable; One HSSx turned on for 120 µs every 50 ms by WAKE3/DIR pin; All other HSSx and WAKEx are off; T_J ≤ 25°C(2)		50	60	µA
$IEXCC_{slp}$	Incremental battery supply current draw when VEXCC is enabled	Sleep or Standby mode; VEXCC enabled in stand-alone configuration and no load. Includes current into VEXMON and VEXCTRL pins			55	µA
VHSS						
$IVHSS_{SLP}$	High-side switch supply (VHSS) current consumption in Sleep mode	Sleep Mode; cyclic sensing wake = off; -40°C ≤ T_J ≤ 85°C		1	2	µA
$IHSS_{NOLOAD\_LP}$	Additional current draw for each HSS turned ON with HSS configured for low-power mode	For each HSS turned ON, No load on HSS output.		10	15	µA
$IHSS_{NOLOAD}$	Additional current draw for each HSS turned ON	For each HSS turned ON, No load on HSS output.		20	30	µA
$UVHSS_R$	High-side switches supply undervoltage recovery	VHSS rising	4.6		4.9	V
$UVHSS_F$	High-side switches supply undervoltage detection; High-side switches turn-off if HSS_UV_DIS = 0b	VHSS falling	4.4		4.7	V
$UVHSS_{HYS}$	High-side switches supply undervoltage detection hysteresis		100			mV
$OVHSS_R$	VHSS over-voltage rising threshold; High-side switches turn-off if HSS_OV_DIS = 0b	VHSS rising	20		22	V
$OVHSS_F$	VHSS over-voltage falling threshold; VHSS must be below thhis threshold to enable the high-side switches again	VHSS falling	18.8		21.2	V
$OVHSS_{HYS}$	VHSS over-voltage threshold hysteresis		800		1200	mV
VCC1 Regulator						
$VCC1_5$	Regulated output	VSUP = 5.5 V to 28 V, ICC1 = 1 to 250 mA	4.9	5	5.1	V
$VCC1_{33}$	Regulated output	VSUP = 5.5 V to 28 V, ICC1 = 1 to 250 mA	3.234	3.3	3.366	V
$ICC1_{SINK}$	VCC1 current sink capability	VSUP = 14 V and register 8'h0D[3] = 0b	–17	–11	–7	µA
		VSUP = 14 V and register 8'h0D[3] = 1b	–155	–112	–75	µA
$ICC1_{LIM-DET}$	VCC1 output current limit detection threshold	VSUP 5.5V to 28V	250		475	mA
$ICC1_{LIM}$	VCC1 output current limit	VCC1 short to ground	300		500	mA
$UVCC1_{5RPR}$	VCC1 undervoltage recovery threshold pre-warning	VCC1 rising	4.65		4.9	V

6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$UVCC1_{5FPR}$	VCC1 undervoltage detection threshold pre-warning	VCC1 falling	4.55		4.8	V
$UVCC1_{5PRHYS}$	Undervoltage pre-warning 5 V LDO hysteresis		70		130	mV
$UVCC1_{5R1}$	VCC1 undervoltage recovery threshold 1	VCC1 rising, Register 8'h0E[4:3] = 00b	4.60		4.85	V
$UVCC1_{5F1}$	VCC1 undervoltage detection threshold 1	VCC1 falling, Register 8'h0E[4:3] = 00b	4.50		4.75	V
$UVCC1_{5R2}$	VCC1 undervoltage recovery threshold 2	VCC1 rising, Register 8'h0E[4:3] = 01b	3.85		4.15	V
$UVCC1_{5F2}$	VCC1 undervoltage detection threshold 2	VCC1 falling, Register 8'h0E[4:3] = 01b	3.75		4.05	V
$UVCC1_{5R3}$	VCC1 undervoltage recovery threshold 3	VCC1 rising, Register 8'h0E[4:3] = 10b	3.25		3.55	V
$UVCC1_{5F3}$	VCC1 undervoltage detection threshold 3	VCC1 falling, Register 8'h0E[4:3] = 10b	3.15		3.45	V
$UVCC1_{5R4}$	VCC1 undervoltage recovery threshold 4	VCC1 rising, Register 8'h0E[4:3] = 11b	4.6		4.85	V
$UVCC1_{5F4}$	VCC1 undervoltage detection threshold 4	VCC1 falling, Register 8'h0E[4:3] = 11b	3.375		3.675	V
$UVCC1_{5HYS4}$	Undervoltage detection 5 V LDO hysteresis	Register 8'h0E[4:3] = 11b		1200		mV
$UVCC1_{5HYS}$	Undervoltage detection 5 V LDO hysteresis	Register 8'h0E[4:3] = 00b, 01b or 10b	50		150	mV
$UVCC1_{33RPR}$	VCC1 undervoltage recovery threshold pre-warning	VCC1 rising	3.1		3.28	V
$UVCC1_{33FPR}$	VCC1 undervoltage detection threshold pre-warning	VCC1 falling	3		3.2	V
$UVCC1_{33PRHYS}$	Undervoltage pre-warning 3.3 V LDO hysteresis		60		120	mV
$UVCC1_{33R1}$	VCC1 undervoltage recovery threshold 1	VCC1 rising, Register 8'h0E[4:3] = 00b	3		3.2	V
$UVCC1_{33F1}$	VCC1 undervoltage detection threshold 1	VCC1 falling, Register 8'h0E[4:3] = 00b	2.95		3.15	V
$UVCC1_{33R2}$	VCC1 undervoltage recovery threshold 2	VCC1 rising, Register 8'h0E[4:3] = 01b	2.55		2.75	V
$UVCC1_{33F2}$	VCC1 undervoltage detection threshold 2	VCC1 falling, Register 8'h0E[4:3] = 01b	2.5		2.7	V
$UVCC1_{33R3}$	VCC1 undervoltage recovery threshold 3	VCC1 rising, Register 8'h0E[4:3] = 10b	2.25		2.45	V
$UVCC1_{33F3}$	VCC1 undervoltage detection threshold 3	VCC1 falling, Register 8'h0E[4:3] = 10b	2.2		2.4	V
$UVCC1_{33R4}$	VCC1 undervoltage recovery threshold 4	VCC1 rising, Register 8'h0E[4:3] = 11b	3		3.2	V
$UVCC1_{33F4}$	VCC1 undervoltage detection threshold 4	VCC1 falling, Register 8'h0E[4:3] = 11b	2.2		2.4	V
$UVCC1_{33HYS4}$	Undervoltage detection 3.3 V LDO hysteresis	Register 8'h0E[4:3] = 11b		800		mV
$UVCC1_{33HYS}$	Undervoltage detection 3.3 V LDO hysteresis	Register 8'h0E[4:3] = 00b, 01b or 10b	30		70	mV
$OVCC1_{5R1}$	Over voltage 5 V VCC threshold to enter sleep mode or fail-safe mode	Ramp Up, Register 8'h0C[7] = 0b	5.25		5.5	V

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6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$OVCC1_{5F1}$	Over voltage 5 V VCC1 threshold	Ramp Down, Register 8'h0C[7] = 0b	5.15		5.4	V
$OVCC1_{5R2}$	Over voltage 5 V VCC1 threshold to enter sleep mode or fail-safe mode	Ramp Up, Register 8'h0C[7] = 1b	5.5		5.7	V
$OVCC1_{5F2}$	Over voltage 5 V VCC1 threshold	Ramp Down, Register 8'h0C[7] = 1b	5.4		5.6	V
$OVCC1_{5HYS}$	Over voltage 5 V VCC threshold hysteresis		50		150	mV
$OVCC1_{33R1}$	Over voltage 3.3 V VCC1 threshold to enter sleep mode or fail-safe mode	Ramp up, Register 8'h0C[7] = 0b	3.45		3.6	V
$OVCC1_{33F1}$	Over voltage 3.3 V VCC1 threshold	Ramp down, Register 8'h0C[7] = 0b	3.4		3.55	V
$OVCC1_{33R2}$	Over voltage 3.3 V VCC1 threshold	Ramp Up, Register 8'h0C[7] = 1b	3.6		3.8	V
$OVCC1_{33F2}$	Over voltage 3.3 V VCC1 threshold to enter sleep mode or fail-safe mode	Ramp Down, Register 8'h0C[7] = 1b	3.5		3.7	V
$OVCC1_{33HYS1}$	Over voltage 3.3 V VCC threshold hysteresis	OVCC1_SEL Register 8'h0C[7] = 0b	30	55	70	mV
$OVCC1_{33HYS2}$	Over voltage 3.3 V VCC threshold hysteresis	OVCC1_SEL Register 8'h0C[7] = 1b	70	105	140	mV
$VCC1_{5SC}$	VCC1 short circuit threshold to enter sleep mode or fail-safe mode for 5 V LDO	VSUP ≥ $VSUP_{(PU)}$	1.7		2.3	V
$VCC1_{33SC}$	VCC1 short circuit threshold to enter sleep mode or fail-safe mode for 3.3 V LDO	VSUP ≥ $VSUP_{(PU)}$		1.22	1.26	V
$V_{5DROP1-VCC1}$	Dropout voltage (VCC1=5V Configuration)	VSUP = 3.5 V, ICC1 = 50 mA			500	mV
$V_{5DROP2-VCC1}$	Dropout voltage (VCC1=5V Configuration)	VSUP = 5 V, ICC1 = 150 mA			500	mV
$V_{33DROP1-VCC1}$	Dropout voltage (VCC1=3.3V Configuration)	VSUP = 3.5 V, ICC1 = 50 mA			500	mV
VCC2 Regulator						
VCC2nom	Normal operation regulated output	VSUP = 6V to 28V, ICC2 = 0 to 100 mA	4.9	5	5.1	V
VCC2red	Reduced operation regulated output	VSUP = 8V - 18V; ICC2 = 10µA - 5mA; Tj = -40°C - 125°C	4.95	5	5.05	V
$ICC2_{LIM-DET}$	VCC2 output current limit detection threshold	VSUP 5.5V to 28V,	125		250	mA
$ICC2_{LIM}$	VCC2 output current limit	VCC2 = 2.5V	150		250	mA
$UVCC2_{R}$	Undervoltage recovery VCC2	VCC2 rising	4.6		4.9	V
$UVCC2_{F}$	Undervoltage detection VCC2	VCC2 falling	4.5		4.75	V
$UVCC2_{HYS}$	Undervoltage detection VCC2 hysteresis		70		175	mV
$OVCC2_{R}$	Over voltage VCC2 LDO threshold	Ramp Up	5.4		5.6	V
$OVCC2_{F}$	Over voltage VCC2 LDO threshold	Ramp Down	5.2		5.5	V
$OVCC2_{HYS}$	Over voltage VCC2 LDO threshold hysteresis		70		175	mV
$VCC2_{SC}$	VCC2 LDO short circuit threshold	VSUP ≥ $VSUP_{(PU)}$	1.7		2.3	V
$V_{5DROP1-VCC2}$	Dropout voltage (5 V LDO output, VCC2)	VSUP = 3.5 V, ICC2 = 50 mA			500	mV
$V_{5DROP2-VCC2}$	Dropout voltage (5 V LDO output VCC2)	VSUP = 5 V, ICC2 = 30 mA			500	mV
VEXCC Regulator						

6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$VEXCC_{18}$	1.8 V PNP output voltage supported	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I_{VCCEXT} ≤ 350 mA	1.764	1.8	1.836	V
$VEXCC_{25}$	2.5 V PNP output voltage supported	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I_{VCCEXT} ≤ 350 mA	2.45	2.5	2.55	V
$VEXCC_{33}$	3.3 V PNP output voltage supported	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I_{VCCEXT} ≤ 350 mA	3.234	3.3	3.366	V
$VEXCC_{5}$	5 V PNP output voltages supported	5.5 V ≤ VSUP ≤ 28 V 10 mA ≤ I_{VCCEXT} ≤ 350 mA	4.9	5	5.1	V
$UVEXCC_R$	VEXCC exiting undervoltage event	5.5 V ≤ VSUP ≤ 28 V	0.87	0.9	0.93	V_{EXCC}
$UVEXCC_F$	VEXCC entering undervoltage event	5.5 V ≤ VSUP ≤ 28 V	0.81	0.85	0.89	V_{EXCC}
$UVEXCC_{HSY}$	VEXCC entering undervoltage hysteresis	5.5 V ≤ VSUP ≤ 28 V	30		350	mV
$OVEXCC_R$	VEXCC entering overvoltage event	5.5 V ≤ VSUP ≤ 28 V	1.12	1.15	1.18	V_{EXCC}
$OVEXCC_F$	VEXCC exiting overvoltage event	5.5 V ≤ VSUP ≤ 28 V	1.07	1.1	1.13	V_{EXCC}
$OVEXCC_{HYS}$	VEXCC exiting overvoltage hysteresis	5.5 V ≤ VSUP ≤ 28 V	45		300	mV
$VEXCC_{SC18}$	VEXCC short circuit detect for 1.8 V and 2.5 V	5.5 V ≤ V_{SUP} ≤ 28 V		1.1	1.26	V
$VEXCC_{SC}$	VEXCC short circuit detect for 3.3 V and 5 V	5.5 V ≤ VSUP ≤ 28 V	1.7		2.3	V
IVEXCC	Input current on VEXCC	VEXCC = 5 V, 3.3 V, 2.5 V and 1.8 V	0	0.5	3	µA
VVEXCTRL	Voltage output on base pin of external PNP	5.5 V ≤ VSUP ≤ 28 V			28	V
IVEXCTRL	Drive current at the base pin of external PNP	VVEXCTRL = 13.5 V	12	40	70	mA
$IVEXCTRL_{LKG}$	Current on base pin VEXCTRL leakage	VVEXCTRL = 13.5; T_j = 25°C			5	µA
IVEXMON	VEXMON pin input current	VEXMON = VSUP	0	4	8	µA
$IVEXMON_{LKG}$	VEXMON pin input leakage current ext PNP disabled	VEXMON = VSUP; T_j = 25°C			5	µA
VSHUNTTH	Output current shunt voltage threshold (1)		0.15	0.2	0.25	V
$t_{RLINC-3P3V}$	Current increase regulation reaction time	VEXCC = 3.3 V to 0 V, Max IVEXCTRL = 20 mA, VEXMON=VSUP See Figure 8-3			20	µs
$t_{RLDEC-3P3V}$	Current decrease regulation reaction time	VEXCC = 0 V to 3.3 V, Max IVEXCTRL = 20 mA, VEXMON=VSUP, See Figure 8-3			5	µs
$t_{RLINC-5V}$	Current increase regulation reaction time	VEXCC = 5 V to 0 V; Max IVEXCTRL = 20 mA, VEXMON=VSUP, See Figure 8-3			20	µs
$t_{RLDEC-5V}$	Current decrease regulation reaction time	VEXCC = 0 V to 5 V; Max IVEXCTRL = 20 mA, VEXMON=VSUP, See Figure 8-3			5	µs
$Ratio_{ICC3/ICC1-5}$	Load sharing ratio 5 (ICC3:ICC1)	6.0V <= V_{SUP} <= 28V; SBC Normal Mode; LS ratio setting 0x1F[3:1]=101b R_{shunt} = 0.25Ω Total load current = 500mA VCC1, VEXCC in regulation (No UV or OC interrupts set during the test)		3.2		

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6.6 Supply Characteristics (continued)

Over recommended operating range (unless otherwise noted). Typical values are specified at VSUP = 14V and T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Ratio_{ICC3/ICC1-5}$	Load sharing ratio 5 (ICC3:ICC1)	6.0V <= V_{SUP} <= 28V; SBC Normal Mode; LS ratio setting 0x1F[3:1]=101b $_{shunt}$ = 0.25Ω Total load current = 300mA VCC1, VEXCC in regulation (No UV or OC interrupts set during the test)		3.5		
$Ratio_{ICC3/ICC1-3}$	Load sharing ratio 3 (ICC3:ICC1)	6.0V <= V_{SUP} <= 28V; SBC Normal Mode; LS ratio setting 0x1F[3:1]=011b R_{shunt} = 0.25Ω Total load current = 500mA VCC1, VEXCC in regulation (No UV or OC interrupts set during the test)		2.2		
$Ratio_{ICC3/ICC1-1}$	Load sharing ratio 1 (ICC3:ICC1)	6.0V <= V_{SUP} <= 28V; SBC Normal Mode; LS ratio setting 0x1F[3:1]=001b R_{shunt} = 0.25Ω Total load current = 300mA VCC1, VEXCC in regulation (No UV or OC interrupts set during the test)		1.3	1.6	
VCAN Supply Input						
IVCAN	Supply current	Normal mode: Recessive, V_{TXD} = VCC1 , VEXCC, VCC1 and VCC2 = On with no load		3	5	mA
		Normal mode: Dominant, V_{TXD} = 0 V, R_L = 60 Ω and C_L = open, typical bus load, VEXCC, VCC1 and VCC2 = On with no load			60	mA
		Normal mode: Dominant, V_{TXD} = 0 V, R_L = 50 Ω and C_L = open, high bus load, VEXCC, VCC1 and VCC2 = On with no load			65	mA
		Normal mode: Dominant with bus fault, V_{TXD} = 0 V, CANH = - 25 V, R_L and C_L = open, VEXCC, VCC1 and VCC2 = On with no load			100	mA
$UVCAN_R$	Supply undervoltage recovery	VCAN rising	4.6		4.85	V
$UVCAN_F$	Supply undervoltage detection	VCAN falling	4.5		4.75	V
$UVCAN_{HYS}$	VCAN Supply undervoltage detections hysteresis		50	100	150	mV

(1) Threshold at which the current limit starts to operate and is only active when VEXCC is configured for stand-alone configuration
(2) Current will be higher for each HSS turned on using direct drive

6.7 Electrical Characteristics

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CAN Driver						
$V_{CANH(D)}$	Bus output voltage (dominant) CANH	See Figure 7-4, V_{CTXD} = 0 V, R_L =45 Ω to 65 Ω, C_L = open, R_{CM} = open	3.0		4.26	V
$V_{CANL(D)}$	Bus output voltage (dominant) CANL		0.75		2.01	V
$V_{CANH(R)}$ $V_{CANL(R)}$	Bus output voltage (recessive)	See Figure 7-1 and Figure 7-4 V_{CTXD} = VCC1, R_L = open (no load), R_{CM} = open	2	2.5	3	V

6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CANH(R)}$ $V_{CANL(R)}$	Terminated bus output voltage (recessive)	V_{CTXD} = VCC1, 45 Ω ≤ R_L ≤ 65 Ω, Split termination capacitance 4.7 nF	2.256		2.756	V
$V_{DIFF(D)}$	Differential output voltage(dominant) on normal bus load	See Figure 7-1 and Figure 7-4 , V_{CTXD} = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	1.5		3	V
$V_{DIFF(D)}$	Differential output voltage(dominant) over extended differential load range	See Figure 7-1 and Figure 7-4 V_{CTXD} = 0 V, 45 Ω ≤ R_L ≤ 70 Ω, C_L = open, R_{CM} = open	1.5		3.3	V
$V_{DIFF(D)}$	Differential output voltage(dominant) on effective resistance during arbitration	See Figure 7-1 and Figure 7-4 V_{CTXD} = 0 V, R_L = 2.24 kΩ, C_L = open, R_{CM} = open	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage(recessive)	See Figure 7-1 and Figure 7-4 , V_{CTXD} = VCC1, R_L = 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open	–50		50	mV
		See Figure 7-1 and Figure 7-4 V_{CTXD} = VCC1, R_L = open (no load), C_L = open, R_{CM} = open	–50		50	mV
$V_{CANH(INACT)}$	Bus output voltage on CANH with bus biasing inactive	See Figure 7-1 and Figure 7-4 , V_{CTXD} = VCC1, R_L = open, C_L = open, R_{CM} = open	–0.1		0.1	V
$V_{CANL(INACT)}$	Bus output voltage on CANL with bus biasing inactive		–0.1		0.1	V
$V_{DIFF(INACT)}$	Bus output voltage on CANH - CANL (recessive) with bus biasing inactive		–0.2		0.2	V
$V_{SYM-VCC}$	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CAN} (8)	See Figure 7-1 and Figure 7-4 , R_L = 60Ω, C_L = open, R_{CM} = open, C_1 = 4.7nF, CTXD = 250 kHz, 1 MHz, 2.5 MHz	0.9		1.1	V/V
$V_{SYM-REC}$	Output symmetry (dominant or recessive) ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{REC} (8)	See Figure 7-1 and Figure 7-4 , R_L = 45Ω to 65Ω, C_L = open, R_{CM} = open, C_1 = 4.7nF, CTXD = 250 kHz, 1 MHz, 2.5 MHz	0.95		1.05	V/V
V_{SYM_DC}	Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$) – $V_{O(CANL)}$) with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, however, at most 1 MHz (2 Mbit/s)	See Figure 7-1 and Figure 7-4 , R_L = 60 Ω, C_L = open, R_{CM} = open, C_1 = 4.7 nF	–400		400	mV
$I_{CANH(OS)}$	Short-circuit steady-state output current, dominant See Figure 7-1 and Figure 7-8	–3.0 V ≤ V_{CANH} ≤ +18.0 V, CANL = open, V_{CTXD} = 0 V	–100			mA
$I_{CANL(OS)}$		–3.0 V ≤ V_{CANL} ≤ +18.0 V, CANH = open, V_{CTXD} = 0 V			100	mA
I_{OS_REC}	Short-circuit steady-state output current, recessive See Figure 7-1 and Figure 7-8	–40 V ≤ V_{BUS} ≤ +40 V, V_{BUS} = CANH = CANL	–5		5	mA
CAN Receiver						
$V_{DIFF\_RX(D)}$	Receiver dominant state differential input voltage range, bus biasing active	–12.0 V ≤ V_{CANL} ≤ +12.0 V –12.0 V ≤ V_{CANH} ≤ +12.0 V See Figure 7-5 and Table 8-3	0.9		8	V
$V_{DIFF\_RX(R)}$	Receiver recessive state differential input voltage range, bus biasing active		–3		0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal mode			135		mV

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6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DIFF\_RX(D\_INACT)}$	Receiver dominant state differential input voltage range, bus biasing inactive	–12.0 V ≤ V_{CANL} ≤ +12.0 V –12.0 V ≤ V_{CANH} ≤ +12.0 V See Figure 7-5 and Table 8-3	1.15		8	V
$V_{DIFF\_RX(R\_INACT)}$	Receiver recessive state differential input voltage range, bus biasing inactive		–3		0.4	V
$I_{LKG-CANH}$, $I_{LKG-CANL}$	Input leakage current on CANH, CANL pins when powered off	CANH = 5V, CANL = 5 V; VCAN = VSUP =0V or connected to GND via 47 kΩ resistor	-5		5	µA
C_I	Input capacitance to ground (CANH or CANL) (9)				20	pF
C_{ID}	Differential input capacitance (9)				10	pF
$R_{DIFF\_PAS\_REC}$	Differential input resistance durring passive recessive state	V_{CTXD} = VCC1, normal mode: –2.0 V ≤ V_{CANH} ≤ +7.0 V; –2.0 V ≤ V_{CANL} ≤ +7.0 V	12		100	kΩ
R_{SE_CANH} R_{SE_CANL}	Single ended Input resistance during passive recessive state	–2.0 V ≤ V_{CANH} ≤ +7.0 V –2.0 V ≤ V_{CANL} ≤ +7.0 V	6		50	kΩ
m_R	Input resistance matching: [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100%	V_{CANH} = V_{CANL} = 5.0 V	–1		1	%
$R_{SE\_SIC\_ACT\_REC}$	Single ended SIC impedance (CANH to common mode bias and CANL to common mode bias) during active recessive drive phase (TCAN295xx variants with CAN FD SIC)	TXD= 0 V, 2 V ≤ $V_{CANH/L}$ ≤ VCC - 2 V if –12 V ≤ $V_{CANH/L}$ ≤ 12 V Use Delta V/ Delta I method (same as used for $R_{SE\_CANH/CANL}$/$R_{DIFF\_PAS\_REC}$ in RX section), no load on bus (TCAN295xx variants with CAN FD SIC)	37.5		66.5	Ω
$R_{DIFF\_SIC\_ACT\_REC}$	Differential input resistance in active recessive drive phase (CANH to CANL) (TCAN295xx variants with CAN FD SIC)	2 V ≤ $V_{CANH/L}$ ≤ VCC - 2 V Duration from TXD= From low-to-high edge to elapse of active recessive drive period (t_{REC_START}), Use Delta V/ Delta I method (same as used for $R_{SE\_CANH/CANL}$/$R_{DIFF\_PAS\_REC}$ in RX section), no load on bus (TCAN295xx variants with CAN FD SIC)	75		133	Ω
LIN						
V_{OH}	HIGH level output voltage(1)	LIN recessive, LTXD = high, I_O = 0 mA, VSUP = 5.5 V to 28 V	0.85			VSUP
V_{OL}	LOW level output voltage(1)	LIN dominant, LTXD = low, VSUP = 5.5 V to 28 V			0.2	VSUP
V_{IH}	HIGH level input voltage(1)	LIN recessive, LTXD = high, I_O = 0 mA, VSUP = 5.5 V to 28 V	0.47		0.6	VSUP
V_{IL}	LOW level input voltage(1)	LIN dominant, LTXD = low, VSUP = 5.5 V to 28 V	0.4		0.53	VSUP
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	LTXD & LRXD open, V_{LIN} = 5.5 V to 45 V, VCC = no load	–0.3		40	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987-4 Param 12)	LTXD = 0 V, V_{LIN} = 18 V, VSUP = 18 V	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	V_{LIN} = 0 V, VSUP = 12 V Driver off/ recessive;	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} ≥ VSUP, 5.5 V ≤ VSUP ≤ 28 V Driver off;			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} = VSUP, Driver off;	–5		5	µA

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6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = VSUP, VSUP = 12 V, 0 V ≤ V_{LIN} ≤ 28 V;	–1		1	mA
$I_{BUSrec\_NO\_GND}$	Leakage current, loss of ground LIN bus is in recessive state	GND = VSUP, VSUP = 12 V = V_{LIN} V;	–100		100	µA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0 V ≤ V_{LIN} ≤ 28 V, VSUP = GND;			10	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up);			0.4	VSUP
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18)	LIN recessive;	0.6			VSUP
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	V_{BUS_CNT} = (V_{IL} + V_{IH})/2;	0.475	0.5	0.525	VSUP
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20) (2)	V_{HYS} = (V_{IH} - V_{IL}); V_{HYS} = (V_{th_rec} - V_{th_dom})(3)	0.07		0.175	VSUP
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path (ISO/DIS 17987 Param 21)	By design and characterization VSUP 5.5V to 18V	0.4	0.7	1.0	V
R_{LIN}	Internal pull-up resistor to V_{SUP} on LIN (ISO/DIS 17987 Param 26)	Normal and Standby modes	27.66	35	48	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, VSUP = 14 V, LIN = GND	–13	–10	–7	µA
$C_{LIN,PIN}$	Capacitance of the LIN pin	(9)			25	pF
LIMP Output (Open-drain)						
V_{OL}	Open-drain output voltage (active low)	External Pull-up; 4.5V < V < 28V, I_{LIMP} = – 6 mA		0.5	1	V
$I_{LKG(LIMP)}$	Output current (inactive)	V_{LIMP} = 0V to 28 V	–2		2	µA
HSS1, HSS2, HSS3, HSS4 (High voltage output)						
R_{dson}	HSS output drain-to-source on resistance	I_O = – 60 mA		7	12	Ω
$I_{OC-DET(HSS)}$	HSS overcurrent detection limit	VHSS = 14 V	150	200	300	mA
$I_{OL(HSS)}$	HSS open load current detection threshold when on and current is falling	VHSS = 14 V	0.4		3.0	mA
$I_{OLHYS(HSS)}$	HSS open load current hysteresis	VHSS = 14 V	0.05	0.45	1	mA
I_{lkg}	Leakage current	HSS = 0 V, Sleep Mode	–1		1	µA
t_R	Output rise time (HSS)	6 V ≤ VHSS ≤ 18 V, R_L = 220 Ω, 20%/80% (8)	0.45		2.5	V/µs
t_F	Output fall time (HSS)	6 V ≤ VHSS ≤ 18 V, R_L = 220 Ω, 80%/20% (8)	0.45		2.5	V/µs
t_{HSS_on}	Threshold for the (VHSS-HSSx) to detect readback fault for each HSS output	VHSS = 14 V, I_{LOAD} = 60 mA, V_{OUT} = 80% of VHSS	30		90	µs
t_{HSS_off}	Switching off delay (HSS) from SPI command to off	VHSS = 14 V, I_{LOAD} = 60 mA, V_{OUT} = 20% of VHSS	30		90	µs
$t_{R\_DD\_SR0}$	Output rise time for HSS in direct drive mode with slow slew rate option	HSS_CNTLx=1000b, VHSS = 13.5 V, R_L = 2.2 kΩ, HSSx going from 20% to 80% of VHSS (8)	1.1	1.25	1.5	V/µs
$t_{F\_DD\_SR0}$	Output fall time for HSS in direct drive mode with slow slew rate option	HSS_CNTLx=1000b, VHSS = 13.5 V, R_L = 2.2 kΩ, HSSx going from 80% to 20% of VHSS (8)	1	1.15	1.4	V/µs
$t_{R\_DD\_SR1}$	Output rise time (HSS) for HSS in direct drive mode with fast slew rate option	HSS_CNTLx=1001b, VHSS = 13.5 V, R_L = 2.2 kΩ, HSSx going from 20% to 80% of VHSS (8)	2.1	2.5	2.8	V/µs

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6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{F\_DD\_SR1}$	Output fall time for HSS in direct drive mode with fast slew rate option	HSS_CNTLx=1001b, VHSS = 13.5 V, R_L = 2.2 kΩ, HSSx going from 80% to 20% of VHSS (8)	2.2	2.5	2.8	V/µs
$t_{HSSDD\_EN\_SR0}$	Enable time from edge change on WAKE3/DIR when configured for direct drive slow slew rate option	HSS_CNTLx=1000b, VHSS = 13.5 V, R_L = 2.2 kΩ, HSSx = 80% of VHSS	55	65	70	µs
$t_{HSSDD\_DIS\_SR0}$	Disable time from edge change on WAKE3/DIR when configured for direct drive with slow slew rate option	HSS_CNTLx=1000b, VHSS = 13.5 V, R_L = 2.2 kΩ, HSSx = 20% of VHSS	60	70	75	µs
$t_{HSSDD\_EN\_SR1}$	Enable time from edge change on WAKE3/DIR when configured for direct drive with fast slew rate option	HSS_CNTLx=1001b, VHSS = 13.5 V, R_L = 2.2 kΩ, HSSx = 80% of VHSS	50	55	65	µs
$t_{HSSDD\_DIS\_SR1}$	Disable time from edge change on WAKE3/DIR when configured for direct drive with fast slew rate option	HSS_CNTLx=1001b, VHSS = 13.5 V, R_L = 2.2 kΩ, HSSx = 20% of VHSS	45	55	60	µs
t_{OCFLTR}	HSS overcurrent filter time for overcurrent fault indication and HSS shutoff. Not applicable for HSS low power mode	VHSS = 14 V; $I_{O(HSS)}$ > $I_{OC-DET(HSS)}$ HSS_OC_FLTR = 0b	10	16	25	µs
t_{OCFLTR}	HSS overcurrent filter time for overcurrent fault indication and HSS shutoff. Not applicable for HSS low power mode	VHSS = 14 V; $I_{O(HSS)}$ > $I_{OC-DET(HSS)}$ HSS_OC_FLTR = 1b	250	300	350	µs
t_{OLFLTR}	HSS open load filter time for open load fault indication. Not applicable for HSS low power mode	VHSS = 14 V	40	64	80	µs
WAKE1, WAKE2, WAKE3 Input Terminal (High voltage input)						
V_{IH}	High-level input voltage (7)	Register setting 01b	2.5		3.5	V
		Register setting 10b	3.8		5	V
		Register setting 11b	5.6		7	V
V_{IL}	Low-level input voltage (7)	Register setting 01b	1.5		2.8	V
		Register setting 10b	3.0		4.2	V
		Register setting 11b	5		6.3	V
V_{IH}	High-level input voltage for DIR pin when any HSS is in direct-drive mode (7)	Standby and Normal Mode only, HSSx set to drirect drive mode	0.7			VCC1
V_{IL}	Low-level input voltage for DIR pin when any HSS is in direct-drive mode (7)	Standby and Normal Mode only, HSSx set to drirect drive mode			0.3	VCC1
I_{IH}	High-level input current	V_{WAKEx} = 6.5V to 28V		2	4	µA
I_{IL}	Low-level input current(9)	WAKE = 1 V		1.2	2.2	µA
$I_{LKG-VBAT-MON}$	Leakage current when Vbat monitoring enabled	V_{WAKE1} = 4 V - 28 V		2	3	µA
$R_{DSON-VBAT-MON}$	On resistance of Vbat switch when Vbat monitoring enabled	V_{WAKE1} = 4 V - 28 V, switch current = 500 µA		155	400	Ω
$I_{LKG-WAKE}$	Leakage current	WAKEx pin disabled and V_{WAKEx} = 40 V		.23	1	µA
t_{WAKE}	Wake up hold time from a wake edge on WAKE in standby or sleep mode for static sensing.	See Figure 8-21 and Figure 8-22			140	µs
$t_{WAKE\_INVALID}$	WAKE pin pulses shorter than this will be filtered out in standby or sleep mode for static sensing.	See Figure 8-21 and Figure 8-22	10			µs

6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
td_IDSTAT	Delay between command via SPI andupdated status of ID pin in IDx_STATregister	IDx pin enabled (register bit IDx_EN= 1b) (8)		300	350	µs
SDI, SCK, nCS, SW, CTXD, LTXD Input Terminals						
V_{IH}	High-level input voltage		0.7			VCC1
V_{IL}	Low-level input voltage				0.3	VCC1
$V_{IHSWINT}$	SW pin high-level input voltage when VCC1 is missing for sleep or fail-safe mode	Register 8'h0E[1] = 1 and/or 8'h0E[2] = 1 and VCC1 missing in sleep or fail-safe mode	1.2			V
$V_{ILSWINT}$	SW low-level input voltage when VCC1 is missing for sleep or fail-safe mode	Register 8'h0E[1] = 1 and/or 8'h0E[2] = 1 and VCC1 missing in sleep or fail-safe mode			0.4	V
$I_{IHSWINT-PD}$	High-level input leakage current for SW pin (active-high) when VCC1 is off	VCC1 off, internal pull-down enabled, Vin = 1.5 V	18		32	µA
$I_{ILSWINT-PD}$	Low-level input leakage current for SW pin (active-high) when VCC1 is off	VCC1 off, internal pull-down enabled, Vin = 0 V	–1		1	µA
$I_{IHSWINT-PU}$	High-level input leakage current for SW pin (active-low) when VCC1 is off	VCC1 off, internal pull-up enabled, Vin = 1.5 V	–60		–20	µA
$I_{ILSWINT-PU}$	Low-level input leakage current for SW pin (active-low) when VCC1 is off	VCC1 off, internal pull-up enabled Vin = 0 V	–85		–35	µA
I_{IH}	High-level input leakage current (Internal pull-up)	Inputs = VCC1 ± 2%	–1		1	µA
I_{IH}	High-level input leakage current (Internal pull-down)	Inputs = VCC1 ± 2%	15		140	µA
I_{IL}	Low-level input leakage current (Internal Pull-up)	Inputs = 0 V, VCC1 ± 2%	–140		–2	µA
I_{IL}	Low-level input leakage current (Internal Pull-down)	Inputs = 0 V, VCC1 ± 2%	–1		1	µA
C_{IN}	Input Capacitance	at 20 MHz	1.5		10	pF
Rpd	Pull-down resistor (SDI, SCK, and SW pins)	These pins will have a pull-down resistor when configured this way.	40	60	80	kΩ
Rpu	Pull-up resistor (SDI, SCK, nCS, SW, CTXD and LTXD pins)	The SDI, SCK, and SW pins will have a pull-up resistor when configured this way. nCS, CTXD, and LTXD always have a pull_up.	40	60	80	kΩ
CRXD, LRXD, SDO, GFO, nINT Output Terminals						
V_{OH}	HIGH level output voltage	I_{OH} = -2 mA	0.8			VCC1
V_{OL}	LOW level output voltage	I_{OL} = 2 mA			0.2	VCC1
nRST Terminal (input/output)						
V_{IH}	High level input switching threshold voltage	Based off of internal voltage	2.1			V
V_{IL}	Low level input switching threshold voltage	Based off of internal voltage			0.8	V
I_{OL}	Low-level output current, open drain	nRST = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	nRST = VCC1	–5		5	µA
R_{PU}	Pull-up resistance (Output pulled up to VCC1)		10	30	50	kΩ
LIN Duty Cycle						

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6.7 Electrical Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D1	Duty Cycle 1 (ISO/DIS 17987 Param 27 and J2602 Normal battery)(4) (5)	$TH_{REC(MAX)}$ = 0.744 x VSUP, $TH_{DOM(MAX)}$ = 0.581 x VSUP, VSUP = 7 V to 18 V, t_{BIT} = 50/52 µs, D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}), (See Figure 7-13, Figure 7-14)	0.396			
D2	Duty Cycle 2 (ISO/DIS 17987 Param 28 and J2602 Normal battery)(4) (5)	$TH_{REC(MIN)}$ = 0.422 x VSUP, $TH_{DOM(MIN)}$ = 0.284 x VSUP, VSUP = 7.6 V to 18 V, t_{BIT} = 50/52 µs, D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 7-13, Figure 7-14)			0.581	
D3	Duty Cycle 3 (ISO/DIS 17987 Param 29 and J2602 Normal battery)(4) (5)	$TH_{REC(MAX)}$ = 0.778 x VSUP, $TH_{DOM(MAX)}$ = 0.616 x VSUP, VSUP = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}), (See Figure 7-13, Figure 7-14)	0.417			
D4	Duty Cycle 4 (ISO/DIS 17987 Param 30 and J2602 Normal battery)(4) (5)	$TH_{REC(MIN)}$ = 0.389 x VSUP, $TH_{DOM(MIN)}$ = 0.251 x VSUP, VSUP = 7.6 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 7-13, Figure 7-14)			0.59	
$D1_{LB}$	Duty Cycle 1 J2602 Low battery (5) (6)	$TH_{REC(MAX)}$ = 0.665 x VSUP, $TH_{DOM(MAX)}$ = 0.499 x VSUP, VSUP = 5.5 V to 7 V, t_{BIT} = 50/52 µs, $D1_{LB}$ = $t_{BUS\_rec(min)/(2\ x\ tBIT)}$ (See Figure 7-13, Figure 7-14)	0.396			
$D2_{LB}$	Duty Cycle 2 J2602 Lowl battery(5) (6)	$TH_{REC(MIN)}$ = 0.496 x VSUP, $TH_{DOM(MIN)}$ = 0.361 x VSUP, VSUP = 6.1 V to 7.6 V, t_{BIT} = 50/52 µs, $D2_{LB}$ = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 7-13, Figure 7-14)			0.581	
$D3_{LB}$	Duty Cycle 3 J2602 Low battery (5) (6)	$TH_{REC(MAX)}$ = 0.665 x VSUP, $TH_{DOM(MAX)}$ = 0.499 x VSUP, VSUP = 5.5 V to 7 V, t_{BIT} = 96 µs, $D3_{LB}$ = $t_{BUS\_rec(min)/(2\ x\ tBIT)}$ (See Figure 7-13, Figure 7-14)	0.417			
$D4_{LB}$	Duty Cycle 4 J2602 Lowl battery (5) (6)	$TH_{REC(MIN)}$ = 0.496 x VSUP, $TH_{DOM(MIN)}$ = 0.361 x VSUP, VSUP = 6.1 V to 7.6 V, t_{BIT} = 96 µs, $D4_{LB}$ = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 7-13, Figure 7-14)			0.59	
$T_{r\text{-}d\ max}$	$t_{REC(MAX)}$ - $t_{DOM(MIN)}$ (5)	$TH_{REC(MAX)}$ = 0.744 x VSUP, $TH_{DOM(MAX)}$ = 0.581 x VSUP, VSUP = 7 V to 18 V, t_{BIT} = 52 µs (19.231 kbps), (See Figure 7-13, Figure 7-14)			10.8	µs
$T_{d\text{-}r\ max}$	$t_{DOM(MAX)}$ - $t_{REC(MIN)}$ (5)	$TH_{REC(MIN)}$ = 0.422 x VSUP, $TH_{DOM(MIN)}$ = 0.284 x VSUP, VSUP = 7.6 V to 18 V, t_{BIT} = 52 µs (19.231 kbps), (See Figure 7-13, Figure 7-14)			8.4	µs
$T_{r\text{-}d\ max}$	$t_{REC(MAX)}$ - $t_{DOM(MIN)}$ (5)	$TH_{REC(MAX)}$ = 0.778 x VSUP, $TH_{DOM(MAX)}$ = 0.616 x VSUP, VSUP = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), (See Figure 7-13, Figure 7-14)			15.9	µs
$T_{d\text{-}r\ max}$	$t_{DOM(MAX)}$ - $t_{REC(MIN)}$ (5)	$TH_{REC(MIN)}$ = 0.389 x VSUP, $TH_{DOM(MIN)}$ = 0.251 x VSUP, VSUP = 7.6 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), (See Figure 7-13, Figure 7-14)			17.28	µs

(1) SAE J2602 loads include: commander: 5.5 nF; 4 kΩ and for a responder: 5.5 nF; 875 Ω
(2) V_{HYS} is defined for both ISO 17987 and SAE J2602-1.
(3) V_{HYS} = (V_{th_rec} - V_{th_dom}) where V_{th_rec} and V_{th_dom} are the actual voltage values from V_{BUSrec} and V_{BUSdom}
(4) ISO 17987 loads include 1 nF; 1 kΩ/ 6.8nF; 660 Ω/ 10 nF; 500 Ω; with t_{BIT} values of 50 µs and 96 µs

(5) SAE J2602 loads include: commander: 5.5 nF; 4 kΩ/ 889 pF; 20 kΩ and for a responder: 5.5 nF; 875 Ω/ 889 pF; 900 Ω; with t_{BIT} values of 52 µs and 96 µs
(6) ISO 17987 does not have a low battery specification. Using the ISO 17987 loads, these low battery duty cycle parameters are covered for t_{BIT} values of 50 µs and 96 µs
(7) Selected using Register 8'h12[1:0] for WAKE1; Register 8'h2B[5:4] for WAKE2; Register 8'h2B[1:0] for WAKE3
(8) Specified by design and characterization
(9) Current based off of setting 11b for the WAKEx pin

6.8 Timing Requirements

Over recommended operating range (unless otherwise noted)

Parameter		Test Condition	MIN	NOM	MAX	UNIT
Supply						
t_{PWRUP}	Time after VSUP exceeds UVSUP and VCC1> UVCC1	Device powers up enters restart			3.5	ms
t_{VCCSS}	Softstart time for VCC1, VCC2 and VEXCC	Time it takes VCC1, VCC2, VEXCC ramp from 0 V to 90% of regulated value		0.75	1.25	ms
t_{UVFLTR}	Under-voltage detection delay time for VCC1, VCC2 and VEXCC		25		50	µs
$t_{UVCC1PR}$	Under-voltage filter time for VCC1 pre-warning		2		12	µs
$t_{UVCANFLTR}$	Under-voltage filter time for VCAN		2		10	µs
t_{OVFLTR}	Over-voltage detect filter time on VCC1, VCC2 and VEXCC		15		50	µs
$t_{OVFLTRVHSS}$	Over-voltage detect filter time on VHSS		4		12	µs
t_{VSC}	Short to ground on VCC1, VCC2 and VEXCC detection delay time		75	100	125	µs
t_{VSCLS}	Short to ground for VCC1 and VEXCC detection delay time when load sharing		75	100	125	µs
t_{LDOON}	Time LDO is on to determine if a fault event is present after a previous uncleared detection	See Figure 7-18		4	5	ms
t_{FS_DUR}	Fail-safe mode exit timer. The timer starts at Fail-safe mode entry and the device exits Fail-safe mode after the timer expires		250	300	350	ms
Mode Change						
$t_{MODE\_STBY\_NOM\_CTRX}$	CAN transceiver state change time based upon SPI write from off or wake capable to on or listen state where CRXD mirror CAN bus				70	µs
$t_{MODE\_STBY\_NOM\_LTRX}$	LIN transceiver state change time based upon SPI write from off or wake capable to on or fast state where LRXD mirror LIN bus				70	µs
$t_{MODE\_NOM\_SLP}$	Time from SPI sleep command where CAN and/or LIN transceiver is off and RXD doesn't reflect the bus	See Figure 7-19			200	µs
$t_{MODE\_NOM\_STBY}$	SPI write to go to standby from normal mode	See Figure 7-20			70	µs
Device Timing						
t_{RSTN_act}	Reset delay after recovering from undervoltage (VCC1 ≥ UVCC1R to nRST release); Short duration	nRST_PULSE_WIDTH = 0b See Figure 7-17	1.5	2	2.5	ms

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6.8 Timing Requirements (continued)

Over recommended operating range (unless otherwise noted)

Parameter		Test Condition	MIN	NOM	MAX	UNIT
t_{RSTN_act}	Reset delay after recovering from undervoltage (VCC1 ≥ UVCC1R to nRST release); long duration	nRST_PULSE_WIDTH=1b See Figure 7-17	10	15	20	ms
t_{NRST_TOG}	Reset pulse duration due to watchdog error; short duration	nRST_PULSE_WIDTH = 0b	1.5	2	2.5	ms
	Reset pulse duration due to watchdog error; long duration	nRST_PULSE_WIDTH = 1b	10	15	20	ms
t_{NRSTIN}	Input pulse required on the nRST pin to recognize a device reset		75	100	125	µs
t_{RSTTO}	Restart timer. Timer starts when VCC1 < UVCC1F or VCC1 > OVCC1R. The device enters fail-safe mode when the timer expires before the VCC1 recovery. (2)	VSUP > UV_{SUP33R} for VCC1=3.3V VSUP > UV_{SUP5R} for VCC1 = 5V Measured from nRST active to LIMP active	3.5	4	4.5	ms
t_{nINT_TI}	nINT output pulse width when nINT_TOG_EN is enabled.	Register 8'h1B[0] = 1b	75	100	125	µs
t_{nINT_TP}	Period between nINT pulses when nINT_TOG_EN is enabled	Register 8'h1B[0] = 1b	75	100	125	µs
$t_{WK\_TIMEOUT}$	CAN bus wake-up timeout value	See Figure 8-17	0.8		2	ms
t_{WK_FILTER}	CAN bus filter requirements for a valid wake up request	See Figure 8-17	0.5		0.95	µs
t_{WK_FILTER}	CAN bus filter requirements for a valid wake up request	See Figure 8-17	0.5		1.8	µs
t_{WK_CYC}	Sampling window for cyclic sensing; Standby or Sleep mode	Register 8'h12[5] = 0b	10	25	35	µs
	Sampling window for cyclic sensing; Standby or Sleep mode	Register 8'h12[5] = 1b	55	70	85	µs
$t_{SILENCE\_CAN}$	Timeout for bus inactivity Timer is reset and restarted, when bus changes from dominant to recessive or vice versa.		0.6		1.2	s
t_{LDT}	Long Duration Timer (LDT) accuracy	Can be programmed to different values using register 8'h1C[6:3]	0.85	1	1.15	
t_{Bias}	Time from the start of a dominant-recessive-dominant sequence	Each phase 6 µs until Vsym ≥ 0.1. See Figure 7-10			250	µs
t_{SW}	SW pin filter time for a state change to be recognized		130			µs
t_{INITWD}	Initial long window for watchdog	WD_CONFIG_1 register 8'h13[1:0] = 00b; see Figure 8-30	127	150	173	ms
	Initial long window for watchdog	WD_CONFIG_1 register 8'h13[1:0] = 01b; see Figure 8-30	255	300	345	ms
	Initial long window for watchdog	WD_CONFIG_1 register 8'h13[1:0] = 10b (default); see Figure 8-30	510	600	690	ms
	Initial long window for watchdog	WD_CONFIG_1 register 8'h13[1:0] = 11b; see Figure 8-30	850	1000	1150	ms
t_{WD}	Window and Q&A watchdog timing accuracy(2)	Window watchdog or Q&A watchdog enabled. The PWM timers have the same accuracy	0.9	1	1.1	
t_{WD-TO}	Timeout WD, Timer1, Timer2 timers accuracy(2)	Timeout WD, cyclic wake, and cyclic sensing wake associated timers	0.85	1	1.15	
t_{CTXD_DTO}	Dominant time out(1)	R_L = 60 Ω, C_L = open	1		5	ms

6.8 Timing Requirements (continued)

Over recommended operating range (unless otherwise noted)

Parameter		Test Condition	MIN	NOM	MAX	UNIT
t_{LTXD_DTO}	LIN dominant state time out		20	45	80	ms
t_{TOGGLE}	RXD pin toggle timing when programmed after a WUP	See Figure 8-17	5	10	15	µs
t_{TSD_SBC}	Duration for which the SBC is in Fail-safe mode after TSD_SBC clears TSDR threshold		0.8	1	1.2	s
F_{OSC-1M}	1 MHz clock frequency		0.936	1.04	1.14	MHz
$F_{OSC-10k}$	10 kHz clock frequency		8.8	10.4	12	kHz

(1) The CTXD dominant time out (t_{CTXD_DTO}) disables the driver of the transceiver once the CTXD has been dominant longer than t_{CTXD_DTO}, which releases the CAN bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after CTXD has been returned HIGH (recessive). While this protects the CAN bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on CTXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{CTXD_DTO} minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ t_{CTXD_DTO} = 11 bits / 1.2 ms = 9.2 kbps.

(2) Specified by design and characterization

6.9 Switching Characteristics

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver and Receiver Characteristics (CAN FD) TCAN294xx Variants						
$t_{prop(TxD-busrec)}$	Propagation delay time, high CTXD to driver recessive	Typical conditions: R_L = 60 Ω, C_L = 100 pF, R_{CM} = open, See Figure 7-4		55	90	ns
$t_{prop(TxD-busdom)}$	Propagation delay time, low CTXD to driver dominant			46	90	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			6	25	ns
$t_{R/F}$	Differential output signal rise time:		10	48	85	ns
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to high CRXD output	Typical conditions: CANL = 1.5 V, CANH = 3.5 V, See Figure 7-5		84	115	ns
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to RXD low output			55	110	ns
t_{LOOP}	Loop Delay(1)	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{CRXD} = 15 pF, 4.5V ≤ VCAN ≤ 5.5 V, VCC1 ± 2%, CAN_SLOPE_CTRL_EN 8'h0E[7] = 0b			215	ns
Driver and Receiver Characteristics (CAN FD SIC) TCAN295xx Variants						
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high TXD edge to driver recessive (dominant to recessive)	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, R_{CM} = open; See Figure 7-4		55	80	ns
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low TXD edge to driver dominant (recessive to dominant)	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, R_{CM} = open; See Figure 7-4		55	80	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, R_{CM} = open; See Figure 7-4		15	25	ns
t_R	Differential output signal rise time:	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, R_{CM} = open; See Figure 7-4		40	60	ns
t_F	Differential output signal fall time:	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, R_{CM} = open; See Figure 7-4		30	55	ns
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to RXD high output (dominant to recessive)	C_{CRXD} = 15 pF; CANL = 1.5 V, CANH = 3.5 V; see Figure 7-5		65	110	ns

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6.9 Switching Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to RXD low output (recessive to dominant)	C_{CRXD} = 15 pF; CANL = 1.5 V, CANH = 3.5 V; see Figure 7-5		60	110	ns
t_{LOOP}	Loop Delay(1)	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, C_{CRXD} = 15 pF, 4.5V ≤ VCAN ≤ 5.5 V, VCC1 ± 2%, see Figure 7-6			190	ns
CAN FD Characteristics (TCAN294xx Variants)						
$t_{\Delta Bit(Bus)2M}$	Transmitted recessive bit width variation @ 2 Mbps, intended for use with bit rates above 1 Mbps up to 2 Mbps(3)	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{CRXD} = 15 pF; See Figure 7-6	-65		30	ns
$t_{\Delta Bit(Bus)5M}$	Transmitted recessive bit width variation @ 5 Mbps, intended for use with bit rates above 2 Mbps up to 5 Mbps(3)	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{CRXD} = 15 pF; See Figure 7-6	-40		10	ns
$t_{\Delta Bit(Bus)8M}$	Transmitted recessive bit width variation @ 5 Mbps, intended for use with bit rates above 5 Mbps up to 8 Mbps(3)	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{CRXD} = 15 pF; See Figure 7-6	-40		10	ns
$t_{\Delta Bit(RXD)2M}$	Received recessive bit width variation @ 2 Mbps(4)	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{CRXD} = 15 pF; See Figure 7-6	-100		50	ns
$t_{\Delta Bit(RXD)5M}$	Received recessive bit width variation @ 5 Mbps(4)	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{CRXD} = 15 pF; See Figure 7-6	-80		20	ns
$t_{\Delta REC}$	Receiver Timing symmetry @ 2 Mbps, intended for use with bit rates above 1 Mbps up to 2 Mbps	Typical conditions: R_L = 60 Ω, C_L = 100 pF, C_{CRXD} = 15 pF	–60	–11	35	ns
	Receiver Timing symmetry @ 5 Mbps, intended for use with bit rates above 2 Mbps up to 5 Mbps		–30		10	ns
CAN FD SIC Characteristics (TCAN295xx Variants)						
$t_{PAS\_REC\_START}$	Signal improvement start time of passive recessive phase	Measured from rising TXD edge with < 5ns slope at 50% threshold, to the end of the signal improvement phase; $R_{DIFF\_PAS\_REC}$ ≥ MIN $R_{DIFF\_ACT\_REC}$; $R_{SE\_CANH/L}$ ≥ MIN $R_{SE\_SIC\_REC}$			530	ns
$t_{ACT\_REC\_START}$	Start time of active signal improvement phase	Measured from rising TXD edge with < 5ns slope at 50% threshold,			120	ns
$t_{ACT\_REC\_END}$	End time of active signal improvement phase	Measured from rising TXD edge with < 5ns slope at 50% threshold,	355			ns
$t_{\Delta Bit(Bus)}$	Transmitted recessive bit width variation	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, C_{CRXD} = 15 pF; $t_{\Delta Bit(Bus)}$ = $t_{Bit(Bus)}$ -$t_{Bit(TXD)}$ See Figure 7-6	-10		10	ns
$t_{\Delta Bit(RXD)}$	Received recessive bit width variation @ 5 Mbps(5)	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, C_{CRXD} = 15 pF; $t_{\Delta Bit(RXD)}$ = $t_{Bit(RXD)}$ -$t_{Bit(TXD)}$ See Figure 7-6	-30		20	ns
$t_{\Delta REC}$	Receiver Timing symmetry variation(2)	Typical conditions: 45 Ω ≤ R_L ≤ 65 Ω, C_L = 100 pF, C_{CRXD} = 15 pF, $t_{\Delta REC}$ = $t_{Bit(RXD)}$ -$t_{Bit(Bus)}$, See Figure 7-6	-20		15	ns
LIN Switching Characteristics (Device variants with LIN)						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{LRXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 7-14)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, (t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4 kΩ, C_{LRXD} = 20 pF (Figure 7-14,)	–2		2	µs

ADVANCE INFORMATION

6.9 Switching Characteristics (continued)

Over recommended operating range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See Figure 8-20	25	100	150	µs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 8-45	10		60	µs
LIN Fast Mode (Device variants with LIN)						
DR	Data Rate	5.5 V ≤ VSUP ≤ 18 V, R_{LIN} = 500 Ω and $C_{LIN(bus)}$ = 600 pF			200	kbps
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{LRXD} = 2.4 kΩ, C_{LRXD} = 20 pF (See Figure 7-14)			5	µs
$t_{txr/f}$	LIN transmitter rise and fall time	5.5 V ≤ VSUP ≤ 18 V, R_{LIN} = 500 Ω and $C_{LIN(bus)}$ = 600 pF			1.5	µs
SPI Switching Characteristics						
f_{SCK}	SCK, SPI clock frequency (2)	Normal and standby modes, Sleep mode - if VCC1 is present, if register BYTE_CNT, 09h[3]=1b (two-byte mode)			2	MHz
f_{SCK}	SCK, SPI clock frequency (2)	Normal and standby modes, Sleep mode - if VCC1 is present, if register BYTE_CNT, 09h[3]=0b (single byte mode)			4	MHz
t_{SCK}	SCK, SPI clock period (2)	Normal and standby modes See Figure 7-16 if register BYTE_CNT, 09h[3]=0b (single byte mode)	250			ns
t_{SCK}	SCK, SPI clock period (2)		500			ns
t_{SCKR}	SCK rise time (2)				40	ns
t_{SCKF}	SCK fall time (2)				40	ns
t_{SCKH}	SCK, SPI clock high (2)		250			ns
t_{SCKH}	SCK, SPI clock high (2)		125			ns
t_{SCKL}	SCK, SPI clock low (2)		250			ns
t_{SCKL}	SCK, SPI clock low (2)		125			ns
t_{nCSS}	nCS chip select setup time (2)		100			ns
t_{nCSH}	nCS chip select hold time (2)		100			ns
t_{nCSD}	nCS chip select disable time, 1-byte mode OR 2-byte mode with f_{SCK} <= 2 MHz (2)	Normal and standby modes 1-byte mode OR 2-byte mode with f_{SCK} <= 2MHz See Figure 7-16	50			ns
t_{nCSD}	nCS chip select disable time, 2-byte mode with f_{SCK} > 2MHz (2)	Normal and standby modes; 2-byte mode with fSCK > 2MHz See Figure 7-16	2			µs
t_{SISU}	Data in setup time (2)	Normal and standby modes; See Figure 7-16	50			ns
t_{SIH}	Data in hold time (2)		50			ns
t_{SOV}	Data out valid (2)				80	ns
t_{RSO}	SO rise time (2)				40	ns
t_{FSO}	SO fall time (2)				40	ns

(1) Time span from signal edge on TXD input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered.
(2) Specified by design
(3) $t_{\Delta Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TXD)}$
(4) $t_{\Delta Bit(RXD)} = t_{Bit(RXD)} - t_{Bit(TXD)}$
(5) For two byte SPI reads and writes, SPI_CONFIG register 8'h09[3] = 1b, the max SPI clock is 2 MHz and what is shown here is for one byte reads and writes.

ADVANCE INFORMATION

7 Parameter Measurement Information

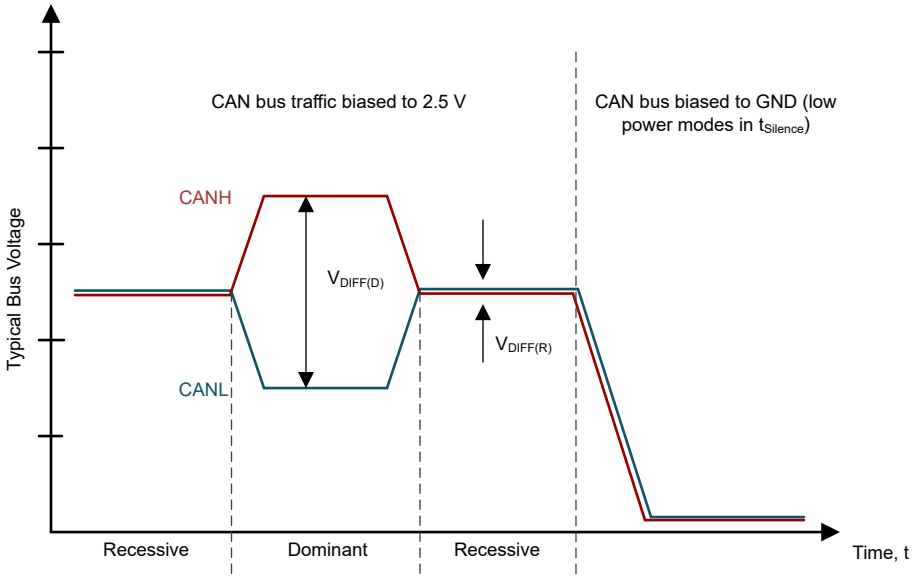
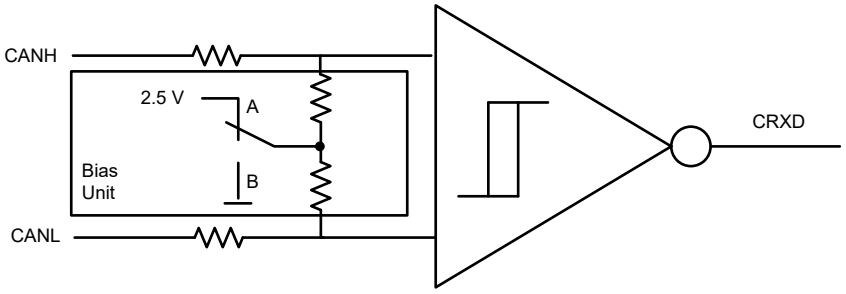


Figure 7-1. Bus States (Physical Bit Representation)



Note

A: Normal, Listen Modes

B: Standby and Sleep Modes (Low Power)

Figure 7-2. Simplified Recessive Common Mode Bias Unit and Receiver

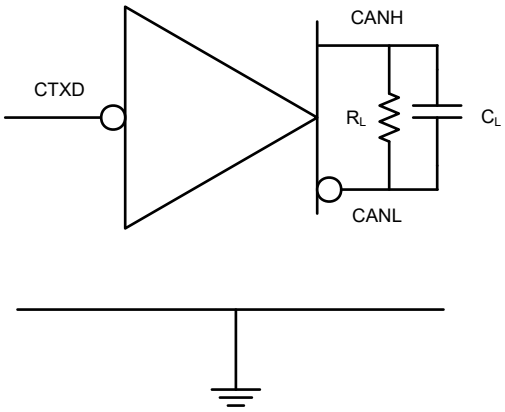


Figure 7-3. Supply Test Circuit

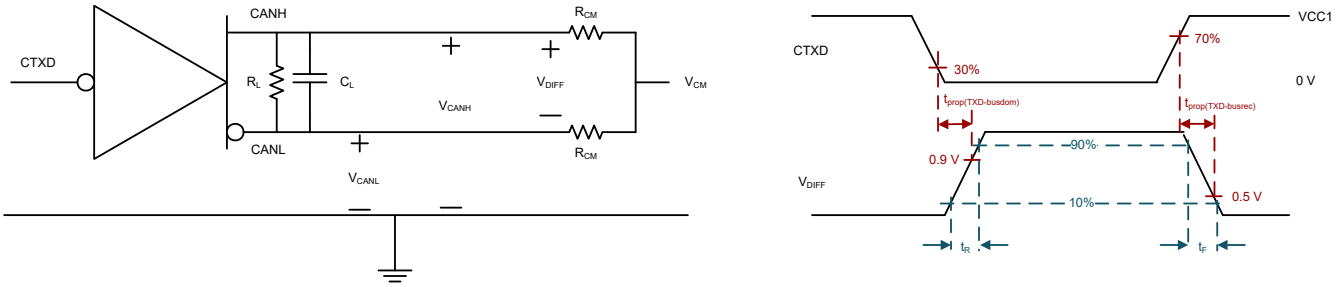


Figure 7-4. Driver Test Circuit and Measurement

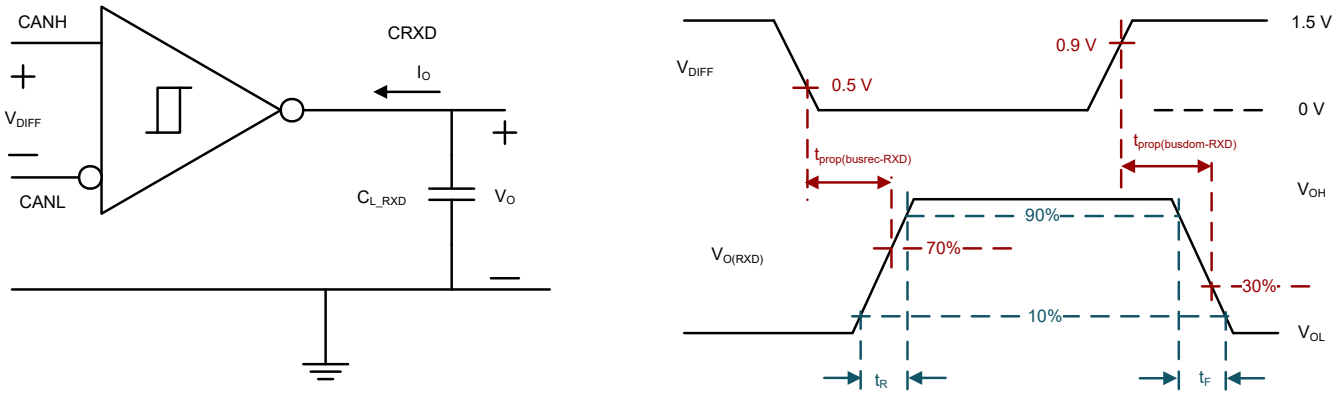


Figure 7-5. Receiver Test Circuit and Measurement

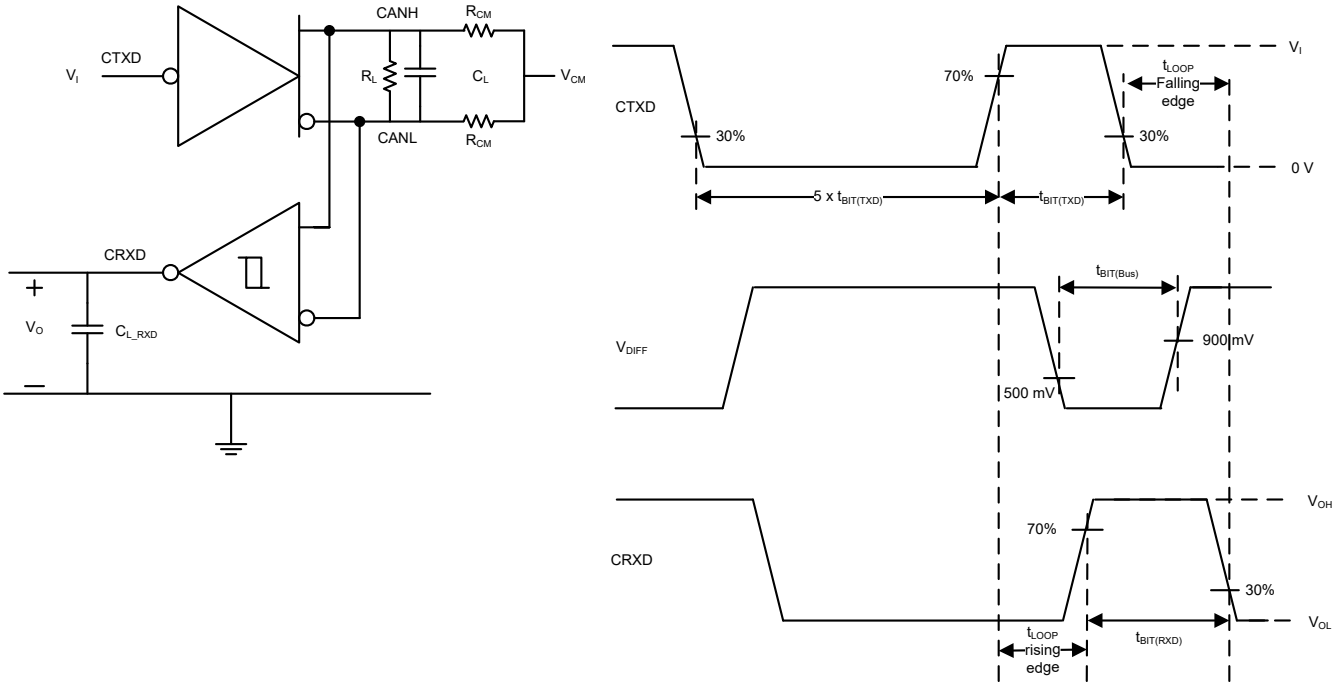


Figure 7-6. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

ADVANCE INFORMATION

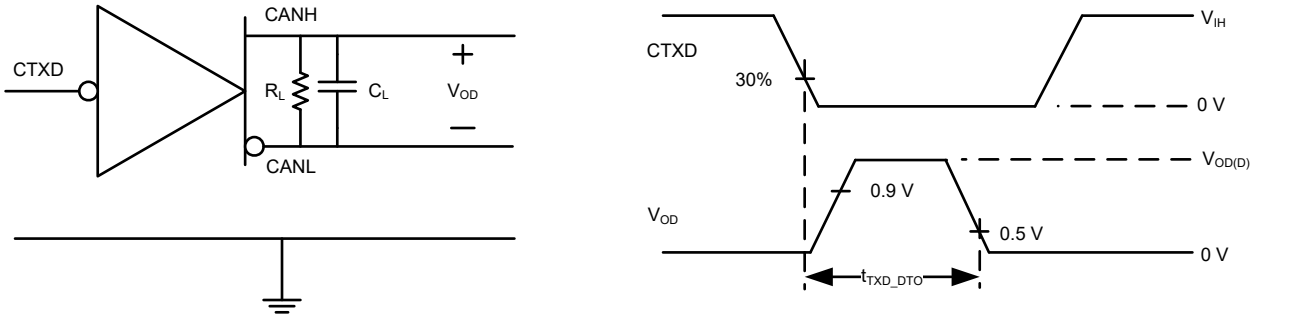


Figure 7-7. TXD Dominant Time Out Test Circuit and Measurement

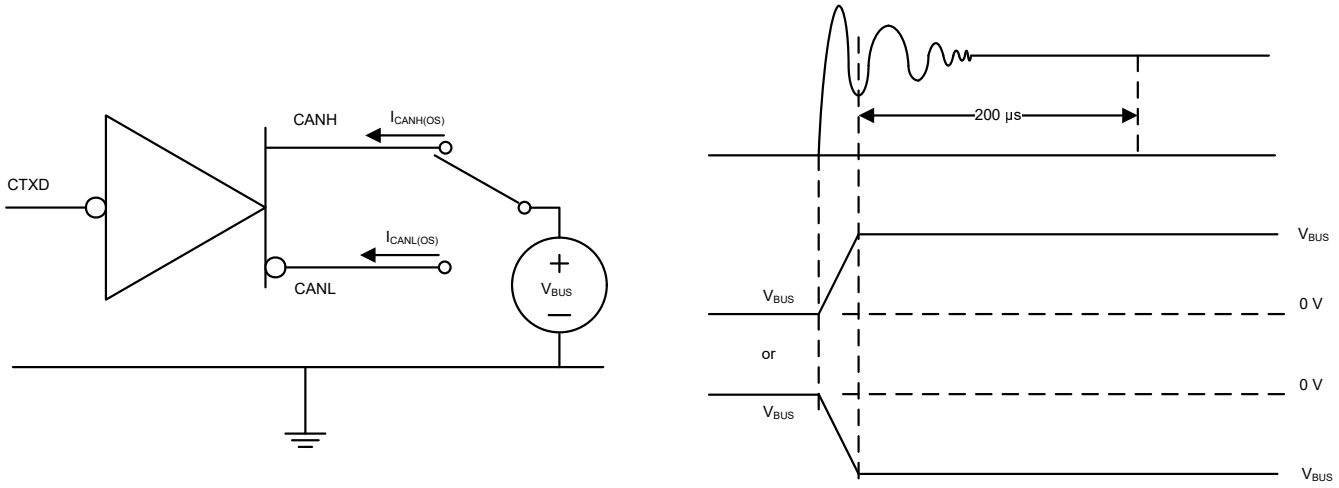


Figure 7-8. Driver Short-Circuit Current Test and Measurement

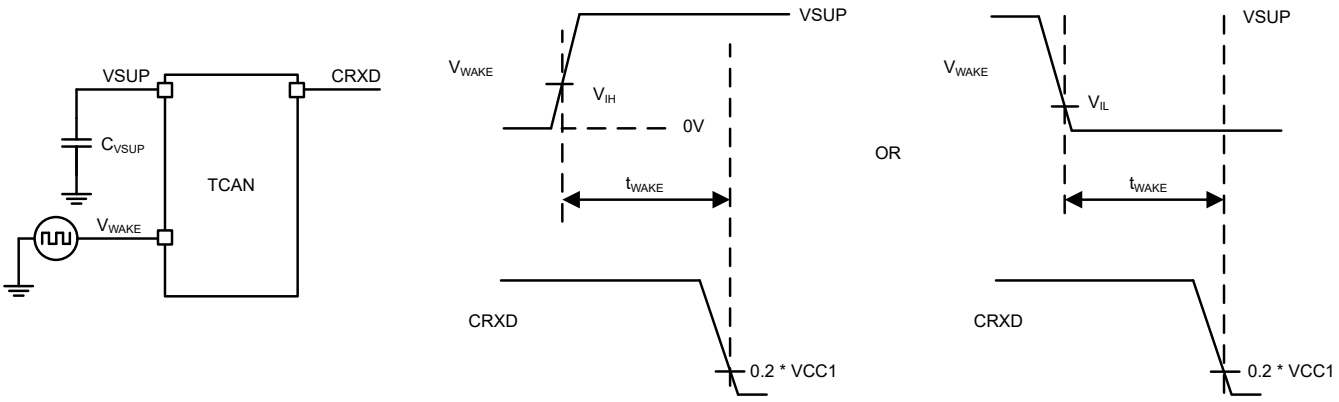


Figure 7-9. t_{WAKE} While Monitoring RXD Output

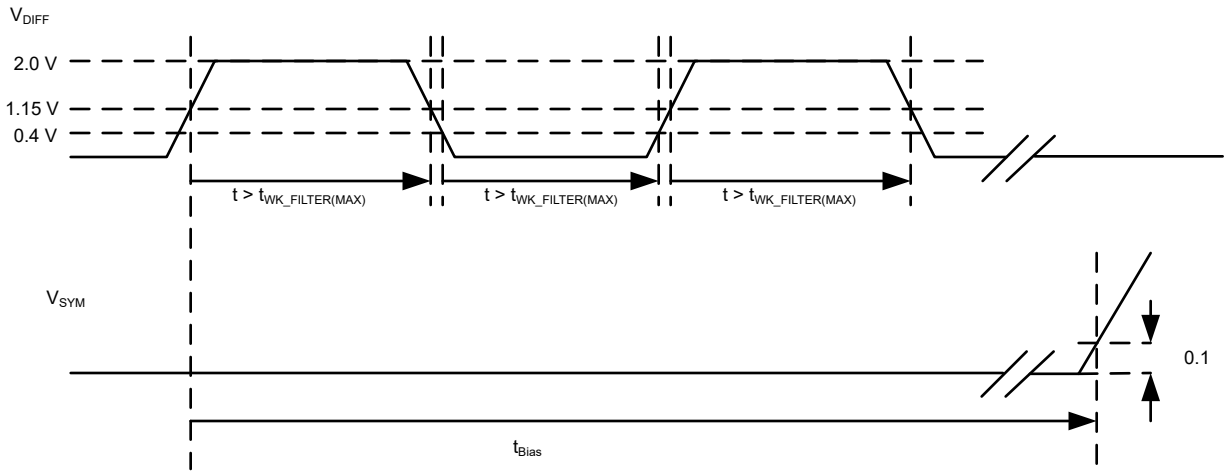


Figure 7-10. Test Signal Definition for Bias Reaction Time Measurement

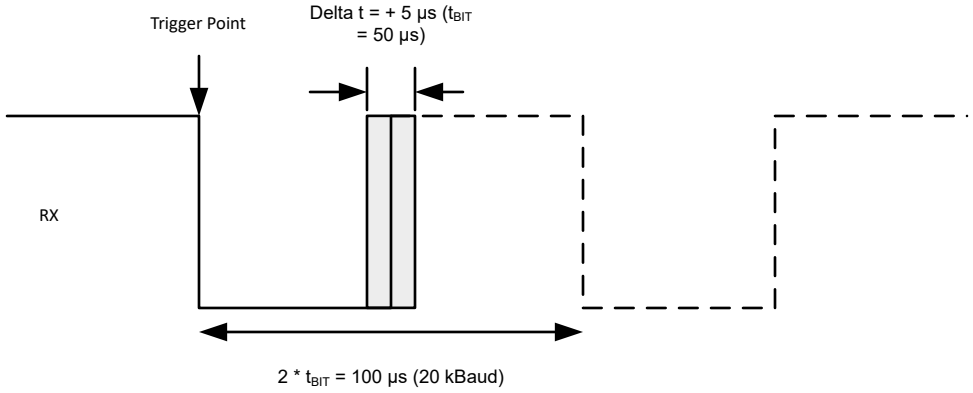


Figure 7-11. LIN RX Response: Operating Voltage Range

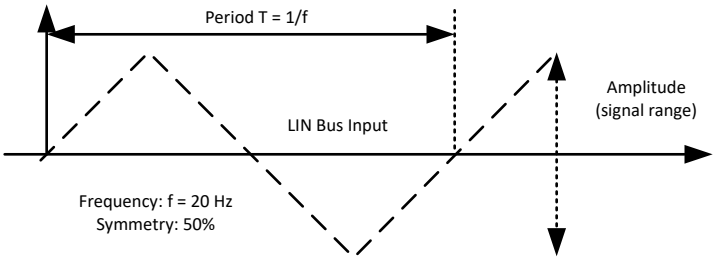


Figure 7-12. LIN Bus Input Signal

ADVANCE INFORMATION

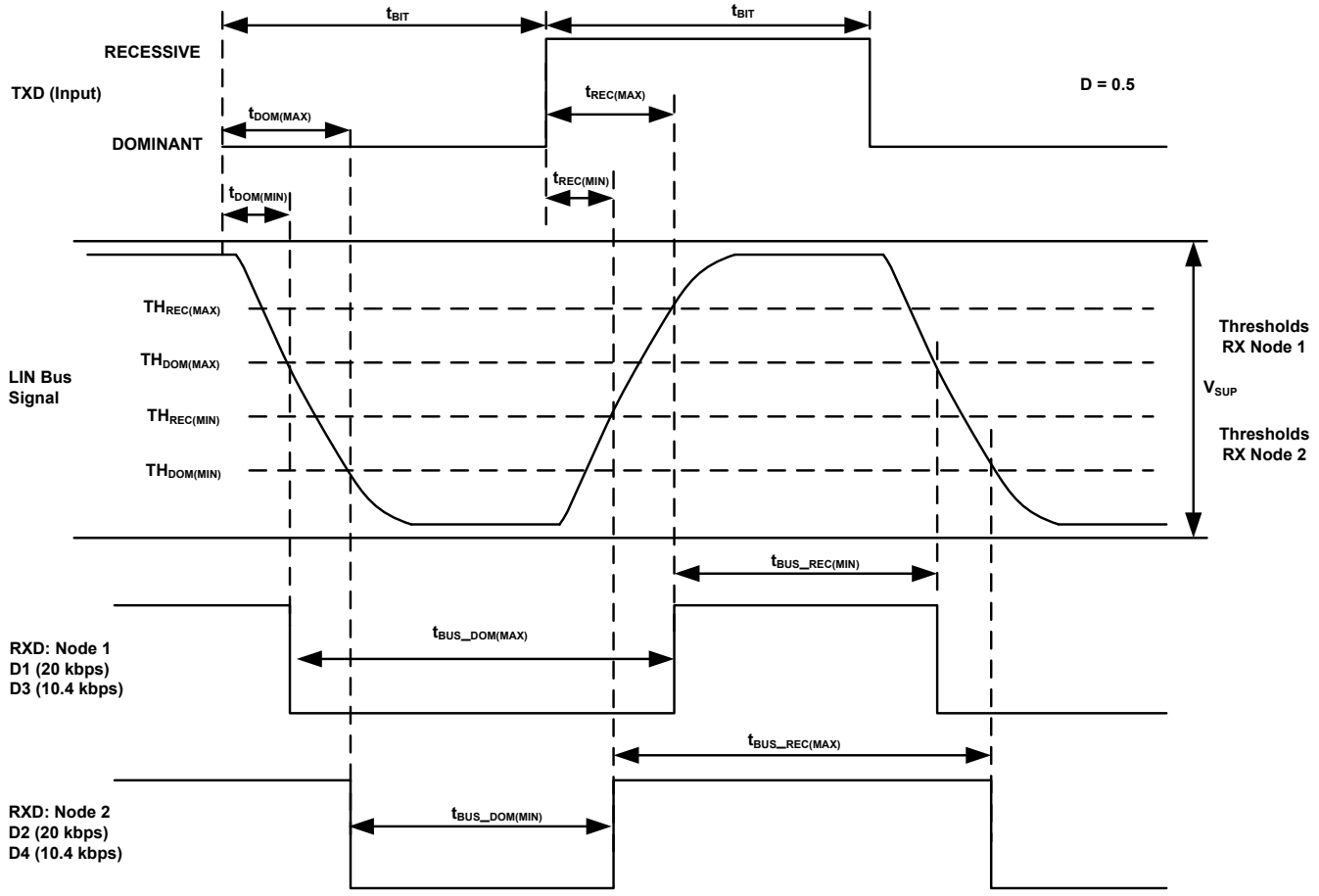


Figure 7-13. Definition of LIN Bus Timing

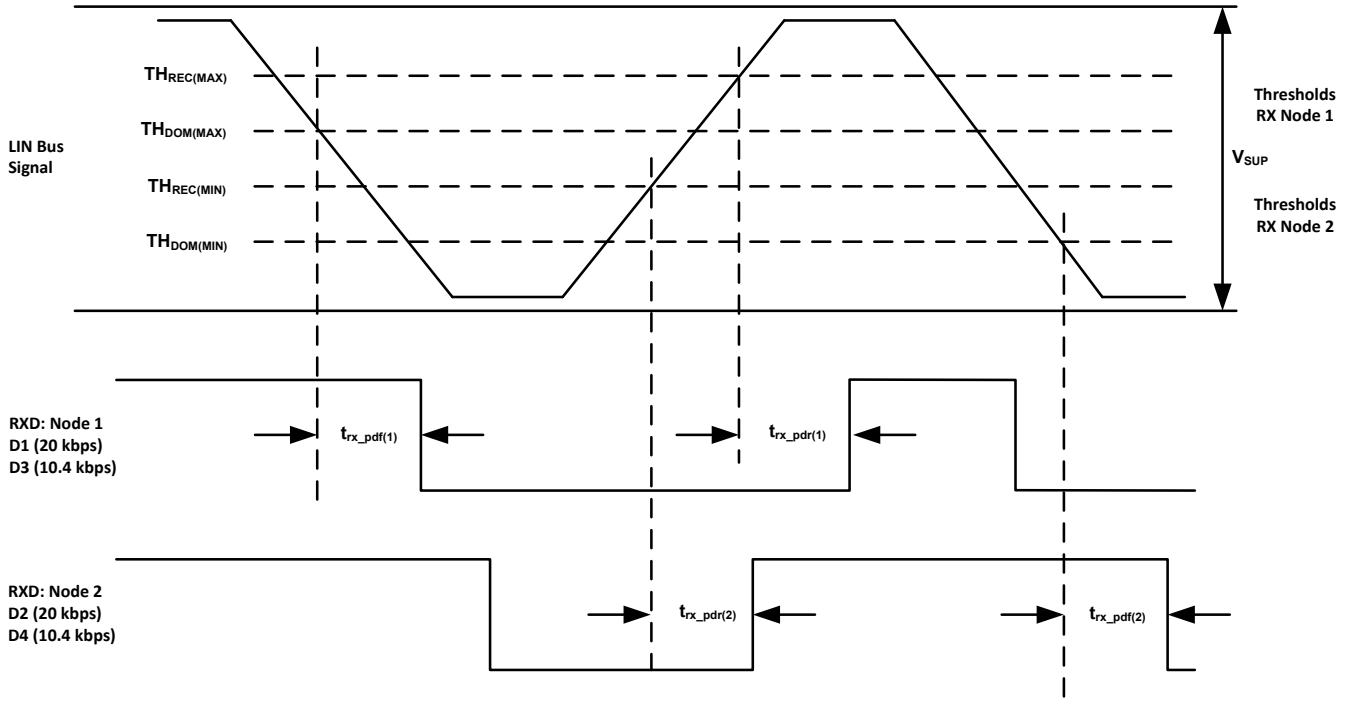


Figure 7-14. LIN Propagation Delay

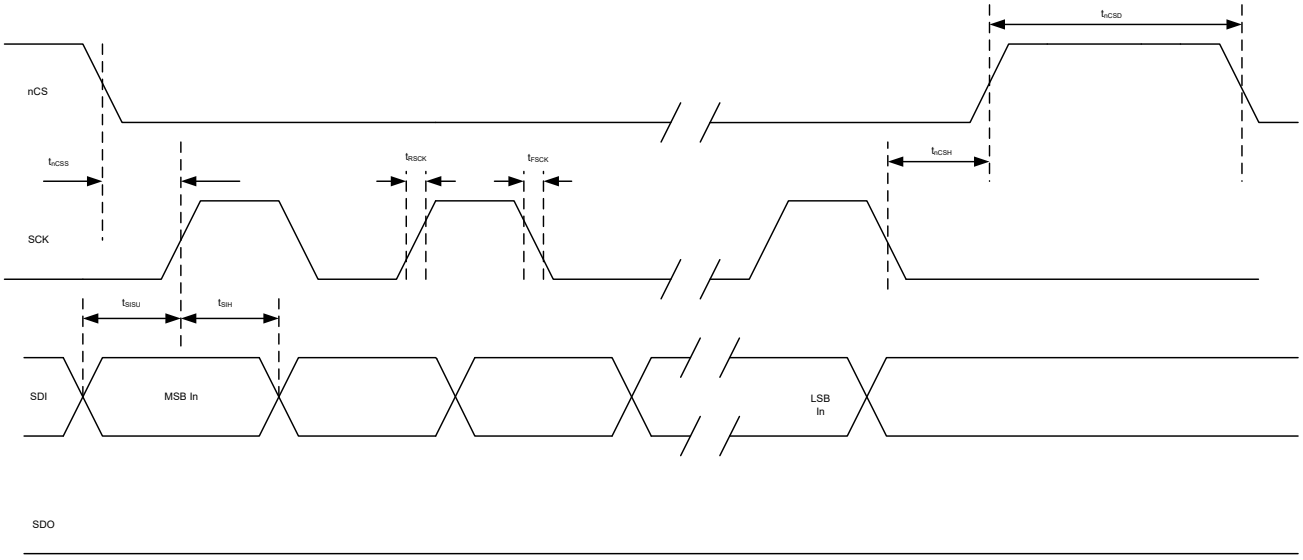


Figure 7-15. SPI AC Characteristic Write

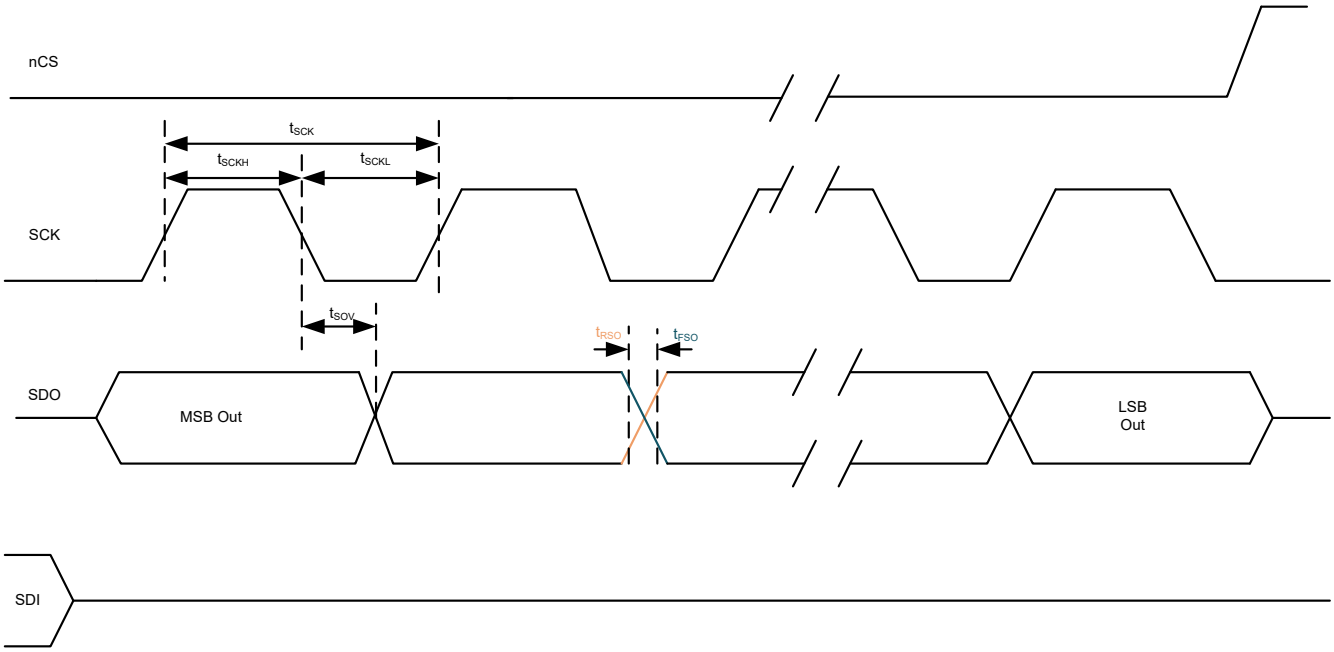


Figure 7-16. SPI AC Characteristic Read

ADVANCE INFORMATION

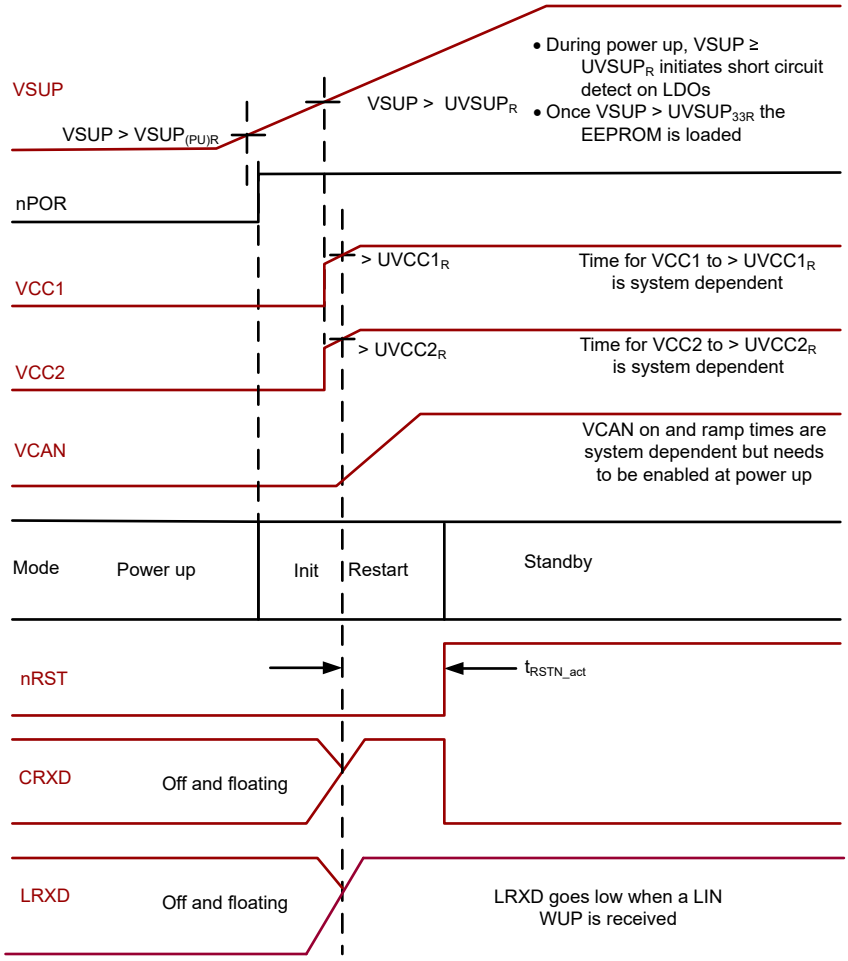


Figure 7-17. Power Up Timing

Note

On initial power up, VEXCC will not turn on as it has not been factory-programmed to do so.

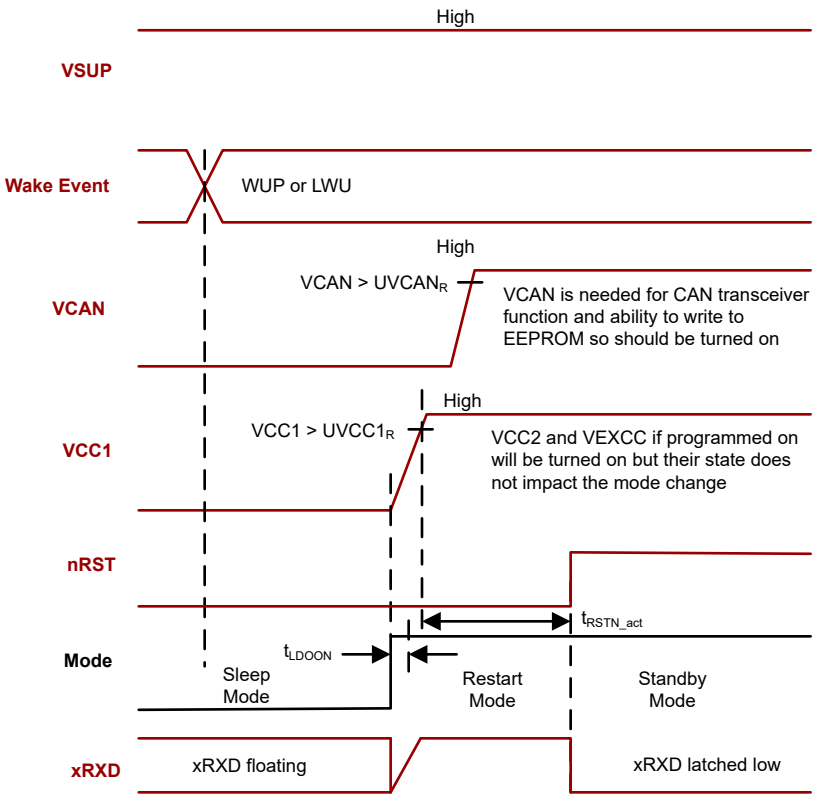


Figure 7-18. Sleep to Restart Timing

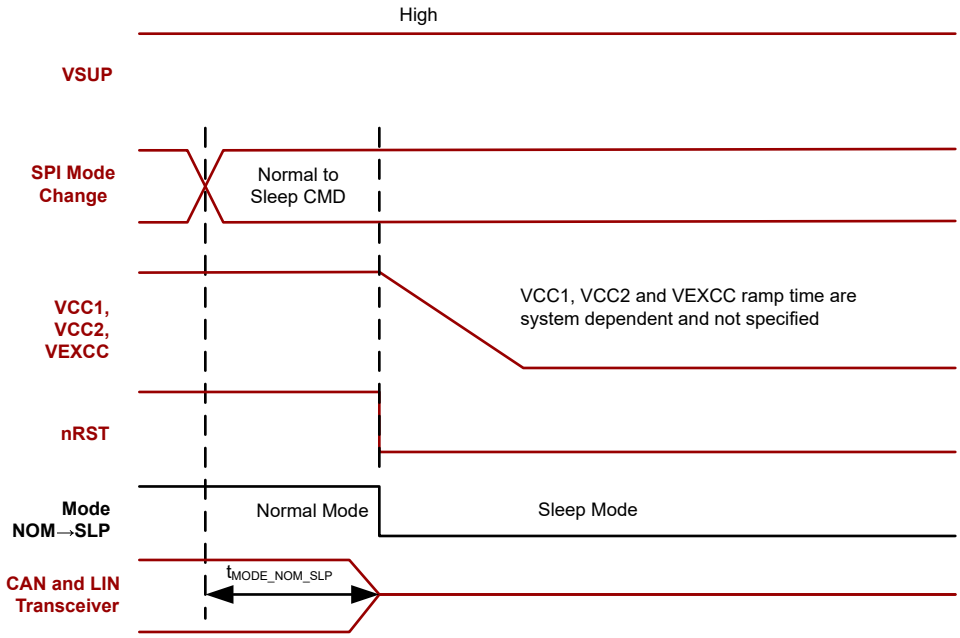


Figure 7-19. Normal to Sleep Timing

Note

The CAN and LIN transceiver can be independently controlled. The timing diagram shown shows the transceivers configured to change states based upon the mode.

ADVANCE INFORMATION

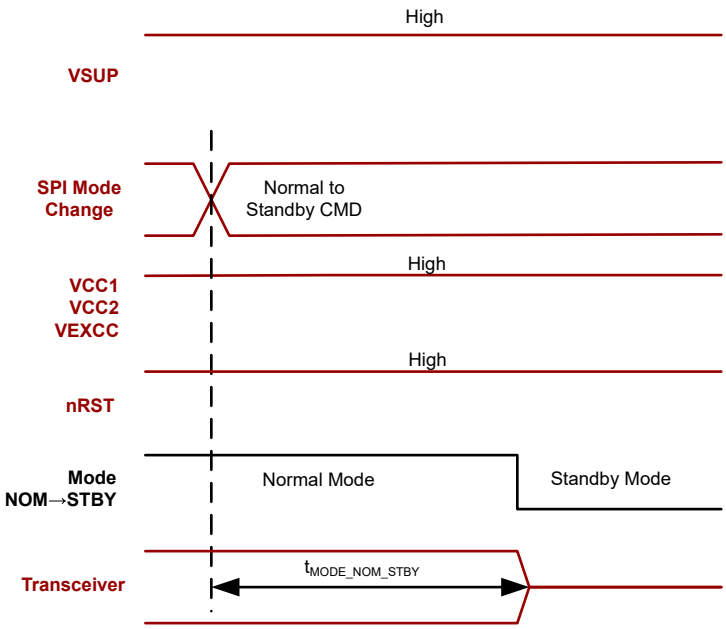


Figure 7-20. Normal to Standby Timing

Note

The CAN and LIN transceiver can be independently controlled. The timing diagram shown shows the transceivers configured to change states based upon the mode.

Note

The red signals are input or output of the TCAN29xx-Q1 and the black signals are internal to the TCAN29xx-Q1. This is for any timing diagram in the data sheet that has red and black colors.

8 Detailed Description

8.1 Overview

The TCAN29xx-Q1 is a family of system basis chips (SBC) that integrate the CAN FD transceiver. The CAN FD transceiver supports data rates up to 5Mbps while meeting the high-speed CAN physical layer standards: ISO 11898-2:2024. The TCAN2957-Q1 integrate a LIN transceiver that supports data rates up to 200kbps when slope control is disabled and programmed for fast mode. The LIN transceiver physical layer transceiver is compliant to LIN 2.2 A and ISO/DIS 17987–4 and SAE J2602 standards. These data rates support end of line programming. The device can also wake up via remote wake up using CAN bus implementing the ISO 11898-2:2024 Wake Up Pattern (WUP). The TCAN29xx-Q1 supports 3.3V and 5V processors based upon VCC1 voltage. The device has a Serial Peripheral Interface (SPI) that connects to a local microprocessor for configuration. The TCAN29xx-Q1 provide a software development pin to help implementer with development. In this mode the watchdog is still active but only sets a flag.

The TCAN29xx-Q1 device family provides VCC1 of either a 3.3V or a 5V output depending upon the orderable part number selected. These devices have a separate 5V LDO, VCC2. The ability to control an external PNP power transistor is provided to support output voltages of 1.8V, 2.5V, 3.3V or 5V at the VEXCC pin. VEXCC output is short to battery protected. A 5V input supply is needed at the VCAN pin for the CAN FD transceiver.

8.2 Functional Block Diagram

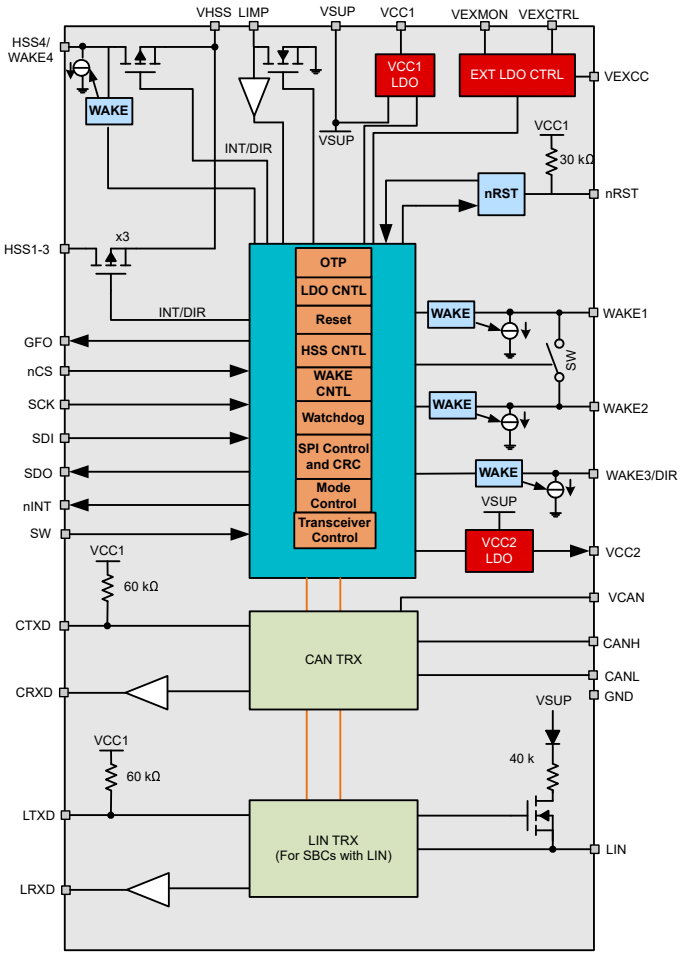


Figure 8-1. TCAN29xx Functional Block Diagram

ADVANCE INFORMATION

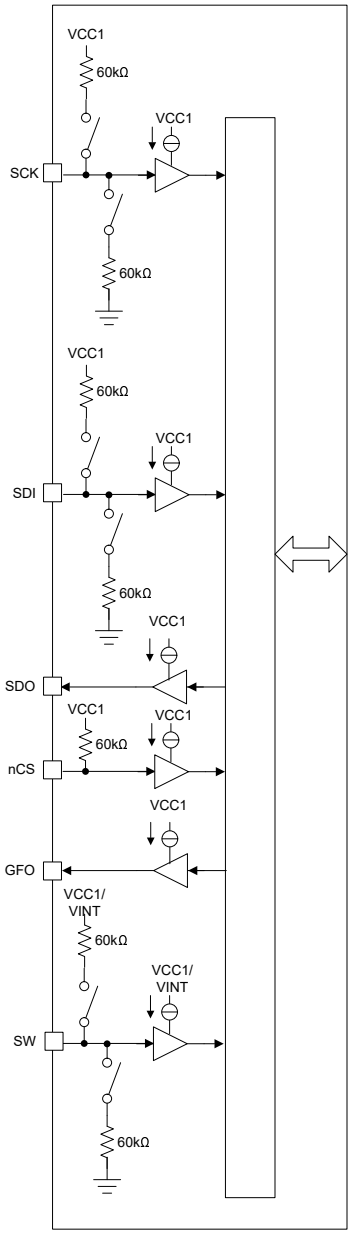


Figure 8-2. Digital Input and Output Block Diagram

8.3 Feature Description

8.3.1 VCC1 Regulator

The VCC1 output pin sources either 3.3V or 5V with load current up to $ICC1_{LIM}$. The VCC1 pin is capable of sinking a current, $ICC1_{SINK}$, depending upon the setting of register VCC1_SINK at 8'h0D[3] and is active when VCC1 is on. Refer to Table 10-1 for the external capacitance requirement on this pin. There are three monitors on VCC1, under-voltage (UVCC1), over-voltage (OVCC1) and short to ground ($VCC1_{SC}$). When load sharing with VEXCC, VCC1 fault monitors are used for both. VCC1 is the main LDO output and sets the digital IO voltage levels. Any fault on VCC1 causes a state change.

8.3.2 VCC2 Regulator

The VCC2 pin provides 5V output with up to 100mA load curent. Refer to Table 10-1 for the external capacitance requirement on this pin. VCC2 must not be taken off board where a short to battery can take place. There are three monitors on VCC2, under-voltage (UVCC2), over-voltage (OVCC2) and short to ground ($VCC2_{SC}$). When

these faults are detected, an interrupt is provided and the LDO may or may not be turned off. No mode change takes place. When VCC2 is on and not in a fault state, register 8'h4F[2], VCC2_STATUS is set to 1b.

8.3.3 VEXCC Regulator

An external PNP can be used to provide VEXCC output in order to reduce internal power dissipation in the device.

- The VEXCC output can support 1.8V, 2.5V, 3.3V and 5V output with up to 350 mA.
- The voltage is selected using SPI register 8'h0D[2:0] and defaults to 1.8V.
- The VEXCC is default off and not turned on until register 8'h0D[5:4] is configured
- VEXCC can be configured as a stand-alone regulator or in a load-sharing mode with VCC1
- Provides current limiting capability with external sense resistor Rshunt
- There are three monitors on VEXCC, under-voltage (UVEXCC), over-voltage (OVEXCC) and short to ground ($VEXCC_{SC}$)
- Regulation status is also reported via register 8'h4F[3], VEXCC_STATUS

The shunt resistor, Rshunt, sets the current limit for the PNP FET. The value for Rshunt must be chosen based on the current limit requirement for the application. The value of this resistor is determined by the VSHUNTH threshold divided by the required current limit, i.e. $VSHUNTH/I_{VEXCC-LIM}$ where $I_{VEXCC-LIM}$ is the required current limit value.

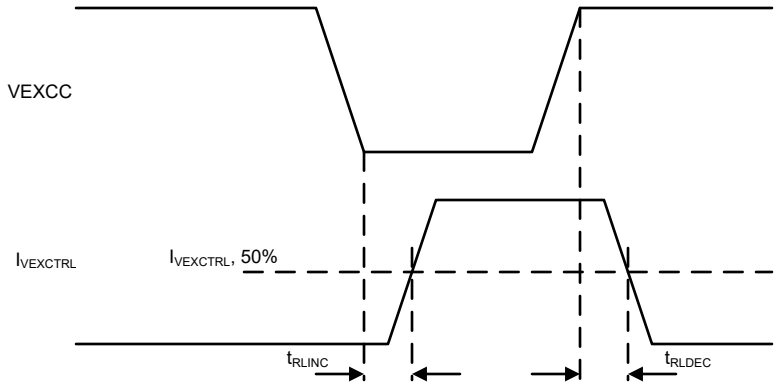


Figure 8-3. VEXCC versus $I_{VEXCTRL}$ Timing Diagarm

Note

- The external PNP transistor power handling capabilities are application specific, and therefore, must be designed according to the selected PNP device along with the PCB properties to prevent thermal damage as the SBC is not able to make sure the thermal protection of the external PNP transistor.
- For limiting current through the external PNP transistor, it is important to connect VEXMON pin to the same power rail that connects to VSUP pin of the device using Rshunt as shown in Figure 8-3.
- If the external PNP collector is being connected to a different voltage rail, the device is not able to provide current limit capability. To avoid issues, the current limit must be disabled by using SBC_CONFIG register 8'h0C[6] VEXCC_ILIM_DIS = 1b. Disabling the current limit does not disable over-voltage, under-voltage, or short circuit detection.

8.3.3.1 VEXCC in Stand-alone Configuration

When used as an stand-alone configuration, see Figure 8-4. VEXCC can be used to power off-board loads e.g. sensors.

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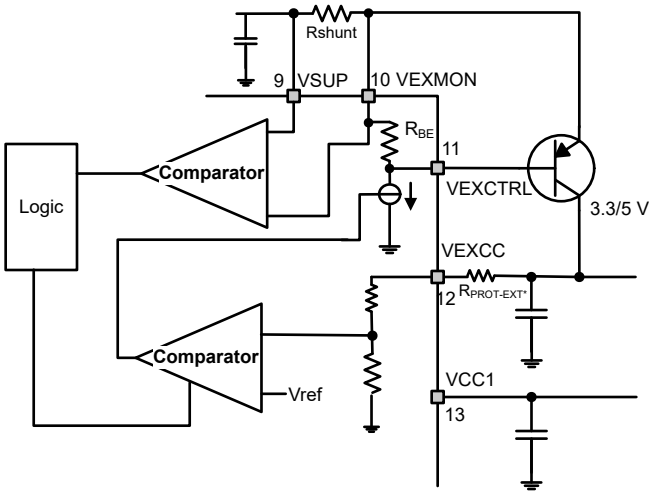

Figure 8-4. Stand-alone External PNP Example

Note

When VEXCC is used to power loads outside the ECUs, a series resistance, $R_{PROT-EXT}$ is recommended to protect against ground shift and for EMC robustness

8.3.3.2 VEXCC in Load-Sharing Conguration with VCC1

When configured for load sharing with VCC1, the ratio of current between VEXCC and VCC1 is determined by the settings in VEXCC_VCC1_LOAD_RATIO bits in register 0x1F. When VEXCC is configured for load sharing, VEXCC must be connected to VCC1 - if not, VCC1 does not startup and the device enters fail-safe mode due to VCC1 not rising above the VCC1SC threshold (short-circuit threshold).

The TCAN29xx-Q1 is not factory-programmed for VEXCC load sharing with VCC1. The device can be programmed for load sharing using the following sequence of steps:

1. Power-up the device with VCC1 shorted to VEXCC on the board; the device powers-up into Standby mode
2. Set VEXCC voltage configuration register, 8'h0D[2:0], to the correct voltage setting. This must be the same as VCC1 setting (3.3V or 5V only)
3. Wait 5ms for output to settle, read VEXCC_STATUS, 8'h4F[3], to confirm VEXCC is in regulation
4. Enable Load Sharing for VEXCC with register 8'h0D[2:0] = 100b
5. VEXT_CFG setting is ignored and VEXCC stays ON in Standby and Normal mode and turns off in Sleep and Fail-safe mode.

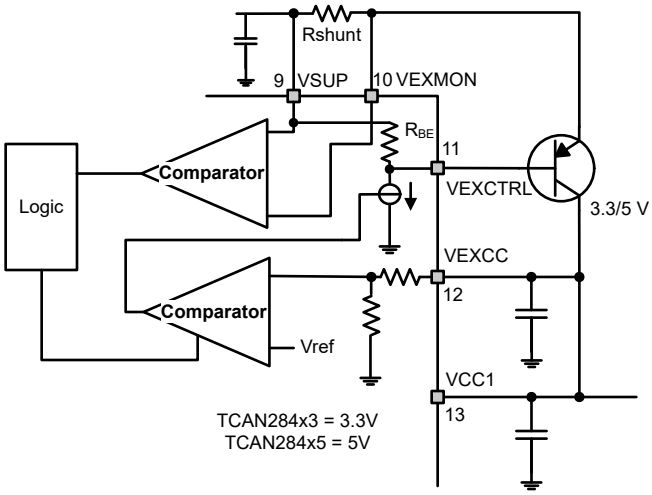

Figure 8-5. External PNP Example with Load Sharing

8.3.3.2.1 VEXCC: Unused Pins Configuration

When VEXCC regulator is not used, it is recommended connection for the pins are as following:

- Connect VEXMON to VSUP; do not leave floating as it can cause increase in quiescent current
- Leave VEXCTRL floating
- Leave VEXCC floating

Do not enable VEXCC via SPI as it leads to increase in quiescent current.

ADVANCE INFORMATION

8.3.4 CAN FD Transceiver

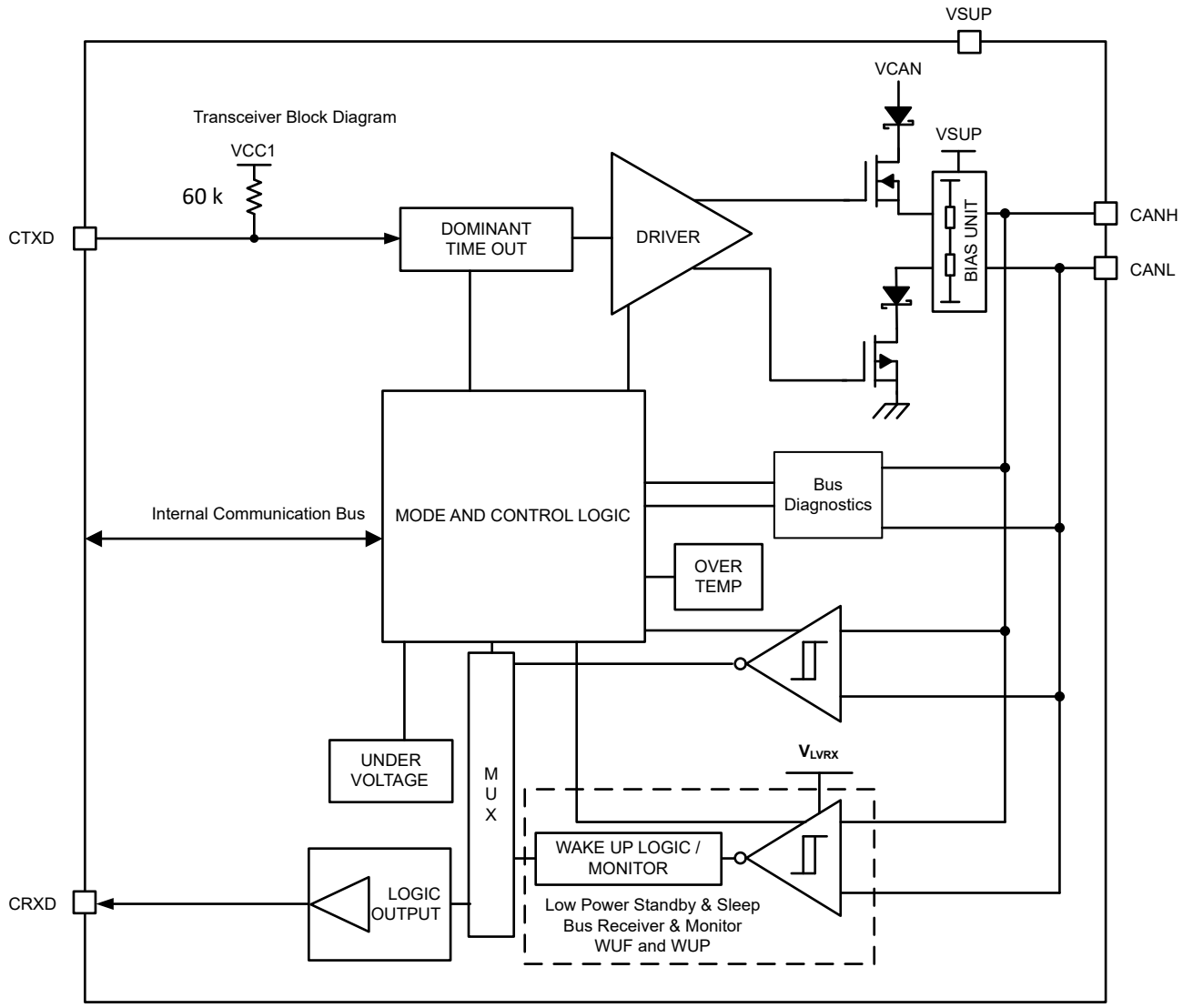

Figure 8-6. CAN FD Transceiver Block Diagram

The CAN FD transceiver can be separately programmed outside of the SBC mode control or tied to the SBC mode control. When tied to the SBC mode control, changing the SBC mode to normal mode will automatically change the transceivers to on. All other states are be wake capable. When programmed separately than the SBC modes, there are certain states that the transceivers cannot be in for the mode. **If a mode change is initiated and the transceiver is not in an allowed state, the mode change does not take place. The MODE_ERR interrupt at 8'h5A[3] is set to 1b.** This includes changing the transceiver configuration to a disallowed state while in the current SBC mode. See Table 8-1 and Figure 8-6 for allowed transceiver configurations for each SBC mode. Here are a few specific cases for consideration.

- A transceiver in Normal mode configured for listen, wake capable and off can transition to standby mode and the state are the same.
- Transitioning to restart mode is wake capable unless the transceiver is programmed off.
- Transitioning from restart mode to standby mode is wake capable unless the transceiver is programmed off.

Note

If the device is in SBC normal mode and the transceivers are programmed on, the TXD pin is checked. If the TXD pin is dominant, the transceiver does not turn on the transmitter until the TXD pin has transitioned to recessive.

The CAN FD transceiver supports off, on, listen and wake capable. The state of the transceiver is programmed using register 8'h10[2:0]. On represents what would be normal mode for a stand-alone transceiver. The CAN transceiver becomes to wake capable when entering fail-safe mode.

The VCAN pin is the 5V supply input for the CAN FD transceiver. VCAN is monitored for under-voltage events, UVCAN. When VCAN is present and not in a fault state, register 8'h4F[1], VCAN_STATUS, will indicate this by being set to 1b. For the CAN FD transceiver to be available VCAN must be present.

Table 8-1. CAN FD Transceiver Programmable State by SBC Mode

SBC Mode	On	Listen	Wake Capable	Off	SBC Mode Control
Normal	✓	✓	✓	✓	On
Standby		✓	✓	✓	Wake Capable
Sleep			✓ default	✓	Wake Capable
Restart			✓ default	✓	Wake Capable
Fail-safe			✓ default	✓	Wake Capable

Note

- When entering SBC restart mode, the transceiver changes wake capable
- When entering SBC fail-safe mode, the transceiver defaults to wake capable.

8.3.4.1 Driver and Receiver Function

The TXD and RXD pins are input and output between the processor and the CAN FD and LIN physical layer transceivers. The digital logic input and output levels for these devices are TTL levels with respect to VCC1 for compatibility with protocol controllers having 3.3V or 5V logic. Table 8-2 and Table 8-3 provides the states of the CAN driver and CAN receiver in each mode.

Table 8-2. Driver Function Table

Transceiver State	TXD Input	Bus Outputs		Driven Bus State
		CANH	CANL	
CAN On	L	H	L	Dominant
	H or Open	Z	Z	Biased Recessive
Wake capable	X	Z	Z	Weak Pull to GND
Off	X	Z	Z	

Table 8-3. CAN Receiver Function Table

Transceiver State	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus States	RXD Terminal
On/Listen	$V_{ID} \geq 0.9V$	Dominant	L
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	H
Wake capable	$V_{ID} \geq 1.15V$	Dominant	See Wake Functions
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \leq 0.4V$	Recessive	
Off	Open ($V_{ID} \cong 0V$)	Open	H

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8.3.4.2 CAN Bus Biasing

Bus biasing can be normal biasing, active in normal mode and inactive in low-power mode. Automatic voltage biasing is where the bus is active in normal mode but is controlled by the voltage between CANH and CANL in lower power modes. See Figure 8-7 for the state diagram on how the TCAN29xx-Q1 performs automatic biasing.

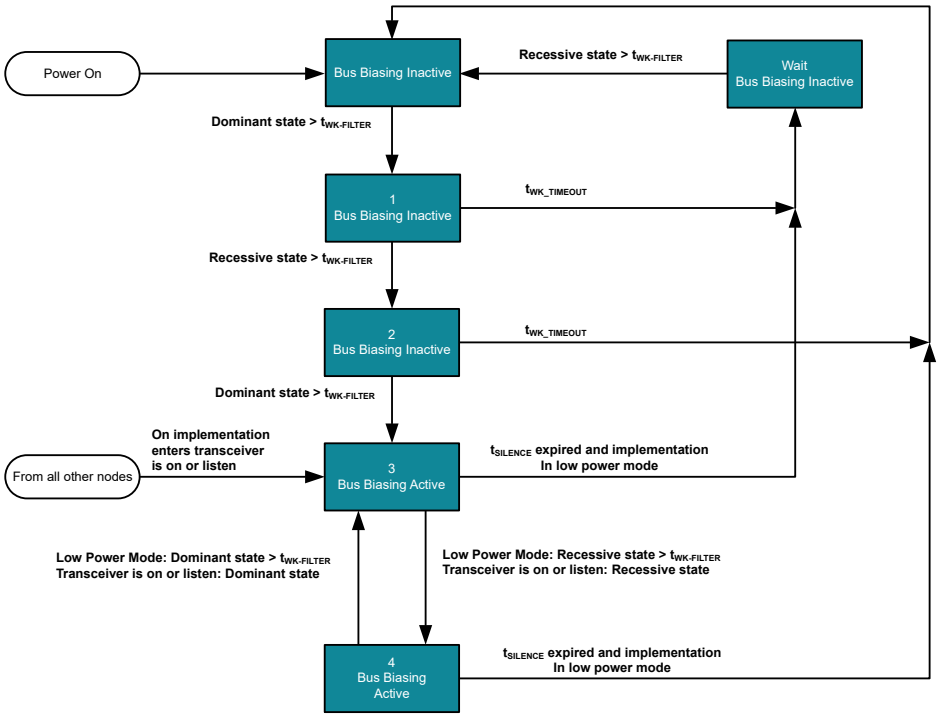

Figure 8-7. Automatic bus biasing state diagram

Note

When entering state 1, the timer, $t_{WK\_TIMEOUT}$, shall be reset and restarted; when entering state 3 or 4, the timer, $t_{SILENCE}$, shall be reset and restarted."

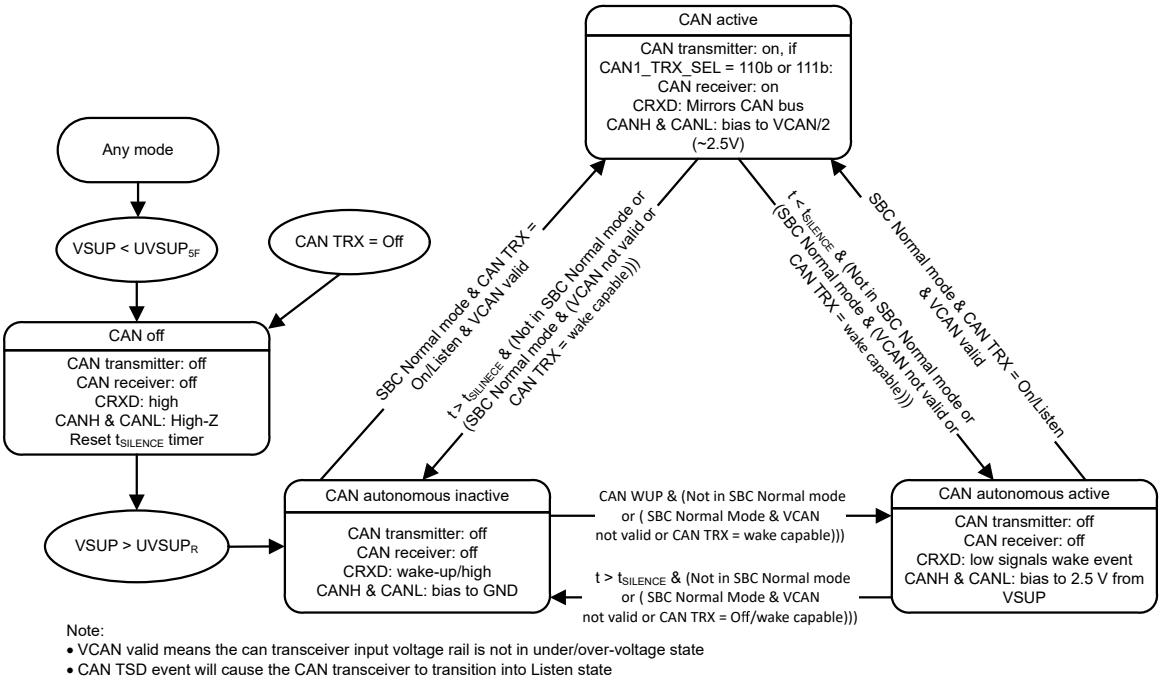

Figure 8-8. Bus biasing

8.3.5 LIN Transceiver

The TCAN2957-Q1 provides a LIN transceiver which supports on, fast, listen, off and wake capable. The state of this transceiver is programmed using register 8'h1D[7:5]. The LIN transceiver becomes wake capable when entering fail-safe mode.

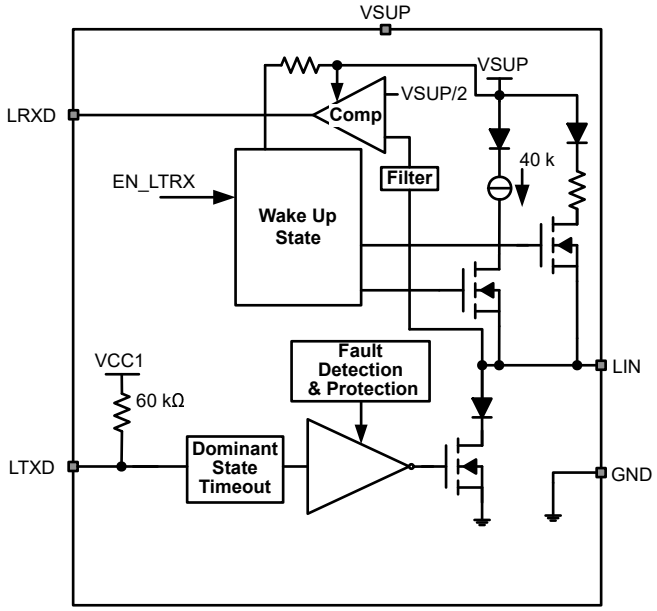

Figure 8-9. TCAN29xx-Q1 LIN Transceiver Block Diagram

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Table 8-4. LIN Transceiver Programmable State by SBC Mode

SBC Mode	On	Fast	Listen	Wake Capable	Off	SBC Mode Control
Normal	✓	✓	✓	✓	✓	On
Standby			✓	✓	✓	Wake Capable
Sleep				✓ default	✓	Wake Capable
Restart				✓ default	✓	Wake Capable
Fail-safe				✓ default	✓	Wake Capable

Note

- When entering SBC restart mode, the transceiver changes to wake capable
- When entering SBC fail-safe mode, the transceiver defaults to wake capable

The LIN pin can survive transient voltages up to 58V. Reverse currents from the LIN to supply (VSUP) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (VSUP). The LIN bus has bus short circuit current limiter shown by I_{BUS_LIM} in the electric specification table.

For the TCAN2947-Q1, the LIN pin is not present and is NU for not used. This pin must not be connected on the board.

8.3.5.1 LIN Transmitter Characteristics

The transmitter meets thresholds and AC parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to VSUP, so no external pull-up components are required for the LIN peripheral node applications. An external pull-up resistor and series diode to VSUP must be added when the device is used for a controller node application. In fast mode the transmitter can support 200kbps data rates.

Table 8-5. Driver Function Table

Transceiver State	TXD Input	LIN Bus Output	Driven Bus State
LIN On	L	L	Dominant
	H or Open	H	Biased Recessive
Wake capable	X	H	
Off	X	Z	

8.3.5.2 LIN Receiver Characteristics

The receiver characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (> 100kbps) than supported by LIN or SAEJ 2602 specifications. This allows the TCAN2957-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system. In fast mode the receiver can support 200kbps.

8.3.5.3 LIN Termination

There is an internal pull-up resistor with a serial diode structure to VSUP, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1kΩ) and a series diode to VSUP must be added when the device is used for commander node applications as per the LIN specification.

Figure 8-10 shows a commander node configuration and how the voltage levels are defined.

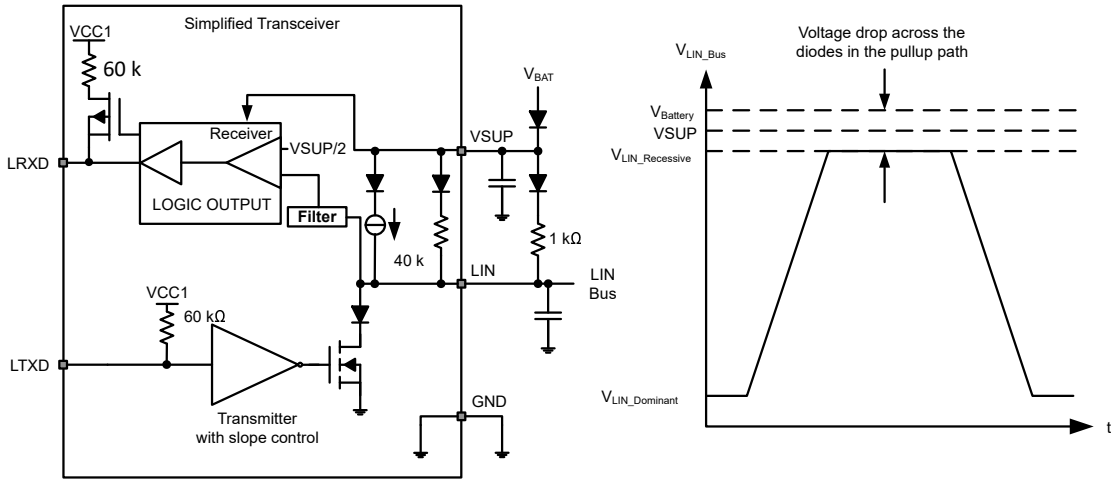

Figure 8-10. Commander node configuration with voltage levels

8.3.6 High-Side Switches

The four integrated high-side switches (HSS1-HSS4) support load current up to $I_{OC(HSS)}$. The control method for each HSSx is accomplished by programming the HSS_CNTL (8'h1E) and HSS_CNTL2 (8'h4D). This control includes any of four PWM settings, two timers, always on/off or direct drive from the WAKE3/DIR pin. The four 10-bit PWMs support 200Hz or 400Hz and can be assigned to any HSSx. To configure PWM3 and PWM4 SBC_CONFIG0 register 8'h0C[5:4] needs to be set to 01b. Once this is set, use the PWM1 and PWM2 configuration registers for programming PWM3 and PWM4. This changes the PWM1 control registers to PWM3 and the PWM2 control registers to PWM4. After configuring the registers, it is best to change 8'h0C[5:4] = 00b; thus, converting the PWM registers back to PWM1 and PWM2. The timers are configured using TIMERx_CONFIG registers 8'h25 and 8'h26.

Any HSS can be connected to any other HSS and synchronized by assigning them the same control mechanism. This allows higher current loads to be used. Assigning PWM1 to HSS1 - HSS4 would synchronize all four high-side switches. Timer1 and Timer2 could be used the same way. For the ability of the MCU to drive the HSSx directly, a direct drive capability using WAKE3/DIR pin is used. The high-side switches and be synchronized using direct drive by programming 1000b to the appropriate HSSx_CNTL fields.

When programing the high-side switches, the following procedure must be used.

- Make sure the selected timer, PWM or direct drive value is at 0.
- Program the selected high-side switch to the desired timer, PWM or direct drive.
  - If multiple HSSx need to be synchrnoized, program the desired HSSx to the same control mechanism (timer/PWM/direct drive).
- For using the timer, program the desired timer period and the ON time. HSSx starts as soon as the on-time is programmed.
- To program the PWM, follow these steps:
  - Program the PWMx_FREQ.
  - Program the PWMx_DC_MSB.
  - Program the PWMx_DC register. **Only after this step, the PWM is programmed**.
    - Any changes to the PWMx_FREQ or PWMx_DC_MSB **must include** programming the PWMx_DC as the last step for the updates to be implemented.
- For direct drive, the device sets the WAKE3_LEVEL at 8'h2B[1:0] VCC1 based input threshold levels to match the output voltage levels of the processor.

When an over-current is detected through an HSS, there is a filter time, t_{OCFLTR}, to determine if over-current is valid. The t_{OCFLTR} can be configure to be a short or long period, configured using register 8'h4F[0]. If the overcurrent condition is valid, a corresponding HSSx over-current interrupt flag is set in the INT_7 register 8'h55, the HSSx is turned off and HSSx_CNTL register is reset to 000b. The HSS is not turned back ON automatically.

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The HSS can be turned ON again after the long t_{OCFLTR} period by writing into the corresponding HSSx_CNTL register. Please note that HSSx over-current flag is not automatically cleared after the fault is cleared.

When an open load fault is detected at an HSS, an interrupt flag is set in the INT_7 register 8'h55. HSS is not turned off due to open load fault. Please note that the open load fault interrupt flags is not automatically cleared after the fault is cleared.

The VHSS pin is also monitored for a high-side switch over-voltage condition based upon OVHSS thresholds. If VHSS exceeds this threshold the high-side switches are turned off. When VHSS drops below this threshold the high-side switches will automatically be enabled to its previous state. Register 8'h4F[7:6] disables the high-side switches from automatically shutting down due to an OVHSS or UVHSS event. HSS_OV_UV_REC, register 8'h4F[5] = 1b enables the high-side switches to go back to the programmed state. If HSS_OV_UV_REC = 0b, the high-side switches stay off due to an over-voltage or under-voltage event on VHSS.

HSS4 can be configured to use one of two timers that allows it to work with WAKE1, WAKE2 and WAKE3 pins supporting cyclic sensing. Cyclic sensing can be used in standby or sleep mode thus reducing mode current due to the HSS being constantly on. Refer to Section 8.3.13.3.2 for further details.

HSS4 pin can also be configured as a wake pin, WAKE4. When configured as WAKE4 pin, HSS4 cannot be used as HSS. In this case, HSS3 will support the cyclic sensing wake function with Timer1 or Timeer2.

Note

- For resistive loads an external capacitor to ground in not required.
- For inductive loads an external 100nF capacitor to ground is needed.
- When using the 10-bit PWM with the HSS it is possible to select values that are unrealizable due to the on and off times of the switch. An example of this would be 00 0000 0001b.

8.3.7 WAKE and Voltage Monitoring Input

WAKE1, WAKE2 and WAKE3/DIR pins are ground biased local wake up (LWU) input pins that are high voltage tolerant. This function is explained further in Section 8.3.13.3. The pins can be both rising and falling edge trigger, meaning it recognizes a LWU on either edge of WAKE pin transition. The pin can be configured to accept a pulse, see Figure 8-23 for timing diagram of this behavior. The WAKE pins are default enabled but can be disabled by using register 8'h2A[7:5], WAKE_PIN_SET, to turn off individual ones. Register 8'h11[7:6] sets the method the pins will use to register a wake event. These pins can be configured for cyclic sensing wake, see Section 8.3.13.3.2, or static wake.

The WAKE pins have four individual thresholds that can be set for a state change.

- Register 8'h12[1:0], WAKE1_LEVEL
- Register 8'h2B[5:4], WAKE2_LEVEL
- Register 8'h2B[1:0], WAKE3_LEVEL

Note

If WAKEx_LEVEL = 10b or 11b is selected and uses static wake, the system designer needs to make sure that VSUP does not cross the wake pin threshold; otherwise, a false wake up can take place. Normal undervoltage events on VSUP does not cause this to take place.

Register 8'h2A[4:0], MULTI_WAKE_STAT, provides which WAKE pin or combination of WAKE pins caused the LWU event. The individual status of the pins, low or high, can be read via SPI in any mode that SPI is available.

- Register 8'h11[5], WAKE1_STAT
- Register 8'h2B[6], WAKE2_STAT
- Register 8'h2B[2], WAKE3_STAT

8.3.7.1 WAKE Pins Alternate Configurations

WAKEx pins can be programmed to provide alternate features. When these pins are configured for the alternate functionality, the local wake up functionality is not available.

8.3.7.1.1 V_{BAT} monitoring

WAKE1 and WAKE2 have an internal switch between them that allows a V_{BAT} monitoring capability. This is accomplished by programming the WAKE_PIN_CONFIG1 register 8'h11[4] WAKE_VBAT_MON to 1b = On, see Figure 8-11. This closes the switch and disables WAKE1 and WAKE2 functionality. Refer to Table 10-1 for the values of R_{WK-BAT} and the resistors R_{DIV1} and R_{DIV2}.

The WAKE1 and WAKE2 pins are capable of working with voltages up to 40V, which allows a high enough voltage onto the WAKE2 pin that the processor pin connected to the WAKE2 pin can be damaged. To avoid this, the OVHSS parameter can be used to turn off the switch. The WAKE1_SENSE bit at WAKE_PIN_CONFIG2 register 8'h12[6] is a dual function register bit. When WAKE_VBAT_MON = 0b the WAKE1_SENSE bit determines whether WAKE1 pin is a static wake input or cyclic wake input. When WAKE_VBAT_MON = 1b the WAKE1_SENSE bit becomes OV_WAKE12SW_DIS. When OV_WAKE12SW_DIS = 0b, the TCAN29xx-Q1 turns off the switch between WAKE1 and WAKE2 when HVSS reaches the OVHSS limit.

This switch is active in Normal and Standby modes (if enabled) and the switch is disabled in Sleep and Fail-safe modes.

Refer to Table 10-1for the recommended values of external components

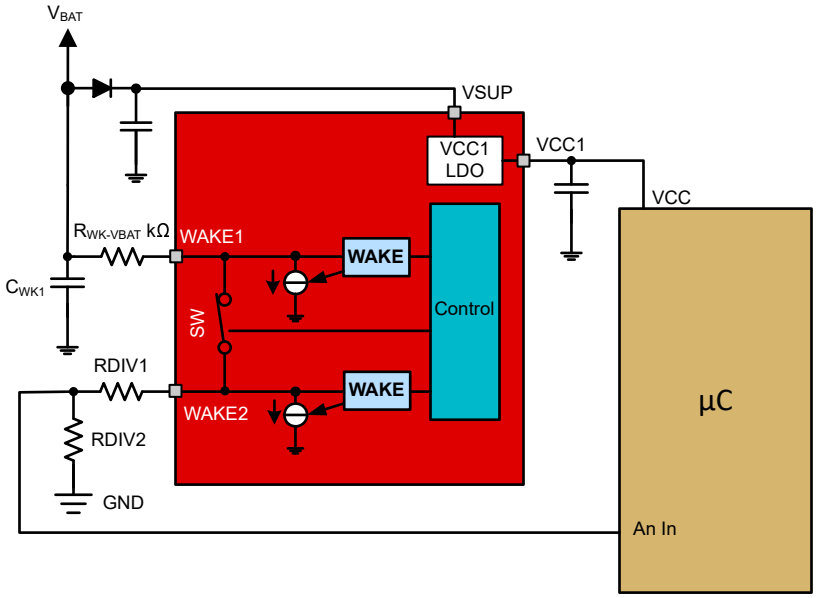

Figure 8-11. V_{BAT} Monitoring Circuit

8.3.7.1.2 Direct Drive

WAKE3/DIR pin can be programmed to directly control any or all of the high-side switches, HSSx, see Figure 8-12. This is accomplished by programming the HSS_CNTLx registers at 8'h1E and 8'h4D to 1000b = Direct Drive pin control for each selected HSSx. This disables the WAKE3 functionality. When using direct drive, there is an enable and disable time based upon the edge change on the WAKE3/DIR pin. This is a power savings feature and shown in Figure 8-13.

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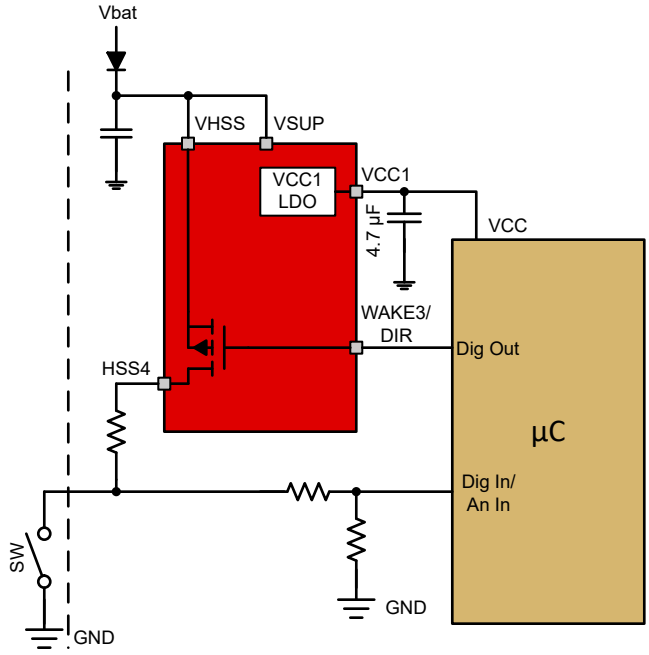

Figure 8-12. HSS4 Direct Drive Example

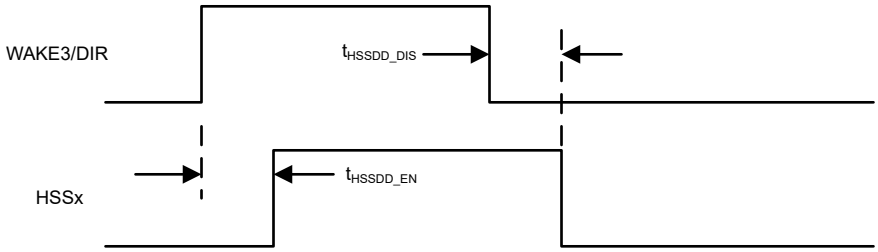

Figure 8-13. Direct Drive Enable and Disable Timing

8.3.7.1.3 Using Wake Pins For Hardware ID Function

Wake pins can also be configured for performing hardware based ID (identification) function by tying the pins to GND or battery terminal to encode ECU location in the vehicle. This alternate configuration is available only to WAKE1-3 pins. This configuration is not available to the WAKE4 pin.

To use the ID function:

- Set IDx_EN=1b
  - This disables the wake function on the corresponding wake pin
- After t_{d_IDSTAT}, the pin connection status is reflected at the IDx_STAT register to indicate whether the pin is connected to GND or VBAT
  - The device uses WAKEx_LEVEL threshold settings to determine the pin is above the VIH threshold (connected to VBAT) or below the VIL (connected to GND) threshold.
- Disabling the ID function by setting IDx_EN=0b resets the IDx_STAT bits to 00b (Unkown)

8.3.8 nRST Pin

The nRST pin is a bi-directional open-drain low side driver that serves several functions, an LDO monitor output for under-voltage events, an indicator to the processor that restart has been entered and a device input reset. nRST is connected to VCC1 through a pull-up resistor, see Figure 8-14.

When a VCC1 under-voltage (UVCC1) event takes place, the device transitions to restart mode and nRST pin is latched low. The nRST pin returns to logic high level with a delay of t_{RSTN_act} after VCC1 rises above UVCC1xR threshold.

If the device enters Restart mode due to a watchdog failure, the pin is pulled low for t_{NRST_TOG}. After this time the device transitions to standby mode and nRST returns to high.

The pin can determine when an input pulse of t_{NRSTIN} is applied causing the device to reset the registers to factory default and enters restart mode.

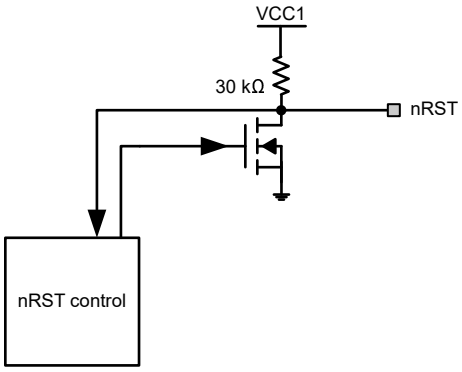

Figure 8-14. nRST Block Diagram

8.3.9 LIMP Output

The LIMP pin is for the limp home function and is an open-drain, active low, output. It is used for a limp home mode if the watchdog has timed out causing a reset. The pin must be pulled up with an external resistor connected to the battery supply, VSUP. For the LIMP pin to be turned off, the watchdog error counter must reach zero from correct input triggers. If programmed any event that triggers the fail-safe mode will also turn on the LIMP pin. The state of this pin can be read back by setting DEVICE_CONFIG register 8'h1A[6] LIMP_RD_EN to 1b. The state of the LIMP pin active (on) or inactive (off) can be read back from LIMP_STATE at 8'h1A[5].

8.3.10 Interrupt Function

The nINT pin is the interrupt output pin of the device to be connected to the processor. When the TCAN29xx-Q1 requires the attention of the processor, this pin is pulled low. After the interrupt is cleared and the nINT pin is released back to high a 1ms delay will take place before another interrupt can take place and latch the nINT pin low again.

This pin is the interrupt output pin to the processor. When the TCAN29xx-Q1 requires the attention of the processor, this pin is pulled low. After the interrupt is cleared and the nINT pin is released back to high, a 1ms delay takes place before another interrupt can take place and latch the nINT pin low again.

The interrupt block is designed as a push-pull output stage referenced to VCC1 supply. When the TCAN29xx-Q1 requires the attention of the processor due to any interrupt-generating event (any unmasked interrupt signalled in the interrupt registers), this pin is pulled low. After the interrupt is cleared the nINT pin is released back to high. A 1ms delay will take place before another interrupt can take place and latch the nINT pin low again.

The nINT pin can be configured to toggle instead of being latched low by writing a 1b to nINT_TOG_EN bit at register 8'h1B[0], see Figure 8-15

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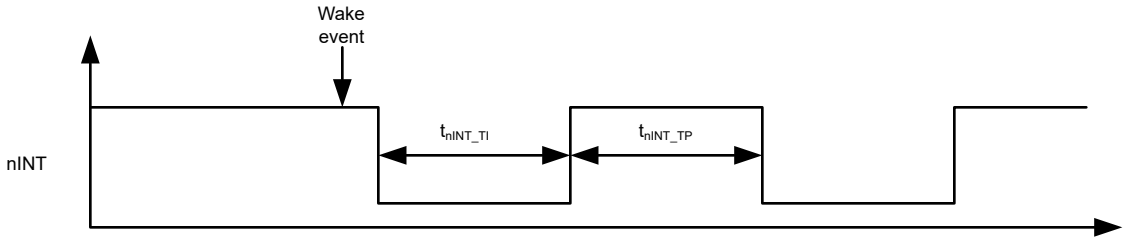

Figure 8-15. nINT Toggling Timing

By default, nINT pin is a global interrupt indicator and is activated for any unmasked interrupt in the interrupt registers 8'h51-8'h55, 8'h5A and 8'h5C. If desired, specific interrupts can be masked such that those interrupts do not activate the nINT pin. The interrupts can be masked using the interrupt enable bits in the registers 8'h51-8'h55, 8'h5D and 8'h60.

All interrupts are stored in the respective interrupt registers until cleared by writing 1b (W1C) via SPI.

8.3.11 SW Pin

During debug or development this pin can be used to disable the watchdog actions. When the pin is active:

- The device expects normal WD triggers, but ignores any mode changes or actions outside of setting the watchdog failure interrupt flag and incrementing and decrementing the watchdog counter.
- CAN transceiver is set to ON
- LIN transceiver (device variants with LIN) is set to ON

When the pin is released:

- The watchdog interrupt flags self-clear, and the watchdog counter either goes back to default or programmed value.
- CAN and LIN transceivers change their mode back to the programmed value

The pin is default active high but can be configured active low by using register 8'h0E[0] = 0b.

When the device is in sleep or fail-safe mode, this pin can be used as a digital wake up pin by enabling this feature using register bit SW_WAKE_EN (8'h0E[1]). When the device wakes up due to a SW pin state change, SWPIN interrupt at 8'h51[1] will be set. If VCC1 is present (Standby and Normal modes), the thresholds are based on VCC1 levels. If VCC1 is not present (Fail-safe mode), the thresholds are based off an internal voltage rail, $V_{IHSWINT}$ and $V_{ILSWINT}$. This pin can then be used to wake up the SBC using an external CAN FD or LIN transceiver or MCU's GPIO pin. This can be accomplished in several ways. If the external transceiver has an inhibit pin, external circuitry can be used to provide a wake input to this pin. The processor can connect directly to this pin and initiate the wake up without using a SPI command.

Figure 8-16 provides a state diagram on how the SW pin behaves.

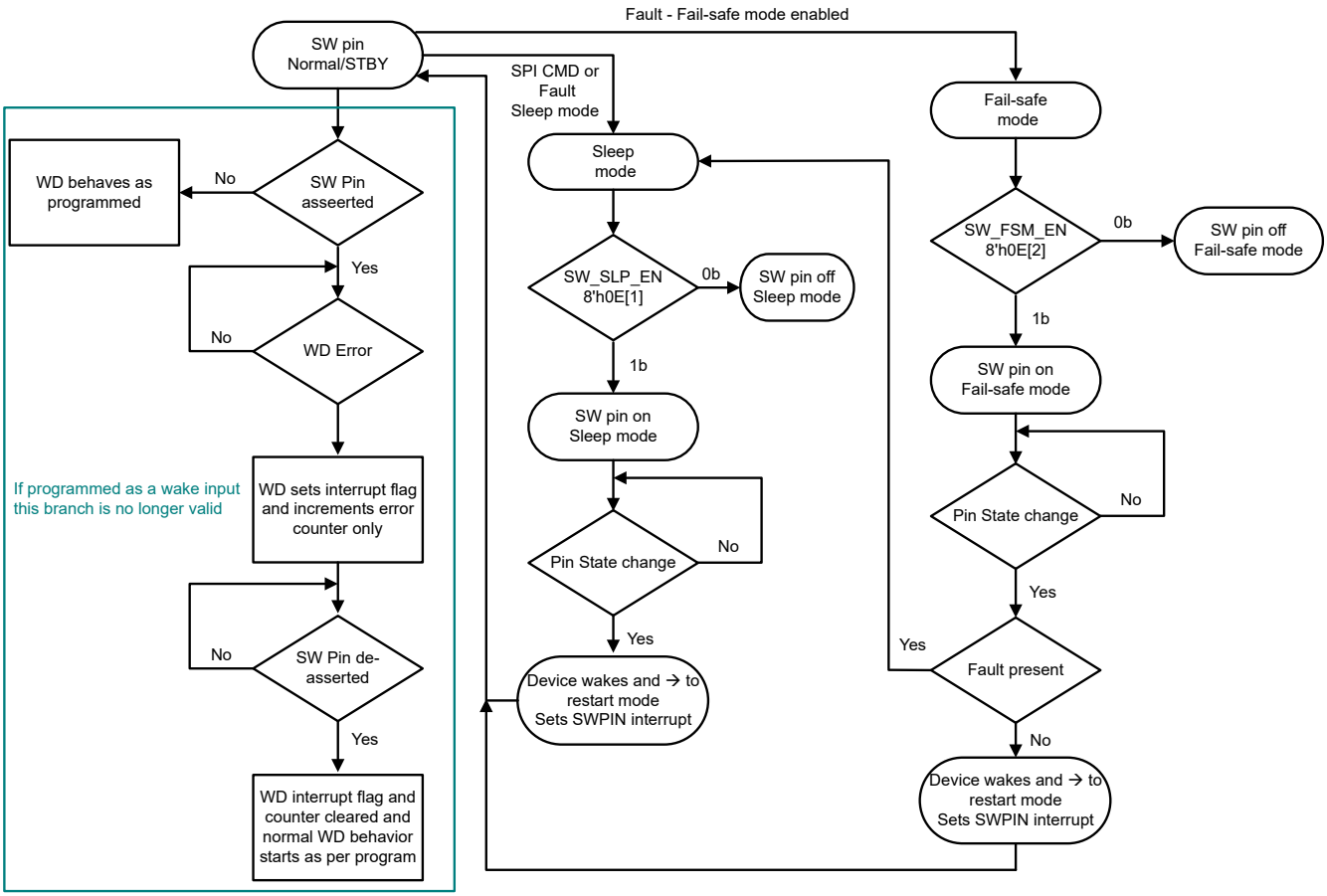

Figure 8-16. SW Pin State Diagram

Note

- The SW pin has a filter timer that the state change has to be at least t_{SW} = 140µs
- The pull-up and pull-down resistor is self-configured based upon register 8'h0E[0] setting. Active high means pull-down active, active low means pull-up active.
- If the device is powered up with the SW pin connected high, the device treats this as no watchdog actions to take place.

8.3.12 GFO Pin

This pin is can be programmed to provide certain information back to the processor. These can be considered interrupts such as a UVCC1 or watchdog failures. The pin can be configured to state which wake event has taken place, bus or local via WAKE pin. Configurable to indicate device has entered fail-safe mode.

Pin can also be configured to act as an enable pin to control an external LIN or CAN transceiver. This is accomplished by configuring the pin to support the correct polarity and then programming the external device mode.

8.3.13 Wake Features

There are multiple ways to wake up from sleep mode.

- CAN bus wake using BWRR
- LIN bus wake (for device versions with LIN)
- Local wake up through the WAKEx pins
- SW pin if programmed as a digital wake input
- Cyclic wake enabled for sleep mode

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Note

- A wake event that takes place prior to the device going to sleep will be treated as a wake event which will prevent the device from entering sleep mode.
- When VCC1 is off in sleep mode, for a wake event, the device to follow the normal wake flow
- When VCC1 is on in sleep mode, for a wake event, the device will set an interrupt, pull RXD low, and perform the programmed VCC1_SLP_ACT at SBC_CONFIG1 register 8'h0E[5]. As SPI will be available, it will be possible to change modes without VCC2 or VEXCC being turned on.
- In the case of cyclic wake event in Sleep mode, VCC1_SLP_ACT configuration has no effect and the device will transition to Stanby mode via Restart mode

  irrespective of the VCC1_SLP_ACT configuration.

8.3.13.1 CAN Bus Wake via CRXD Request (BWRR) in Sleep Mode

The TCAN29xx-Q1 supports low power sleep and standby modes and uses a wake up from the CAN bus mechanism called bus wake via CRXD Request (BWRR). Once this pattern is received, the TCAN29xx-Q1 automatically switches to standby mode from sleep mode and insert an interrupt onto the nINT pin, if enabled, to indicate to a host microprocessor that the bus is active, and the processor should wake up and service the TCAN29xx-Q1. The low power receiver and bus monitor are enabled in sleep mode to allow for CRXD Wake Requests via the CAN bus. A wake-up request is output to the CRXD (driven low) as shown in Figure 8-17. The external CAN FD controller monitors CRXD for transitions (high to low) and reactivate the device to normal mode based on the CRXD Wake Request. The CAN bus terminals are weakly pulled to GND during this mode, see Figure 7-2.

This device uses the wake-up pattern (WUP) from ISO 11898-2: 2024 to qualify bus traffic into a request to wake the host microprocessor. The bus wake request is signaled to the integrated CAN FD controller by a falling edge and low corresponding to a “filtered” bus dominant on the CRXD terminal (BWRR).

The wake-up pattern (WUP) consists of

- A filtered dominant bus of at least t_{WK_FILTER} followed by
- A filtered recessive bus time of at least t_{WK_FILTER} followed by
- A second filtered dominant bus time of at least t_{WK_FILTER}
- A second filtered recessive bus time of at least t_{WK_FILTER} (for CAN-FD SIC version of the device only)

Once the WUP is detected, the device starts issuing wake up requests (BWRR) on the CRXD pin. The behavior of this pin is determined by register 8'h12[2]. If 8'h12[2] = 0b the CRXD pin is pulled low once the WUP pattern has been received that meets the dominant, recessive, dominant filtered times. The first filtered dominant initiates the WUP and the bus monitor is now waiting on a filtered recessive, other bus traffic does not reset the bus monitor. Once a filtered recessive is received, the bus monitor is now waiting on a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon receiving of the second filtered dominant the bus monitor recognizes the WUP and transition to BWRR output. Immediately upon verification receiving a WUP the device transitions the bus monitor into BWRR mode. This is indicated on the CRXD pin by latching it low, thus the CRXD output during BWRR matches the classical 8 pin CAN devices that used the single filtered dominant on the bus as the wake-up request mechanism from ISO 11898-2: 2024.

For a dominant or recessive to be considered “filtered”, the bus must be in that state for more than t_{WK_FILTER} time. Due to variability in the t_{WK_FILTER} the following scenarios are applicable.

- Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and thus no BWRR is generated.
- Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a BWRR may be generated.
- Bus state times more than $t_{WK\_FILTER(MAX)}$ is always detected as part of a WUP; thus, a BWRR is always generated.

See Figure 8-17 for the timing diagram of the WUP. Additionally, the TCAN295x-Q1 family of devices support the extended WUP pattern based on the configuration of register bit CAN_WUP_PATTERN. See Figure 8-18 for the timing diagram.

The pattern and t_{WK_FILTER} time used for the WUP and BWRR prevents noise and bus stuck dominant faults from causing false wake requests while allowing any CAN or CAN FD message to initiate a BWRR. If the device is switched to normal mode or an under-voltage event occurs on V_{CC} the BWRR is lost. The WUP pattern must take place within the $t_{WK\_TIMEOUT}$ time; otherwise, the device is in a state waiting for the next recessive and then a valid WUP pattern.

If 8'h12[2] = 1b, the CRXD pin toggles low too high too low for t_{TOGGLE} = 10 µS until the device is put into normal mode or listen mode. BWRR is active in standby mode upon power up and once coming out of sleep mode or certain fail-safe mode conditions. If a SPI write puts the device into standby mode, the CRXD pin is high until a wake event takes place. The CRXD pin then behaves like it would when in sleep mode.

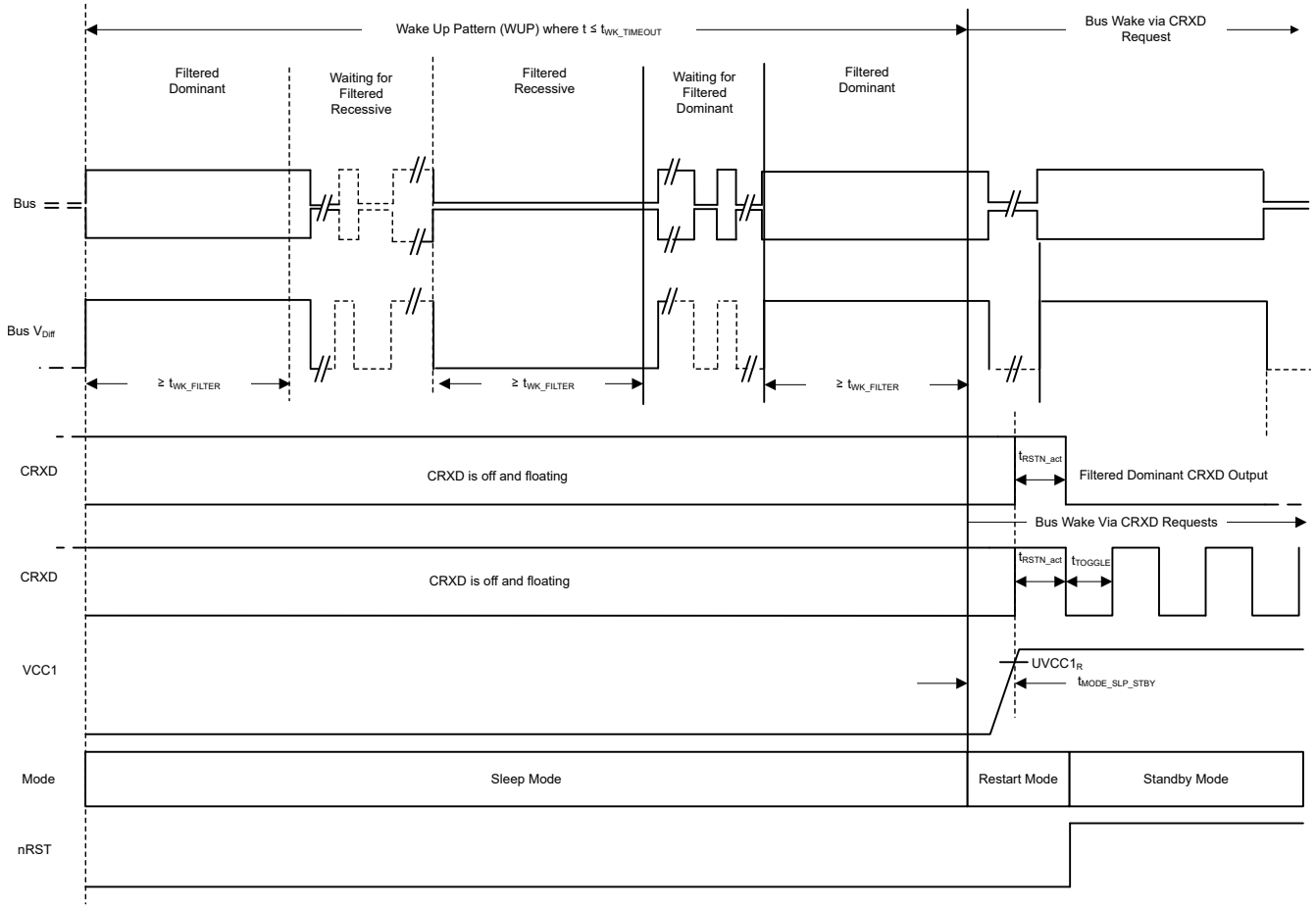

Figure 8-17. Wake Up Pattern (WUP) and Bus Wake via CRXD Request (BWRR) with CAN_WUP_PATTERN=0b

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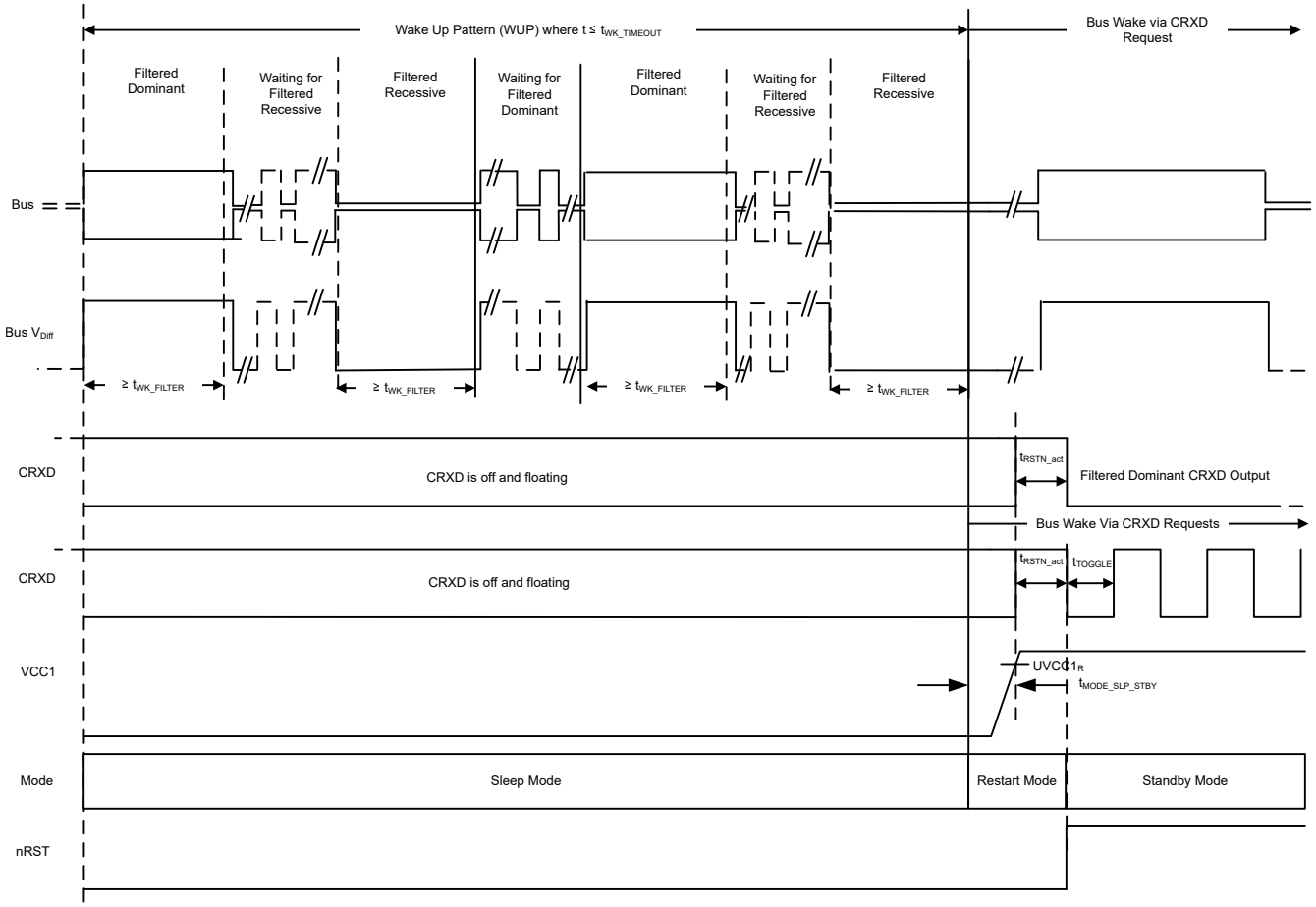

Figure 8-18. Extended Wake Up Pattern (WUP) and Bus Wake via CRXD Request (BWRR) with CAN_WUP_PATTERN=1b

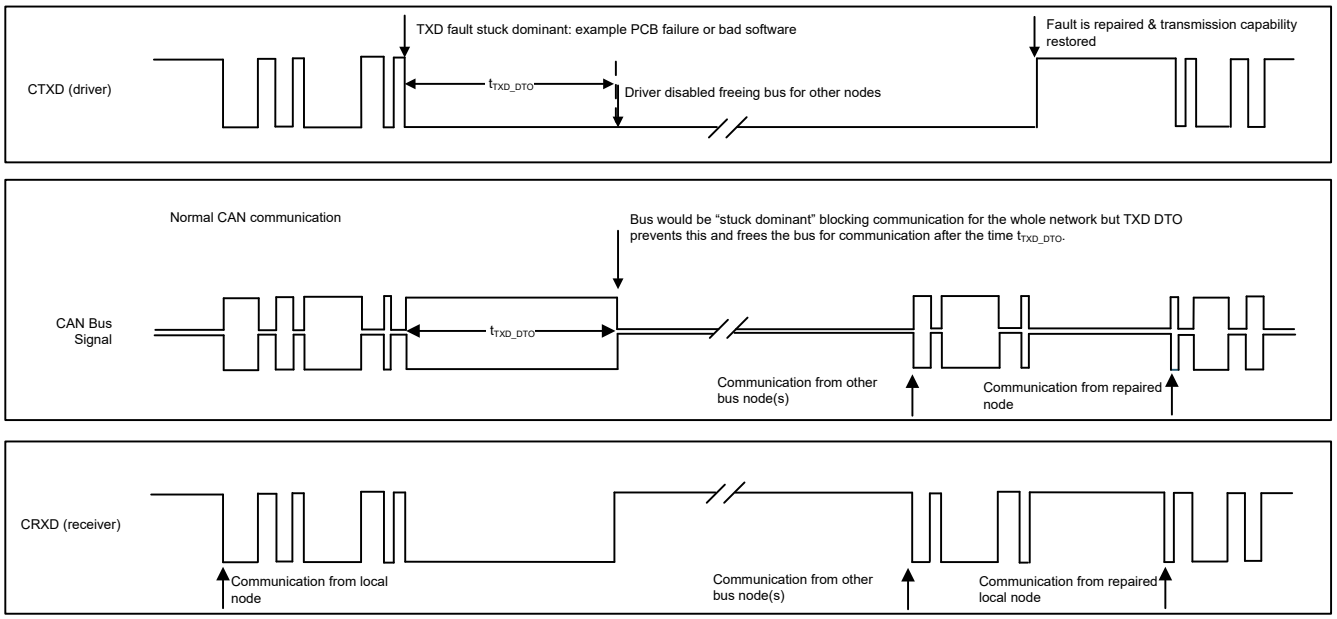

Figure 8-19. Example timing diagram with CTXD DTO

Note

CAN wake from WUP signal can be disabled by programming CAN1_TRX_SEL at register 8'h10[2:0] = 010b.

8.3.13.2 LIN Bus Wake

Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on the LIN bus where the dominant state is held for the t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground. The LIN bus wake event is indicated by LRXD being pulled low once the device enters standby mode.

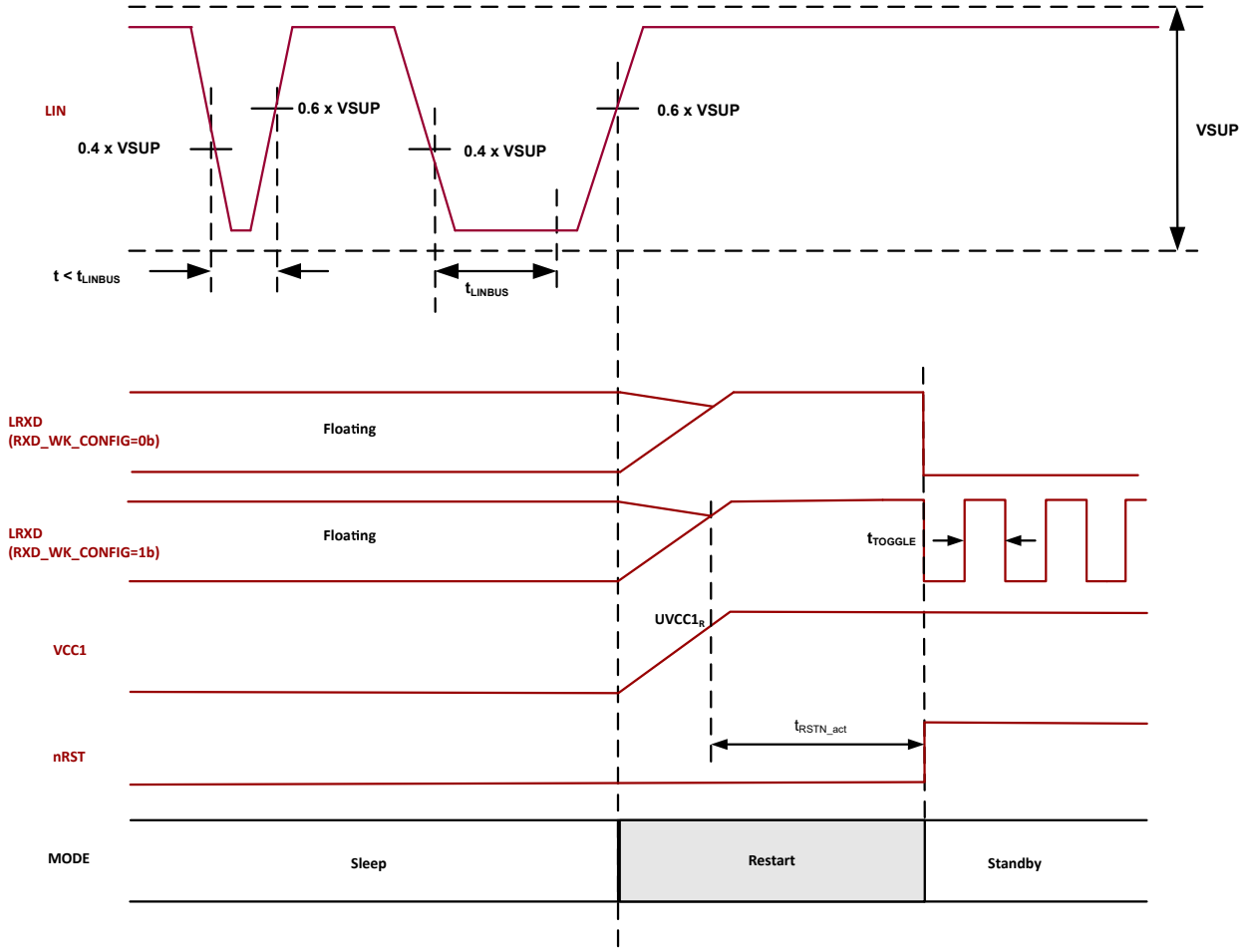

Figure 8-20. LIN bus wake

8.3.13.3 Local Wake Up (LWU) via WAKEx Input Terminal

The WAKEx terminals are a highly configurable ground based, high voltage capable inputs which can be used for local wake up (LWU) request via a voltage transition. There are two methods for this wake event. A static wake based on a level changed on the pin or a timing based, cyclic sensing where the WAKEx pin is periodically turned on and a change during this on time is the trigger event is checked.

The device provides a WAKE pin status change update using reg 2Ah[4:0] showing which WAKE pin has changed states.

There are two methods of utilizing the WAKE pins:

- Static wake

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- Cyclic sensing wake

The WAKE pins have a global control for which method a wake takes place, rising edge, falling edge, bi-directional, pulse or filtered pulse. The WAKE pins have programmable thresholds

8.3.13.3.1 Static Wake

The WAKEx pins default to bi-directional input but can be configured for rising edge and falling edge transitions, see Figure 8-21 and Figure 8-22, by using WAKE_CONFIG register 8'h11[7:6]. WAKE pins are ground based wake inputs and can be used with a switch to ground or V_{SUP}. The WAKEx pins input thresholds can be based on VCC1 levels which would allow a direct connection to the processor or a switch to the VCC1 rail. If the terminal is not used, it must be connected to ground to avoid unwanted parasitic wake up. Once the device enters sleep mode the WAKEx terminals voltage level need to be at either a low state or high state for t_{WAKE} before a state transition for a WAKE input can be determined. A pulse width less than $t_{WAKE\_INVALID}$ is filtered out.

The LWU circuitry is active in sleep mode, standby mode and transition state off going to sleep. If a valid LWU event occurs the device transitions to standby mode. The LWU circuitry is not active in normal mode.

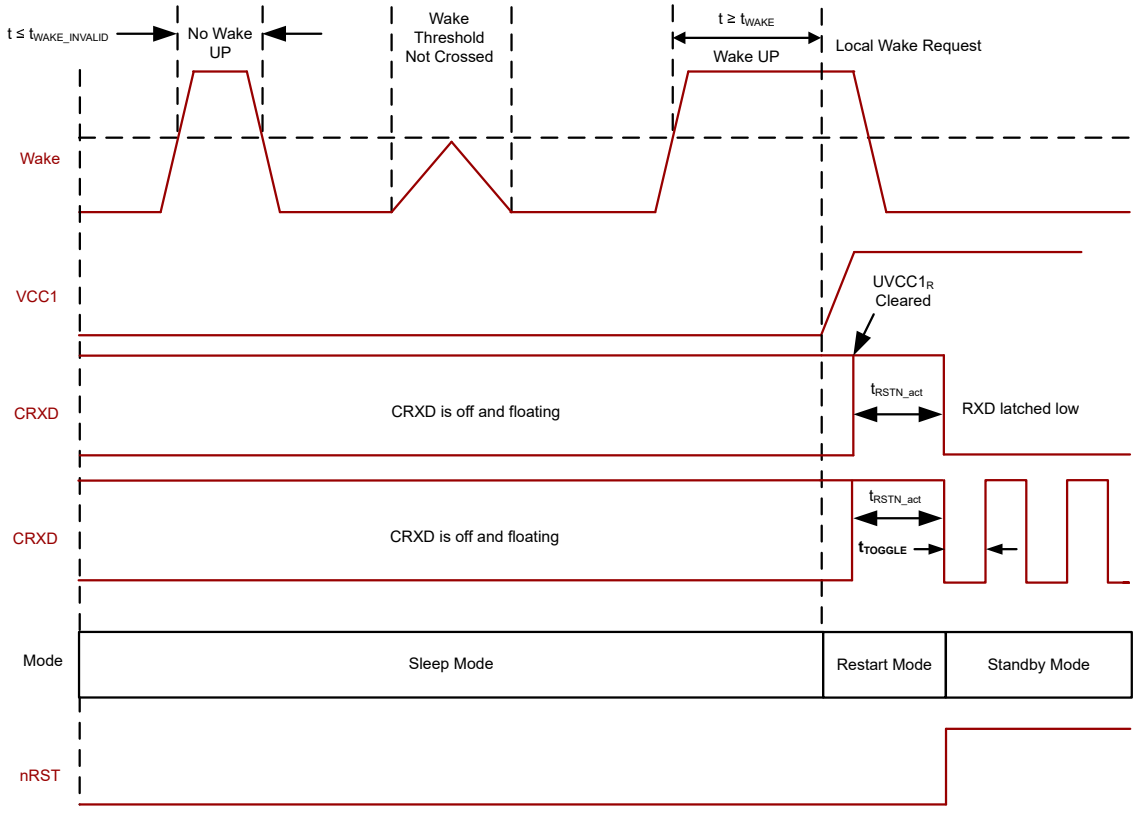

Figure 8-21. Local Wake Up – Rising Edge

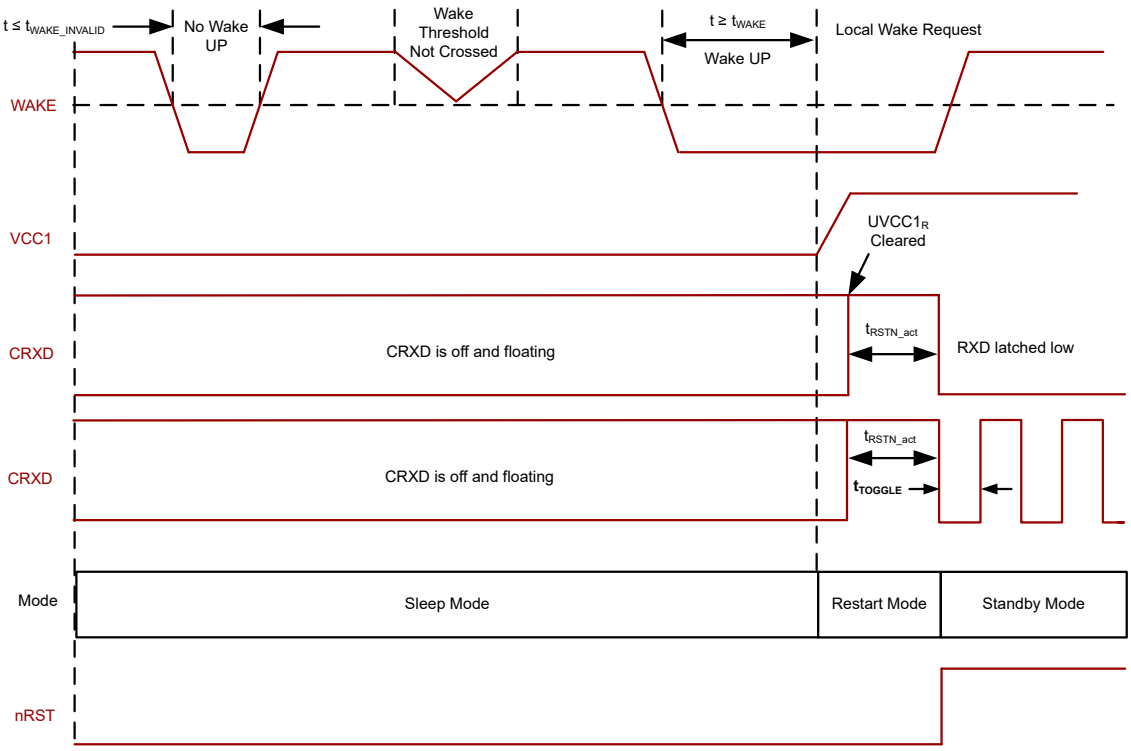

Figure 8-22. Local Wake Up – Falling Edge

Note

When either a rising or falling edge is selected for the WAKE pins the state prior to the edge requires a t_{WAKE} period of time.

- If a rising edge is selected and the device goes to sleep with WAKE high, a low of at least t_{WAKE} must be present prior to the rising edge wake event
- If a falling edge is selected and the device goes to sleep with WAKE low, a high of at least t_{WAKE} must be present prior to the falling edge wake event
- This requirement is not necessary for a bidirectional edge (default)
- Figure 8-21 and Figure 8-22 provide examples of a rising or falling edge WAKE input. RXD is pulled low once VCC1 > UVCC1 and standby mode is entered.

The WAKE terminal can be configured for a pulse, see Figure 8-23, by using WAKE_CONFIG register 8'h11[7:6]. The terminal can be configured to work off a pulse only. The pulse must be between $t_{WK\_WIDTH\_MIN}$ and $t_{WK\_WIDTH\_MAX}$. This figure provides three examples of pulses and whether the device will wake or not wake. $t_{WK\_WIDTH\_MIN}$ is determined by the value for $t_{WK\_WIDTH\_INVALID}$ is set to in register 8'h11[3:2]. There are two regions where a pulse may or may not be detected. By using register 8'h1B[1], WAKE_WIDTH_MAX_DIS, the pulse mode can be configured as a filtered wake input. Writing a 1 to this bit will disable $t_{WK\_WIDTH\_MAX}$ and the WAKE input is based upon the configuration of register 8'h11[3:2] which selects a $t_{WK\_WIDTH\_INVALID}$ and $t_{WK\_WIDTH\_MIN}$ value. A WAKE input of less than $t_{WK\_WIDTH\_INVALID}$ is filtered out and if longer than $t_{WK\_WIDTH\_MIN}$ the device will enter restart mode and turn on the LDOs. The region between the two may or may not be counted, see Figure 8-24. Register 8'h12[7] determines the direction of the pulse or filter edge that is recognized. The status of the WAKE pin can be determined from register 8'h11[5:4]. When a WAKE pin change takes place the device will register this as a rising edge or falling edge. This is latched until a 00 is written to the bits.

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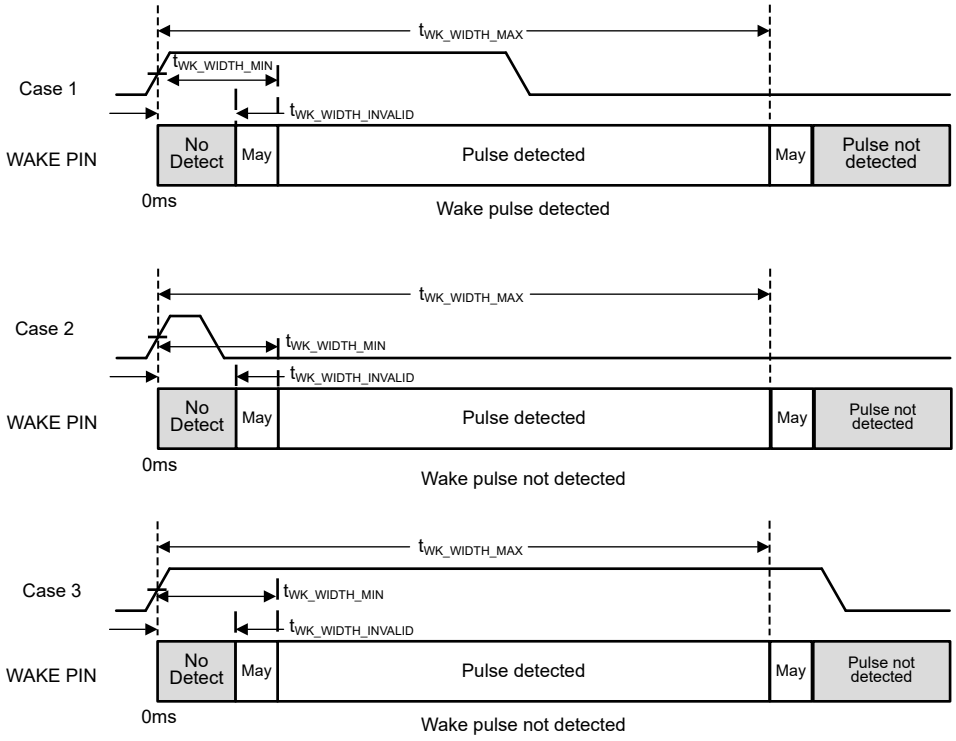

Figure 8-23. WAKE Pin Pulse Behavior

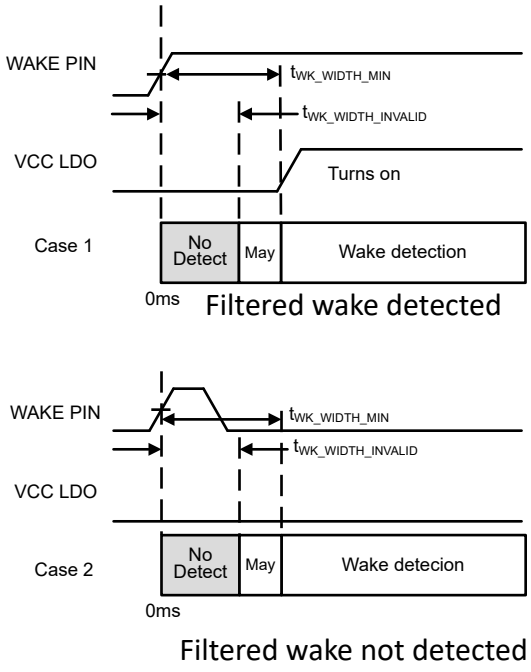

Figure 8-24. WAKE Pin Filtered Behavior

8.3.13.3.2 Cyclic Sensing Wake

When using cyclic sense WAKE, the quiescent current of the device in sleep mode is reduced as the WAKE circuitry is only active during the on time of the selected HSS4 pin, see Figure 8-25 as an example. Periodically the HSS4 pin turns on applying VSUP to the external local wake circuitry. Each time, WAKEx sets a bit stating the pin is high or low and compares the bit to the previous state. If there has been a change, then the device

wakes up; otherwise, the device remains in sleep mode. See Figure 8-26 for a timing diagram. The wake time is based upon t_{WK_CYC} as shown in Figure 8-26. The period and pulse width are determined by register 8'h12[5].

If HSS4/WAKE4 pin is configured to be used as a wake pin, HSS3 must be used as the high-side switch for cyclic sensing function.

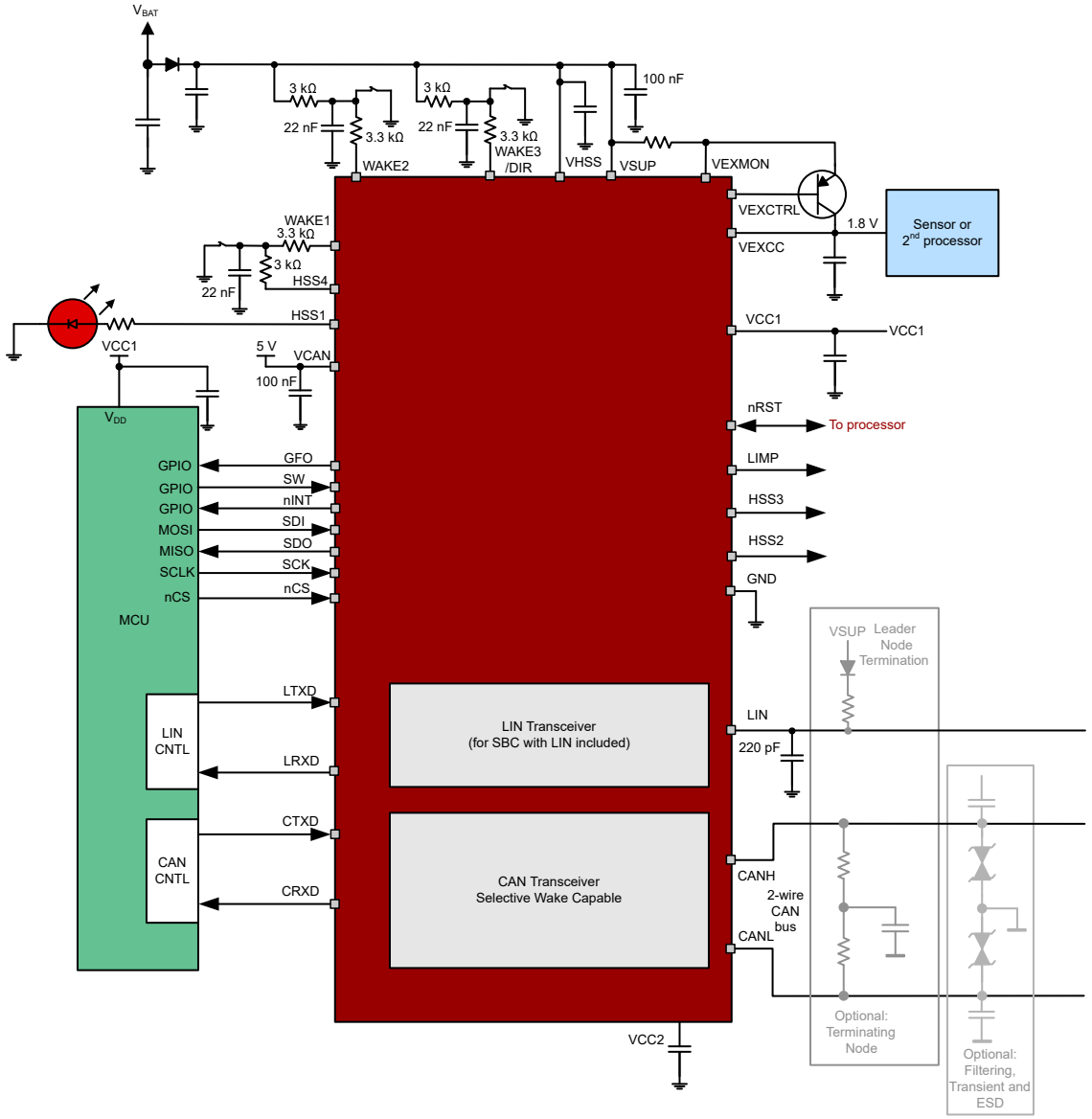

Figure 8-25. Application drawing with cyclic sensing configuration

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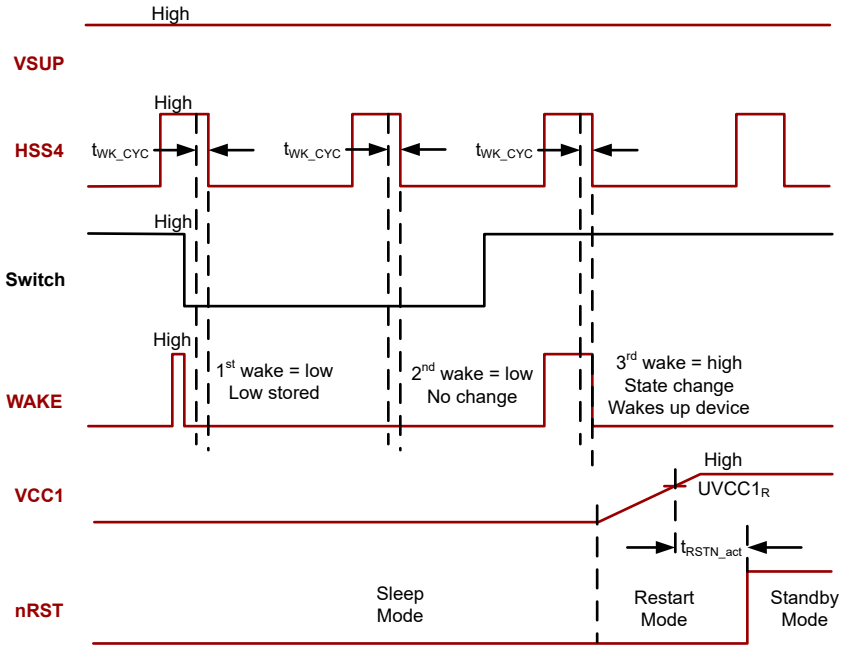

Figure 8-26. Cyclic sensing timing diagram

8.3.13.4 Cyclic Wake

Cyclic Wake is similar to cyclic sensing wake in that it uses Timer1 or Timer2 to periodically wake. This feature is available in Normal and Standby modes. When enabled, at the start of the programmed on time, the device will pull nINT low for programmed-on time and release. The first on time pulse is ignored but each afterward causes the interrupt. Cyclic wake is enabled by using register 8'h25[3] for Timer1 or 8'h26[3] for Timer2. See Table 8-6 for registers used to program cyclic wake feature. Timers are configured using their registers.

Table 8-6. Cyclic Wake Registers

Address	Default	Field	Description
8'h25[3]	0b	TIMER1_CYC_WK_EN	Setting to 1b associates the cyclic wake timer to Timer1
8'h26[3]	0b	TIMER2_CYC_WK_EN	Setting to 1b associates the cyclic wake timer to Timer2

Note

- By configuring Cyclic Wake to Timer1 or Timer2, the device performs the cycle wake function in Normal and Standby mode.

For longer duration cyclic wake or cyclic wake function in Sleep mode, refer to the Long Duration Timer section.

8.3.13.5 Direct Drive in Sleep Mode

Direct drive is where the high-side switch is controlled directly from the WAKE3/DIR pin of the device. This is configured by assigning direct drive to any combination of high-side switches. See Section 8.3.7.1 for how this feature is implemented. Direct drive does not wake the device, but methods to wake the device are provided.

- As VCC1 is on when using direct drive, SPI commands can be used to wake the device up from sleep mode.
- Configure SW pin as a digital wake input by setting SW_SLP_EN to 1b in register SBC_CONFIG1 8'h0E[1].
- An unused WAKE1 or WAKE2 pin can be used to wake the device by the processor. The pin thresholds have to be configured to meet the processor requirements.

8.3.14 Long Duration Timer

TCAN29xx-Q1 features a long duration timer (LDT) that can be programmed to perform various pre-configured actions when the timer expires. The LDT can be configured in Normal or Standby modes. The timer provides 16 pre-set duration options with maximum duration of 7 days.

To activate the LDT:

- Select the LDT_FUNCTION (Register 0x1C[2:1])
- Set the timer duration using LDT_TIMER_SET (Register 0x1C[6:3])
- Set LDT_EN=1b

Refer to the table below for the LDT_FUNCTION configuration and the corresponding actions performed

The timer is reset and disabled if the device enters Restart or Fail-safe mode. The timer needs to be reconfigured again after the device enters Standby or Normal mode.

Table 8-7. Long Duration Timer Function

LDT_FUNCTION	SBC Normal or Standby mode	SBC Sleep Mode
00b	Timer starts as soon as LDT_EN is set to 1b in the SBC Normal or Standby mode. After the timer expires, an interrupt is generated and nINT goes low if the interrupt flag is not masked.	No entry to Sleep mode after the timer expires
01b	Timer starts as soon as LDT_EN is set to 1b in the SBC Normal or Standby mode. After the timer expires, the device enters Sleep mode if there are no other pending wake interrupts. LDT interrupt is set.	Device stays in Sleep mode unless a wake event wakes up the device into Standby mode
10b	Timer can be configured and enabled in SBC Normal or Standby mode. Timer does not start until Sleep mode is entered.	The timer starts when the device enters Sleep mode via SPI command. After the timer expiry, the device wakes up into Standby mode and sets LDT_WAKE interrupt to dincate the timer based wake up
11b	Timer starts as soon as LDT_EN is set. The device enters Sleep mode after the timer expires if there are no pending wake interrupts.	The LDT restarts the timer again after entering the Sleep mode and exits Sleep mode after the timer expires. LDT_WAKE interrupt is set to indicate timer based wake-up.

8.3.15 Safety Features

The TCAN29xx-Q1 has several protections features that are described as follows.

8.3.15.1 Watchdog

The device has an integrated watchdog function. The device provides a default window based, time-out and question and answer (Q&A) watchdog using SPI programming at WD_CONFIG_1 register 8'h13[7:6], WD_CONFIG. The watchdog configuration and type can only be programmed when the device is in standby mode. Normal mode supports all three watchdog configurations while standby mode defaults to timeout. When the device enters standby mode, the watchdog configuration automatically changes to a timeout watchdog. The standby mode watchdog can be configured to the same type as normal mode by programming register 8'h13[2] = 1b. The watchdog is default off in sleep mode but can be configured to be active as a timeout watchdog by programming WD_SLP_EN at register 8'h13[3] = 1b.

When entering standby mode from restart mode, there is a nRST transition from low to high. This transition starts the t_{INITWD} timer, and includes the t_{RSTN_act} timer in restart mode. A WD trigger input must take place prior

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to this initial long window times out. The initial long window defaults to 600ms but can be programmed to other values, WD_LW_SEL at register 8'h13[1:0]. When entering normal mode, the programmed watchdog timer starts based upon the programmed configuration. The watchdog timer is off in sleep, restart and fail-safe modes. The LIMP pin provides a limp home capability. When in sleep mode, the LIMP pin is off. When the error counter exceeds the watchdog trigger event level, the LIMP pin turns pulling the LIMP pin to ground as described in the LIMP pin section.

The watchdog has extensive configurable including the ability to select the time-out or Q&A watchdog. Watchdog is default enabled for standby mode, but can be disabled by setting register 8'h14[0] = 1b. Register 8'h13[7:6] can be set to 00b to disable the WD. There is a WD error counter available, see Section 8.3.15.1.1 for description of this counter. Figure 8-27 provides a flow chart on the watchdog in standby mode. Watchdog can be enabled in sleep mode, but only behaves as a time-out watchdog. VCC1 must be enabled for sleep mode. Figure 8-28 flow chart provides the behavior of the device when the watchdog is enabled or disabled in sleep mode.

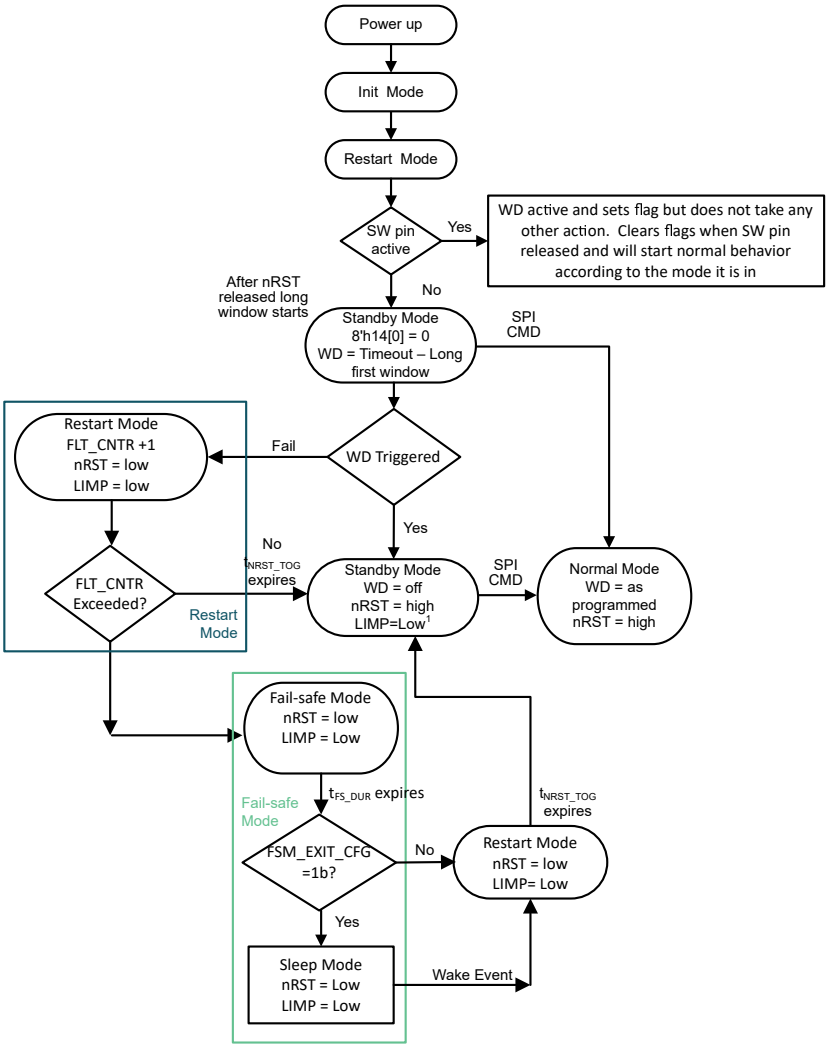

Figure 8-27. Watchdog in Standby Mode

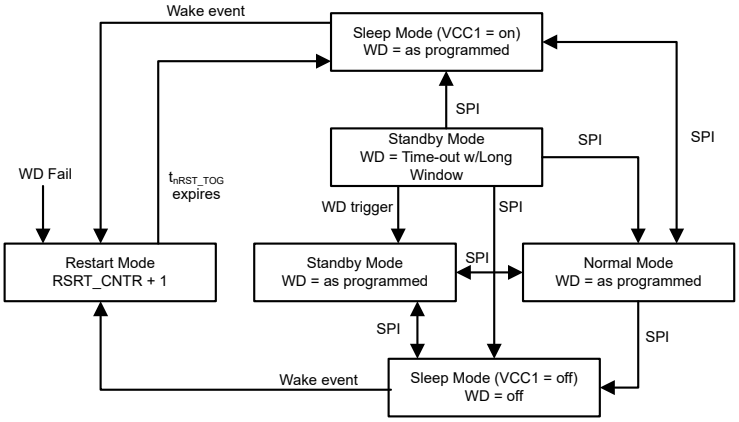

Figure 8-28. Watchdog in Sleep Mode

Note

- When the mode is changed the watchdog timer does not restart. If standby mode is configured for timeout and the Q&A watchdog is enabled, the recommendation is to trigger the watchdog in standby mode prior to changing to normal mode to avoid a watchdog error by missing answers due to limited window time.

8.3.15.1.1 Watchdog Error Counter and Action

The device has a watchdog error counter. This counter is an up down counter that increments for every missed window or incorrect input watchdog trigger event. For every correct input trigger, the counter decrements but does not drop below zero. The default trigger for this counter is to trigger a watchdog event is for every event. This counter can be configured at register 8'h16[7:4] which sets the limit for incorrect input triggers up to 15. The error counter can be read at register 8'14[4:1].

Once the programmed WD error counter limit has been exceeded, the device transitions to restart mode which pulls nRST low for t_{NRST_TOG}. The error counter resets back to 0 at this point. Once t_{NRST_TOG} times out the device will transition back to standby mode releasing nRST high. If the WD failure causes the restart counter to exceed its programmed limit, the device will transition to either fail-safe mode if enabled or to sleep mode.

8.3.15.1.2 Watchdog SPI Programming

Registers 8’h13, 8'h14, and 8’h16 configure the watchdog function. The TCAN29xx-Q1 watchdog can be set as a timeout, window, or Q&A watchdog by setting 8’h13[6] to the method of choice. The timer for each of these watchdog configurations is based upon registers 8’h13[5:4] WD prescaler and 8’h14[7:5] WD timer and is in ms. See Table 8-8 for the achievable times and more detail. If using smaller time windows, it is suggested to use the timeout version of the watchdog, but not required. This is for times between 4ms and 64 ms. The programmed time is also used for the Q&A watchdog which is programmed at registers 8'h2D through 8'h2F.

Table 8-8. Timeout, Window, and Q&A Watchdog Timer Configuration (ms)

WD_TIMER	8'h13[5:4] WD_PRE			
8'h14[7:5]	**00 (default)**	01	10	11
000	4	8	12	16
001	32	64	96	128
010	128	256	384	512
011 (default)	**256**	384	512	768
100	512	1024	1536	2048
101	2048	4096	6144	8192
110	10240	20240	RSVD	RSVD
111	RSVD	RSVD	RSVD	RSVD

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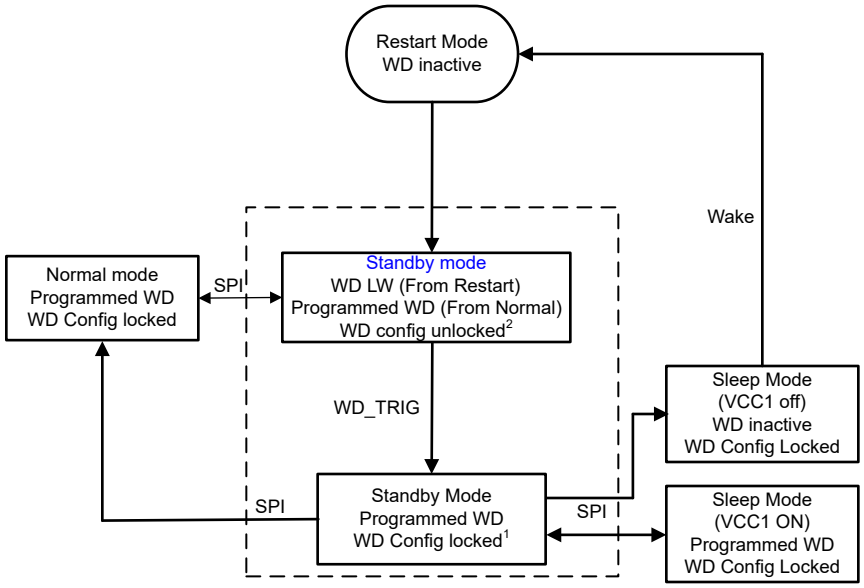
Note

The watchdog timing can only be configured in standby mode if unlocked.

8.3.15.1.2.1 Watchdog Configuration Registers Lock and Unlock

To avoid inadvertent watchdog configuration changes, the TCAN29xx-Q1 family implements a watchdog configuration register locking and unlocking mechanism. Registers 8'h13, 8'h14, 8'16 and 8'h2D are only programmable in standby mode and are the registers that become locked. These registers automatically lock with the first WD input trigger event or when transitioning to normal mode via SPI command. The unlocking mechanism is transitioning to standby mode; which allows one write to each of the four registers. If the registers are locked while in standby mode, the device must transition to normal mode and then back to standby mode. The WD can be enabled in sleep mode and is only capable of timeout and the configuration registers are locked. See Figure 8-29;which shows the described behavior.



1 As long as SW pin is active in Standby mode, WD is unlocked for programming in Standby mode
2 Allows one write to registers 8'h13, 8'h14, 8'h16 and 8'h2D before WD trigger.

Figure 8-29. Watchog Configuration Registers Locking and Unlocking Flow Chart

8.3.15.1.3 Watchdog Timing

The TCAN29xx-Q1 provides three methods for setting up the watchdog, window, timeout and question and answer. Question and Answer watch dog is covered in Question and Answer Watchdog. If more frequent, < 64 ms, input trigger events are desired it is suggested to us the timeout watchdog, but not required.

When using the window watchdog, it is important to understand the closed and open window aspects. The device is set up with a 50%/50% open and closed window and is based on an internal oscillator with a ±10% accuracy range. To determine when to provide the input trigger, this variance needs to be considered. Using the 64ms nominal total window, t_{WINDOW}, provides a closed and open window that are each 32ms. Taking the ±10% internal oscillator into account means t_{WINDOW} could be between 57.6ms and 70.4ms. The closed, t_{CLOSED}, and open window, t_{OPEN}, would then be between 28.8ms and 35.2ms. Using t_{WINDOW} of 57.6 ms and t_{CLOSED} of 35.2ms, the total t_{OPEN} is 22.4ms. The safe trigger area needs to happen at the 46.4ms ± 11.2ms which is half the t_{OPEN} min + t_{CLOSED} max. The same method is used for the other window values. Figure 8-30 provides the above information graphically. This also describes the response 1 and response 2 windows for the Q&A watchdog.

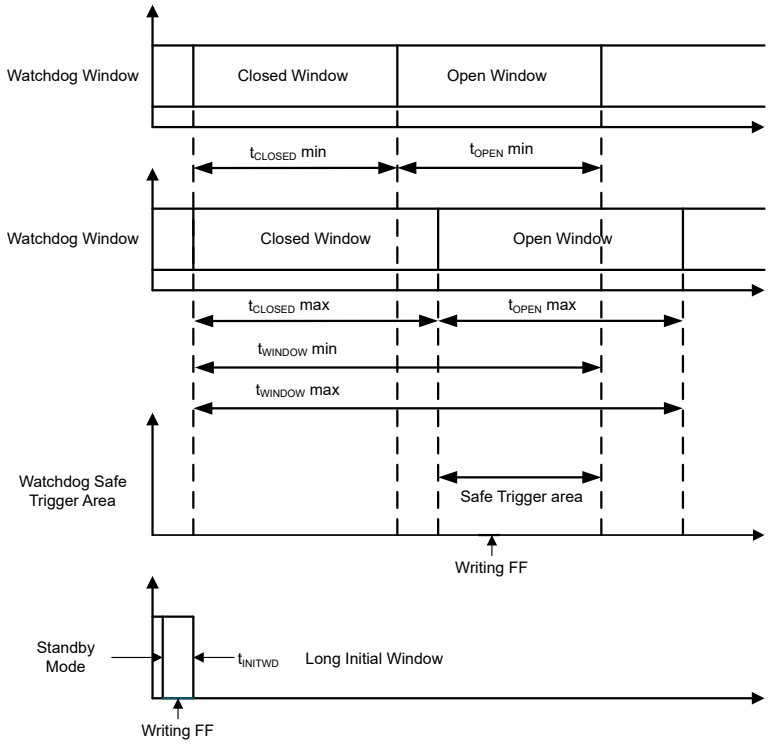


Figure 8-30. Watchdog Timing Diagram

8.3.15.1.4 Question and Answer Watchdog

The devices include a question and answer watchdog selectable from SPI. Device defaults to window watchdog.

Question and Answer WD Example explains the WD initialization events.

8.3.15.1.4.1 WD Question and Answer Basic Information

A Question and Answer (Q&A) watchdog is a type of watchdog where instead of simply resetting the watchdog via a SPI write, the MCU must read a 'question' from the device, do math based on the question, and then write the computed answers back to the device. The correct answer is a 4-byte response. Each byte must be written in order, and with the correct timing to have a correct answer.

There are 2 watchdog windows, referred to as WD Response window #1 and WD Response window #2 (Figure 8-31 WD QA Windows as example). The size of each window is 50% of the total watchdog window time, $t_{WD\_RESP\_WIN1}$ + $t_{WD\_RESP\_WIN2}$, which is selected from the WD_TIMER and WD_PRE register bits.

Each watchdog question and answer is a full watchdog cycle. The general process is that the MCU reads the question during WD Response Window #1. The CPU must perform a mathematical function on the question, resulting in 4 bytes of answers. 3 of the 4 answer bytes must be written to the answer register within the WD Response Window #1, in correct order. The last answer must be written to the answer register after the first response window, inside of WD Response Window #2. If all 4 answer bytes were correct and in the correct order, then the response is considered good, the error counter is decremented and a new question is generated, starting the cycle over again. Once the fourth answer is written into WD Response Window #2, that window is terminated and a new WD Response Window #1 is started.

If anything is incorrect or missed, the response is considered bad and the watchdog question will NOT change. In addition, an error counter is incremented. Once this error counter exceeds the threshold (defined in the WD_ERR_CNT_SET register field), the watchdog failure action is performed. Examples of actions are an interrupt, or reset toggle, and so on.

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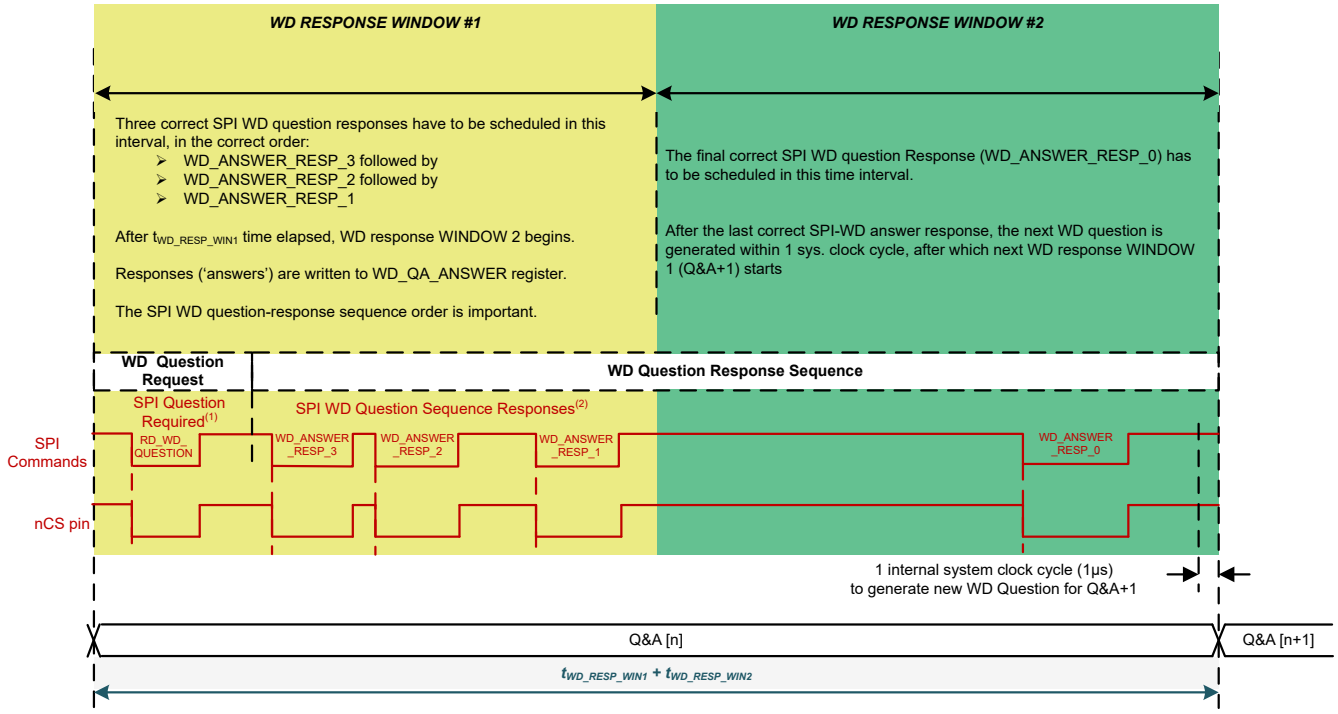


A. The MCU is not required to request the WD question. The MCU can start with correct answers, WD_ANSWER_RESP_x bytes anywhere within RESPONSE WINDOW 1. The new WD question is always generated within one system clock cycle after the final WD_ANSWER_RESP_0 answer during the previous WD Q&A sequence run.

B. The MCU can schedule other SPI commands between the WD_ANSWER_RESPx responses (even a command requesting the WD question) without any impact to the WD function as long as the WD_ANSWER_RESP_[3:1] bytes are provided within the RESPONSE WINDOW 1 and WD_ANSWER_RESP_0 is provided within the RESPONSE WINDOW 2.

Figure 8-31. WD Q&A Sequence Run

8.3.15.1.4.2 Question and Answer Register and Settings

There are several registers used to configure the watchdog registers, see Table 8-9.

Table 8-9. List of Watchdog Related Registers

Register Address	Register Name	Description
0x13	WD_CONFIG_1	Watchdog configuration and action in event of a failure
0x14	WD_CONFIG_2	Sets the time of the window, and shows current error counter value
0x15	WD_INPUT_TRIG	Register to reset or start the watchdog
0x16	WD_RST_PULSE	Sets error counter threshold
0x2D	WD_QA_CONFIG	Configuration related to the QA configuration
0x2E	WD_QA_ANSWER	Register for writing the calculated answers
0x2F	WD_QA_QUESTION	Reading the current QA question

The WD_CONFIG_1 and WD_CONFIG_2 registers mainly deal with setting up the watchdog window time length. Refer to Table 8-8 to see the options for window sizes, and the required values for the WD_TIMER values and WD_PRE values. Take note that each of the 2 response windows are half of the selected value. Due to the need for several bytes of SPI to be used for each watchdog QA event, it is recommended that windows greater than 64ms be used when using the QA watchdog functionality.

There are also different actions that can be performed when the watchdog error counter exceeds the error counter threshold.

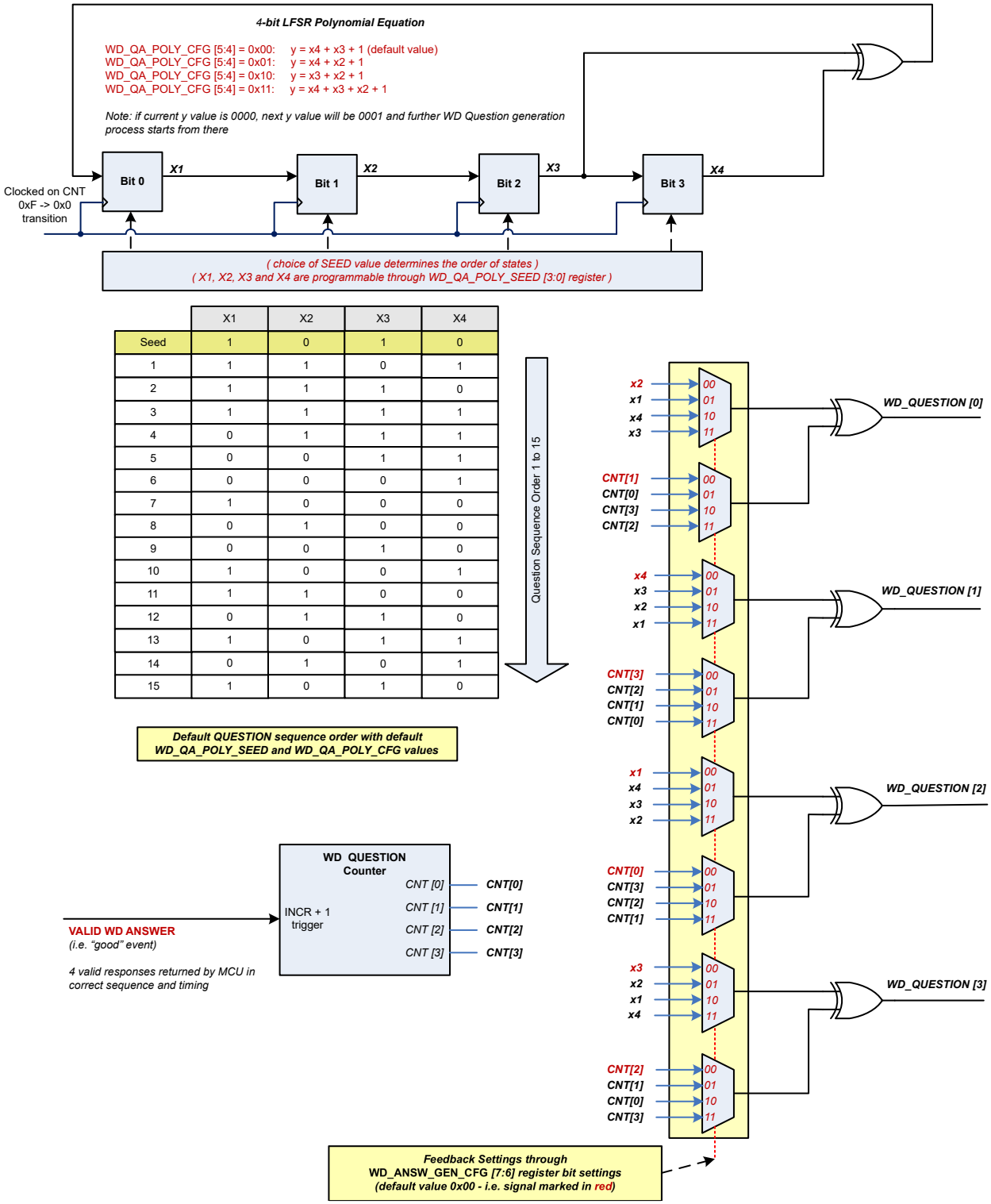
8.3.15.1.4.3 WD Question and Answer Value Generation

The 4-bit WD question, WD_QA_QUESTION[3:0], is generated by 4-bit Markov chain process. A Markov chain is a stochastic process with Markov property, which means that state changes are probabilistic, and the future state depends only on the current state. The valid and complete WD answer sequence for each WD Q&A mode is as follows:

- WD Q&A mode expectations:
  1. Three correct SPI WD answers are received during RESPONSE WINDOW 1.
  2. One correct SPI WD answer is received during RESPONSE WINDOW 2.
  3. In addition to the previously listed timing, the sequence of four responses shall be correct.

The WD question value is latched in the WD_QUESTION bits of the WD_QA_QUESTION register and can be read out at any time.

The Markov chain process is clocked by the 4-bit Question counter at the transition from 1111b to 0000b. This includes the condition of a correct answer (correct answer value and correct timing response). The logic combination of the 4-bit questions WD_QA_QUESTION [3:0] generation is given in Figure 8-32. The question counter is reset to default value of 0000b and the Markov chain is re-initialized to programmed register value when a watchdog fail puts the device in restart mode.



	X1	X2	X3	X4
Seed	1	0	1	0
1	1	1	0	1
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	1	0	0	0
8	0	1	0	0
9	0	0	1	0
10	1	0	0	1
11	1	1	0	0
12	0	1	1	0
13	1	0	1	1
14	0	1	0	1
15	1	0	1	0

A. • Register 8'h2D[3:0] WD_QA_POLY_SEED maps as bit 3 = X1, bit 2 = X2. bit 1 = X3 and bit 0 = X4.
• If the current *y* value is 0000, the next *y* value is 0001. The next watchdog question generation process starts from that value. Any changes to WD_QA_CONFIG register in Standby mode re-initializes the Markov chain to the current register value. The question counter is not affected.

Figure 8-32. Watchdog Question Generation

8.3.15.1.4.3.1 Answer Comparison

The 2-bit, watchdog-answer counter, WD_ANSW_CNT[1:0], counts the number of received answer-bytes and controls the generation of the reference answer-byte as shown in Figure 8-33. At the start of each watchdog sequence, the default value of the WD_ANSW_CNT[1:0] counter is 11b to indicate that the watchdog expects the MCU to write the correct Answer-3 in WD_QA_ANSWER[7:0].

The device sets the WD_QA_ERR status bit as soon as one answer byte is not correct. The device clears this status bit only if the MCU writes a '1' to this bit.

8.3.15.1.4.3.2 Sequence of the 2-bit Watchdog Answer Counter

The sequence of the 2-bit, watchdog answer-counter is as follows for each counter value:

- WD_ANSW_CNT[1:0] = 11b:
  1. The watchdog calculates the reference Answer-3.
  2. A write access occurs. The MCU writes the Answer-3 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-3 with the Answer-3 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 10b and sets the WD_QA_ERR status bit to 1 if the Answer-3 byte was incorrect.
- WD_ANSW_CNT[1:0] = 10b:
  1. The watchdog calculates the reference Answer-2.
  2. A write access occurs. The MCU writes the Answer-2 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-2 with the Answer-2 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 01b and sets the WD_QA_ERR status bit to 1 if the Answer-2 byte was incorrect.
- WD_ANSW_CNT[1:0] = 01b:
  1. The watchdog calculates the reference Answer-1.
  2. A write access occurs. The MCU writes the Answer-1 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-1 with the Answer-1 byte in WD_QA_ANSWER[7:0].
  4. The watchdog decrements the WD_ANSW_CNT[1:0] bits to 00b and sets the WD_QA_ERR status bit to 1 if the Answer-1 byte was incorrect.
- WD_ANSW_CNT[1:0] = 00b:
  1. The watchdog calculates the reference Answer-0.
  2. A write access occurs. The MCU writes the Answer-0 byte in WD_QA_ANSWER[7:0].
  3. The watchdog compares the reference Answer-0 with the Answer-0 byte in WD_QA_ANSWER[7:0].
  4. The watchdog sets the WD_QA_ERR status bit to 1 if the Answer-0 byte was incorrect.
  5. The watchdog starts a new watchdog sequence and sets the WD_ANSW_CNT[1:0] to 11b.

The MCU needs to clear the bit by writing a '1' to the WD_QA_ERR bit

Table 8-10. Set of WD Questions and Corresponding WD Answers Using Default Setting

QUESTION IN WD_QA_QUESTION REGISTER	WD ANSWER BYTES (EACH BYTE TO BE WRITTEN INTO WD_QA_ANSWER REGISTER)			
	WD_ANSWER_RESP_3	WD_ANSWER_RESP_2	WD_ANSWER_RESP_1	WD_ANSWER_RESP_0
WD_QUESTION	WD_ANSW_CNT[1:0] 11b	WD_ANSW_CNT[1:0] 10b	WD_ANSW_CNT[1:0] 01b	WD_ANSW_CNT[1:0] 00b
0x0	FF	0F	F0	00
0x1	B0	40	BF	4F
0x2	E9	19	E6	16
0x3	A6	56	A9	59
0x4	75	85	7A	8A
0x5	3A	CA	35	C5
0x6	63	93	6C	9C
0x7	2C	DC	23	D3
0x8	D2	22	DD	2D
0x9	9D	6D	92	62
0xA	C4	34	CB	3B
0xB	8B	7B	84	74
0xC	58	A8	57	A7
0xD	17	E7	18	E8
0xE	4E	BE	41	B1
0xF	01	F1	0E	FE

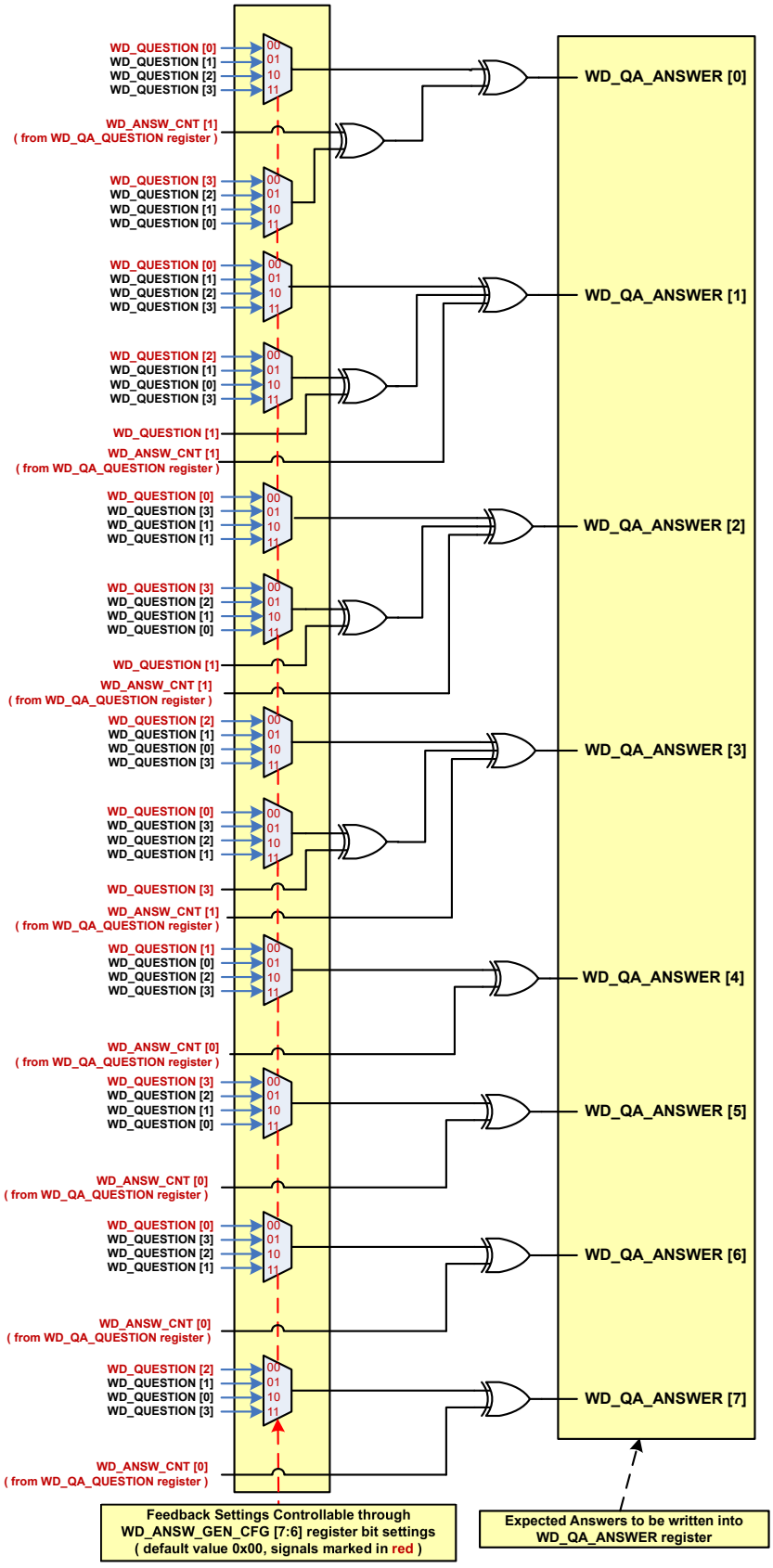


Figure 8-33. WD Expected Answer Generation

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Table 8-11. Correct and Incorrect WD Q&A Sequence Run Scenarios

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register)[1]	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
0 answer	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	No answer
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
0 answer	1 CORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 CORRECT answer			
2 CORRECT answers	1 CORRECT answer			
0 answer	1 INCORRECT answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 CORRECT answer	1 INCORRECT answer			
2 CORRECT answers	1 INCORRECT answer			
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in WIN1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 CORRECT answers			
2 CORRECT answer	2 CORRECT answers			
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 CORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 CORRECT answer	3 INCORRECT answers			
2 CORRECT answers	2 INCORRECT answers			
0 answer	3 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 CORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
2 INCORRECT answers	1 CORRECT answer			
0 answer	3 INCORRECT answers	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
1 INCORRECT answer	2 INCORRECT answers			
2 INCORRECT answers	1 INCORRECT answer			
0 answer	4 CORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 CORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 CORRECT answers		1b	
2 INCORRECT answers	2 CORRECT answers			
0 answer	4 INCORRECT answers	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Less than 3 INCORRECT ANSWERS in RESPONSE WINDOW 1 and more than 1 INCORRECT ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] = 4)
1 INCORRECT answer	3 INCORRECT answers			
2 INCORRECT answers	2 INCORRECT answers			
3 CORRECT answers	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD Question	1b	Less than 4 CORRECT ANSWERS in RESPONSE WINDOW 1 and more than 0 ANSWER in RESPONSE WINDOW 2 (Total WD_ANSW_CNT[1:0] < 4)
2 CORRECT answers	0 answer		1b	
1 CORRECT answer	0 answer			
3 CORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Decrement WD failure counter -New WD cycle starts with a new WD question	0b	CORRECT SEQUENCE
3 CORRECT answers	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
3 INCORRECT answers	0 answer	-New WD cycle starts after the end of RESPONSE WINDOW 2 -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received < 4
3 INCORRECT answers	1 CORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4

Table 8-11. Correct and Incorrect WD Q&A Sequence Run Scenarios (continued)

NUMBER OF WD ANSWERS		ACTION	WD_QA_ERR (in WD_QA_QUESTION Register)(1)	COMMENTS
RESPONSE WINDOW 1	RESPONSE WINDOW 2			
3 INCORRECT answers	1 INCORRECT answer	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	Total Answers Received = 4
4 CORRECT answers	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	
3 CORRECT answers + 1 INCORRECT answer	Not applicable	-New WD cycle starts after the 4th WD answer -Increment WD failure counter -New WD cycle starts with the same WD question	1b	4 CORRECT or INCORRECT ANSWERS in RESPONSE WINDOW 1
2 CORRECT answers + 2 INCORRECT answers	Not applicable			
1 CORRECT answer + 3 INCORRECT answers	Not applicable			

(1) WD_QA_ERR is the logical OR of all QA watchdog errors

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8.3.15.1.4.4 Question and Answer WD Example

For this example, see the single sequence with the following configuration settings, Table 8-12.

Table 8-12. WD Function Initialization

Item	Value	Description
Watchdog window size	1024 ms	Window size of 1024 ms
Answer Generation Option	0 (default)	Answer generation configuration
Question Polynomial	0 (default)	Polynomial used to generate the question
Question polynomial seed	A (default)	Polynomial seed used to generate questions
WD Error Counter Limit	15	On the 15th fail event, do the watchdog action

8.3.15.1.4.4.1 Example Configuration for Desired Behavior

Table 8-13 configures the part for the example behavior. Most of the settings are power on defaults.

Table 8-13. Example Register Configuration Writes

Step	Register	Data
1	WD_CONFIG_1 (0x13)	[W] 0b11010000 / 0xD0
2	WD_CONFIG_2 (0x14)	[W] 0b10000000 / 0x80
3	WD_RST_PULSE (0x16)	[W] 0b11110000 / 0xF0
4	WDT_QA_CONFIG (0x2D)	[W] 0b00001010 / 0x0A

8.3.15.1.4.4.2 Example of Performing a Question and Answer Sequence

The normal sequence summary is as follows:

1. Read the question
2. Calculate the 4 answer bytes
3. Send 3 of them within the first response window
4. Wait and send the last byte in the second response window

See Table 8-14 for an example of the first loop sequence.

Table 8-14. Example First Loop

Step	Register	Data	Description
1	WD_QA_QUESTION (0x2F)	[R] 0x0C	Read the question. Question is 0x0C
2	WD_QA_ANSWER (0x2E)	[W] 0x58	Write answer 3
3	WD_QA_ANSWER (0x2E)	[W] 0xA8	Write answer 2
4	WD_QA_ANSWER (0x2E)	[W] 0x57	Write answer 1
5	WD_QA_ANSWER (0x2E)	[W] 0xA7	Write answer 0 once window 2 has started

The user can read the WD_QA_QUESTION[6] (0x2F) register to determine if WD_QA_ERR is set.

8.3.15.2 Under/Over Voltage Lockout and Unpowered Device

The device monitors all of the supply rails of the device, both input (VSUP, VHSS and VCAN) and output (VCC1, VCC2 and VEXCC). For the input supply rails, all are monitored for under-voltage and VHSS can be monitored for over-voltage. For the output supply rails, all are monitored for under-voltage, over-voltage and short circuit

failures. Each of these fault events have a corresponding interrupt with VSUP and VCC1 faults causing device SBC mode changes. See Table 8-15 for the relationship between VSUP, VCC1, VCC2 and VEXCC faults.

The device monitors VCC1, VCC2 and VEXCC for over-voltage condition. Over-voltage is represented by OVCC1, OVCC2 and OVEXCC. The TCAN29xx-Q1 monitors VCC1, VCC2 and VEXCC for short to ground conditions. Short to ground is represented by $VCC1_{33SC}$, $VCC1_{5SC}$, $VCC2_{SC}$ and $VEXCC_{SC}$.

The device monitors the high-side switches supply voltage, VHSS, for over-voltage events. This can be disabled by writing 1b to 8'h4F[7], HSS_OV_DIS. Under-voltage is monitored on the HVSS supply, UVHSS. This can be disabled by writing 1b to 8'h4F[6], HSS_UV_DIS. The HSS switches will automatically recover from an OVHSS or UVHSS unless disabled by writing 1b to 8'h4F[5], HSS_OV_UV_REC.

Table 8-15. VSUP, VCC1, VCC2 and VEXCC Faults and Device Mode

VSUP	VCC1	VCC2	VEXCC	Device Mode
> UVSUP	> UVCC1	> UVCC2	NA	Normal or Standby
> UVSUP	< $UVCC1_{PR}$	> UVCC2	NA	Previous Mode
> UVSUP	< UVCC1	> UVCC2	NA	Restart
> UVSUP	> UVCC1	< UVCC2	NA	Previous Mode
> UVSUP	> UVCC1	> UVCC2	< UVEXCC	Previous Mode
> UVSUP	> OVCC1	NA	NA	Fail-safe or Sleep
> UVSUP	> UVCC1	> OVCC2	NA	Previous Mode
> UVSUP	> UVCC1	NA	< OVEXCC	Previous Mode
> UVSUP	< $VCC1_{SC}$	NA	NA	Fail-safe or Sleep
> UVSUP	> UVCC1	< $VCC2_{SC}$	NA	Previous Mode
> UVSUP	> UVCC1	NA	< $VEXCC_{SC}$	Previous Mode

Note

If a permanent fault on VCC1 takes place and fail-safe mode is disabled, it is possible to get into a loop between restart and sleep mode due to wake events and VCC1 SBC fault.

- It is recommended to enable fail-safe mode when VCC1 is programmed on for sleep mode.
- To avoid the loop situation for a permanent fault with fail-safe mode enabled, it is recommended to use FSM_CONFIG register 8'h17[7:4] = 0100b which is FSM_CNTR_ACT and places the device into sleep mode with LDOs off until a power cycle reset takes place.

8.3.15.2.1 Under-voltage

The device monitors VSUP, VHSS, VCAN, VEXCC, VCC1 and VCC2 for under-voltage events. Under-voltage events are represented by $UVSUP_{xR/F}$, $UVHSS_{R/F}$, $UVCAN_{R/F}$, $VCC1_{xR/F}$, $UVCC2_{R/F}$ and $UVEXCC_{xR/F}$. The x represents the voltage level, R is when voltage level is ramping up and F is when voltage level is ramping down. Behavior of the device is dependent upon when supply rail is in under-voltage.

VCC1 is the LDO that provides power for the digital input/output pins and is expected to be connected to the node processor. VCC1 has a under-voltage pre-warning threshold and four programmable under-voltage threshold. When the under-voltage pre-warning event takes place an interrupt is set, INT_6 register 8'h5C[6] and the nINT pin is pulled low. Once VCC1 reaches one of the programmed thresholds, SBC_CONFIG1 register 8'h0E[4:3], the device to transition to restart mode and latch nRST low until the LDO voltage exceeds the under-voltage rising threshold. nRST remains latched low and the device will stay in restart mode for t_{RSTN_act} after clearing the UV threshold. For UVCC1, there is a filter time, t_{UVFLTR}, that under-voltage event must last longer than for the device to enter restart mode.

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8.3.15.2.1.1 VSUP and VHSS Under-voltage

VSUP is the primary input supply rail required for the device to function properly. There are three voltage levels monitored by the device, power on reset and two under-voltage level. For all functions and output voltage rails to be in regulation the device must exceed $UVSUP_{5R}$. If VSUP is in under-voltage, the device loses the supply source needed to keep the internal regulators in regulation. This causes the device to go into a state where communication between the microprocessor and the TCAN29xx-Q1 is disabled. In this mode the device is still active but VCC1, VCC2 and VEXCC may be experiencing under voltage events and other functions is not active, like watchdog. No mode change can take place. The device is not able to receive information from the bus; thus, does not pass any signals from the bus, including any Bus Wake via BWRR signals to the microprocessor. VCC1 determines which UVSUP level, $UVSUP_{33R/F}$ or $UVSUP_{5R/F}$, is used for this. If VSUP keeps ramping down and drops below $VSUP_{(PU)F}$, the device enters powered off state. When VSUP returns, the device comes up as if there was an initial power on. All registers are reset to their default values. During an UVSUP event, the device has some functionality. The LDOs are in pass through mode until VSUP ≥ $UVSUP_{xxR}$ and VCC1 exceeds its $UVCC1_{xxR}$ level. At this time, the device will transition to restart mode.

For devices where VCC1 is 5V, $UVSUP_{5R/F}$ is the only VSUP under-voltage rail monitored. When VSUP drops below $UVSUP_{5F}$, The CAN and LIN transceivers are turned off and LDOs are in pass thru mode. See Table 8-16 for relationship between VSUP, $VCC1_5$, VCAN, device mode and transceivers.

When VCC1 is 3.3V, both $UVSUP_{33R/F}$ and $UVSUP_{5R/F}$ are monitored. When powering up, VSUP has to exceed $UVSUP_{33R}$ for VCC1 to be in regulation and above $UVSUP_{5R}$ for VCC2 and other functions of the device to work properly. When VSUP is ramping down, $UVSUP_{5F}$ is the first UVSUP level that sets an UVSUP5 interrupt flag, register 8'h52[4], and turns off the CAN transceiver. The LIN transceiver is still functioning, but may not meet the data sheet electrical and timing specifications. If VSUP keeps dropping, the next level is $UVSUP_{33F}$. When this is reached, the $UVSUP_{33}$ interrupt flag is set, register 8'h52[3]. When this level is reached, the LIN transceiver is turned off. See Table 8-17 for relationship between VSUP, $VCC1_{33}$, VCAN, device mode and transceivers.

Under-voltage on the high-side switches power, VHSS, is indicated by interrupt INT_4 register 8'5A[0] UVHSS. How the high-side switches behave due to an UVHSS event is determined by HSS_CNTL3 register 8'h4F[6:5].

Table 8-16. Under-voltage Events for $VCC1_5$, Device State and Transceiver State

VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER	LIN TRANSCEIVER
> $UVSUP_5$	> $UVCC1_5$	> UVCAN	Normal or Standby	As Programmed	As Programmed
> $UVSUP_5$	< $UVCC1_5$	NA	Restart	Wake capable or off	Wake capable or off
> $UVSUP_5$	> $UVCC1_5$	> UVCAN	Previous State	As Programmed	As Programmed
> $UVSUP_5$	> $UVCC1_5$	> UVCAN	Previous State	As Programmed	As Programmed
> $UVSUP_5$	< $UVCC1_5$	< UVCAN	Previous State	Wake capable, Silent or off	As Programmed

Table 8-17. Under-voltage Events for $VCC1_{33}$, Device State and Transceiver State

VSUP	VCC1	VCAN	DEVICE STATE	CAN TRANSCEIVER	LIN TRANSCEIVER
> $UVSUP_5$	> $UVCC1_{33}$	> UVCAN	Normal or Standby	As Programmed	As Programmed
> $UVSUP_5$	< $UVCC1_{33}$	NA	Restart	Wake capable or off	Wake capable or off
> $UVSUP_5$	> $UVCC1_{33}$	> UVCAN	Previous State	As Programmed	As Programmed
< $UVSUP_5$ > $UVSUP_{33}$	> $UVCC1_{33}$	NA	Normal or Standby	Off	As Programmed
< $UVSUP_5$ > $UVSUP_{33}$	< $UVCC1_{33}$	NA	Restart	Off	Off
> $UVSUP_5$	> $UVCC1_{33}$	< UVCAN	Normal or Standby	Wake capable, Silent or off	As Programmed

Note

- If a thermal shut down or short circuit event takes place while the regulator is in UV, the device transitions to sleep mode (fail-safe mode disabled) or fail-safe mode if enabled.
- When UVCC1 does not clear by the time the restart timer expires, the device will determine if fail-safe mode is enabled. If not enabled the device will transition to sleep mode and turn off VCC1. When VCC1 is enabled on for sleep mode, an UVCC1 event will proceed in the same manner.
- OVSUPHSS is not shown in the table as it only impacts the high-side switches.

8.3.15.2.1.2 VCC1 Under-voltage

VCC1 is the LDO that provides power for the digital input/output pins and is expected to be connected to the node processor. VCC1 is monitored for under-voltage and has two levels that are monitored, pre-warning ($UVCC1_{xPR}$) and under-voltage ($UVCC1_{XXR/FX}$). The under-voltage has one of four levels that can be programmed using register 8'h0E[4:3], UVCC1_SEL. Of the supply rails providing external power, VCC1 is the only one considered an SBC fault which causes a state change. When the under-voltage pre-warning event takes place an interrupt is set, INT_6 register 8'h5C[6] and the nINT pin is pulled low. Once VCC1 reaches one of the programmed thresholds, SBC_CONFIG1 register 8'h0E[4:3], the device transitions to restart mode and latches nRST low until VCC1 exceeds the under-voltage rising threshold. nRST remains latched low and the device stays in restart mode for t_{RSTN_act} after clearing the UV threshold. For UVCC1, there is a filter time, $t_{UVFLTR,}$ that the under-voltage event must last longer than for the device to enter restart mode, See Figure 8-34 for UVCC1 behavior.

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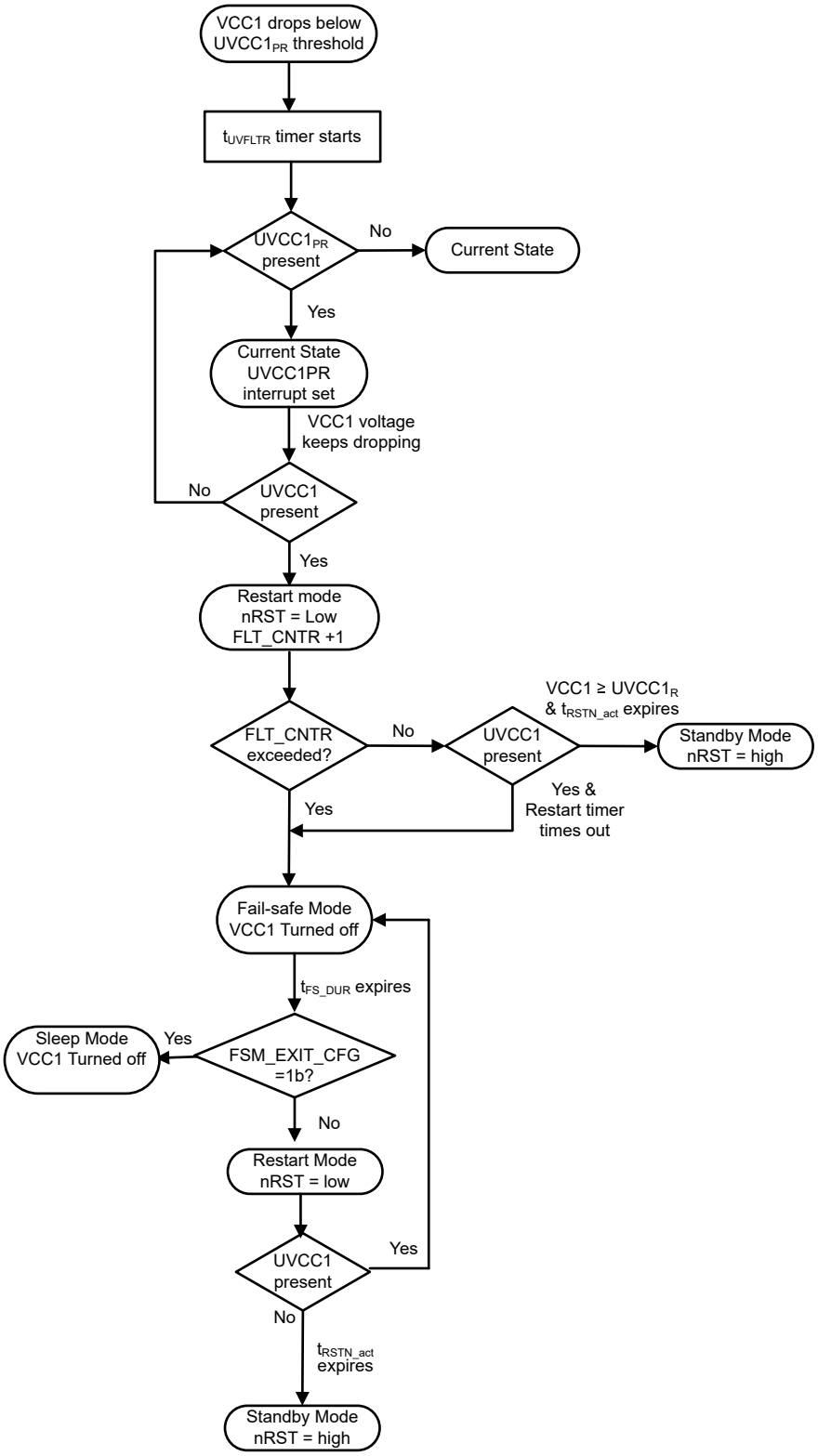

Figure 8-34. UVCC1 State Diagram

8.3.15.2.1.3 VCC2 and VEXCC Under-voltage

A UVCC2 or UVEXCC sets interrupt flags, but do not cause a mode change. See Figure 8-35 and Figure 8-36 for under-voltage behavior

- Register INT_6; 8'h5C[5] is the interrupt for UVEXCC
- Register INT_6; 8'h5C[2] is the interrupt for UVCC2

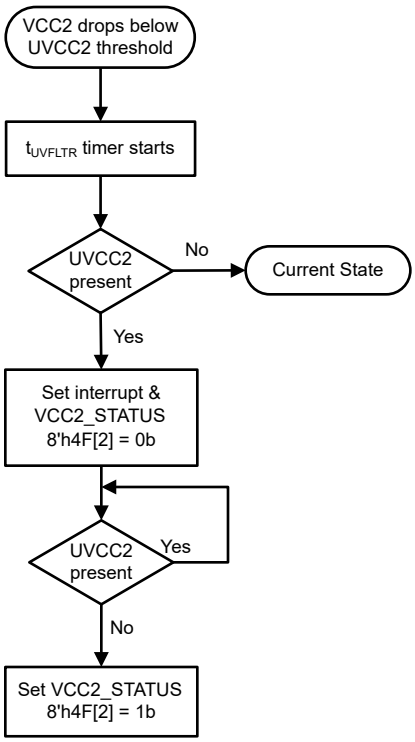

Figure 8-35. UVCC2 State Diagram

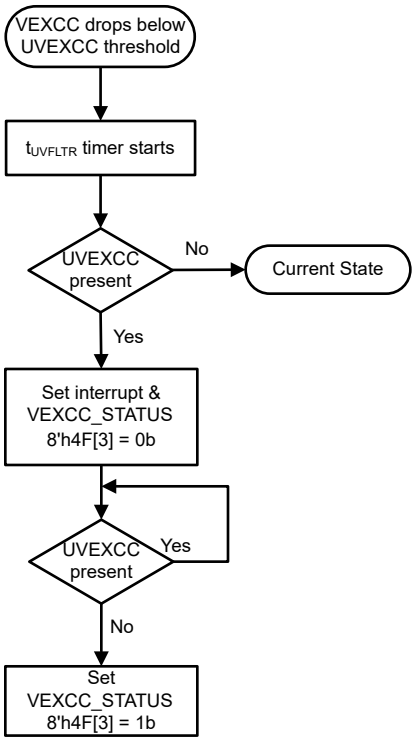

Figure 8-36. UVEXCC State Diagram

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8.3.15.2.1.4 VCAN Under-voltage

If VCAN drops below UVCAN under-voltage detection, the CAN transmitter switches off and disengage from the bus until VCAN has recovered. The CAN receiver is still active. See Figure 8-37 on how the device behaves. The device is designed to be an "ideal passive" or “no load” to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational. Logic terminals also have low leakage currents when the device is unpowered, so the terminals do not load other circuits which may remain powered.

The UVLO circuit monitors both rising and falling edge of a power rail when ramping and declining.

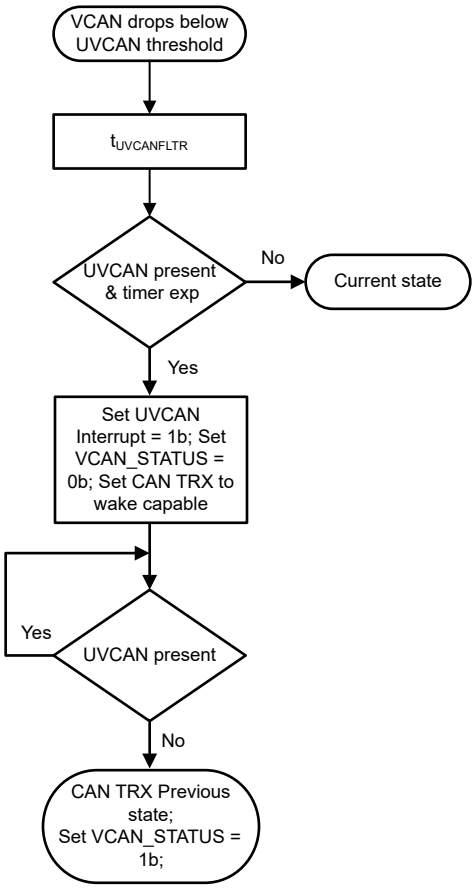

Figure 8-37. UVCAN State Diagram

Note

- UVCAN comparator is only enabled when the CAN transceiver is programmed on or in listen.

8.3.15.2.2 VCC1, VCC2 and VEXCC Over-voltage

TCAN29xx-Q1 monitors VCC1, VEXCC and VCC2 for over-voltage condition. Over-voltage is represented by OVCC1, OVCC2 and OVEXCC. When OVCC1 occurs, the device enters either fail-safe mode, if enabled, or sleep mode. When OVCC2 or OVEXCC takes place, the LDOs are turned off and an interrupt flag is set but no mode change takes place. When entering fail-safe mode, the device turns off all the LDOs and starts the t_{FS_DUR} timer. After this timer times out, OVCC1 is checked for over-voltage. If the OV event has cleared, the device enters Restart mode if FSM_EXIT_CFG=0b. If FSM_EXIT_CFG=1b, the device enters Sleep mode. If OVCC1 is still present, the device remains in Fail-safe mode. See Figure 8-38, Figure 8-39 and Figure 8-40 for device behavior during an over-voltage event.

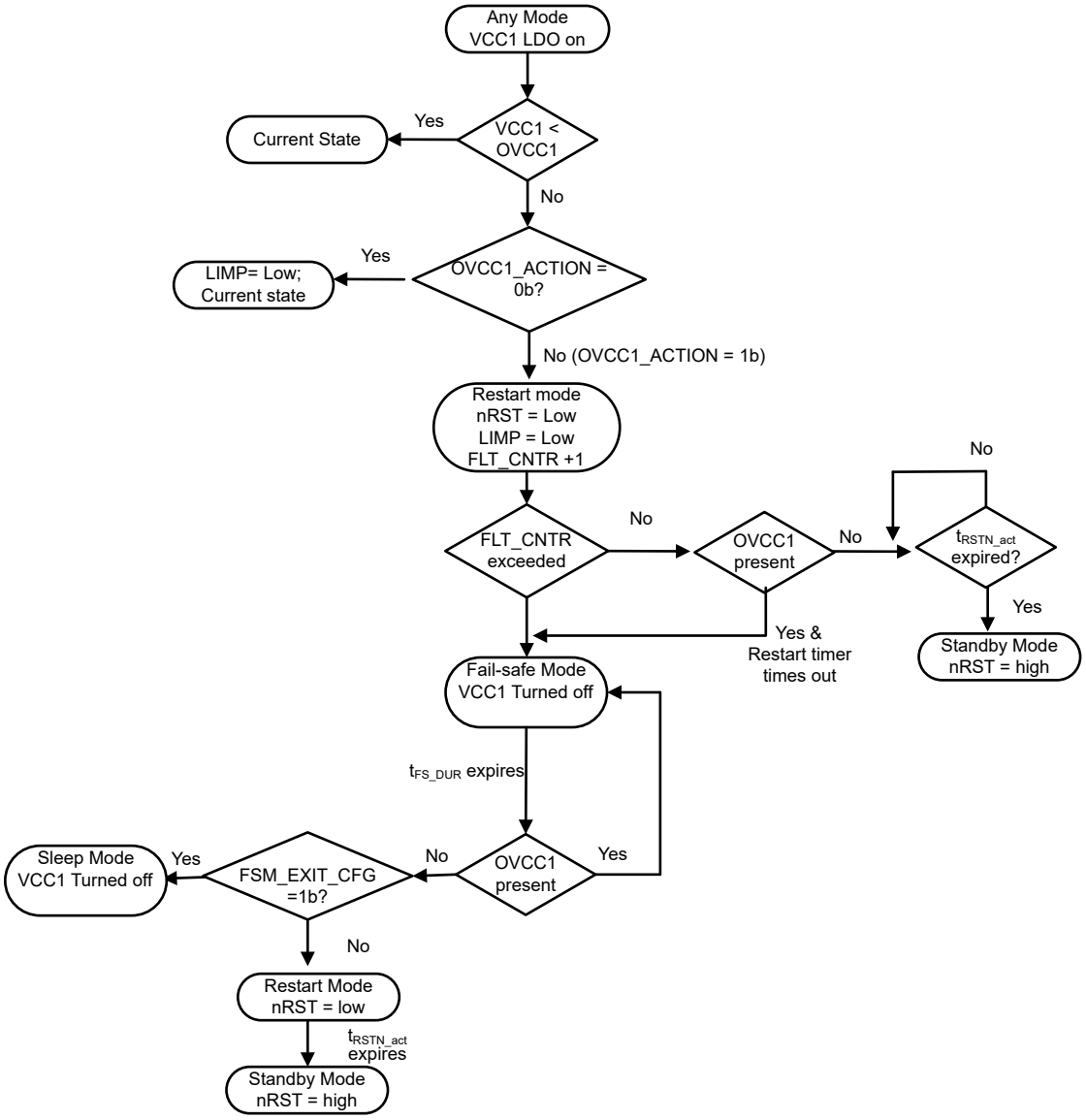

Figure 8-38. OVCC1 State Diagram

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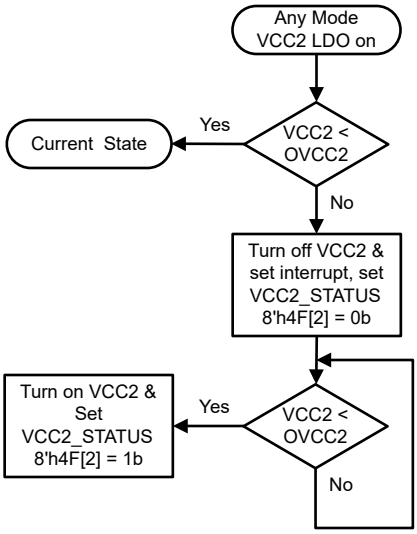

Figure 8-39. OVCC2 State Diagram

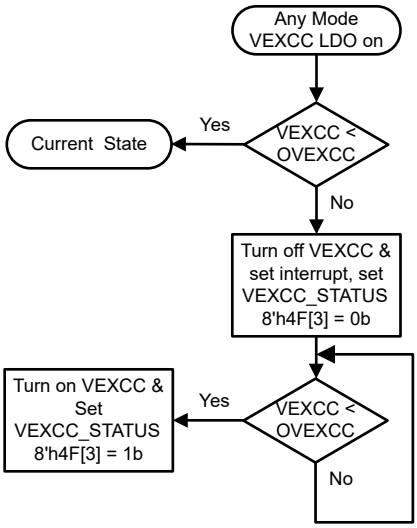

Figure 8-40. OVEXCC State Diagram

8.3.15.2.3 VCC1, VCC2 and VEXCC Short Circuit

The TCAN29xx-Q1 monitors VCC1, VEXCC and VCC2 (CAN LDO) for short to ground conditions. Short to ground is represented by $VCC1_{33SC}$, $VCC1_{5SC}$, $VCC2_{SC}$ and $VEXCC_{SC}$. A short to ground turns off the LDO. When a $VCC1_{SC}$ occurs, VCC1 is turned off and the device enters Fail-safe mode. A short circuit event cannot be monitored while the LDO is off. After the t_{FS_DUR} timer expires, if FSM_EXT_CFG=0b, the device transitions to Restart mode and checks if the the fault is cleared. wake event causes VCC1 to be turned on for t_{LDOON} to see if the SC event is still present. If the fault is still present, the device transitions back to Fail-safe mode. If the fault is cleared, the device transitions to Standby mode. When in Fail-safe mode, after the t_{FS_DUR} timer expires, if FSM_EXT_CFG=1b, the device transitions to Sleep mode and needs a wake event to enter Restart mode. See Figure 8-41, Figure 8-42 and Figure 8-43 for device behavior during a short to ground event.

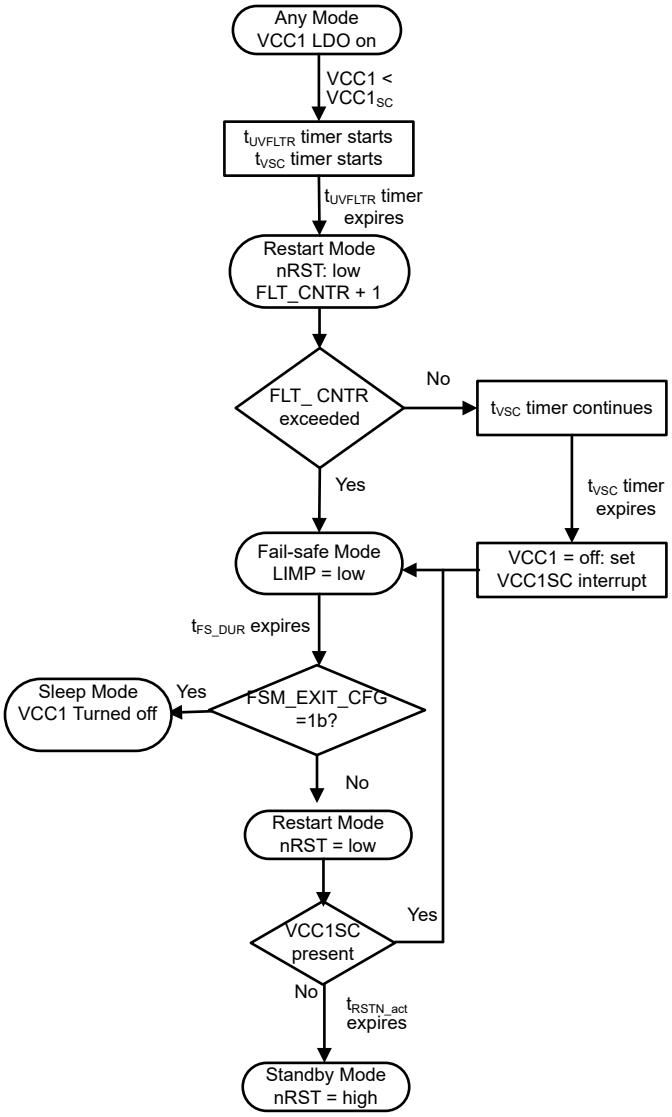

Figure 8-41. $VCC1_{SC}$ State Diagram

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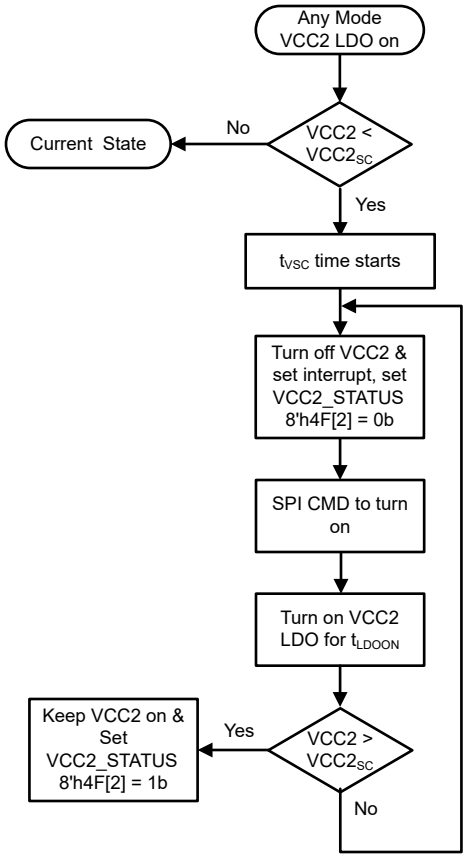

Figure 8-42. $VCC2_{SC}$ State Diagram

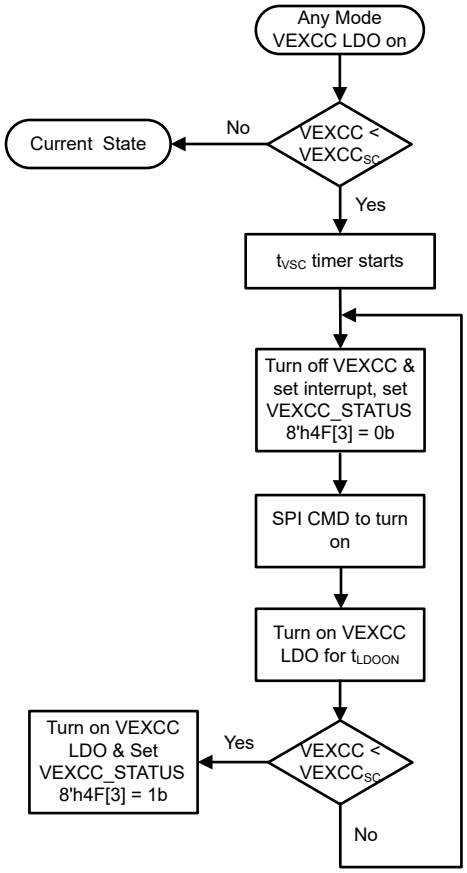

Figure 8-43. $VEXCC_{SC}$ State Diagram

8.3.15.3 Analog Built-in Self Test (ABIST)

The TCAN29xx-Q1provides an analog built-in self test mechanism to verify the correctness of voltage supervisory functions.

The ABIST is executed on-deman and can be launched in Standby and Normal mode via SPI request from the MCU.

To run ABIST:

- Read the bit ABIST_RUN_CMD and confirm it is 0b -this indicates ABIST is ready to run.
- Set ABIST_RUN_CMD =1b - the bit stays set to 1b until ABIST is completed
- ABIST_DONE bit is set to 1b and ABIST_RUN_CMD bit set to 0b when ABIST is completed.

ABIST_RUN_CMD runs ABIST on the following voltage monitoring circuits:

- Undervolatge (UV) monitoring circuits of VCC1, VCC2, VEXCC, VCAN, VSUP and VHSS
- Overvoltage (OV) montioring circuits of VCC1, VCC2, VEXCC, VHSS
- Short-circuit monitoring circuits of VCC1, VCC2 and VEXCC
- UV/OV monitoring circuits of internal LDOs

If there are any failures after ABIST is completed, the device sets the corresponding interrupt bit in INT_BIST1 (0x63) and INT_BIST2 (0x64) registers. The interrupt will be indicated on the nINT pin if ABIST_INT_EN=1b (default). The device can be configured to take addtional action per configuration of the ABIST_ERR_ACTION bit in register 0x4B, as shown in Table 8-18.

Table 8-18. ABIST_ERR_ACTION Configuration

ABIST_ERR_ACTION	Action taken
00b	Set corresponding ABIST failure interrupt

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Table 8-18. ABIST_ERR_ACTION Configuration (continued)

ABIST_ERR_ACTION	Action taken
01b	Set interrupt and turn on LIMP
10b	Set interrupt, LIMP and enter-fail safe mode.

8.3.15.4 Clock Monitoring

When enabled using ENABLE_CLKMON bit, TCAN29xx-Q1 monitors the internal 1MHz and 10k clocks anytime the 1MHz clock is expected to be operational. If the clock monitoring circuit detects an error in either of the clocks:

- Interrupt flag, CLKMON_FAIL is set.
- LIMP pin is activated

  If ABIST_ERR_ACTION=1b

The clock monitoring circuits detects an error if:

- Either 1MHz or 10kHz clock are stuck high or low.
- Either 1MHz or 10kHz clock are deviate more than ±20% from the nominal value.

8.3.15.5 Bandgap Cross-Monitoring

The TCAN29xx-Q1 integrates a bandgap cross-monitor, BG_XMON, which continuously compares the bandgap used as a reference for voltage regulation and voltage monitoring, BG1, with the second independent bandgap, BG2. When enabled via ENABLE_BGXMON bit, the BG_XMON detects an error when difference between the two bandgap reference voltages exceeds the detection threshold. When an error is detected it sets the interrupt flag and indicates via the interrupt pin, nINT, if ABIST_INT_EN=1b (default).

The device can be configured to take additional action when BG_XMON detects an error.

When enabled via SPI command, the BG_XMON operates continuously in SBC Normal Mode, and runs periodcally (every 50ms) in Standby and Sleep modes to save power.

8.3.15.6 Device Reset

The TCAN29xx-Q1 family has three methods to reset the device. Two are accomplished with SPI commands and are a soft reset and hard reset. Soft reset and hard reset are accomplished by writing a 1b to DEVICE_RST register 8'h19[1] for soft reset or to 8'h19[0] for hard reset. nRST is used as a full power on reset by pulling nRST low for t_{NRSTIN}.

When performing a soft reset, the following takes place:

- Registers are reset to default values
- VCC1 and VCC2 do not change state
- Device transitions to standby mode

When performing a hard reset via SPI or via nRST pin, the following takes place:

- Device transitions to Init mode
- Registers are reset to default values
- Most of the internal device logic is reset to default
- VCC1 and VCC2 do not change state
- Device then transitions to restart mode and finally to standby mode where the device can be reprogrammed

8.3.15.7 Floating Terminals

There are internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See Table 8-19 for details on terminal bias conditions.

Table 8-19. Terminal Bias

TERMINAL	PULL-UP or PULL-DOWN	COMMENT
SW	60kΩ Pull-down or Pull-up	When SW pin is active high pin weakly biases input to GND. When SW pin is active low pin weakly biases input to either VCC1 or internal voltage rail
SCK	60kΩ Pull-down or Pull-up	Automatically configures to pull-up or pull-down based upon the SPI mode selected which weakly biases input • Mode 0 or 1 configures for pull-down • Mode 2 or 3 configures for pull-up
SDI	60kΩ Pull-down or Pull-up	Configured as either a pull-up or pull-down based upon SDI_POL configuration in SPI_CONFIG register 8'h09[2] which weakly biases input
nCS	60kΩ Pull-up	Weakly biases input so the device is not selected
nRST	30kΩ Pull-up	Pulled-up to VCC1
LIN	40kΩ Pull-up	Weakly biases
LTXD	60kΩ Pull-up	Weakly biases input
CTXD	60kΩ Pull-up	Weakly biases input

Note

The internal bias must not be relied upon as only termination, especially in noisy environments, but must be considered a fail-safe protection. Special care needs to be taken when the device is used with MCUs using open drain outputs.

8.3.15.8 LIN Bus Stuck Dominant System Fault: False Wake Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. Figure 8-44 and Figure 8-45 show the behavior of this protection.

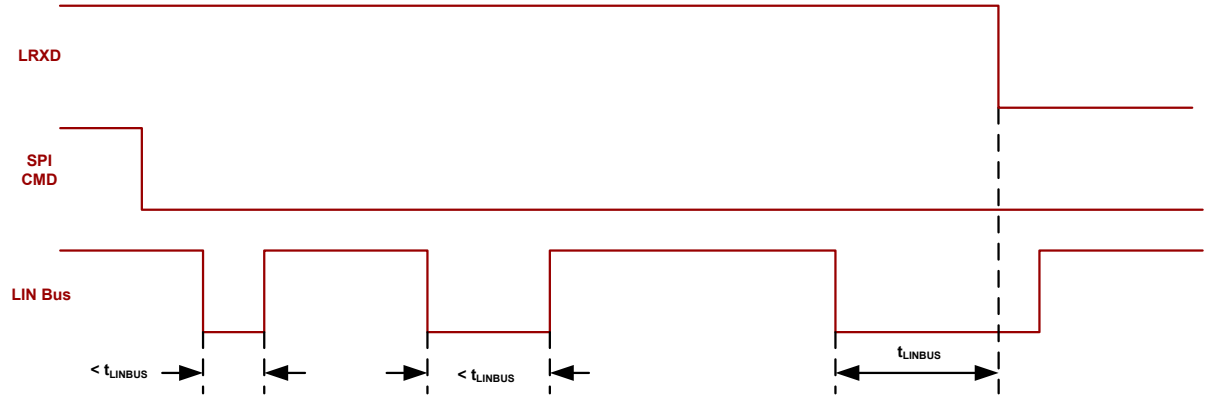

Figure 8-44. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake Up

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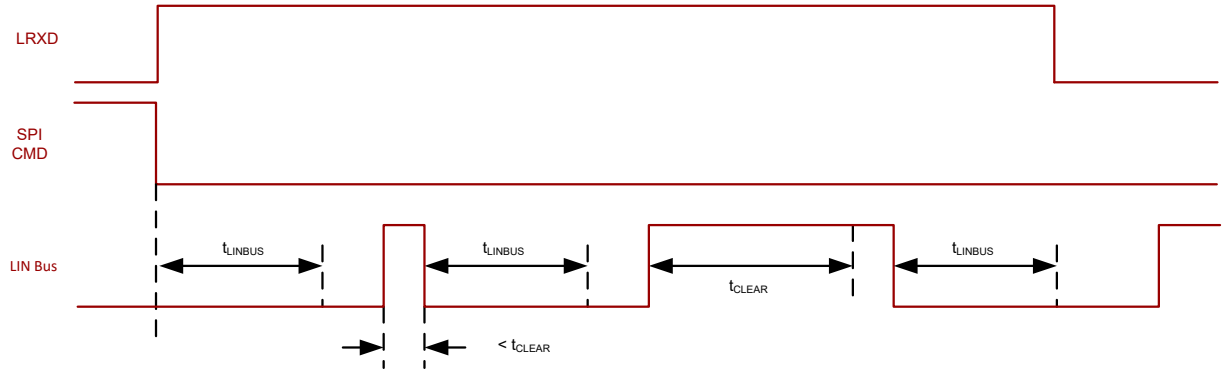

Figure 8-45. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wake Up

8.3.15.9 Thermal Shutdown

The device has two thermal sensors in the device to monitor the junction temperature of the die.

1. Covers VCC1 LDO and external PNP control, VEXCC
2. Covers VCC2 LDO, CAN transceiver and LIN transceiver

There is a thermal shutdown pre-warning provided that is set when the junction temperature of VCC1 LDO,and external PNP control, VEXCC, hits the warning temperature level. When this temperature sensor reaches the pre-warning rising, TSDWR, an interrupt is set for pre-warning. There are three interrupts a thermal event. The behavior of the device depends upon which sensor hits the thermal event. This is a device preservation feature.

- INT_6 register 8'h5C[7] is TSDW interrupt
- INT_2 register 8'h52[1] is TSD_VCC1_VEXCC interrupt
- INT_3 register 8'h53[1] is TSD_CAN_LIN interrupt which includes VCC2 LDO

Exceeding the maximum junction temperature for > t_{TSD} causes interrupt flags to be set and is indicated by pulling nINT low. If VCC1 or VEXCC causes the TSD event; the device turns off these LDOs and enter either fail-safe mode (if enabled) or sleep mode. The nRST pin is pulled to ground during this TSD event. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the TSDF temperature for 1s, the device transitions from fail-safe mode to restart mode and turn on VCC1 and VEXCC (if enabled). A thermal shut down interrupt flag is set but not indicated on nINT pin as VCC1 is off. This event will turn off the high side switches by resetting the HSS1-4_CNTL registers. If thermal shutdown event happens while the device is in fail-safe or sleep mode and cyclic sensing is enabled, the cyclic sensing function is lost as HSS4 is turned off.

If TSD is detected by the second sensor which covers the transceivers and VCC2. Both CAN and LIN transmitters is disabled placing them into listen mode. VCC2 LDO is disabled and the interrupt flag is set. This does not cause an SBC state change. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the TSDF temperature, the CAN and LIN transmitters is re-enabled. After 1s of further wait time, VCC2 LDO is turned on. Note that UVCC2 is not set because the LDO has been disabled. Read VCC2_STATUS at register 8'h4F[2] to determine when VCC2 has been re-enabled. If VCC2 is used in the system as the supply source for VCAN, then the VCC2 off condition creates a UVCAN condition. The CAN transceiver changes to wake capable, and cannot be re-enabled until VCC2 is fully powered again. VCC2_STATUS is also indicating the status of VCAN. When VCC2_STATUS=1b, the CAN transceiver is re-enabled and UVCAN interrupt flag can be cleared.

8.3.15.10 Bus Fault Detection and Communication

The TCAN29xx-Q1 provides an optional CAN bus fault detection feature if CAN_FAULT_DET_EN=1b. When enabled, the TCAN29xx-Q1 detects the CAN bus shorted to ground or battery voltage and sets the corresponding interrupt flag as shown in Table 8-20. The bus fault detection is performed while transmitting a dominant signal on the CAN bus. If the fault condition persists for four consecutive dominant-to-recessive bit

transitions, the corresponding interrrupt flag is set. The CAN bus fault interrupt flags can be cleared if the fault condition does not exist for four consecutive dominant-to-recessive bit transitions.

See Figure 8-46 as an example of node locations and how they can impact the ability to determine the actual fault location. Figure 8-47 shows the various bus faults based upon the three-node configuration. Table 8-20 shows what can be detected and by which device.

Bus fault detection is a system level situation. If the fault is occurring at the ECU then the general communication of the bus is compromised. For complete coverage of a node a system level diagnostic step is needed for each node and the ability to communicate this back to a central point.

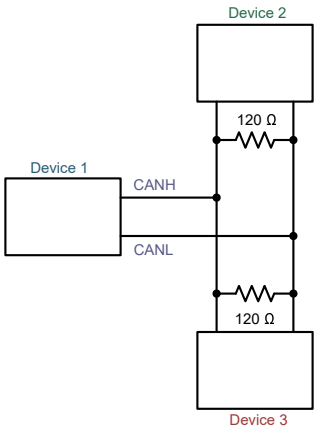

Figure 8-46. Three Node Example

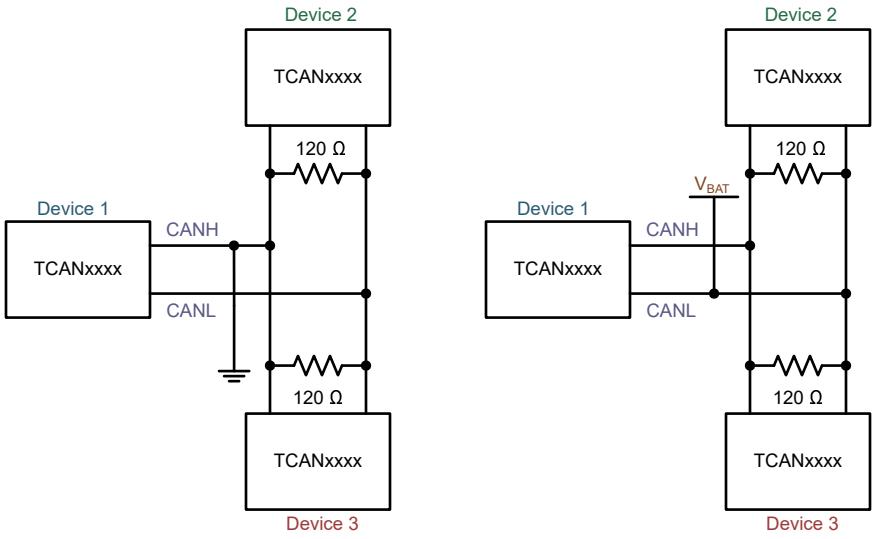

Figure 8-47. Examples of CAN Bus Short Detection

Table 8-20. Bus Fault Pin State and Detection Table

Fault #	CANH	CANL	Interrupt Flag Location
1	Shorted to GND	X	CANBUSGND, 8'h54[1]
2	X	Shorted to V_{bat}	CANBUSVBAT, 8'h54[0]

8.3.16 SPI Communication

The SPI communication uses a standard SPI interface. Physically the digital interface pins are nCS (Chip Select Not), SDI (SPI Data In), SDO (SPI Data Out) and SCK SPI Clock). Each SPI transaction is initiated by a seven bit address with a R/W bit. The device can be configured for one data byte or two date bytes per transaction

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depending upon the value of the BYTE_CNT bit at SPI_CONFIG register 8'h09[3]. The default is one byte. When two byte is selected, the second data byte is for address + 1.

The data shifted out on the SDO pin for the transaction always starts with the register 8'h50[7:0] which is the global interrupt register. This register provides the high-level interrupt status information about the device. The data byte which are the 'response' to the address and R/W byte are shifted out next. See Figure 8-48 and Figure 8-49 for read and write method when cyclic redundancy (CRC) is disabled. For two byte read see Figure 8-51. When a two bite SPI write takes place, the current information in the address and address + 1 is fed back out on the SDO pin, see Figure 8-50

The device defaults to mode 0 where SPI data input data on SDI is sampled on the low to high edge of SCK. The SPI output data on SDO is changed on the high to low edge of SCK. The device can be configured to support Mode 1 - 3 by using MODE_SEL in SPI_CONFIG register 8'h09[1:0]. SPI communication figures are based upon Mode 0.

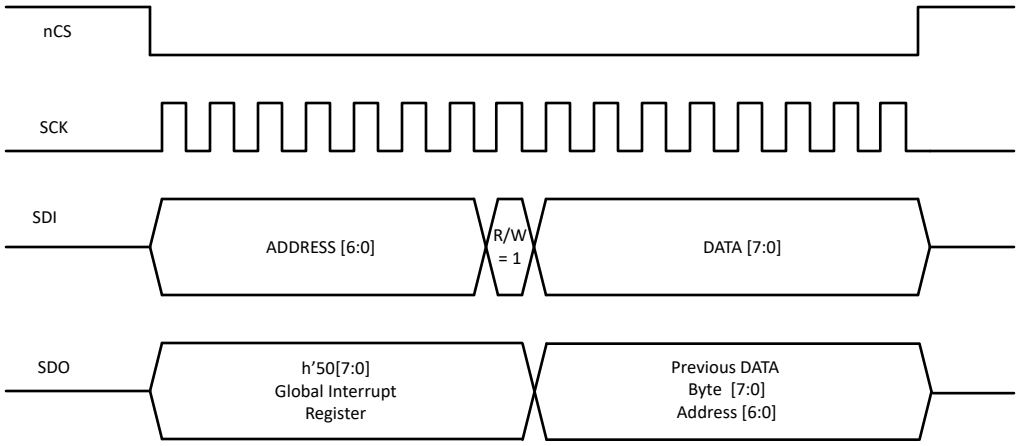

Figure 8-48. SPI Write

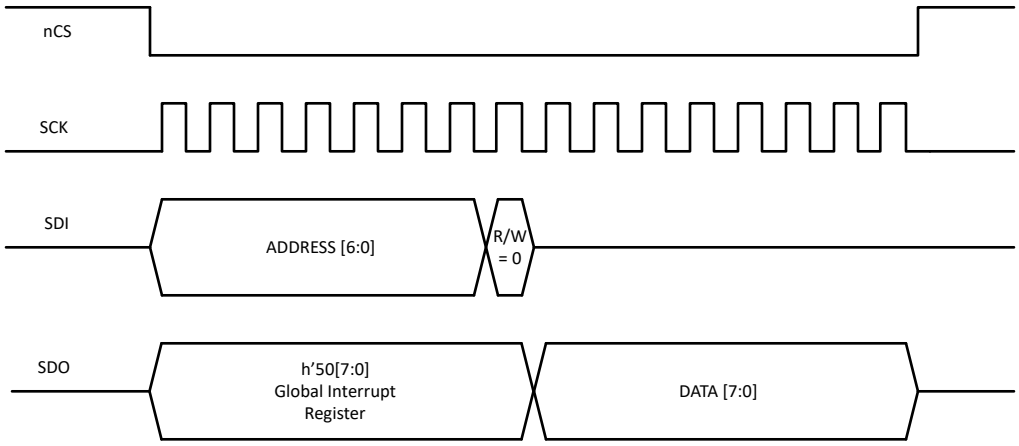

Figure 8-49. SPI Read

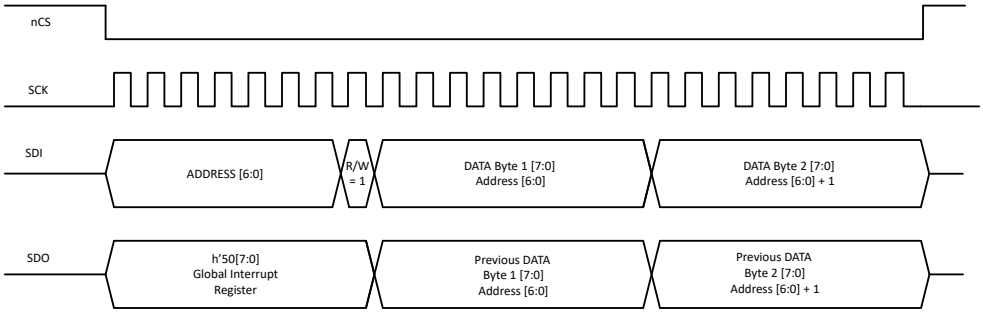

Figure 8-50. Two Byte SPI Write

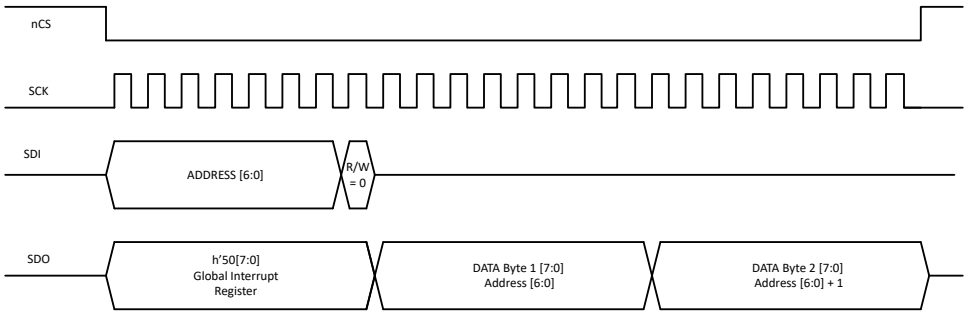

Figure 8-51. Two Byte SPI Read

8.3.16.1 Cyclic Redundancy Check

The TCAN29xx-Q1 family cyclic redundancy check (CRC) for SPI transactions, default disabled. Register 'h0A[0] can be used to enable this feature. The default polynomial supports AutoSAR CRC8H2F, $X^8 + X^5 + X^3 + X^2 + X + 1$, see Table 8-21. CRC8 according to SAE J1850 is also supported and can be selected at register 8'h0B[0]. When CRC is enabled, the a filler byte of 00h is used to calculate the CRC value during a read/write operation, see Figure 8-52 and Figure 8-53 for one byte data that includes CRC. CRC is not implemented when two byte data is configured.

Table 8-21. CRC8H27

SPI Transactions	
CRC result width	8 bits
Polynomial	2Fh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	DFh
Magic Check	42h

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Table 8-22. CRC8 SAE J1850

SPI Transactions	
CRC result width	8 bits
Polynomial	1Dh
Initial value	FFh
Input data reflected	No
Result data reflected	No
XOR value	FFh
Check	4Bh
Magic Check	C4h

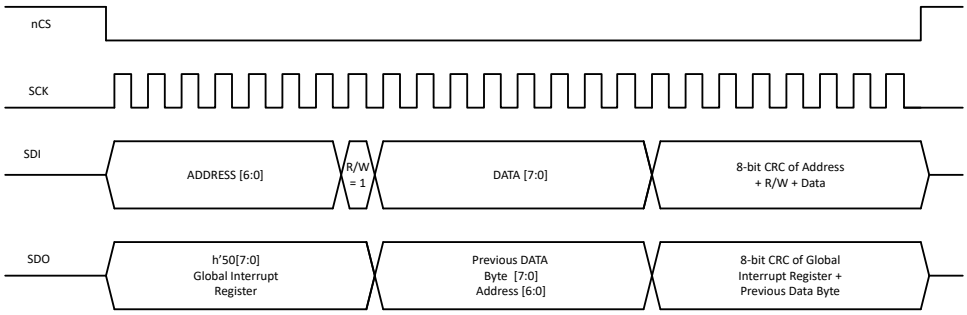

Figure 8-52. One Byte CRC SPI Write

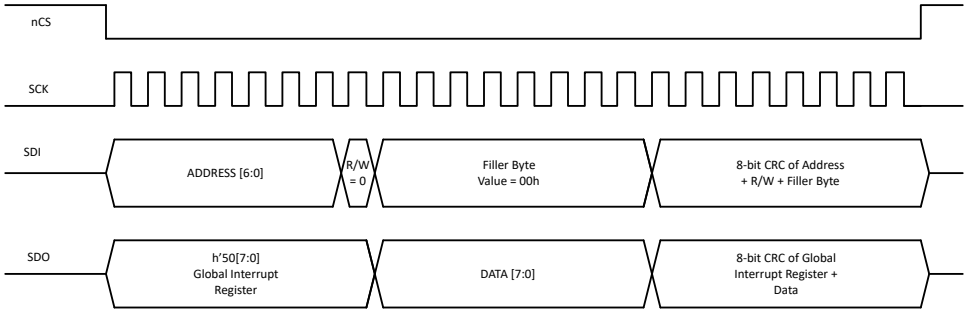

Figure 8-53. One Byte CRC SPI Read

8.3.16.2 Chip Select Not (nCS):

This input pin is used to select the device for a SPI transaction. The pin is active low, so while nCS is high the SPI Data Output (SDO) pin of the device is high impedance allowing an SPI bus to be designed. When nCS is low the SDO driver is activated and communication may be started. The nCS pin is held low for a SPI transaction. A special feature on this device allows the SDO pin to immediately show the Global Fault Flag on a falling edge of nCS.

8.3.16.3 SPI Clock Input (SCK):

This input pin is used to input the clock for the SPI to synchronize the input and output serial data bit streams. The default SPI mode 0 is where data input is sampled on the rising edge of SCK and the SPI data output is changed on the falling edge of the SCK. See Figure 8-54. Figure shown provides the timing based upon Mode 0 which is the default. Table 8-23 provides the configurable modes with the clock phase.

Table 8-23. SPI Modes

Mode	CPOL[1]	CPHA[2]	Clock Phase
0	0	0	Data sampled on rising edge and shifted on falling edge

Table 8-23. SPI Modes (continued)

Mode	CPOL(1)	CPHA(2)	Clock Phase
1	0	1	Data sampled on falling edge and shifted on rising edge
2	1	0	Data sampled on rising edge and shifted on falling edge
3	1	1	Data sampled on falling edge and shifted on rising edge

(1) CPOL is the clock polarity where 0 = logic low and 1 = logic high
(2) CPHA is the clock phase

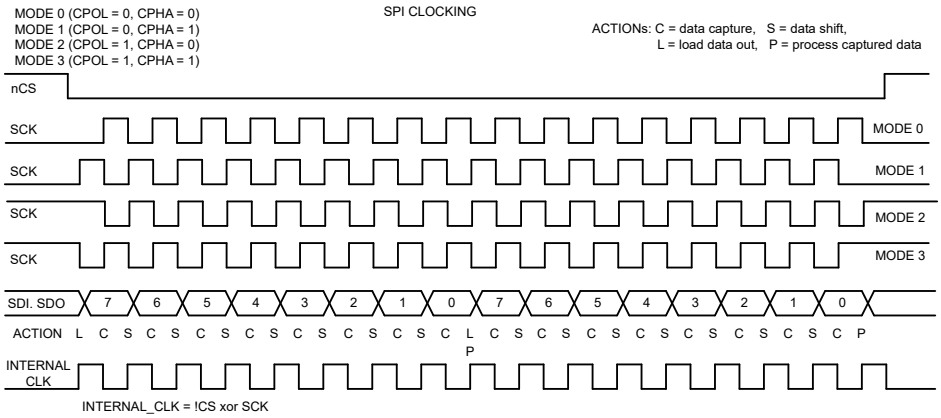

Figure 8-54. SPI Clocking

8.3.16.4 SPI Data Input (SDI):

This input pin is used to shift data into the device. Once the SPI is enabled by a low on nCS, the SDI samples the input shifted data on each rising edge of the SPI clock (SCK). The data is shifted into an 8-bit shift register. After eight (8) clock cycles and shifts, the addressed register is read giving the data to be shifted out on SDO. After eight clock cycles, the shift register is full and the SPI transaction is complete. If the command code is a write, the new data is written into the addressed register only after exactly 8 bits have been shifted in by SCK and the nCS has a rising edge to deselect the device. If there are not exactly 8 bits shifted in to the device during one SPI transaction (nCS low), the SPI command is ignored, the SPIERR flag is set and the data is not written into the device preventing any false actions by the device.

8.3.16.5 SPI Data Output (SDO):

This pin is high impedance until the SPI output is enabled via nCS. Once the SPI is enabled by a low on nCS, the SDO is immediately driven high or low showing the Global Fault Flag status which is also the first bit (bit 7) to be shifted out if the SPI is clocked. On the first falling edge of SCK, the shifting out of the data continues with each falling edge on SCK until all 8 bits have been shifted out the shift register.

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8.4 Device Functional Modes

The TCAN29xx-Q1 has several SBC operating modes: Normal, Standby, Sleep, Restart and Fail-safe. The first three mode selections are made by the SPI register, 8'h10[2:0]. Fail-safe mode is entered due to various fault conditions. The CAN FD and LIN transceivers are independently controlled. See Table 8-24 for the various SBC modes and status of each block during each SBC mode.

Table 8-24. Mode Overview

Module	Restart	Sleep	Standby	Normal	Fail-safe
nINT	High (if VCC1 present) High-Z (UVCC1)	High-Z	Active	Active	High-Z
GFO	Programmed active state (VCC1 present) off others	High-Z	Active	Active	High-Z
SW	Wake capable/Off	Wake capable/Off	Wake capable/ software dev mode	Wake capable/ software dev mode	Wake capable/Off
HSSx	Off	As Programmed	As Programmed	As Programmed	Off
LIMP (Open-drain active low)	Same as previous state: Low from fail-safe mode or from WD error	Previous state prior to entering sleep mode	Previous state prior to entering Standby	Previous state prior to entering Normal mode	Asserted Low
WAKEx	Wake capable/Off	As Programmed	As Programmed	As Programmed	Wake capable/off
CRXD	High (if VCC1 present) High-Z (UVCC1)	High-Z	Transceiver configuration dependent	Transceiver configuration dependent	High-Z
LRXD	High (if VCC1 present) High-Z (UVCC1)	High-Z	Transceiver configuration dependent	Transceiver configuration dependent	High-Z
nRST	Low	Low	High	High	Low
SPI	Off	Off	Active	Active	Off
Watchdog	Off	Off	Configurable, As programmed	Fixed, As programmed in the Standby mode	Off
CAN Transceiver	Wake-capable/Off	Wake-capable/Off	Silent/Wake-capable/Off	On/Silent/Wake-capable/Off	Wake-capable/Off
LIN Transceiver	Wake-capable/Off	Wake-capable/Off	Silent/Wake-capable/Off	On/Silent/Wake-capable/Off	Wake-capable/Off
LIN Bus Termination	Weak current pull-up	Weak current pull-up	35kΩ (typical)	35kΩ (typical)	Weak current pull-up
VCC1	On or Ramping	Off	On	On	Off
VCC2	On or Ramping	As programmed; off by default	On (default); programmable off	On (default); programmable off	Off
VEXCC	On or Ramping	As programmed; off by default	Programmable	Programmable	Off

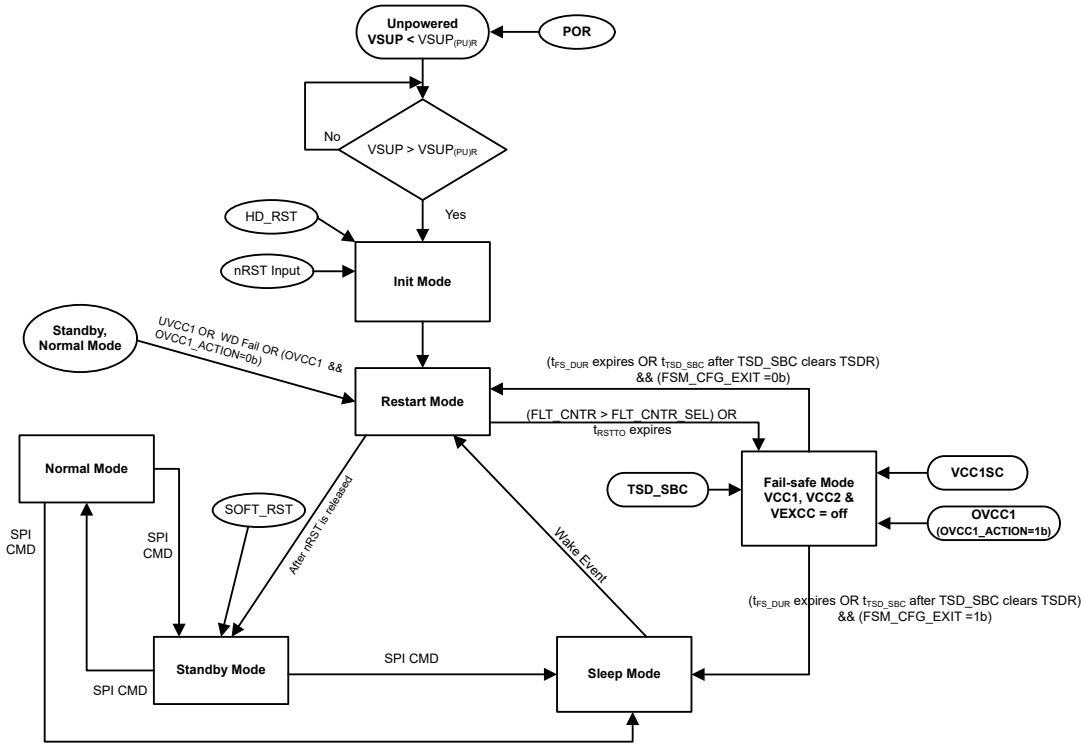

Figure 8-55. Device State Diagram

8.4.1 Init Mode

This is the initial mode of operation upon powering up. This is a transitional mode that is entered once VSUP is above $VSUP_{(PU)R}$ threshold. The device transitions to restart mode once the device defaults are set.

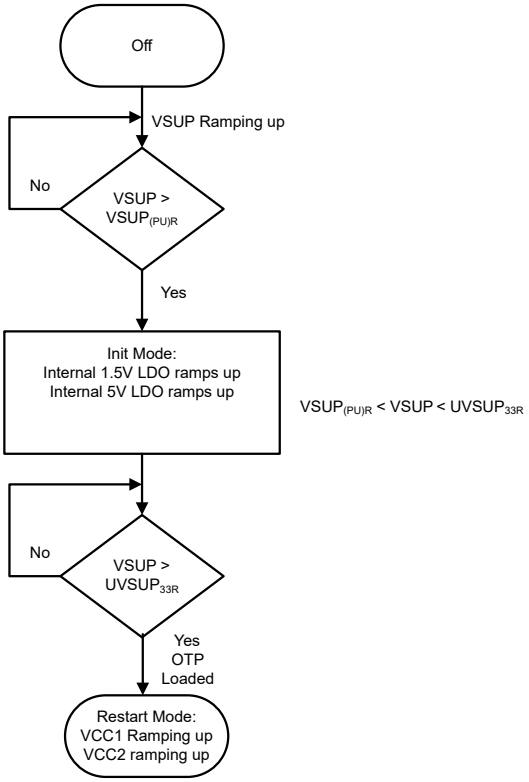

Figure 8-56. Init Mode

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8.4.2 Normal Mode

The SBC Normal mode is the full-function operating mode of the SBC. After power-up, the device enters Standby mode and microcontroller has to move the SBC into Normal mode via SPI command. The SBC can be moved to the low power modes such as Standby mode or Sleep mode via SPI command.

Refer to Table 8-24 for configurability and status of different SBC blocks in the SBC Normal mode.

8.4.3 Standby Mode

Ths SBC Standby mode is the low power mode with VCC1 on. Upon initial power up, the device automatically enters standby mode from Restart mode. This transition happens when VCC1 > $UVCC1_R$ and t_{RSTN_act} time has expired. VCC2 is turned on at power up but is not required to be greater than UVCC2 to transition to standby mode. The device also enters Stabdby mode after existing Restart mode (due to Watchdog or VCC1 faults). The microcontroller can also put the device in Standby mode via SPI command from Normal mode. A wake-up event on CAN, LIN and WAKEx pins create an interrupt but no SBC mode change will occur. Refer to Table 8-24 or configurability and status of different SBC blocks in the SBC Standby mode.

8.4.4 Restart Mode

The SBC Restart mode holds the microncontroller in reset via nRST pin. The SBC Restart mode is entered for multiple reasons:

- At initial power-up, as the regulators are ramping up
- Undervoltage on VCC1 when in SBC Normal and Standby modes
- Overvoltage on VCC1 when in SBC Normal or Standby modes (when OVCC1_ACTION=1b)
- Watchdog failure
- Wake event from SBC Sleep mode or recovery from Fail-safe mode

When the device enters Restart mode, nRST pin is pulled low. The device remains in Restart mode for at least t_{RSTN_act} after VCC1 > $UVCC1_R$ (if entered due to UVCC1) or due to Watchdog fault.

When the SBC Restart mode is entered due to UVCC1 or OVCC1 (with OVCC1_ACTION=0b only), a Restart timer (t_{RSTTO}) is started. If the device does not exit the Restart mode prior to the timer timing out (by clearing VCC1 faults), the device will transition to fail-safe mode.

Each time the Restart mode is entered from Normal or Standby modes due to a fault, the fault counter, FLT_CNTR, is incremented. The device enters Fail-safe mode if the fault counter (FLT_CNTR) reaches the threshold FLT_CNTR_SEL. The FLT_CNTR is cleared when the device enters Fail-safe mode. FLT_CNTR_SEL is programmable using register 8'h28[7:4], which sets the number of times restart can be entered before transitioning to Fail-safe mode, up to 15 times. The counter can be disabled by programming the counter to 0000b. To prevent the transition to Fail-safe mode due to FLT_CNTR overflow, the counter can be cleared periodically by writing Fh into FLT_CNTR.

From SBC Restart mode, the device automatically enters SBC Standby mode if fault counter has not exceeded the threshold or Restart timer has not timed out. nRST pin is released at the transition to SBC Standby mode.

Note

If the fault counter is disabled, configured to 0000b, a loop from restart to standby back to restart is possible due to a constant watchdog failure.

8.4.5 Fail-safe Mode

The device enters Fail-safe mode when certain fault events take place.

Device enters fail-safe mode due to:

- Reaching the FLT_CTR threshold
- Short-circuit event on VCC1
- Thermal shutdown threshold is exceeded in the TSD_SBC sensor
- Internal clock monitoring circuits indicate a fault
- ABIST_ERR_ACTION = 10b and ABIST error flags are set

On entering fail-safe mode:

- Corresponding fault interrupts are set and FSM_SLP_STAT bits are set to indicate the readon for the Fail-safe mode entry
  - Interrupts and the FSM_SLP_STAT can be read after recovery into Standby mode
- LIMP pin is activated
- VCC1, VCC2 and VEXCC are turned off
- HSSx are turned off
- WAKEx pins mointor for wake events if they were configured to do so.
- FLT_CNTR is reset

Device exits fail-safe mode after t_{FS_DUR} , except in the case of entering Fail-safe mode due to TSD_SBC. In case of TSD_SBC triggering the Fail-safe mode entry, the device exits the Fail-safe mode 1s after the temperature drops below the TSDR threshold (thermal shutdown release).

After existing the Fail-safe mode, the device enters:

- Restart mode if FSM_EXIT_CFG =0b
- Sleep mode if FSM_EXIT_CFG =1b. If there were pending wake events from the Fail-safe mode, the device exits Sleep mode and enters Restart mode
  - If no wakes were enabled, CAN and LIN transceivers are set to wake-capable when entering Sleep mode from Fail-safe mode.

If the faults causing Fail-safe mode entry still exist in Restart mode, the device enters fail-safe mode again.

8.4.6 Sleep Mode

The SBC Sleep mode is the power saving mode for the device. Sleep mode can be entered via SPI command from Standby or Normal mode. Sleep mode may also be entered from Fail-safe mode if FSM_EXIT_CFG is set to 1b.

To enter Sleep mode via SPI command:

- All existing wake interrupts must be cleared.
- At least one wake source must be configured ON for Sleep mode

If the above conditions are not met, the device does not enter Sleep mode and sets a MODE_ERR interrupt, 8'h5A[3]. In addition, attempt to enter Sleep mode without clearing wake interrupts will send the device to Standby mode via Restart mode.

While the device is in sleep mode, the following conditions exist.

- VCC1 is turned off
- VCC2 is fixed as configured before entering Sleep mode
- VEXCC is fixed as configured before entering Sleep mode
- CAN changes to wake-capable or OFF as per the configuration
- LIN changes to wake-capable or OFF as per the configuration
- WAKE pins are as configured.
- If cyclic sensing function is enabled for Sleep mode, HSS4 or HSS3 (if HSS4 configured as a WAKE pin) will periodically turn on.
- SW pin wake function will be enabled if configured to do so.
- Long duration timer (LDT) runs as configured for the Sleep mode

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9 Device Registers

Table 9-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 9-1 must be considered as reserved locations and the register contents should not be modified.

Table 9-1. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	DEVICE_ID_29xx	Device Part Number	Section 9.1
8h	REV_ID	Major and Minor Revision	Section 9.2
9h	SPI_CONFIG	SPI mode configuration	Section 9.3
Ah	CRC_CNTL	SPI CRC control	Section 9.4
Bh	CRC_POLY_SET	Sets SPI CRC polynomial	Section 9.5
Ch	SBC_CONFIG	SBC, HSS and VCC2 select	Section 9.6
Dh	VREG_CONFIG1	Configures VCC1 regulator	Section 9.7
Eh	SBC_CONFIG1	SBC Configuration	Section 9.8
Fh	GEN_PURPOSE_REG1	Read and Write General purpose Register	Section 9.9
10h	CAN_CNTRL_1	CAN transceiver 1 control	Section 9.10
11h	WAKE_PIN_CONFIG1	WAKE pin configuration 1	Section 9.11
12h	WAKE_PIN_CONFIG2	WAKE pin configuration 2	Section 9.12
13h	WD_CONFIG_1	Watchdog configuration 1	Section 9.13
14h	WD_CONFIG_2	Watchdog configuration 2	Section 9.14
15h	WD_INPUT_TRIG	Watchdog input trigger	Section 9.15
16h	WD_RST_PULSE	Watchdog output pulse width	Section 9.16
17h	FSM_CONFIG	Fail safe mode configuration	Section 9.17
19h	DEVICE_CONFIG0	Device reset	Section 9.18
1Ah	DEVICE_CONFIG1	Device configuration 1	Section 9.19
1Bh	DEVICE_CONFIG2	Device configuration 2	Section 9.20
1Ch	LDT_TIMER	Long Duration Timer	Section 9.21
1Dh	LIN_CNTL	LIN configuration	Section 9.22
1Eh	HSS_CNTL	High side switch 1 and 2 control	Section 9.23
1Fh	DEVICE_CONFIG3	HSS low power enable and VEXCC load sharing current limit	Section 9.24
20h	PWM1_CNTL1	PWM1 Frequency and MSB bits of duty cycle	Section 9.25
21h	PWM1_CNTL2	PWM1 eight LSB bits of duty cycle	Section 9.26
23h	PWM2_CNTL1	PWM2 Frequency and two MSB bits of duty cycle	Section 9.27
24h	PWM2_CNTL2	PWM2 eight LSB bits of duty cycle	Section 9.28
25h	TIMER1_CONFIG	High side switch timer 1 configuration	Section 9.29
26h	TIMER2_CONFIG	High side switch timer 2 configuration	Section 9.30
28h	FLT_CNTR	Restart counter configuration	Section 9.31
29h	nRST_GFO_CNTL	nRST and GFO pin control	Section 9.32
2Ah	WAKE_PIN_CONFIG3	Wake pin enabling and reporting which WAKE pin caused the wake event	Section 9.33
2Bh	WAKE_PIN_CONFIG4	WAKE2 and WAKE3 threshold and status	Section 9.34
2Dh	WD_QA_CONFIG	Q/A Watchdog configuration	Section 9.35
2Eh	WD_QA_ANSWR	Q/A Answer register	Section 9.36
2Fh	WD_QA_QUESTION	Q/A question register	Section 9.37
4Bh	ABIST_CONFIG	ABIST configuration. Applicable only to TCAN29xxB (ASIL-B) device versions. Not applicable to QM device versions	Section 9.38

Table 9-1. DEVICE Registers (continued)

Offset	Acronym	Register Name	Section
4Ch	ABIST_STATUS	ABIST Run status. Applicable only to TCAN29xxB (ASIL-B) device versions. Not applicable to QM device versions	Section 9.39
4Dh	HSS_CNTL2	HSS3 and HSS4 configuration	Section 9.40
4Fh	HSS_CNTL3	HSS OV/UV action configuration and LDO status bits	Section 9.41
50h	INT_GLOBAL	Global Interrupt register	Section 9.42
51h	INT_1	Interrupt 1	Section 9.43
52h	INT_2	Interrupt 2	Section 9.44
53h	INT_3	Interrupt 3	Section 9.45
54h	INT_CANBUS_1	CAN interrupt	Section 9.46
55h	INT_7	Interrupt 7	Section 9.47
56h	INT_EN_1	Masking bits for INT_1	Section 9.48
57h	INT_EN_2	Masking bits for INT_2	Section 9.49
58h	INT_EN_3	Masking bits for INT_3	Section 9.50
59h	INT_EN_CANBUS_1	Masking bits for INT_CANBUS_1	Section 9.51
5Ah	INT_4	Interrupt 4	Section 9.52
5Bh	INT_5	Interrupt 5	Section 9.53
5Ch	INT_6	Interrupt 6	Section 9.54
5Eh	INT_EN_4	Masking bits for INT_4	Section 9.55
5Fh	INT_EN_5	Masking bits for INT_5	Section 9.56
60h	INT_EN_6	Masking bits for INT_6	Section 9.57
62h	INT_EN_7	Masking bits for INT_7	Section 9.58
63h	INT_BIST1	ABIST related interrupts	Section 9.59
64h	INT_BIST2	ABIST related interrupts	Section 9.60
75h	GEN_PURPOSE_REG2		Section 9.61
76h	GEN_PURPOSE_REG3		Section 9.62
77h	GEN_PURPOSE_REG4		Section 9.63
78h	ID_PIN_STATUS	WAKE pin connection status bits for hardware ID	Section 9.64
79h	WAKE_ID_CONFIG1	Enabling the hardware ID function for WAKE1-2	Section 9.65
7Ah	WAKE_ID_CONFIG2	Enabling the hardware ID function for WAKE3	Section 9.66
7Bh	WAKE_PIN_CONFIG5		Section 9.67

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Complex bit access types are encoded to fit into small table cells. Table 9-2 shows the codes that are used for access types in this section.

Table 9-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W0C	W 0C	Write 0 to clear
W1C	W 1C	Write 1 to clear
Reset or Default Value		

Table 9-2. Device Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

9.1 DEVICE_ID_29xx Register (Offset = 0h) [Reset = 00h]

DEVICE_ID_29xx is shown in Figure 9-1 and described in Table 9-3.

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Device part number. Offset = 0h + y; where y = 0h to 7h

Figure 9-1. DEVICE_ID_29xx Register

7	6	5	4	3	2	1	0
DEVICE_ID							
R-00000000b							

Table 9-3. DEVICE_ID_29xx Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEVICE_ID	R	00000000b	The DEVICE_ID[1:8] registers determine the part number of the device. The reset values and value of each DEVICE_ID register are listed for the corresponding register address Address 00h = 43h = C Address 01h = 32h = 2 Address 02h = 39h = 9 Address 03h = 34h = 4 (TCAN294xx-Q1) (non-SIC) Address 03h = 35h = 5 (TCAN295xx-Q1) (SIC) Address 04h = 35h = 5 for TCAN29x5x-Q1 (w/o LIN) Address 04h = 37h = 7 for TCAN29x7x-Q1 (w/ LIN) Address 05h = 33h = 3 for TCAN29xx3-Q1 (3.3V) Address 05h = 35h = 5 for TCAN29xx5-Q1 (5V) Address 06h = 42h = B for TCAN29xxxB-Q1 (ASIL-B) Address 06h = 4Dh = M for TCAN29xxxM-Q1 (QM) Address 07h = RSVD

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9.2 REV_ID Register (Offset = 8h) [Reset = 1Xh]

REV_ID is shown in Figure 9-2 and described in Table 9-4.

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Figure 9-2. REV_ID Register

7	6	5	4	3	2	1	0
Major_Revision				Minor_Revision			
RH-0001b				RH-xxxxb			

Table 9-4. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Major_Revision	RH	0001b	Major die revision indicates the full layer revisions. 1h indicates the original revision. 0001b = 1
3-0	Minor_Revision	RH	xxxxb	Minor die revision to indicates metal layer revisions 0000b = 0 0001b = 1

9.3 SPI_CONFIG Register (Offset = 9h) [Reset = 00h]

SPI_CONFIG is shown in Figure 9-3 and described in Table 9-5.

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Figure 9-3. SPI_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED				BYTE_CNT	SDI_POL	SPI_MODE	
R-0b				R/W-0b	R/W-0b	R/W-00b	

Table 9-5. SPI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved
3	BYTE_CNT	R/W	0b	Selects the data byte count for a read or write operation. Note that for two byte configuration, SPI CRC is not available 0b = One byte 1b = Two byte
2	SDI_POL	R/W	0b	Selects the idle polarity of the SDI input pin by configuring the internal pull-up or pull-down resistor configuration 0b = Pull-down 1b = Pull-up
1-0	SPI_MODE	R/W	00b	Configures the SPI mode 00b = Mode 0 (CPOL is 0, CPHA is 0) 01b = Mode 1 (CPOL is 0, CPHA is 1) 10b = Mode 2 (CPOL is 1, CPHA is 0) 11b = Mode 3 (CPOL is 1, CPHA is 1)

9.4 CRC_CNTL Register (Offset = Ah) [Reset = 00h]

CRC_CNTL is shown in Figure 9-4 and described in Table 9-6.

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Figure 9-4. CRC_CNTL Register

7	6	5	4	3	2	1	0
RESERVED							CRC_EN
R-0b							R/W-0b

Table 9-6. CRC_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0b	Reserved
0	CRC_EN	R/W	0b	SPI CRC 8 control. Note: CRC cannot be enabled in SPI two-byte mode (bit is always set to 0b if BYTE_CNT=1b) 0b = Disable 1b = Enable

9.5 CRC_POLY_SET Register (Offset = Bh) [Reset = 00h]

CRC_POLY_SET is shown in Figure 9-5 and described in Table 9-7.

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Figure 9-5. CRC_POLY_SET Register

7	6	5	4	3	2	1	0
RESERVED							POLY_8_SET
R-0b							R/W-0b

Table 9-7. CRC_POLY_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0b	Reserved
0	POLY_8_SET	R/W	0b	Sets the 8-bit polynomial for CRC. 0b = X^8 + X^5 + X^3 + X^2 + X + 1 (0x2F) 1b = X^8 + X^4 + X^3 + X^2 + 1 (0x1D SAE J1850)

9.6 SBC_CONFIG Register (Offset = Ch) [Reset = 06h]

SBC_CONFIG is shown in Figure 9-6 and described in Table 9-8.

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Figure 9-6. SBC_CONFIG Register

7	6	5	4	3	2	1	0
VCC1_OV_SEL	VEXCC_ILIM_DIS	PWM_SEL	RESERVED	SBC_MODE_SEL		VCC2_CFG	
R/W-0b	R/W-0b	R/W-0b	R-0b	RH/W-01b		R/W-10b	

Table 9-8. SBC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VCC1_OV_SEL	R/W	0b	OVCC1 threshold selection bit 0b = Lower threshold 1b = Higher threshold
6	VEXCC_ILIM_DIS	R/W	0b	VEXCC current limit disable 0b = Enabled 1b = Disabled
5	PWM_SEL	R/W	0b	Determines which PWM is selected for programming 0b = PWM1 and PWM2 1b = PWM3 and PWM4
4	RESERVED	R	0b	Reserved
3-2	SBC_MODE_SEL	RH/W	01b	Determines the mode that the SBC is in 00b = Sleep 01b = Standby 10b = Normal 11b = Reserved
1-0	VCC2_CFG	R/W	10b	VCC2 voltage regulator configuration 00b = VCC2 off in all SBC modes 01b = VCC2 on in all SBC modes except Failsafe 10b = VCC2 on in all SBC modes except Sleep and Failsafe 11b = Reserved

9.7 VREG_CONFIG1 Register (Offset = Dh) [Reset = 00h]

VREG_CONFIG1 is shown in Figure 9-7 and described in Table 9-9.

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Figure 9-7. VREG_CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED		VEXT_CFG		VCC1_SINK	VEXT_V_CFG		
R-0b		R/W-00b		R/W-0b	R/W-000b		

Table 9-9. VREG_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	Reserved
5-4	VEXT_CFG	R/W	00b	VEXCC external PNP configuration 00b = Off in all SBC modes 01b = On in all SBC modes except Fail-safe mode 10b = On in all SBC modes except Sleep and Fail-safe modes 11b = RSVD
3	VCC1_SINK	R/W	0b	VCC1 current sink strength selection 0b = 10µA 1b = 1000µA
2-0	VEXT_V_CFG	R/W	000b	External PNP voltage control 000b = 1.8V 001b = 2.5V 010b = 3.3V 011b = 5V 100b = Load sharing

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9.8 SBC_CONFIG1 Register (Offset = Eh) [Reset = 01h]

SBC_CONFIG1 is shown in Figure 9-8 and described in Table 9-10.

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Figure 9-8. SBC_CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	UVCC1_SEL		RESERVED	SW_WAKE_EN	SW_POL_SEL
R-0b	R-0b	R-0b	R/W-00b		R-0b	R/W-0b	R/W-1b

Table 9-10. SBC_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	RESERVED	R	0b	Reserved
5	RESERVED	R	0b	Reserved
4-3	UVCC1_SEL	R/W	00b	VCC1 under-voltage threshold selection 00b = Threshold 1 01b = Threshold 2 10b = Threshold 3 11b = Threshold 4
2	RESERVED	R	0b	Reserved
1	SW_WAKE_EN	R/W	0b	Enables the SW pin to become a digital wake up pin 0b = Disabled 1b = Enabled
0	SW_POL_SEL	R/W	1b	SW pin polarity select 0b = Active low 1b = Active high

9.9 GEN_PURPOSE_REG1 Register (Offset = Fh) [Reset = 00h]

GEN_PURPOSE_REG1 is shown in Figure 9-9 and described in Table 9-11.

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Figure 9-9. GEN_PURPOSE_REG1 Register

7	6	5	4	3	2	1	0
GEN_PURPOSE_REG1							
R/W-00000000b							

Table 9-11. GEN_PURPOSE_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GEN_PURPOSE_REG1	R/W	00000000b	General Purpose Register1. Store generic information or test SPI communication

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9.10 CAN_CNTRL_1 Register (Offset = 10h) [Reset = 04h]

CAN_CNTRL_1 is shown in Figure 9-10 and described in Table 9-12.

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Figure 9-10. CAN_CNTRL_1 Register

7	6	5	4	3	2	1	0
RSVD	TXD_DTO_DIS	CAN_FAULT_DET_EN	CAN_WUP_PATTERN	RESERVED	CAN1_TRX_SEL		
R-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-100b		

Table 9-12. CAN_CNTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	Reserved 0b = Disabled 1b = Enabled
6	TXD_DTO_DIS	R/W	0b	CAN TXD Dominant time out disable control 0b = Enabled 1b = Disabled
5	CAN_FAULT_DET_EN	R/W	0b	CAN bus fault detection enable 0b = Disabled 1b = Enabled
4	CAN_WUP_PATTERN	R/W	0b	Determines CAN or CAN-XL style WUP 0b = D/R/D 1b = D/R/D/R (XL)
3	RESERVED	R	0b	Reserved
2-0	CAN1_TRX_SEL	R/W	100b	CAN transceiver control 000b = Off 001b = Reserved 010b = SBC Mode Control WUP disabled 011b = Reserved 100b = Wake capable 101b = Listen 110b = SBC Mode Control 111b = On

9.11 WAKE_PIN_CONFIG1 Register (Offset = 11h) [Reset = 00h]

WAKE_PIN_CONFIG1 is shown in Figure 9-11 and described in Table 9-13.

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Figure 9-11. WAKE_PIN_CONFIG1 Register

7	6	5	4	3	2	1	0
WAKE_CONFIG		WAKE1_STAT	WAKE_VBAT_MON	RESERVED		RESERVED	
R/W-00b		RH-0b	R/W-0b	R-0b		R-0b	

Table 9-13. WAKE_PIN_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WAKE_CONFIG	R/W	00b	Wake pin configuration: Note: Pulse requires more programming 00b = Bi-directional - either edge 01b = Rising edge 10b = Falling edge 11b = Reserved
5	WAKE1_STAT	RH	0b	Provides status of WAKE1 pin. 0b = Low 1b = High
4	WAKE_VBAT_MON	R/W	0b	Closes the switch between WAKE1 and WAKE2 enabling VBAT monitoring capability. br# Note: When WAKE_VBAT_MON is on, WAKE1 and WAKE2 cannot be used as local wake input pins. 0b = Off (default) 1b = On
3-2	RESERVED	R	0b	Reserved
1-0	RESERVED	R	0b	Reserved

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9.12 WAKE_PIN_CONFIG2 Register (Offset = 12h) [Reset = 02h]

WAKE_PIN_CONFIG2 is shown in Figure 9-12 and described in Table 9-14.

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Figure 9-12. WAKE_PIN_CONFIG2 Register

7	6	5	4	3	2	1	0
RESERVED	WAKE1_SENSE/ OV_WAKE12SW_DIS	TWK_CYC_SET	nINT_SEL		RXD_WK_CONFIG	WAKE1_LEVEL	
R-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-10b	

Table 9-14. WAKE_PIN_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	WAKE1_SENSE/ OV_WAKE12SW_DIS	R/W	0b	This bit is a dual function bit which is determined by how the WAKE_VBAT_MON bit is configured: When WAKE_VBAT_MON = 0b the bit is WAKE1_SENSE and configures the WAKE1 pin for static or cyclic wake 0b = Static 1b = Cyclic When WAKE_VBAT_MON = 1b the bit becomes OV_WAKE12SW_DIS, which is used to enable/disable the internal switch between WAKE1 and WAKE2 pins under OVHSS condition 0b = Switch is disabled due to OVHSS and re-enabled when the voltage is below OVHSS threshold 1b = Switch remains enabled even under OVHSS condition 0b = Static/ WAKE12 switch disabled due to OVHSS 1b = Cyclic/WAKE12 switch remains enabled under OVHSS
5	TWK_CYC_SET	R/W	0b	Sets the tWK_CYC time (µs) for determining WAKE pin status for cyclic sensing for all WAKE pins 0b = 35µs 1b = 100µs
4-3	nINT_SEL	R/W	00b	nINT configuration selection 00b = Global interrupt 01b = Watchdog failure output 10b = Bus fault interrupt 11b = Wake request
2	RXD_WK_CONFIG	R/W	0b	Configures RXD pin behavior from a wake event 0b = Pulled low 1b = Toggle
1-0	WAKE1_LEVEL	R/W	10b	Sets the WAKE1 pin input thresholds. 00b = Reserved 01b = 2.5V 10b = 4V 11b = 6V

9.13 WD_CONFIG_1 Register (Offset = 13h) [Reset = 82h]

WD_CONFIG_1 is shown in Figure 9-13 and described in Table 9-15.

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Figure 9-13. WD_CONFIG_1 Register

7	6	5	4	3	2	1	0
WD_CONFIG		WD_PRE		WD_STBY_EN_ON_WK	WD_STBY_TYPE	WD_LW_SEL	
R/W-10b		R/W-00b		R/W-0b	R/W-0b	R/W-10b	

Table 9-15. WD_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_CONFIG	R/W	10b	Watchdog configuration 00b = Disabled 01b = Timeout 10b = Window 11b = Q&A
5-4	WD_PRE	R/W	00b	Watchdog prescalar 00b = Factor 1 01b = Factor 2 10b = Factor 3 11b = Factor 4
3	WD_STBY_EN_ON_WK	R/W	0b	Enables the watchdog in Stabdy mode (if WD is disabled in Stabdby mode) on wake event. WD will start with long window and then switch to the programmed watchdog per WD_STBY_TYPE
2	WD_STBY_TYPE	R/W	0b	Selects the watchdog type in Standby mode if enabled 0b = Timeout 1b = Matches the watchdog type in Normal mode
1-0	WD_LW_SEL	R/W	10b	Selects the long window duration in Standby mode. 00b = 150 ms 01b = 300 ms 10b = 600 ms (default) 11b = 1000 ms

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9.14 WD_CONFIG_2 Register (Offset = 14h) [Reset = 60h]

WD_CONFIG_2 is shown in Figure 9-14 and described in Table 9-16.

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Figure 9-14. WD_CONFIG_2 Register

7	6	5	4	3	2	1	0
WD_TIMER			WD_ERR_CNT				WD_STBY_DIS
R/W-011b			RH-0000b				R/W-0b

Table 9-16. WD_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	WD_TIMER	R/W	011b	Sets window or timeout times based upon the WD_PRE setting, See WD_TIMER table
4-1	WD_ERR_CNT	RH	0000b	Watchdog error counter Running count of errors up to 15 errors
0	WD_STBY_DIS	R/W	0b	Disables the watchdog in standby mode. 0b = Enabled 1b = Disabled

9.15 WD_INPUT_TRIG Register (Offset = 15h) [Reset = 00h]

WD_INPUT_TRIG is shown in Figure 9-15 and described in Table 9-17.

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Figure 9-15. WD_INPUT_TRIG Register

7	6	5	4	3	2	1	0
WD_INPUT							
R/W1C-00000000b							

Table 9-17. WD_INPUT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_INPUT	R/W1C	00000000b	Write FFh to trigger WD at appropriate time

9.16 WD_RST_PULSE Register (Offset = 16h) [Reset = 00h]

WD_RST_PULSE is shown in Figure 9-16 and described in Table 9-18.

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Figure 9-16. WD_RST_PULSE Register

7	6	5	4	3	2	1	0
WD_ERR_CNT_SET				FLT_CNTR			
R/W-0000b				RH/W1C-0000b			

Table 9-18. WD_RST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	WD_ERR_CNT_SET	R/W	0000b	Sets the watchdog event error counter that upon overflow the watchdog output and action will trigger
3-0	FLT_CNTR	RH/W1C	0000b	Provides the number of times the device has entered restart mode due to a fault and can be cleared prior to reaching the FLT_CNTR_SEL value. The counter is cleared on entering fail-safe mode or when the FLT_CNTR_SEL value is changed

9.17 FSM_CONFIG Register (Offset = 17h) [Reset = 10h]

FSM_CONFIG is shown in Figure 9-17 and described in Table 9-19.

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Figure 9-17. FSM_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED			OVCC1_ACTION	FSM_SLP_STAT			FSM_EXIT_CFG
R-0b			R/W-1b	RH-000b			R/W-0b

Table 9-19. FSM_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved
4	OVCC1_ACTION	R/W	1b	Action to take if OVCC1 event occurs. OVCC1 interrupt is set. 0b = LIMP pin is activated. No SBC mode change 1b = Enter restart mode, increment FLT_CNTR and activate LIMP pin
3-1	FSM_SLP_STAT	RH	000b	Reason for entering fai-lsafe or sleep mode 000b = Status Clear 001b = Thermal shut down event 010b = ABIST FAIL (ASIL-B version devices only) 011b = VCC1 fault 100b = OTP CRC Error (ASIL-B only) 101b = OSC Check Fail 110b = Reserved 111b = Fault counter exceeded These values are held until cleared by writing oh to FSM_CNTR_STAT
0	FSM_EXIT_CFG	R/W	0b	Configures how fail-safe mode is exited 0b = Auto exit to restart mode after tFS_DUR 1b = Auto exit to Sleep mode after tFS_DUR

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9.18 DEVICE_CONFIG0 Register (Offset = 19h) [Reset = 00h]

DEVICE_CONFIG0 is shown in Figure 9-18 and described in Table 9-20.

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Figure 9-18. DEVICE_CONFIG0 Register

7	6	5	4	3	2	1	0
NVM_REV				RESERVED		SF_RST	HD_RST
R-0000b				R-0b		R/W1C-0b	R/W1C-0b

Table 9-20. DEVICE_CONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	NVM_REV	R	0000b	Internal NVM revision
3-2	RESERVED	R	0b	Reserved
1	SF_RST	R/W1C	0b	Soft Reset: Writing a 1 causes a soft reset. Device registers return to default values while keeping the regulators on. No reset is generated on the nRST pin POR bit is also cleared due to soft reset.
0	HD_RST	R/W1C	0b	Hard Reset: Forces a power on reset on writing a 1. This will set the PWRON interrupt flag. Reset is generated on the nRST pin.

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9.19 DEVICE_CONFIG1 Register (Offset = 1Ah) [Reset = 00h]

DEVICE_CONFIG1 is shown in Figure 9-19 and described in Table 9-21.

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Figure 9-19. DEVICE_CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED	LIMP_RD_EN	LIMP_STATE	RESERVED	LIMP_SEL_RESET		LIMP_RESET	RESERVED
R-0b	R/W-0b	RH-0b	R-0b	R/W-00b		R/W1C-0b	R-0b

Table 9-21. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	LIMP_RD_EN	R/W	0b	Enables the LIMP pin read back buffer to provide the status of the LIMP pin and reflected at LIMP_STATE 0b = Disabled 1b = Enabled
5	LIMP_STATE	RH	0b	Reads back the state of the LIMP pin 0b = Inactive 1b = Active
4	RESERVED	R	0b	Reserved
3-2	LIMP_SEL_RESET	R/W	00b	Selects the method to reset/turn off LIMP 00b = On third successful input tirgger the error counter receives 01b = First correct input trigger 10b = Reserved 11b = Reserved
1	LIMP_RESET	R/W1C	0b	LIMP reset
0	RESERVED	R	0b	Reserved

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9.20 DEVICE_CONFIG2 Register (Offset = 1Bh) [Reset = 00h]

DEVICE_CONFIG2 is shown in Figure 9-20 and described in Table 9-22.

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Figure 9-20. DEVICE_CONFIG2 Register

7	6	5	4	3	2	1	0
RESERVED						RESERVED	nINT_TOG_EN
R-0b						R-0b	R/W-0b

Table 9-22. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0b	Reserved
1	RESERVED	R	0b	Reserved
0	nINT_TOG_EN	R/W	0b	Enables the nINT pin to toggle instead of being latched low for an interrupt 0b = Disabled 1b = Enabled

9.21 LDT_TIMER Register (Offset = 1Ch) [Reset = 28h]

LDT_TIMER is shown in Figure 9-21 and described in Table 9-23.

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Figure 9-21. LDT_TIMER Register

7	6	5	4	3	2	1	0
LDT_EN	LDT_TIMER_SET				LDT_FUNCTION		RESERVED
R/W-0b	R/W-0101b				R/W-00b		R-0b

Table 9-23. LDT_TIMER Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDT_EN	R/W	0b	Enbables the Long Duration Timer. When expired, the device enters Sleep state. 0b = Disabled 1b = Enabled
6-3	LDT_TIMER_SET	R/W	0101b	Sets the Long Duration Time 0000b = 5s 0001b = 10s 0010b = 30s 0011b = 1m 0100b = 15m 0101b = 30m 0110b = 1h 0111b = 2h 1000b = 6h 1001b = 12h 1010b = 1d 1011b = 2d 1100b = 3d 1101b = 4d 1110b = 5d 1111b = 7d
2-1	LDT_FUNCTION	R/W	00b	Configures the action to perform when the LDT expires 00b = Set interrupt only. No mode change 01b = Enter Sleep mode after the LDT expires 10b = LDT starts when SBC enters Sleep mode via SPI and wakes up from Sleep mode after the LDT expires. 11b = Start the LDT timer in the current mode and enter Sleep mode on LDT expiry. Start the LDT timer in Sleep mode and wake up from Sleep mode when LDT expires again
0	RESERVED	R	0b	Reserved

9.22 LIN_CNTL Register (Offset = 1Dh) [Reset = 20h]

LIN_CNTL is shown in Figure 9-22 and described in Table 9-24.

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Figure 9-22. LIN_CNTL Register

7	6	5	4	3	2	1	0
LIN_TRX_CNTRL			LIN1_TXD_DTO_DIS	RESERVED			
RH/W-001b			R/W-0b	R-0b			

Table 9-24. LIN_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LIN_TRX_CNTRL	RH/W	001b	LIN transceiver control 000b = Off 001b = Wake Capable 010b = On 011b = Fast 100b = Listen 101b = SBC Mode Control 110b = Reserved 111b = Reserved
4	LIN1_TXD_DTO_DIS	R/W	0b	LIN LTXD1 dominant state timeout disable 0b = Enabled 1b = Disabled
3-0	RESERVED	R	0b	Reserved

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9.23 HSS_CNTL Register (Offset = 1Eh) [Reset = 00h]

HSS_CNTL is shown in Figure 9-23 and described in Table 9-25.

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Figure 9-23. HSS_CNTL Register

7	6	5	4	3	2	1	0
HSS1_CNTL				HSS2_CNTL			
R/W-0000b				R/W-0000b			

Table 9-25. HSS_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HSS1_CNTL	R/W	0000b	Control for high side switch 1 0000b = Off 0001b = PWM1 0010b = PWM2 0011b = Timer1 0100b = Timer2 0101b = On 0110b = PWM3 0111b = PWM4 1000b = Direct Drive with slow slew rate setting 1001b = Direct Drive with faster slew rate setting
3-0	HSS2_CNTL	R/W	0000b	Control for high side switch 2 0000b = Off 0001b = PWM1 0010b = PWM2 0011b = Timer1 0100b = Timer2 0101b = On 0110b = PWM3 0111b = PWM4 1000b = Direct Drive with slow slew rate setting 1001b = Direct Drive with faster slew rate setting

9.24 DEVICE_CONFIG3 Register (Offset = 1Fh) [Reset = 00h]

DEVICE_CONFIG3 is shown in Figure 9-24 and described in Table 9-26.

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Figure 9-24. DEVICE_CONFIG3 Register

7	6	5	4	3	2	1	0
HSS4_LP_EN	HSS3_LP_EN	HSS2_LP_EN	HSS1_LP_EN	VEXCC_VCC1_LOAD_RATIO			RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-000b			R-0b

Table 9-26. DEVICE_CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSS4_LP_EN	R/W	0b	Configures the low power mode for HSS4. Note: Overcurrent and open load detection are not available in low power mode. Recommendation is to check for these faults by turning on the HSS in regular mode before turning on the low power mode. 0b = Low power mode disabled 1b = Low power mode enabled
6	HSS3_LP_EN	R/W	0b	Configures the low power mode for HSS3 Note: Overcurrent and open load detection are not available in low power mode. Recommendation is to check for these faults by turning on the HSS in regular mode before turning on the low power mode. 0b = Low power mode disabled 1b = Low power mode enabled
5	HSS2_LP_EN	R/W	0b	Configures the low power mode for HSS2 Note: Overcurrent and open load detection are not available in low power mode. Recommendation is to check for these faults by turning on the HSS in regular mode before turning on the low power mode. 0b = Low power mode disabled 1b = Low power mode enabled
4	HSS1_LP_EN	R/W	0b	Configures the low power mode for HSS1 Note: Overcurrent and open load detection are not available in low power mode. Recommendation is to check for these faults by turning on the HSS in regular mode before turning on the low power mode. 0b = Low power mode disabled 1b = Low power mode enabled
3-1	VEXCC_VCC1_LOAD_RATIO	R/W	000b	Configures the load sharing ratio VEXCC/VCC1 based on the external sense resistor value. Refer to the look-up table for the ratio vs external resistor value 000b = Ratio 1 001b = Ratio 2 010b = Ratio 3 011b = Ratio 4 100b = Ratio 5 101b = Ratio 6 110b = Ratio 7 111b = Ratio 8
0	RESERVED	R	0b	Reserved

9.25 PWM1_CNTL1 Register (Offset = 20h) [Reset = 00h]

PWM1_CNTL1 is shown in Figure 9-25 and described in Table 9-27.

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Figure 9-25. PWM1_CNTL1 Register

7	6	5	4	3	2	1	0
PWM1_FREQ	RESERVED					PWM1_DC_MSB	
R/W-0b	R-0b					R/W-00b	

Table 9-27. PWM1_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM1_FREQ	R/W	0b	Selects PWM1 frequency (Hz) 0b = 200 1b = 400
6-2	RESERVED	R	0b	Reserved
1-0	PWM1_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM1 duty cycle select. Works with 'h21[7:0] 00b = 100% off when used with 'h21[7:0] 11b = 100% on when used with h21[7:0]

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9.26 PWM1_CNTL2 Register (Offset = 21h) [Reset = 00h]

PWM1_CNTL2 is shown in Figure 9-26 and described in Table 9-28.

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Figure 9-26. PWM1_CNTL2 Register

7	6	5	4	3	2	1	0
PWM1_DC							
R/W-00000000b							

Table 9-28. PWM1_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM1_DC	R/W	00000000b	Bits 7-0 for 10-bit PWM1 duty cycle select. Works with 'h20[1:0]

9.27 PWM2_CNTL1 Register (Offset = 23h) [Reset = 00h]

PWM2_CNTL1 is shown in Figure 9-27 and described in Table 9-29.

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Figure 9-27. PWM2_CNTL1 Register

7	6	5	4	3	2	1	0
PWM2_FREQ	RESERVED					PWM2_DC_MSB	
R/W-0b	R-0b					R/W-00b	

Table 9-29. PWM2_CNTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PWM2_FREQ	R/W	0b	Selects PWM2 frequency (Hz) 0b = 200 1b = 400
6-2	RESERVED	R	0b	Reserved
1-0	PWM2_DC_MSB	R/W	00b	Most significant two bits for 10-bit PWM2 duty cycle select. Works with 'h24[7:0] 00b = 100% off when used with 'h24[7:0] 11b = 100% on when used with 'h24[7:0]

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9.28 PWM2_CNTL2 Register (Offset = 24h) [Reset = 00h]

PWM2_CNTL2 is shown in Figure 9-28 and described in Table 9-30.

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Figure 9-28. PWM2_CNTL2 Register

7	6	5	4	3	2	1	0
PWM2_DC							
R/W-00000000b							

Table 9-30. PWM2_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PWM2_DC	R/W	00000000b	Bits 7-0 for 10-bit PWM2 duty cycle select. Works with 'h23[1:0]

9.29 TIMER1_CONFIG Register (Offset = 25h) [Reset = 00h]

TIMER1_CONFIG is shown in Figure 9-29 and described in Table 9-31.

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Figure 9-29. TIMER1_CONFIG Register

7	6	5	4	3	2	1	0
TIMER1_ON_WIDTH				TIMER1_CYC_WK_EN	TIMER1_PERIOD		
R/W-0000b				R/W-0b	R/W-000b		

Table 9-31. TIMER1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER1_ON_WIDTH	R/W	0000b	Sets the high side switch on time (ms) for timer 1 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = Reserved
3	TIMER1_CYC_WK_EN	R/W	0b	Enables Cyclic Wake using Timer 1 0b = Disabled 1b = Enabled
2-0	TIMER1_PERIOD	R/W	000b	Sets the timer period (ms) for timer 1 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

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9.30 TIMER2_CONFIG Register (Offset = 26h) [Reset = 00h]

TIMER2_CONFIG is shown in Figure 9-30 and described in Table 9-32.

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Figure 9-30. TIMER2_CONFIG Register

7	6	5	4	3	2	1	0
TIMER2_ON_WIDTH				TIMER2_CYC_WK_EN	TIMER2_PERIOD		
R/W-0000b				R/W-0b	R/W-000b		

Table 9-32. TIMER2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TIMER2_ON_WIDTH	R/W	0000b	Sets the high side switch on time (ms) for timer 2 0000b = Off (HSS is high impedance) 0001b = 0.1 0010b = 0.3 0011b = 0.5 0100b = 1 0101b = 10 0110b = 20 0111b = 30 1000b = 40 1001b = 50 1010b = 60 1011b = 80 1100b = 100 1101b = 150 1110b = 200 1111b = Reserved
3	TIMER2_CYC_WK_EN	R/W	0b	Enables Cyclic Wake using Timer 2 0b = Disabled 1b = Enabled
2-0	TIMER2_PERIOD	R/W	000b	Sets the timer period (ms) for timer 2 000b = 10 001b = 20 010b = 50 011b = 100 100b = 200 101b = 500 110b = 1000 111b = 2000

9.31 FLT_CNTR Register (Offset = 28h) [Reset = 00h]

FLT_CNTR is shown in Figure 9-31 and described in Table 9-33.

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Figure 9-31. FLT_CNTR Register

7	6	5	4	3	2	1	0
FLT_CNTR_SEL				RESERVED			
R/W-0000b				R-0b			

Table 9-33. FLT_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FLT_CNTR_SEL	R/W	0000b	Selects the number of times the device can enter restart mode prior to device entering fail-safe mode, 0 to 15 times. Note: Writing 0h disables the fault counter. The device moves between the Restart to Standby mode until the root cause for the Restart entry is fixed (WD fail or UV/OVCC1)
3-0	RESERVED	R	0b	Reserved

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9.32 nRST_GFO_CNTL Register (Offset = 29h) [Reset = 0Ch]

nRST_GFO_CNTL is shown in Figure 9-32 and described in Table 9-34.

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Figure 9-32. nRST_GFO_CNTL Register

7	6	5	4	3	2	1	0
RESERVED		nRST_PULSE_WIDTH	GFO_POL_SEL	GFO_SEL			RESERVED
R-0b		R/W-0b	R/W-0b	R/W-110b			R-0b

Table 9-34. nRST_GFO_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	Reserved
5	nRST_PULSE_WIDTH	R/W	0b	Sets the pulse width for nRST when the device enters restart mode due to WD failure or nRST release delay after VCC1 clears UVCC1 threshold 0b = 2ms 1b = 1 ms
4	GFO_POL_SEL	R/W	0b	Selects the polarity for the GFO pin Note: When 8'h29[3:1] = 110b, this bit determines the state of the GFO output 0b = Active low 1b = Active high
3-1	GFO_SEL	R/W	110b	Selects the information that will cause this pin to be pulled to the state selected by 'h29[4] for tNRST_TOG except for when general purpose output is selected 000b = VCC1/2 interrupt (overvoltage, undervoltage or short) 001b = WD interrupt event (each one) 010b = Reserved 011b = Local wake request (LWU) 100b = Bus wake request (WUP) 101b = Restart counter exceeded (indicated in standby mode) 110b = General purpose output 111b = CAN Bus fault
0	RESERVED	R	0b	Reserved

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9.33 WAKE_PIN_CONFIG3 Register (Offset = 2Ah) [Reset = E0h]

WAKE_PIN_CONFIG3 is shown in Figure 9-33 and described in Table 9-35.

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Figure 9-33. WAKE_PIN_CONFIG3 Register

7	6	5	4	3	2	1	0
WAKE3_PIN_SET	WAKE2_PIN_SET	WAKE1_PIN_SET	WAKE4_PIN_SET/HSS4_DIS	WAKE4_WAKE	WAKE3_WAKE	WAKE2_WAKE	WAKE1_WAKE
R/W-1b	R/W-1b	R/W-1b	R/W-0b	R/W0C-0b	R/W0C-0b	R/W0C-0b	R/W0C-0b

Table 9-35. WAKE_PIN_CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE3_PIN_SET	R/W	1b	Configures whether WAKE3 is active or inactive 0b = WAKE3 inactive 1b = WAKE3 active
6	WAKE2_PIN_SET	R/W	1b	Configures whether WAKE2 is active or inactive 0b = WAKE2 inactive 1b = WAKE2 active
5	WAKE1_PIN_SET	R/W	1b	Configures whether WAKE1 is active or inactive 0b = WAKE1 inactive 1b = WAKE1 active
4	WAKE4_PIN_SET/ HSS4_DIS	R/W	0b	Configures WAKE4 function at HSS4/WAKE4 pin. Setting this bit to 1b sets HSS4_CNTL = 000b, disabling HSS4 at HSS4/WAKE4 pin 0b = WAKE4 inactive 1b = WAKE4 active
3	WAKE4_WAKE	R/W0C	0b	Indicates if there was a wake event on WAKE4 pin 0b = No wake event on WAKE4 1b = Wake event on WAKE4
2	WAKE3_WAKE	R/W0C	0b	Indicates if there was a wake event on WAKE3 pin 0b = No wake event on WAKE3 1b = Wake event on WAKE3
1	WAKE2_WAKE	R/W0C	0b	Indicates if there was a wake event on WAKE2 pin 0b = No wake event on WAKE2 1b = Wake event on WAKE2
0	WAKE1_WAKE	R/W0C	0b	Indicates if there was a wake event on WAKE1 pin 0b = No wake event on WAKE1 1b = Wake event on WAKE1

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9.34 WAKE_PIN_CONFIG4 Register (Offset = 2Bh) [Reset = 22h]

WAKE_PIN_CONFIG4 is shown in Figure 9-34 and described in Table 9-36.

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Figure 9-34. WAKE_PIN_CONFIG4 Register

7	6	5	4	3	2	1	0
WAKE2_SENSE	WAKE2_STAT	WAKE2_LEVEL		WAKE3_SENSE	WAKE3_STAT	WAKE3_LEVEL	
R/W-0b	RH-0b	R/W-10b		R/W-0b	RH-0b	R/W-10b	

Table 9-36. WAKE_PIN_CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE2_SENSE	R/W	0b	WAKE2 pin configured for static or cyclic wake 0b = Static 1b = Cyclic
6	WAKE2_STAT	RH	0b	Provides status of WAKE2 pin. 0b = Low 1b = High
5-4	WAKE2_LEVEL	R/W	10b	Sets the WAKE2 pin input thresholds. 00b = Reserved 01b = 2.5V 10b = 4V 11b = 6V
3	WAKE3_SENSE	R/W	0b	WAKE3 pin configured for static or cyclic wake 0b = Static 1b = Cyclic
2	WAKE3_STAT	RH	0b	Provides status of WAKE3 pin. 0b = Low 1b = High
1-0	WAKE3_LEVEL	R/W	10b	Sets the WAKE3 pin input thresholds. Note: When using WAKE3 as a direct drive input, the pin thresholds are automatically configured by the device as 0.7*VCC1 for VIH-min and 0.3*VCC1 for VIL-max 00b = Reserved 01b = 2.5V 10b = 4V 11b = 6V

9.35 WD_QA_CONFIG Register (Offset = 2Dh) [Reset = 0Ah]

WD_QA_CONFIG is shown in Figure 9-35 and described in Table 9-37.

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Figure 9-35. WD_QA_CONFIG Register

7	6	5	4	3	2	1	0
WD_ANSW_GEN_CFG		WD_QA_POLY_CFG		WD_QA_POLY_SEED			
R/W-00b		R/W-00b		R/W-1010b			

Table 9-37. WD_QA_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	WD_ANSW_GEN_CFG	R/W	00b	WD answer generation configuration
5-4	WD_QA_POLY_CFG	R/W	00b	WD Q&A polynomial configuration
3-0	WD_QA_POLY_SEED	R/W	1010b	WD Q&A polynomial seed value loaded when device is in the RESET state

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9.36 WD_QA_ANSWR Register (Offset = 2Eh) [Reset = 00h]

WD_QA_ANSWR is shown in Figure 9-36 and described in Table 9-38.

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Figure 9-36. WD_QA_ANSWR Register

7	6	5	4	3	2	1	0
WD_QA_ANSWER							
R/W1C-00000000b							

Table 9-38. WD_QA_ANSWR Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	WD_QA_ANSWER	R/W1C	00000000b	MCU Q&A Watchdog answer byte

9.37 WD_QA_QUESTION Register (Offset = 2Fh) [Reset = 3Ch]

WD_QA_QUESTION is shown in Figure 9-37 and described in Table 9-39.

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Figure 9-37. WD_QA_QUESTION Register

7	6	5	4	3	2	1	0
RESERVED	QA_ERROR	WD_ANSW_CNT		WD_QUESTION			
R-0b	R/W1C-0b	RH-11b		RH-1100b			

Table 9-39. WD_QA_QUESTION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	QA_ERROR	R/W1C	0b	Watchdog Q&A answer error flag
5-4	WD_ANSW_CNT	RH	11b	Current state of received watchdog Q&A error counter
3-0	WD_QUESTION	RH	1100b	Current watchdog question value

9.38 ABIST_CONFIG Register (Offset = 4Bh) [Reset = 04h]

ABIST_CONFIG is shown in Figure 9-38 and described in Table 9-40.

Return to the Summary Table.

Applicable only to TCAN29xxB (ASIL-B) device versions. Not applicable to QM device versions

Figure 9-38. ABIST_CONFIG Register

7	6	5	4	3	2	1	0
ABIST_RUN_CMD	ENABLE_BGXMON	ENABLE_IBIASMON	ENABLE_CLKMON	RESERVED	ABIST_INT_EN	ABIST_ERR_ACTION	
RH/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-1b	R/W-00b	

Table 9-40. ABIST_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ABIST_RUN_CMD	RH/W	0b	Enable ABIST run by writing 1h into this register to start ABIST on demand. The bit clears after ABIST is completed and ready to run again 0b = ABIST is currently not running 1b = Writing 1b Starts ABIST and bit read 1b until ABIST completes
6	ENABLE_BGXMON	R/W	0b	Enables the bandgap cross-monitoring function in ASIL-B version of the devices. When enabled this function runs continuously in Normal mode and periodically in low power nodes to save power 0b = Bandgap cross-monitoring is disabled 1b = Bandgap cross-monitoring is enabled
5	ENABLE_IBIASMON	R/W	0b	Enables the internal bias current monitoring function in ASIL-B version of the devices. When enabled this function runs continuously in Normal mode and periodically in low power nodes to save power 0b = Bias current monitoring is disabled 1b = Bias current monitoring is enabled
4	ENABLE_CLKMON	R/W	0b	Enables the 1MHz clock monitoring in ASIL-B version of the devices. 0b = 1MHz clock monitoring is disabled 1b = 1MHz clock monitoring is enabled
3	RESERVED	R	0b	Reserved
2	ABIST_INT_EN	R/W	1b	Enable/disable nINT pin mask for the ABIST interrupt flags 0b = Masks the ABIST interrupts from activating the nINT pin 1b = Activates the nINT pin due to ABIST interrupts
1-0	ABIST_ERR_ACTION	R/W	00b	Configure the action to take in case of ABIST failure 00b = No action, only set the corresponding BIST fail interrupts 01b = Turn on LIMP 10b = Device enters fail-safe mode and turns on LIMP 11b = Reserved

9.39 ABIST_STATUS Register (Offset = 4Ch) [Reset = 00h]

ABIST_STATUS is shown in Figure 9-39 and described in Table 9-41.

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Applicable only to TCAN29xxB, (ASIL-B) device versions. Not applicable to QM device versions

Figure 9-39. ABIST_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ABIST_DONE
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	RH-0b

Table 9-41. ABIST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	RESERVED	R	0b	Reserved
5	RESERVED	R	0b	Reserved
4	RESERVED	R	0b	Reserved
3	RESERVED	R	0b	Reserved
2	RESERVED	R	0b	Reserved
1	RESERVED	R	0b	Reserved
0	ABIST_DONE	RH	0b	Provides the status of ABIST of internal clocks 0b = Not done 1b = Done

9.40 HSS_CNTL2 Register (Offset = 4Dh) [Reset = 00h]

HSS_CNTL2 is shown in Figure 9-40 and described in Table 9-42.

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Figure 9-40. HSS_CNTL2 Register

7	6	5	4	3	2	1	0
HSS3_CNTL				HSS4_CNTL			
R/W-0000b				R/W-0000b			

Table 9-42. HSS_CNTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HSS3_CNTL	R/W	0000b	Control for high side switch 3 0000b = Off 0001b = PWM1 0010b = PWM2 0011b = Timer1 0100b = Timer2 0101b = On 0110b = PWM3 0111b = PWM4 1000b = Direct Drive with slow slew rate setting 1001b = Direct Drive with faster slew rate setting
3-0	HSS4_CNTL	R/W	0000b	Control for high side switch 4. Configuring Wake functionality at using WAKE4_PIN_SET sets these bits to 0h (disabled HSS function at HSS4/WAKE4) 0000b = Off 0001b = PWM1 0010b = PWM2 0011b = Timer1 0100b = Timer2 0101b = On 0110b = PWM3 0111b = PWM4 1000b = Direct Drive with slow slew rate setting 1001b = Direct Drive with faster slew rate setting

9.41 HSS_CNTL3 Register (Offset = 4Fh) [Reset = 00h]

HSS_CNTL3 is shown in Figure 9-41 and described in Table 9-43.

Return to the Summary Table.

Figure 9-41. HSS_CNTL3 Register

7	6	5	4	3	2	1	0
HSS_OV_SD_DIS	HSS_UV_SD_DIS	HSS_OV_UV_REC	RESERVED	VEXCC_STATUS	VCC2_STATUS	VCAN_STATUS	HSS_OC_FLTR
R/W-0b	R/W-0b	R/W-0b	R-0b	RH-0b	RH-0b	RH-0b	R/W-0b

Table 9-43. HSS_CNTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSS_OV_SD_DIS	R/W	0b	Disables high-side switches from shutting down due to an OVHSS event 0b = HSS shut off due to OVHSS 1b = HSS do not shut-off due to OVHSS
6	HSS_UV_SD_DIS	R/W	0b	Disables high-side switches from shutting down due to an UVHSS event 0b = HSS shut off due to OVHSS 1b = HSS do not shut-off due to OVHSS
5	HSS_OV_UV_REC	R/W	0b	Disables the high-side switches from automatically recovering to the previous state due to an OVHSS or UVHSS event 0b = HSS recover automatically after OVHSS/UVHSS faults removed 1b = HSS do not recover automatically after OVHSS/UVHSS faults removed. SPI command necessary to restart HSS
4	RESERVED	R	0b	Reserved
3	VEXCC_STATUS	RH	0b	Provides the status of the VEXCC regulator 0b = UVEXCC or off 1b = In regulation
2	VCC2_STATUS	RH	0b	VCC2 LDO status 0b = UVCC2 or off 1b = In regulation
1	VCAN_STATUS	RH	0b	VCAN LDO status 0b = UVCAN or off 1b = In regulation
0	HSS_OC_FLTR	R/W	0b	Configures the HSS overcurrent filter time between the short and long duration. Applies to all four HSS. 0b = short duration filter 1b = long duration filter

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9.42 INT_GLOBAL Register (Offset = 50h) [Reset = 00h]

INT_GLOBAL is shown in Figure 9-42 and described in Table 9-44.

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Figure 9-42. INT_GLOBAL Register

7	6	5	4	3	2	1	0
INT_7	INT_1	INT_2	INT_3	INT_CANBUS	INT_4	INT_BIST1_OR_INT_BIST2	INT_5_OR_INT_6
RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	RH-0b	RH-0b

Table 9-44. INT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_7	RH	0b	Logical OR of INT_7
6	INT_1	RH	0b	Logical OR of INT_1
5	INT_2	RH	0b	Logical OR of INT_2
4	INT_3	RH	0b	Logical OR of INT_3
3	INT_CANBUS	RH	0b	Logical OR of INT_CANBUS register
2	INT_4	RH	0b	Logical OR of INT_4
1	INT_BIST1_OR_INT_BIST2	RH	0b	Logical OR of INT_BIST1, INT_BIST2
0	INT_5_OR_INT_6	RH	0b	Logical OR of INT_5, INT_6

9.43 INT_1 Register (Offset = 51h) [Reset = 00h]

INT_1 is shown in Figure 9-43 and described in Table 9-45.

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Figure 9-43. INT_1 Register

7	6	5	4	3	2	1	0
WD	CANINT_1	LWU	LDT	RESERVED	CANSLNT_1	SWPIN_WU	CANDOM_1
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-45. INT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD	R/W1C	0b	Watchdog event interrupt. NOTE: This interrupt bit will be set for every watchdog error event and does not rely upon the Watchdog error counter
6	CANINT_1	R/W1C	0b	CAN bus wake up interrupt
5	LWU	R/W1C	0b	Local wake up
4	LDT	R/W1C	0b	Long Duration Timer bit is set when the LDT timer has expires
3	RESERVED	R	0b	Reserved
2	CANSLNT_1	R/W1C	0b	CAN bus inactive for tSILENCE
1	SWPIN_WU	R/W1C	0b	SW pin wake up interrupt
0	CANDOM_1	R/W1C	0b	CAN bus stuck dominant

9.44 INT_2 Register (Offset = 52h) [Reset = 40h]

INT_2 is shown in Figure 9-44 and described in Table 9-46.

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Figure 9-44. INT_2 Register

7	6	5	4	3	2	1	0
RESERVED	PWRON	OVCC1	UVSUP5	UVSUP3	UVCC1	TSD_SBC	RESERVED
R-0b	R/W1C-1b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R-0b

Table 9-46. INT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	PWRON	R/W1C	1b	Power on
5	OVCC1	R/W1C	0b	VCC1 overvoltage
4	UVSUP5	R/W1C	0b	UVSUP5 undervoltage
3	UVSUP3	R/W1C	0b	UVSUP3 undervoltage
2	UVCC1	R/W1C	0b	VCC1 undervoltage
1	TSD_SBC	R/W1C	0b	SBC Thermal Shutdown due to VCC1, VEXCC Or HSS
0	RESERVED	R	0b	Reserved

9.45 INT_3 Register (Offset = 53h) [Reset = 00h]

INT_3 is shown in Figure 9-45 and described in Table 9-47.

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Figure 9-45. INT_3 Register

7	6	5	4	3	2	1	0
SPIERR	RESERVED	FSM	CRCERR	VCC1SC	FLT_CNT	TSD_CAN_LIN	CRC_OTP
R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-47. INT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR	R/W1C	0b	Sets when SPI status bit sets
6	RESERVED	R	0b	Reserved
5	FSM	R/W1C	0b	Entered fail-safe mode
4	CRCERR	R/W1C	0b	SPI transcation CRC error detected
3	VCC1SC	R/W1C	0b	VCC1 short detected
2	FLT_CNT	R/W1C	0b	Restart counter exceeded programmed count
1	TSD_CAN_LIN	R/W1C	0b	Thermal Shutdown due to VCC2 or CAN or LIN
0	CRC_OTP	R/W1C	0b	OTP CRC error

9.46 INT_CANBUS_1 Register (Offset = 54h) [Reset = 00h]

INT_CANBUS_1 is shown in Figure 9-46 and described in Table 9-48.

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Figure 9-46. INT_CANBUS_1 Register

7	6	5	4	3	2	1	0
UVCAN	RESERVED					CANBUSGND	CANBUSBAT
R/W1C-0b	R-0b					R/W1C-0b	R/W1C-0b

Table 9-48. INT_CANBUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVCAN	R/W1C	0b	UVCAN interrupt
6-2	RESERVED	R	0b	Reserved
1	CANBUSGND	R/W1C	0b	CAN bus shorted to GND or CANH shorted to GND
0	CANBUSBAT	R/W1C	0b	CAN bus shorted to Vbat or CANL shorted to Vbat

9.47 INT_7 Register (Offset = 55h) [Reset = 00h]

INT_7 is shown in Figure 9-47 and described in Table 9-49.

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Figure 9-47. INT_7 Register

7	6	5	4	3	2	1	0
HSSOC1	HSSOL1	HSSOC2	HSSOL2	HSSOC3	HSSOL3	HSSOC4	HSSOL4
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-49. INT_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSOC1	R/W1C	0b	High side switch 1 over current
6	HSSOL1	R/W1C	0b	High side switch 1 open load
5	HSSOC2	R/W1C	0b	High side switch 2 over current
4	HSSOL2	R/W1C	0b	High side switch 2 open load
3	HSSOC3	R/W1C	0b	High side switch 3 over current
2	HSSOL3	R/W1C	0b	High side switch 3 open load
1	HSSOC4	R/W1C	0b	High side switch 4 over current
0	HSSOL4	R/W1C	0b	High side switch 4 open load

9.48 INT_EN_1 Register (Offset = 56h) [Reset = F7h]

INT_EN_1 is shown in Figure 9-48 and described in Table 9-50.

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Figure 9-48. INT_EN_1 Register

7	6	5	4	3	2	1	0
WD_EN	CANINT_EN	LWU_EN	LDT_INT_EN	RESERVED	CANSLNT_EN	SWPIN_WU_EN	CANDOM_EN
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b

Table 9-50. INT_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WD_EN	R/W	1b	Watchdog event detected mask
6	CANINT_EN	R/W	1b	CAN bus wake up interrupt mask
5	LWU_EN	R/W	1b	Local wake up mask
4	LDT_INT_EN	R/W	1b	LDT mask
3	RESERVED	R	0b	Reserved
2	CANSLNT_EN	R/W	1b	CAN silent mask
1	SWPIN_WU_EN	R/W	1b	SW pin wake up interrupt mask
0	CANDOM_EN	R/W	1b	CAN bus stuck dominant mask

9.49 INT_EN_2 Register (Offset = 57h) [Reset = 7Eh]

INT_EN_2 is shown in Figure 9-49 and described in Table 9-51.

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Figure 9-49. INT_EN_2 Register

7	6	5	4	3	2	1	0
RESERVED	PWRON_EN	OVCC1_EN	UVSUP5_EN	UVSUP3_EN	UVCC1_EN	TSD_SBC_EN	SME_EN
R-0b	R-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-0b

Table 9-51. INT_EN_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	PWRON_EN	R	1b	Power on flag enable (not changeable)
5	OVCC1_EN	R/W	1b	VCC1 overvoltage mask
4	UVSUP5_EN	R/W	1b	VSUP5 undervoltage mask
3	UVSUP3_EN	R/W	1b	UVSUP3 undervoltage mask
2	UVCC1_EN	R/W	1b	VCC1 undervoltage mask
1	TSD_SBC_EN	R/W	1b	Masking bit for SBC Thermal Shutdown
0	SME_EN	R	0b	SME enable (read-only)

9.50 INT_EN_3 Register (Offset = 58h) [Reset = BFh]

INT_EN_3 is shown in Figure 9-50 and described in Table 9-52.

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Figure 9-50. INT_EN_3 Register

7	6	5	4	3	2	1	0
SPIERR_EN	RESERVED	FSM_EN	CRCERR_EN	VCC1SC_EN	FLT_CNT_EN	TSD_CAN_EN	OTP_CRC_EN
R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-1b

Table 9-52. INT_EN_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SPIERR_EN	R/W	1b	SPI error interrupt mask
6	RESERVED	R	0b	Reserved
5	FSM_EN	R/W	1b	Fail-safe status flag mask
4	CRCERR_EN	R/W	1b	SPI CRC error interrupt mask
3	VCC1SC_EN	R/W	1b	VCC1 short circuit interrupt mask
2	FLT_CNT_EN	R/W	1b	Restart counter exceeded programmed count mask
1	TSD_CAN_EN	R/W	1b	Masking bit for CAN/VCC2 thermal shutdown
0	OTP_CRC_EN	R	1b	OTP CRC Error (not maskable)

9.51 INT_EN_CANBUS_1 Register (Offset = 59h) [Reset = 83h]

INT_EN_CANBUS_1 is shown in Figure 9-51 and described in Table 9-53.

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Figure 9-51. INT_EN_CANBUS_1 Register

7	6	5	4	3	2	1	0
UVCAN_EN	RESERVED					CANBUSGND_EN	CANBUSBAT_EN
R/W-1b	R-0b					R/W-1b	R/W-1b

Table 9-53. INT_EN_CANBUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UVCAN_EN	R/W	1b	UVCAN interrupt mask
6-2	RESERVED	R	0b	Reserved
1	CANBUSGND_EN	R/W	1b	CAN bus shorted to GND enable
0	CANBUSBAT_EN	R/W	1b	CAN bus shorted to Vbat enable

9.52 INT_4 Register (Offset = 5Ah) [Reset = 00h]

INT_4 is shown in Figure 9-52 and described in Table 9-54.

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Figure 9-52. INT_4 Register

7	6	5	4	3	2	1	0
LIN_WUP	LIN_DTO	RESERVED	LDT_WAKE	MODE_ERR	OVHSS	RESERVED	UVHSS
R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b

Table 9-54. INT_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN_WUP	R/W1C	0b	LIN bus wake
6	LIN_DTO	R/W1C	0b	LIN dominant state timeout, LTXD_DTO
5	RESERVED	R	0b	Reserved
4	LDT_WAKE	R/W1C	0b	LDT Wake interrupt from Sleep
3	MODE_ERR	R/W1C	0b	Illegal transceiver state for mode change request
2	OVHSS	R/W1C	0b	VHSS over-voltage for high-side switches
1	RESERVED	R	0b	Reserved
0	UVHSS	R/W1C	0b	VHSS under-voltage for high-side switches

9.53 INT_5 Register (Offset = 5Bh) [Reset = 00h]

INT_5 is shown in Figure 9-53 and described in Table 9-55.

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Figure 9-53. INT_5 Register

7	6	5	4	3	2	1	0
VCC1OC	VCC2OC	VEXCCOC	CLKMON_FAIL	HSS4_READBACK_FAIL	HSS3_READBACK_FAIL	HSS2_READBACK_FAIL	HSS1_READBACK_FAIL
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-55. INT_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VCC1OC	R/W1C	0b	VCC1 LDO in overcurrent condition
6	VCC2OC	R/W1C	0b	VCC2 LDO in overcurrent condition
5	VEXCCOC	R/W1C	0b	VEXCC LDO in overcurrent condition
4	CLKMON_FAIL	R/W1C	0b	Internal clock monitor fail interrupt.
3	HSS4_READBACK_FAIL	R/W1C	0b	HSS4 readback check has failed
2	HSS3_READBACK_FAIL	R/W1C	0b	HSS3 readback check has failed
1	HSS2_READBACK_FAIL	R/W1C	0b	HSS2 readback check has failed
0	HSS1_READBACK_FAIL	R/W1C	0b	HSS1 readback check has failed

9.54 INT_6 Register (Offset = 5Ch) [Reset = 00h]

INT_6 is shown in Figure 9-54 and described in Table 9-56.

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Figure 9-54. INT_6 Register

7	6	5	4	3	2	1	0
TSDW	UVCC1PW	UVEXCC	OVEXCC	VEXCCSC	UVCC2	OVCC2	VCC2SC
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-56. INT_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSDW	R/W1C	0b	Thermal shutdown warning
6	UVCC1PW	R/W1C	0b	VCC1 undervoltage pre-warning
5	UVEXCC	R/W1C	0b	VEXCC under-voltage
4	OVEXCC	R/W1C	0b	VEXCC over-voltage
3	VEXCCSC	R/W1C	0b	VEXCC short-circuit
2	UVCC2	R/W1C	0b	VCC2 pin undervoltage
1	OVCC2	R/W1C	0b	VCC2 pin overvoltage
0	VCC2SC	R/W1C	0b	VCC2 pin short circuit

9.55 INT_EN_4 Register (Offset = 5Eh) [Reset = DDh]

INT_EN_4 is shown in Figure 9-55 and described in Table 9-57.

Return to the Summary Table.

Figure 9-55. INT_EN_4 Register

7	6	5	4	3	2	1	0
LIN_WUP_EN	LIN_DTO_EN	RESERVED	LDT_WAKE_EN	MODE_ERR_EN	OVHSS_EN	RESERVED	UVHSS_EN
R/W-1b	R/W-1b	R-0b	R/W-1b	R/W-1b	R/W-1b	R-0b	R/W-1b

Table 9-57. INT_EN_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LIN_WUP_EN	R/W	1b	LIN bus wake interrupt mask
6	LIN_DTO_EN	R/W	1b	LIN dominant state timeout interrupt mask
5	RESERVED	R	0b	Reserved
4	LDT_WAKE_EN	R/W	1b	Masking bit for LDT Wake from Sleep
3	MODE_ERR_EN	R/W	1b	Illegal transceiver state for mode change request mask
2	OVHSS_EN	R/W	1b	VHSS over-voltage for high-side switches mask
1	RESERVED	R	0b	Reserved
0	UVHSS_EN	R/W	1b	VHSS under-voltage for high-side switches mask

9.56 INT_EN_5 Register (Offset = 5Fh) [Reset = FFh]

INT_EN_5 is shown in Figure 9-56 and described in Table 9-58.

Return to the Summary Table.

Figure 9-56. INT_EN_5 Register

7	6	5	4	3	2	1	0
VCC1OC_EN	VCC2OC_EN	VEXCCOC_EN	CLKMON_FAIL_EN	HSS4_RB_FAIL_EN	HSS3_RB_FAIL_EN	HSS2_RB_FAIL_EN	HSS1_RB_FAIL_EN
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 9-58. INT_EN_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VCC1OC_EN	R/W	1b	Interrupt enable for VCC1OC fault
6	VCC2OC_EN	R/W	1b	Interrupt enable for VCC2OC fault
5	VEXCCOC_EN	R/W	1b	Interrupt enable for VEXCCOC fault
4	CLKMON_FAIL_EN	R/W	1b	Interrupt enable for CLKMON_FAIL interrupt
3	HSS4_RB_FAIL_EN	R/W	1b	Interupt enable for HSS4_RB_FAIL
2	HSS3_RB_FAIL_EN	R/W	1b	Interupt enable for HSS3_RB_FAIL
1	HSS2_RB_FAIL_EN	R/W	1b	Interupt enable for HSS2_RB_FAIL
0	HSS1_RB_FAIL_EN	R/W	1b	Interupt enable for HSS1_RB_FAIL

9.57 INT_EN_6 Register (Offset = 60h) [Reset = FFh]

INT_EN_6 is shown in Figure 9-57 and described in Table 9-59.

Return to the Summary Table.

Figure 9-57. INT_EN_6 Register

7	6	5	4	3	2	1	0
TSDW_EN	UVCC1PW_EN	UVEXCC_EN	OVEXCC_EN	VEXCCSC_EN	UVCC2_EN	OVCC2_EN	VCC2SC_EN
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 9-59. INT_EN_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSDW_EN	R/W	1b	Thermal shutdown warning mask
6	UVCC1PW_EN	R/W	1b	VCC1 undervoltage pre-warning mask
5	UVEXCC_EN	R/W	1b	VEXCC under-voltage
4	OVEXCC_EN	R/W	1b	VEXCC over-voltage
3	VEXCCSC_EN	R/W	1b	VEXCC short-circuit
2	UVCC2_EN	R/W	1b	VCC2 pin undervoltage mask
1	OVCC2_EN	R/W	1b	VCC2 pin overvoltage mask
0	VCC2SC_EN	R/W	1b	VCC2 pin short circuit mask

9.58 INT_EN_7 Register (Offset = 62h) [Reset = FFh]

INT_EN_7 is shown in Figure 9-58 and described in Table 9-60.

Return to the Summary Table.

Figure 9-58. INT_EN_7 Register

7	6	5	4	3	2	1	0
HSSOC1_EN	HSSOL1_EN	HSSOC2_EN	HSSOL2_EN	HSSOC3_EN	HSSOL3_EN	HSSOC4_EN	HSSOL4_EN
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b

Table 9-60. INT_EN_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSOC1_EN	R/W	1b	High side switch 1 over current interrupt mask
6	HSSOL1_EN	R/W	1b	High side switch 1 open load interrupt mask
5	HSSOC2_EN	R/W	1b	High side switch 2 over current interrupt mask
4	HSSOL2_EN	R/W	1b	High side switch 2 open load interrupt mask
3	HSSOC3_EN	R/W	1b	High side switch 3 over current interrupt mask
2	HSSOL3_EN	R/W	1b	High side switch 3 open load interrupt mask
1	HSSOC4_EN	R/W	1b	High side switch 4 over current interrupt mask
0	HSSOL4_EN	R/W	1b	High side switch 4 open load interrupt mask

9.59 INT_BIST1 Register (Offset = 63h) [Reset = 00h]

INT_BIST1 is shown in Figure 9-59 and described in Table 9-61.

Return to the Summary Table.

Applicable only to TCAN29xxB, (ASIL-B) device versions. Not applicable to QM device versions

Figure 9-59. INT_BIST1 Register

7	6	5	4	3	2	1	0
ABIST_UVSUP_ERR	ABIST_INT_LDO_ERR	ABIST_UVOV_HSS_ERR	RESERVED	ABIST_UVCAN_ERR	BGXMON_ERR	IBIAS_MON_ERR	ABIST_VCC1SC_ERR
R/W1C-0b	R/W1C-0b	R/W1C-0b	R-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-61. INT_BIST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ABIST_UVSUP_ERR	R/W1C	0b	ABIST error on UVUP5 and UVSUP33 voltage monitors
6	ABIST_INT_LDO_ERR	R/W1C	0b	ABIST error on internal LDO UV/OV voltage monitors
5	ABIST_UVOV_HSS_ERR	R/W1C	0b	ABIST error on OV/OVHSS voltage monitors
4	RESERVED	R	0b	Reserved
3	ABIST_UVCAN_ERR	R/W1C	0b	ABIST error on UVCAN voltage monitors
2	BGXMON_ERR	R/W1C	0b	Internal bandgap cross-monitor error
1	IBIAS_MON_ERR	R/W1C	0b	Internal current bias monitor error
0	ABIST_VCC1SC_ERR	R/W1C	0b	ABIST error on VCC1SC voltage monitor

9.60 INT_BIST2 Register (Offset = 64h) [Reset = 00h]

INT_BIST2 is shown in Figure 9-60 and described in Table 9-62.

Return to the Summary Table.

Applicable only to TCAN29xxB, (ASIL-B) device versions. Not applicable to QM device versions

Figure 9-60. INT_BIST2 Register

7	6	5	4	3	2	1	0
ABIST_UVCC1_ERR	ABIST_OVCC1_ERR	ABIST_VCC2SC_ERR	ABIST_UVCC2_ERR	ABIST_OVCC2_ERR	ABIST_VEXCCSC_ERR	ABIST_UVEXCC_ERR	ABIST_OVEXCC_ERR
R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b	R/W1C-0b

Table 9-62. INT_BIST2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ABIST_UVCC1_ERR	R/W1C	0b	ABIST error on UVCC1 voltage monitor
6	ABIST_OVCC1_ERR	R/W1C	0b	ABIST error on OVCC1 voltage monitor
5	ABIST_VCC2SC_ERR	R/W1C	0b	ABIST error on VCC2SC voltage moniotr
4	ABIST_UVCC2_ERR	R/W1C	0b	ABIST error on UVCC2 voltage monitor
3	ABIST_OVCC2_ERR	R/W1C	0b	ABIST error on OVCC2 voltage monitor
2	ABIST_VEXCCSC_ERR	R/W1C	0b	ABIST error on VEXCCSC voltage monitor
1	ABIST_UVEXCC_ERR	R/W1C	0b	ABIST error on UVEXCC voltage monitor
0	ABIST_OVEXCC_ERR	R/W1C	0b	ABIST error on OVEXCC voltage monitor

9.61 GEN_PURPOSE_REG2 Register (Offset = 75h) [Reset = 00h]

GEN_PURPOSE_REG2 is shown in Figure 9-61 and described in Table 9-63.

Return to the Summary Table.

Figure 9-61. GEN_PURPOSE_REG2 Register

7	6	5	4	3	2	1	0
GEN_PURPOSE_REG1							
R/W-00000000b							

Table 9-63. GEN_PURPOSE_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GEN_PURPOSE_REG1	R/W	00000000b	General Purpose Register2. Store generic information or test SPI communication

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9.62 GEN_PURPOSE_REG3 Register (Offset = 76h) [Reset = 00h]

GEN_PURPOSE_REG3 is shown in Figure 9-62 and described in Table 9-64.

Return to the Summary Table.

Figure 9-62. GEN_PURPOSE_REG3 Register

7	6	5	4	3	2	1	0
GEN_PURPOSE_REG2							
R/W-00000000b							

Table 9-64. GEN_PURPOSE_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GEN_PURPOSE_REG2	R/W	00000000b	General Purpose Register3. Store generic information or test SPI communication

9.63 GEN_PURPOSE_REG4 Register (Offset = 77h) [Reset = 00h]

GEN_PURPOSE_REG4 is shown in Figure 9-63 and described in Table 9-65.

Return to the Summary Table.

Figure 9-63. GEN_PURPOSE_REG4 Register

7	6	5	4	3	2	1	0
GEN_PURPOSE_REG3							
R/W-00000000b							

Table 9-65. GEN_PURPOSE_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GEN_PURPOSE_REG3	R/W	00000000b	General Purpose Register3. Store generic information or test SPI communication

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9.64 ID_PIN_STATUS Register (Offset = 78h) [Reset = 00h]

ID_PIN_STATUS is shown in Figure 9-64 and described in Table 9-66.

Return to the Summary Table.

Figure 9-64. ID_PIN_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		ID3_STAT		ID2_STAT		ID1_STAT	
R-0b		R/W0C-00b		R/W0C-00b		R/W0C-00b	

Table 9-66. ID_PIN_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	Reserved
5-4	ID3_STAT	R/W0C	00b	Status of the WAKE3/ID3 pin connection 00b = Unknown 01b = Connected to GND 10b = Connected to VSUP 11b = Reserved
3-2	ID2_STAT	R/W0C	00b	Status of the WAKE2/ID2 pin connection 00b = Unknown 01b = Connected to GND 10b = Connected to VSUP 11b = Reserved
1-0	ID1_STAT	R/W0C	00b	Status of the WAKE1/ID1 pin connection 00b = Unknown 01b = Connected to GND 10b = Connected to VSUP 11b = Reserved

9.65 WAKE_ID_CONFIG1 Register (Offset = 79h) [Reset = 00h]

WAKE_ID_CONFIG1 is shown in Figure 9-65 and described in Table 9-67.

Return to the Summary Table.

Figure 9-65. WAKE_ID_CONFIG1 Register

7	6	5	4	3	2	1	0
ID2_EN	RESERVED			ID1_EN	RESERVED		
R/W-0b	R-0b			R/W-0b	R-0b		

Table 9-67. WAKE_ID_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ID2_EN	R/W	0b	Enable ID function on WAKE2 pin
6-4	RESERVED	R	0b	Reserved
3	ID1_EN	R/W	0b	Enable ID function on WAKE1 pin
2-0	RESERVED	R	0b	Reserved

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9.66 WAKE_ID_CONFIG2 Register (Offset = 7Ah) [Reset = 00h]

WAKE_ID_CONFIG2 is shown in Figure 9-66 and described in Table 9-68.

Return to the Summary Table.

Figure 9-66. WAKE_ID_CONFIG2 Register

7	6	5	4	3	2	1	0
RSVD	RESERVED			ID3_EN	RESERVED		
R/W-0b	R-0b			R/W-0b	R-0b		

Table 9-68. WAKE_ID_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	
6-4	RESERVED	R	0b	Reserved
3	ID3_EN	R/W	0b	Enable ID function on WAKE3 pin
2-0	RESERVED	R	0b	Reserved

9.67 WAKE_PIN_CONFIG5 Register (Offset = 7Bh) [Reset = 20h]

WAKE_PIN_CONFIG5 is shown in Figure 9-67 and described in Table 9-69.

Return to the Summary Table.

Figure 9-67. WAKE_PIN_CONFIG5 Register

7	6	5	4	3	2	1	0
WAKE4_SENSE	WAKE4_STAT	WAKE4_LEVEL		RESERVED			
R/W-0b	RH-0b	R/W-10b		R-0b			

Table 9-69. WAKE_PIN_CONFIG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WAKE4_SENSE	R/W	0b	WAKE4 pin configured for static or cyclic sensing wake 0b = Static sensing 1b = Cyclic sensing
6	WAKE4_STAT	RH	0b	Provides status of WAKE4 pin. 0b = Low 1b = High
5-4	WAKE4_LEVEL	R/W	10b	Sets the WAKE3 pin input thresholds. 00b = Reserved 01b = 2.5V 10b = 4V 11b = 6V
3-0	RESERVED	R	0b	Reserved

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TCAN29xx-Q1 family supports CAN FD communication while certain device also supports LIN communication

10.2 Typical Application

The TCAN29xx-Q1 SBC family is typically used in applications with a host microprocessor or FPGA that requires CAN FD and LIN support while using the devices many features like its watchdog, advanced bus fault diagnostics for CAN FD bus and high side switches. Below are typical applications configuration for 3.3V microprocessor applications. These devices work with 3.3V and 5V microprocessors depending upon the value of VCC1. The bus termination is shown for illustrative purposes.

Figure 10-1 shows the TCAN2957-Q1 with different functions than the previous application.

- VCC1 providing power to MCU
- External PNP providing power to a system sensor or second MCU
- HSS1 and HSS2 connected together to provide higher current to an external component.
- Cyclic sensing with the WAKE pin and HSS4

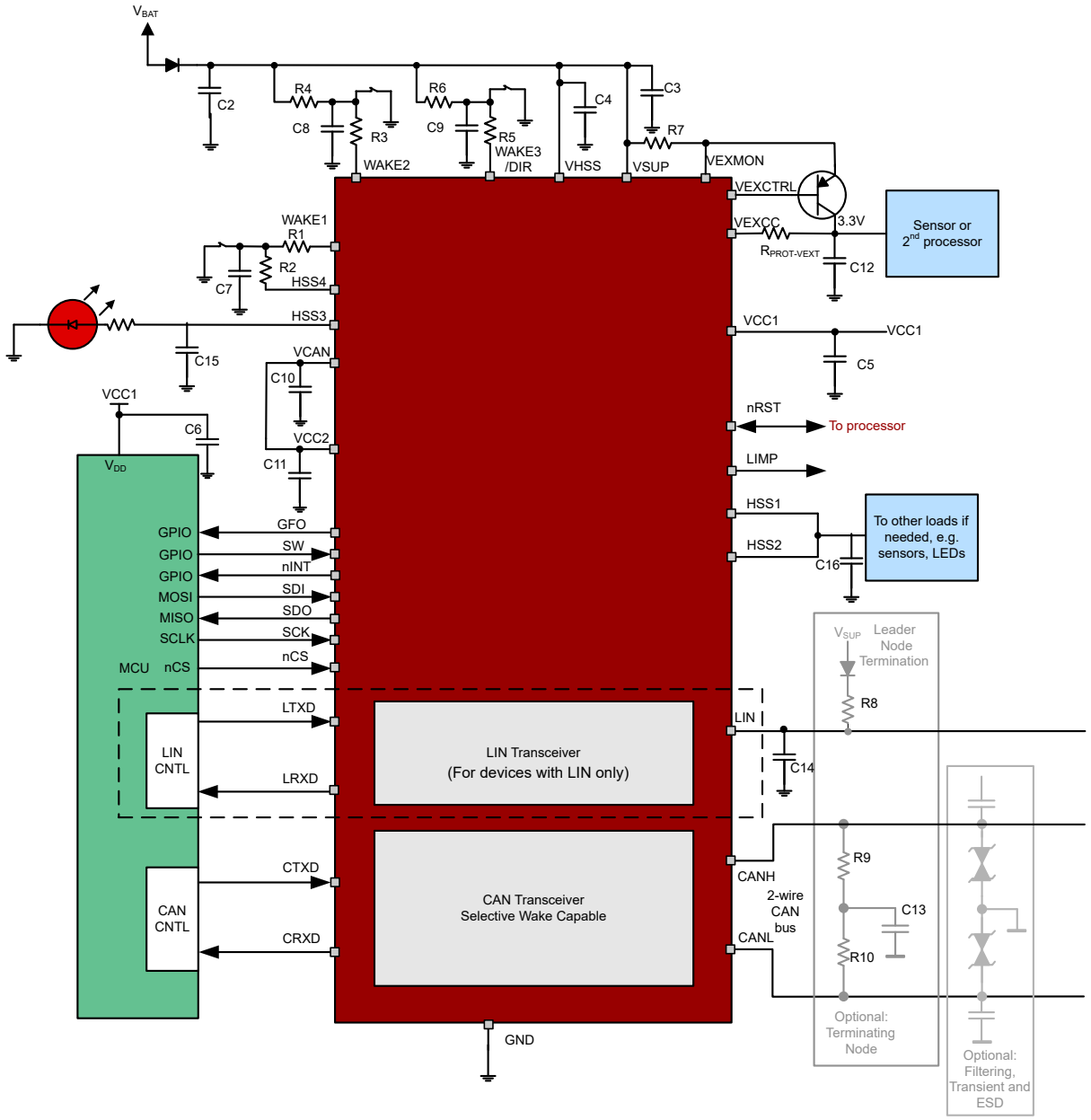

Figure 10-1. Typical CAN and LIN Applications for TCAN2957-Q1 with Synchronized High Side Switch

Table 10-1. External Component Values

Component	Typical Value	Comments
Capacitance		
C2	22µF	Decoupling capacitance to cut-off battery spike, protect from ISO pulses. May need higher capacitance per application requirements
C3, C4	100nF, low ESR	Decoupling capacitance, place the capacitance close to the pin of the IC to help with EMC robustness
C5	4.7µF, low ESR	Per application requirements. Min. 1µF required for LDO stability; higher capacitance value recommended here for EMC robustness and help with load transients
C6	Refer to microcontroller manual for capacitance requirement per application.	To improve stability of supply for microcontroller, not needed for SBC.

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Table 10-1. External Component Values (continued)

Component	Typical Value	Comments
Capacitance		
C7, C8, C9, C_{WK1}	22nF	Required for EMC robustness; only needed if WAKE pins are connected to ECU pins
C10	100nF, low ESR	Needed for VCAN supply stability, place close to the pin of the IC
C11	4.7µF, low ESR	Per application requirements. Min. 1µF required for LDO stability; higher capacitance value recommended here for EMC robustness and help with load transients
C12	4.7µF, low ESR	Per application requirements. Min. 4.7µF required for LDO stability and EMC robustness
C13	4.7nF	If CAN split termination is needed, per OEM requirement
C14	220pF	LIN termination capacitance
C15, C16	100nF	Only needed if HSS is driving ECU-external loads; for EMC protection
Resistances		
R1, R3, R5	3.3kΩ	Series resistance to limit the current into WAKE pin and protect from ISO pulses
R2, R4, R6	3kΩ	Sets the wetting current needed for the switch, as required by the application
R7	Vshunt/I_limit Ω	Shunt resistance to set the current limit on VEXCC, as required by the application
R8	1kΩ	LIN leader node termination, if used as a leader node
R9, R10	60Ω	CAN termination, if needed, per OEM requirement
$R_{WK-VBAT}$	5.1kΩ	To limit the current through the battery monitoring switch
R_{DIV1}, R_{DIV2}	To limit the voltage at the MCU ADC pin below its Abs Max or ADC input range	Per the MCU ADC pin requirement and max battery voltage requirement
$R_{PROT-EXT}$	100Ω	Needed only if the pin supplies loads outisde the ECU. Needed for protection against ground shift and for EMC robustness

10.2.1 Design Requirements

The ISO 11898-2:2024 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the TCAN29xx-Q1. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2:2024. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. The device is specified to meet the 1.5V requirement with a 50Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the device is a minimum of 30kΩ. If 100 of the devices are in parallel on a bus, this is equivalent to a 300Ω differential load worst case. That transceiver load of 300Ω in parallel with the 60Ω gives an equivalent loading of 50Ω. Therefore, the TCAN29xx-Q1 theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898-2:2024 standard of 40m by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate. This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2:2024 CAN standard. The flexibility comes with the responsibility of good network design and balancing tradeoffs.

10.2.1.1 Normal Mode Application Note

When using the device in systems which monitor the CRXD or TRXD pin for a wake-up request, special care must be taken during the mode transitions. The output of the RXD pin is based upon the programmed state of the transceiver and remains latched low, if wake capable, until the transceiver is placed into a different state.

10.2.1.2 Standby Mode Application Note

If the device detects an under voltage on VSUP, the CRXD pin transitions low, and signals to the software that the device has transitioned to standby mode. The nINT pin is pulled low to indicate a UVSUP event. The device must be programmed to the expected mode. This includes the transceiver.

10.2.1.3 LTXD Dominant State Timeout Application Note

The maximum dominant LTXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for controller and peripheral node applications. Thus, there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

10.2.2 Detailed Design Procedures

10.2.2.1 CAN Detailed Design Procedure

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network. Termination may be a single 120Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

10.2.2.2 LIN Detailed Design Procedures

The TCAN2957-Q1 LIN transceiver has been developed with the internal LIN responder pull-up resistor to meet ISO 17987-4:2023. This tightening of the pull-up and designing the network with lower bus capacitance allows longer network lengths or more LIN nodes on the bus. Controller node applications require and external 1kΩ pull-up resistor and serial diode.

10.2.3 Device Brownout information

The brownout behavior of the device depends upon VCC1 and whether VSUP drops below $VSUP_{(PU)F}$. For devices where VCC1 = 5V, the device behaves as per Figure 10-2. When VSUP continues to fall to below $VSUP_{(PU)F}$, the device behaves as a power on reset as per Figure 10-3. $UVSUP_{5F}$ is used for turning off VEXCC and UVSUP5R is used to turn on VEXCC is programmed to be on.

When VCC1 = 3.3V, Both $UVSUP_{5R/F}$ and $UVSUP_{33R/F}$ are used. The device behaves as per Figure 10-4 when VSUP drops below $UVSUP_{33F}$ but stays above $VSUP_{(PU)F}$. When VSUP continues to fall to below $VSUP_{(PU)F}$, the device behaves as a power on reset as per Figure 10-5.

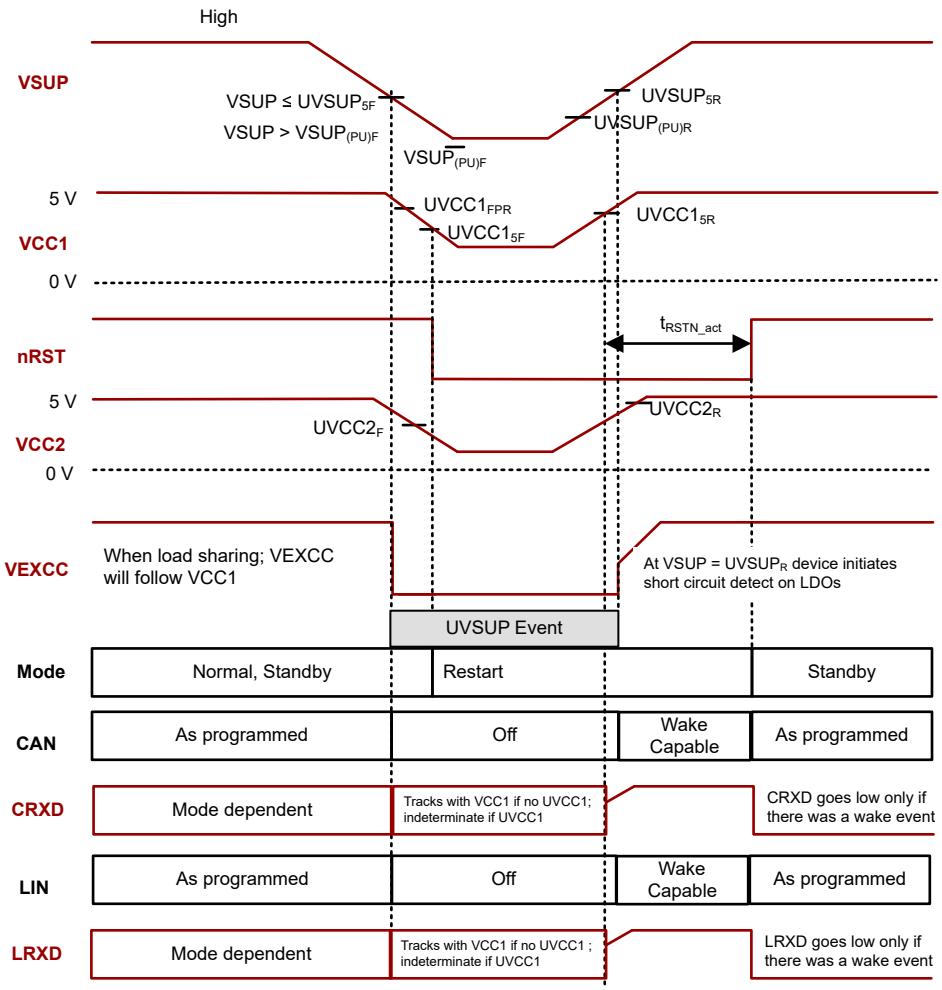

Figure 10-2. Brownout Above $VSUP_{(PU)F}$ for VCC1 = 5V

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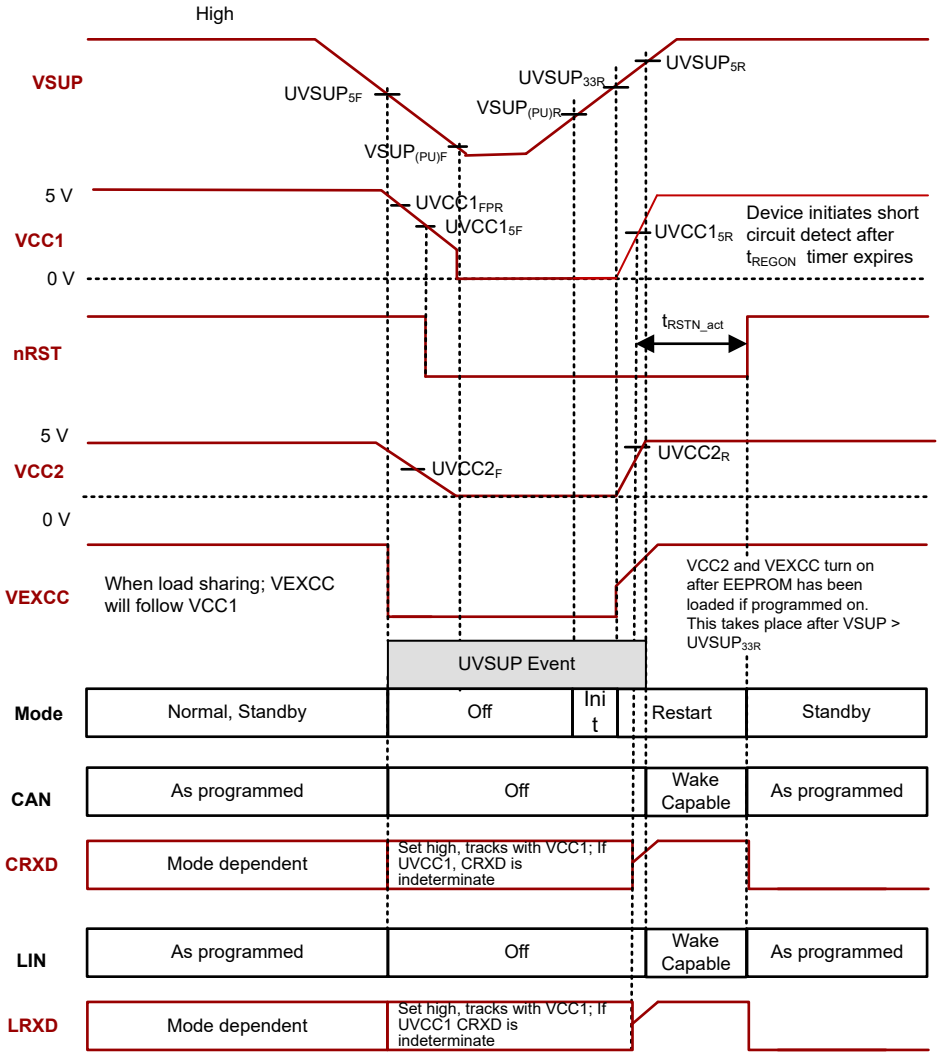

Figure 10-3. Brownout Below $VSUP_{(PU)F}$ for VCC1 = 5V

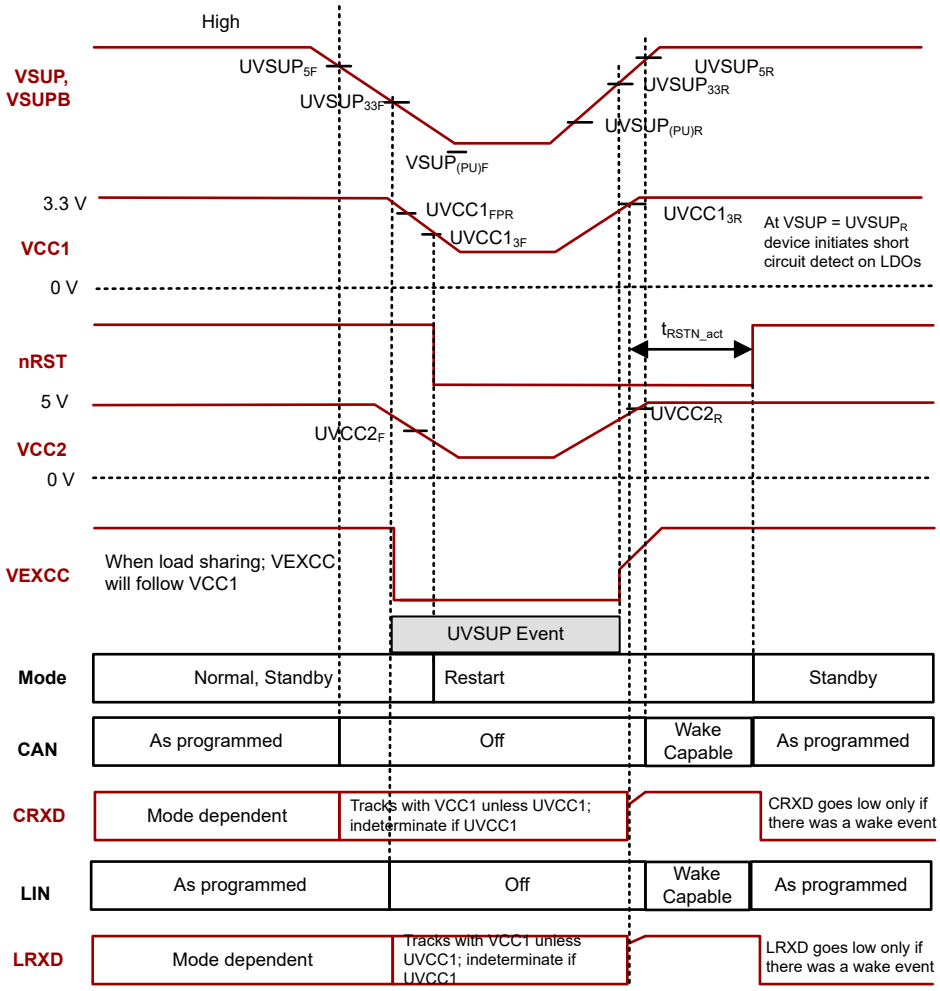

Figure 10-4. Brownout Above $VSUP_{(PU)F}$ for VCC1 = 3.3V

ADVANCE INFORMATION

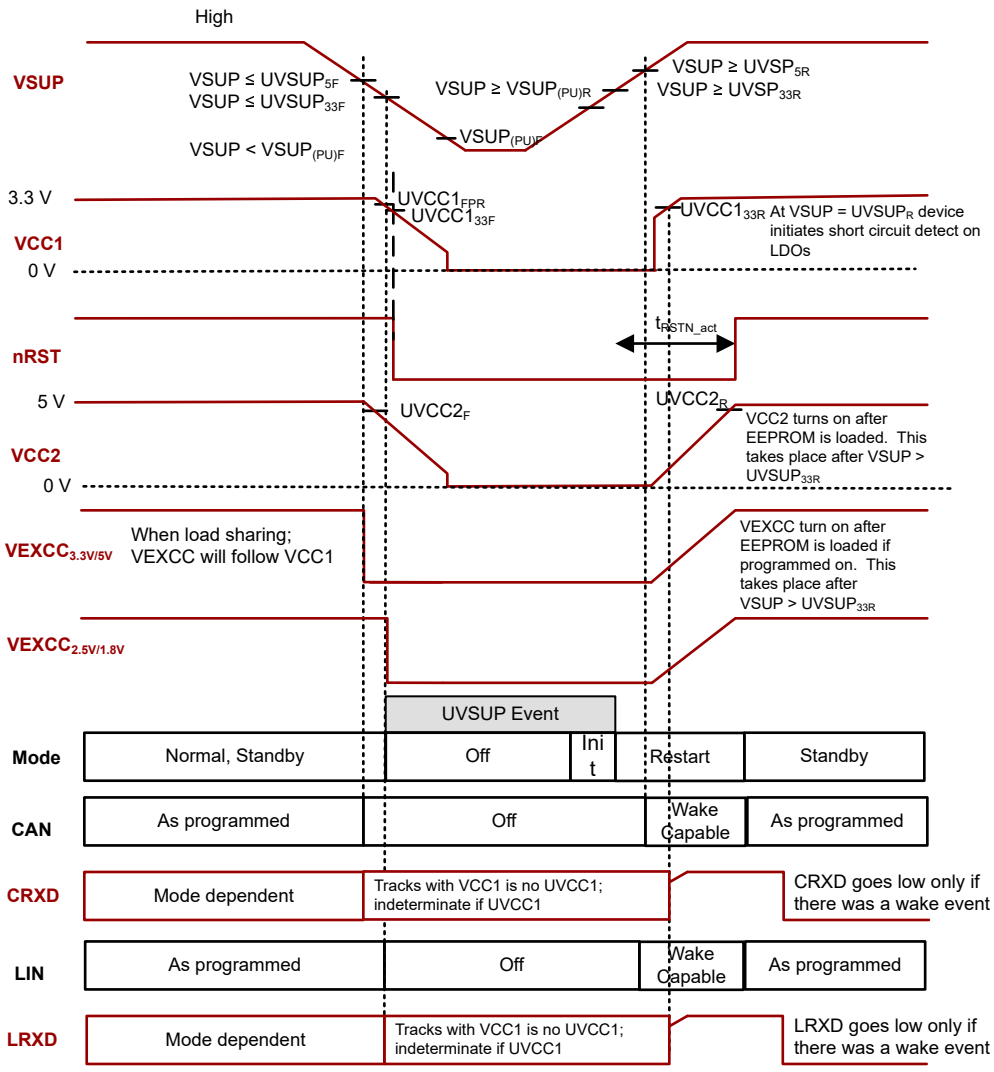

Figure 10-5. Brownout Below $VSUP_{(PU)F}$ for VCC1 = 3.3V

10.3 Power Supply Recommendations

The TCAN29xx-Q1 is designed to operate off of the battery VSUP and VCAN. To support a wide range of microprocessors the logic I/O and SPI are powered off of VCC1 which supports levels 3.3V and 5V. The CAN FD transceiver 5 V supply is powered from VCAN input. Refer to Table 10-1 for the recommended values of the external components required on the input and output supply terminals.

10.4 Layout

Robust and reliable bus node design often requires the use of external transient protection device to protect against EFT and surge transients that can occur in industrial environments. Because ESD and transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high-frequency layout techniques must be applied during PCB design. The family comes with high on-chip IEC ESD protection, but if higher levels of system level immunity are desired external TVS diodes can be used. TVS diodes and bus filtering capacitors can be placed as close to the on-board connectors as possible to prevent noisy transient events from propagating further into the PCB and system.

10.4.1 Layout Guidelines

Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. The layout example provides information on components around the device. A series common mode choke (CMC) is placed on the CANH and CANL lines between and connector J1. Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. Use supply and ground planes to provide low inductance.

Note

High-frequency currents follows the path of least impedance and not the path of least resistance.

Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

- Bypass and bulk capacitors must be placed as close as possible to the supply terminals of transceiver, examples are 100nF capacitors on VCC1, VCC2 and VCAN; COUT on VCC1 and CVCC2 on VCC2
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, RTERM, with the center or split tap of the termination connected to ground using capacitor CSPLIT. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to make sure the terminating node is not removed from the bus thus also removing the termination.

10.4.2 Layout Example

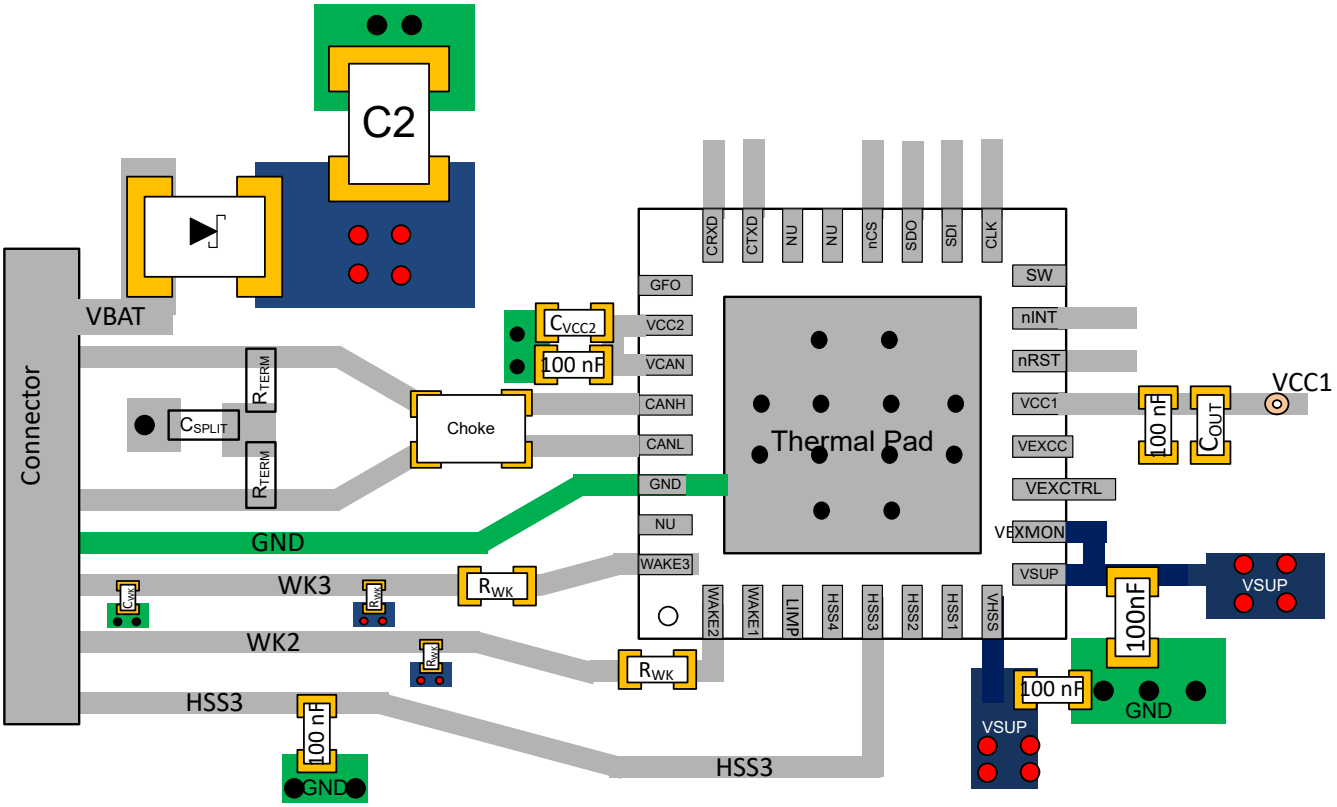

Figure 10-6. Example Layout

11 Device and Documentation Support

This device conforms to the following CAN standards. The core of what is needed is covered within this system spec, however reference must be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources are helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

11.1 Documentation Support

11.1.1 CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2024: High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode)
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps

11.1.2 LIN Transceiver Physical Layer Standards

- ISO/DIS 17987-1: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
- ISO/DIS 17987-4: 2023 Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V
- SAEJ2602-1: LIN Network for Vehicle Applications
- LIN2.0, LIN2.1, LIN2.2 and LIN2.2A specification

11.1.3 EMC Requirements:

- SAEJ2962-2: US3 requirements for CAN Transceivers (-2, -5, GM will propose updates to address -6 + FD, but this is the best place for a working start)
- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for CAN and LIN
- ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
- ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
- ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
- ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
- IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
- IEC 61000-4-2
- IEC 61967-4
- CISPR25

11.1.4 Conformance Test Requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer
- ISO/DIS 17987-7: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
- SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test

11.1.5 Related Documentation

- “A Comprehensible Guide to Controller Area Network”, Wilfried Voss, Copperhill Media Corporation
- “CAN System Engineering: From Theory to Practical Applications”, 2nd Edition, 2013; Dr. Wolfhard Lawrenz, Springer.

ADVANCE INFORMATION

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

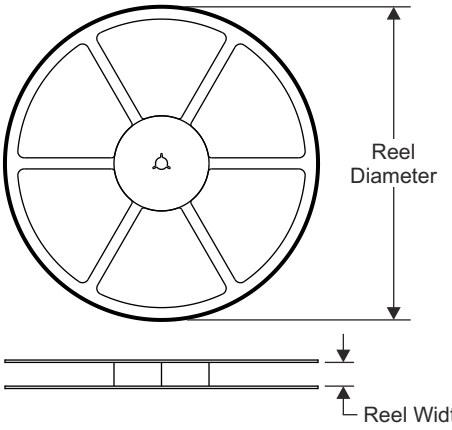
DATE	REVISION	NOTES
August 2026	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

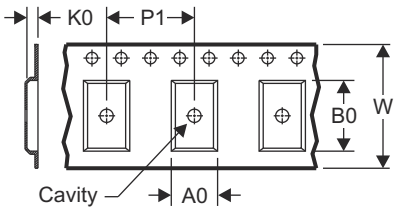
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information

REEL DIMENSIONS

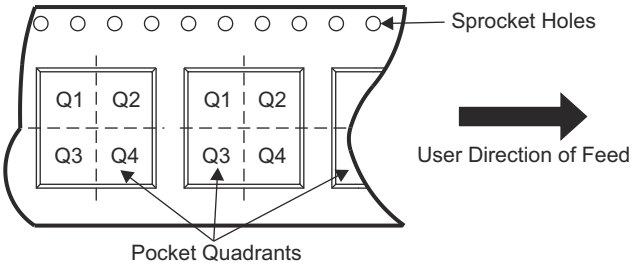


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

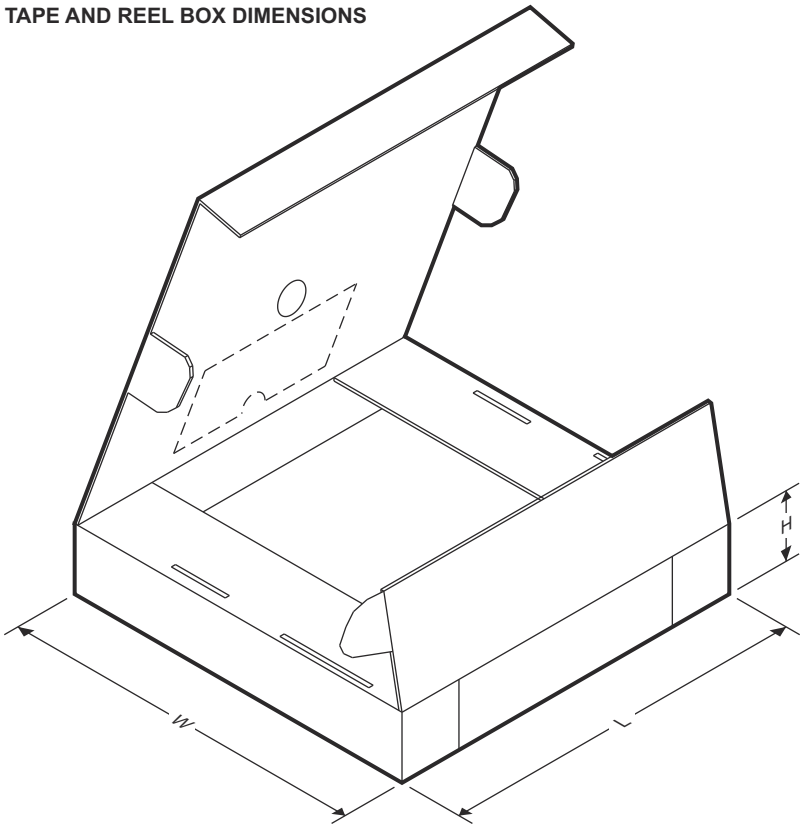
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTCAN29575BRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
PTCAN29573BRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
PTCAN29475BRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
PTCAN29473BRHBRQ1	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

ADVANCE INFORMATION

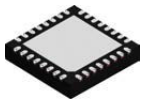
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTCAN29575BRHBRQ1	VQFN	RHB	32	5000	360	360	36
PTCAN29573BRHBRQ1	VQFN	RHB	32	5000	360	360	36
PTCAN29475BRHBRQ1	VQFN	RHB	32	5000	360	360	36
PTCAN29473BRHBRQ1	VQFN	RHB	32	5000	360	360	36

13.2 Mechanical Data

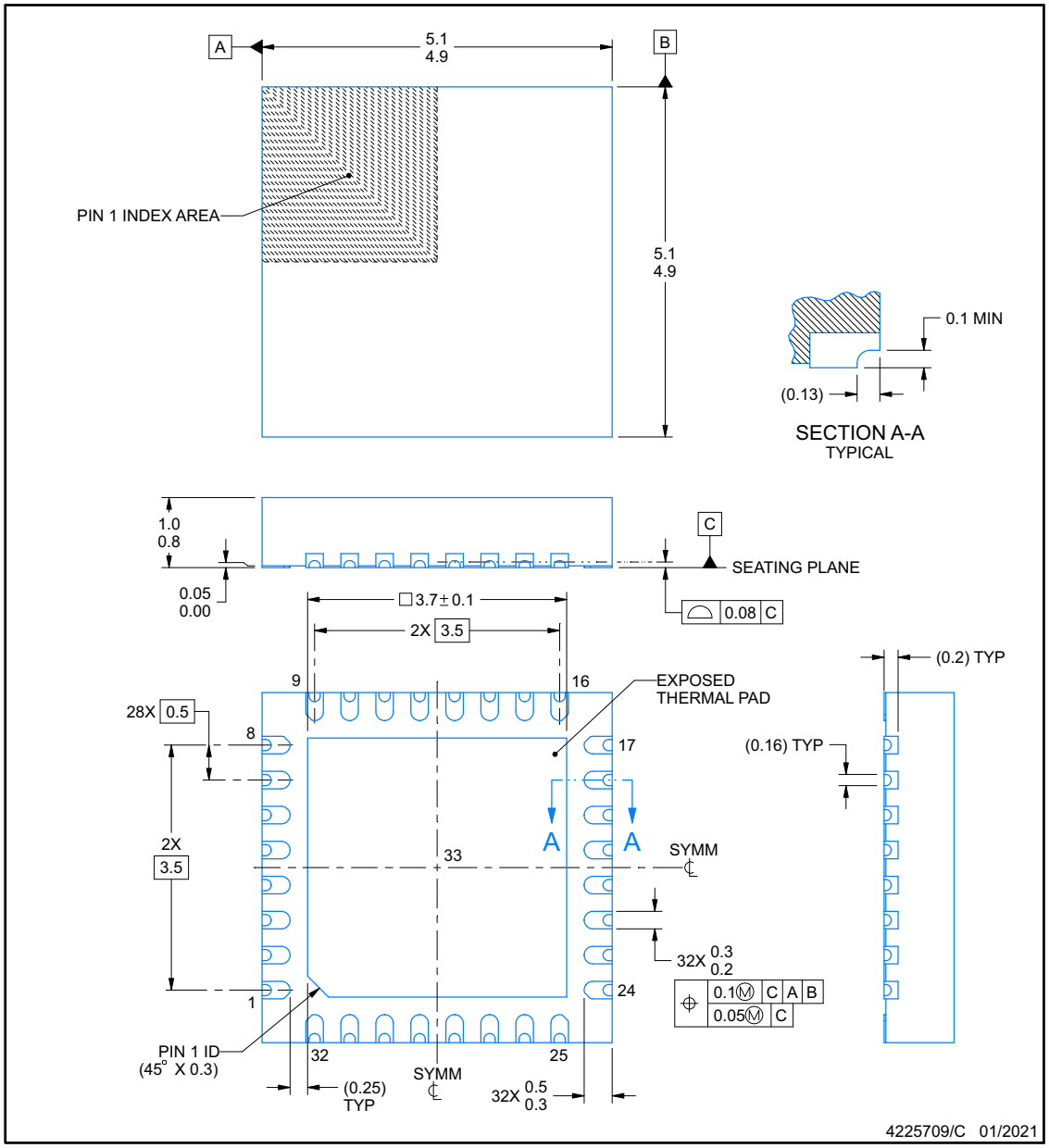
RHB0032U



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

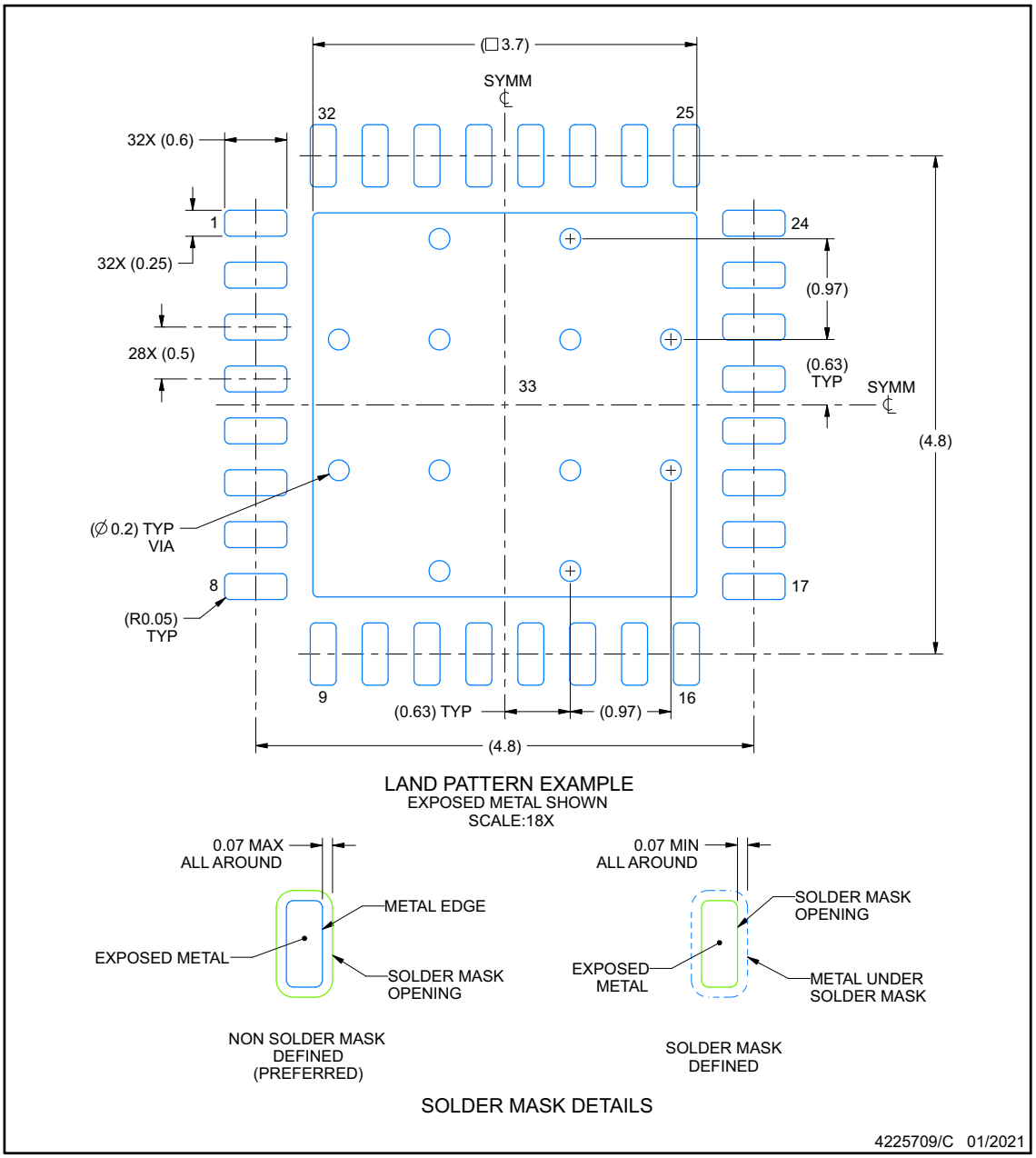
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RHB0032U — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



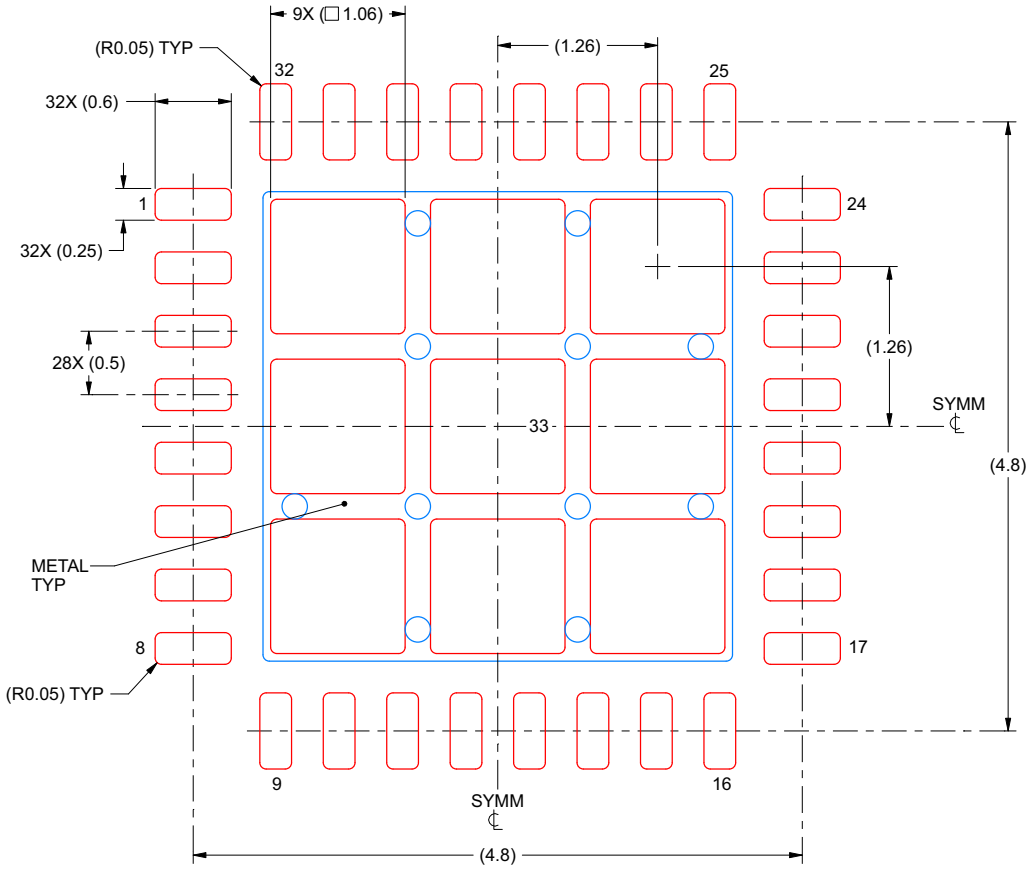
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032U — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225709/C 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTCAN29575BRHBRQ1	Active	Preproduction	VQFN (RHB) | 32	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

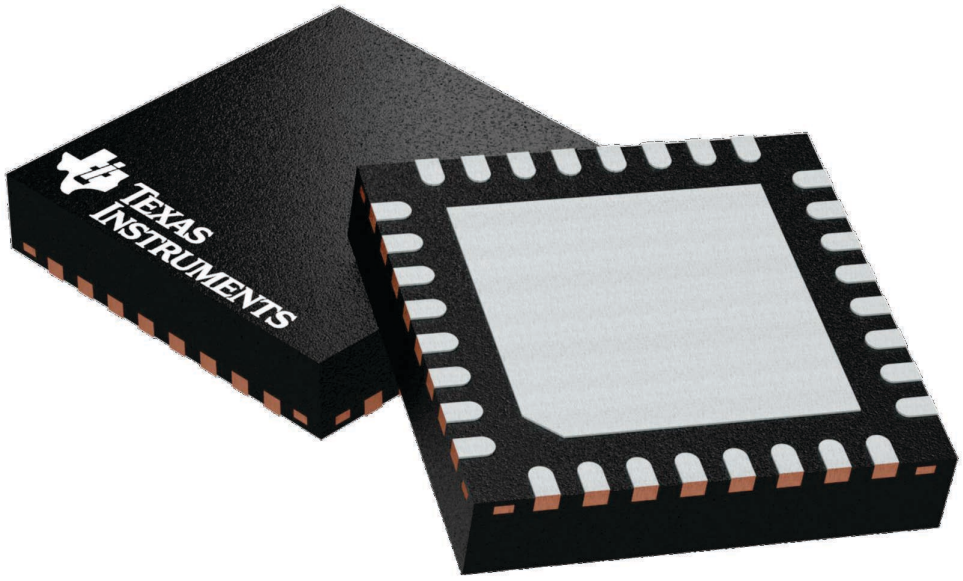
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

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