TCAN957-Q1 Automotive Fault-Protected CAN FD Transceiver With Silent Mode

1 Features

- AEC-Q100 qualified for automotive applications
  - Human body model (HBM) ESD protection: ±12kV for CANH and CANL pins as per AEC Q100-002
  - Charged-device model (CDM) ESD protection: ±500V as per AEC Q100-011
  - IEC 62228-3 contact discharge: ±8kV (unpowered)
- Compatible with ISO 11898-2:2024 physical layer standard
- Functional Safety-Capable
  - Documentation will be available upon device release to aid in functional safety system design
- Support of classical CAN and optimized CAN FD performance at 2Mbps and 5Mbps
  - Short and symmetrical propagation delays for enhanced timing margin
- TCAN957V-Q1 I/O voltage range supports 2.9V to 5.25V
- Support for 12V battery applications
- Receiver common mode input voltage: ±12V
- Protection features:
  - Bus fault protection: ±40V
  - Undervoltage protection
  - TXD-dominant time-out (DTO)
  - Thermal-shutdown protection (TSD)
- Operating modes: normal and silent
- Optimized behavior when unpowered
  - Bus and logic pins are high impedance (no load to operating bus or application)
  - Hot-plug capable: power up and down glitch free operation on bus and RXD output
- 8-pin SOIC and leadless VSON-8 package with improved automated optical inspection (AOI) capability

2 Applications

- Automotive and transportation
  - Body control modules
  - Automotive gateway
  - Advanced driver assistance system (ADAS)
  - Infotainment

3 Description

The TCAN957-Q1 is a high-speed controller area network (CAN) transceiver that meets the physical layer requirements of the ISO 11898-2:2024 high-speed CAN specification. The transceiver is designed for classical CAN and CAN FD networks up to 5 megabits per second (Mbps).

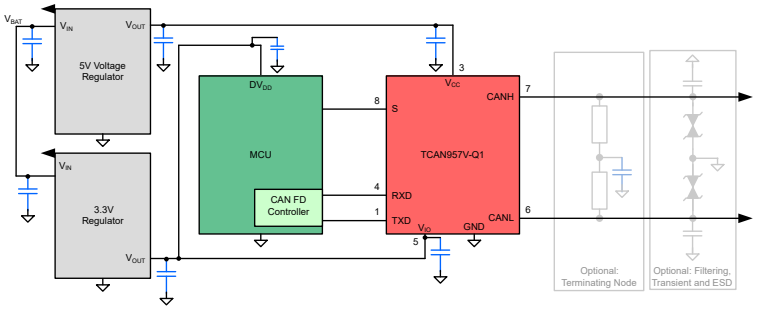
The transceiver supports two modes of operation; normal mode and silent mode. The transceiver also includes many protection and diagnostic features including thermal shutdown (TSD), TXD-dominant timeout (DTO), and bus fault protection up to ±40V. The device has defined fail-safe behavior in supply undervoltage or floating pin scenarios.

The transceiver features an integrated level shifter on the V_{IO} pin which supplies internal logic-level translation for interfacing the transceiver I/Os directly to 3.3V, or 5V logic level. These transceivers are available in both industry-standard SOIC-8 and VSON-8 packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN957-Q1	D (SOIC, 8)	4.9mm × 6mm
	DRB (VSON, 8)	3mm × 3mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

ADVANCE INFORMATION

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

ADVANCE INFORMATION

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Comparison Table....3
5 Pin Configuration and Functions....4
6 Specifications....5
6.1 Absolute Maximum Ratings....5
6.2 ESD Ratings....5
6.3 ESD Ratings, IEC Specification....5
6.4 Recommended Operating Conditions....6
6.5 Thermal Characteristics....6
6.6 Power Supply Characteristics....6
6.7 Dissipation Ratings....7
6.8 Electrical Characteristics....7
6.9 Switching Characteristics....8
6.10 Typical Characteristics....9
7 Parameter Measurement Information....11
8 Detailed Description....14
8.1 Overview....14
8.2 Functional Block Diagram....14
8.3 Feature Description....15
8.4 Device Functional Modes....19
9 Application and Implementation....20
9.1 Typical Application....20
9.2 System Examples....23
9.3 Power Supply Recommendations....23
9.4 Layout....24
10 Device and Documentation Support....25
10.1 Receiving Notification of Documentation Updates....25
10.2 Support Resources....25
10.3 Trademarks....25
10.4 Electrostatic Discharge Caution....25
10.5 Glossary....25
11 Revision History....25
12 Mechanical, Packaging, and Orderable Information....25

Copyright © 2026 Texas Instruments Incorporated

4 Device Comparison Table

DEVICE NUMBER	LOW VOLTAGE I/O LOGIC SUPPORT ON PIN 5	PIN 8 MODE SELECTION
TCAN957-Q1	No	Silent mode
TCAN957V-Q1	Yes	Silent mode

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

5 Pin Configuration and Functions

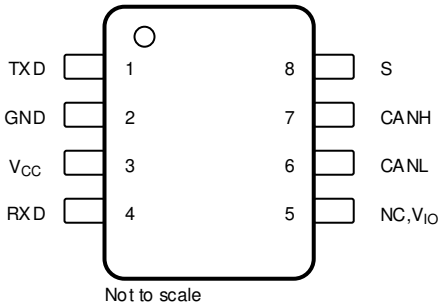


Figure 5-1. D Package, 8-Pin SOIC (Top View)

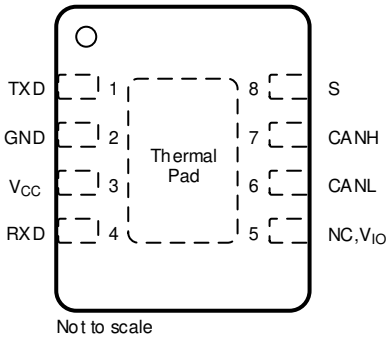


Figure 5-2. DRB Package, 8-Pin VSON (Top View)

Table 5-1. Pin Functions

PINS		TYPE	DESCRIPTION
NAME	NO.		
TXD	1	Digital Input	CAN transmit data input, integrated pullup
GND	2	GND	Ground connection
V_{CC}	3	Supply	5V supply voltage
RXD	4	Digital Output	CAN receive data output, tri-state when powered off
NC	5	—	No connect (not internally connected); devices without V_{IO}
V_{IO}		Supply	I/O supply voltage
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
S	8	Digital Input	Silent mode control input, integrated pull-up
Thermal Pad (VSON only)		—	Connect the thermal pad to any internal PCB ground plane using multiple vias for best thermal performance.

Copyright © 2026 Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage (CANH, CANL)	–40	40	V
V_{DIFF}	Max differential voltage range between CANH and CANL	–40	40	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Operating virtual junction temperature range	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±2000	V
			HBM classifiifation level 3B for global pins CANH & CANL	±12000	V
		Charged-device model (CDM), per AEC Q100-011		±500	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings, IEC Specification

				VALUE	UNIT
V_{ESD}	System level electro-static discharge (ESD)(1)	CAN bus terminals (CANH, CANL) to GND	IEC 62228-3: Unpowered Contact Discharge	±8000	V
V_{Tran}	ISO7637 ISO Pulse Transients(2)	CAN bus terminals (CANH, CANL)	Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	ISO7637 Slow transients pulse(3)	CAN bus terminals (CANH, CANL) to GND	Direct coupling capacitor "slow transient pulse" with 100nF coupling capacitor - powered	±30	V

(1) Tested according to IEC 62228-3 CAN Transcievers (2018), Section 6.4; DIN EN 61000-4.
(2) Tested according to IEC 62228-3 CAN Transcievers (2018), Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(3) Tested according to ISO 7637-3 (2017); Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IO}	Supply voltage for I/O level shifter	2.9		5.25	V
$I_{OH(RXD)}$	RXD terminal high level output current	–2			mA
$I_{OL(RXD)}$	RXD terminal low level output current			2	mA
T_J	Operational free-air temperature (see thermal characteristics table)	–40		150	°C

6.5 Thermal Characteristics

THERMAL METRIC(1)		TCAN957(V)-Q1		UNIT
		D (SOIC)	DRB (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.1	76.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.2	74.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.5	45.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.3	7.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	72.1	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	21.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Supply Characteristics

Over recommended operating conditions with T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant	TXD = 0V, R_L = 60Ω, C_L = open			70	mA
			TXD = 0V, R_L = 50Ω, C_L = open			80	mA
		Dominant with bus fault	TXD = 0V, CANH = CANL = ±25V, R_L = open, C_L = open			130	mA
		Recessive, TCAN957V	TXD = V_{IO}, R_L = 50Ω, C_L = open, RCM = open			10	mA
		Recessive, TCAN957	TXD = V_{CC}, R_L = 50Ω, C_L = open, RCM = open			10	mA
	Supply current silent mode		TXD = V_{CC}, R_L = 50Ω, C_L = open			3	mA
I_{IO}	I/O supply current normal mode (Devices with V_{IO})	Dominant	RXD floating, TXD = 0V			400	µA
		Recessive	RXD floating, TXD = V_{IO}			150	µA
	I/O supply current silent mode (Devices with V_{IO})		RXD floating, TXD = V_{IO}			45	µA
UV_{VCC}	Rising under voltage detection on V_{CC} for protected mode				4.2	4.6	V
	Falling under voltage detection on V_{CC} for protected mode			3.5	4	4.5	V
UV_{VIO}	Rising under voltage detection on V_{IO}				2.5	2.9	V
	Falling under voltage detection on V_{IO}			2.1	2.4		V

Copyright © 2026 Texas Instruments Incorporated

6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5V, V_{IO} = 3.3V, T_J = 27°C, R_L = 60Ω, C_{L_RXD} = 15pF TXD input = 250kHz 50% duty cycle square wave		90		mW
		V_{CC} = 5.25V, V_{IO} = 3.3V, T_J = 150°C, R_L = 60Ω, C_{L_RXD} = 15pF TXD input = 2.5MHz 50% duty cycle square wave		110		mW

6.8 Electrical Characteristics

Over recommended operating conditions with T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics						
$V_{CANH(D)}$	Bus output voltage (dominant) CANH	V_{TXD} = 0V, R_L = 50Ω to 65Ω, C_L = open, R_{CM} = open	2.75		4.5	V
$V_{CANL(D)}$	Bus output voltage (dominant) CANL	V_{TXD} = 0V, R_L = 50Ω to 65Ω, C_L = open, R_{CM} = open	0.5		2.25	V
$V_{CANH(R)}$ $V_{CANL(R)}$	Bus output voltage (recessive)	V_{TXD} = V_{CC}, R_L = open (no load), R_{CM} = open	2		3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}	R_{TERM} = 60Ω, C_L = open, C_{SPLIT} = 4.7nF	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)	R_L = 60Ω, C_L = open	–400		400	mV
$V_{DIFF(D)}$	Differential output voltage normal mode Dominant	V_{TXD} = 0V, R_L = 50Ω to 65Ω, C_L = open, R_{CM} = open	1.5		3	V
		V_{TXD} = 0V, 45Ω ≤ R_L ≤ 70Ω, C_L = open	1.4		3.3	V
		V_{TXD} = 0V, R_L = 2240Ω, C_L = open	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage normal mode Recessive	V_{TXD} = V_{CC}, R_L = 60Ω, C_L = open	–120		12	mV
		Normal mode, TXD = V_{CC}, R_L = open, C_L = open	–50		50	mV
$I_{CANH(OS)}$	Short-circuit steady-state output current, Dominant	–3V ≤ V_{CANH} ≤ +18V, CANL = open, V_{TXD} = 0V	–115			mA
$I_{CANL(OS)}$		–3V ≤ V_{CANL} ≤ +18V, CANH = open, V_{TXD} = 0V			115	mA
I_{OS_REC}	Short-circuit steady-state output current; Recessive	–40V ≤ V_{BUS} ≤ +40V, V_{BUS} = CANH = CANL	–5		5	mA
Receiver Electrical Characteristics						
$V_{DIFF_RX(D)}$	Receiver dominant state differential input voltage range, bus biasing active	–12V ≤ V_{CANL} ≤ +12V –12V ≤ V_{CANH} ≤ +12V	0.9		8	V
$V_{DIFF_RX(R)}$	Receiver recessive state differential input voltage range, bus biasing active	–12V ≤ V_{CANL} ≤ +12V –12V ≤ V_{CANH} ≤ +12V	–3		0.5	V
V_{HYS}	Hysteresis voltage for input-threshold, normal mode	-12V ≤ V_{CM} ≤ 12V		80		mV
V_{CM}	Common mode range:		–12		12	V
$I_{LKG(IOFF)}$	Power-off (unpowered) bus input leakage current	V_{CANH} = V_{CANL} = 5V			5	µA
C_I	Input capacitance to ground (CANH or CANL)	V_{TXD} = V_{CC}, V_{IO} = V_{CC}			20	pF
C_{ID}	Differential input capacitance	V_{TXD} = V_{CC}, V_{IO} = V_{CC}			10	pF
m_R	Input resistance matching: [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100%	V_{CANH} = V_{CANL} = 5V	–2%		2%	
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	TCAN957-Q1	0.7 × V_{CC}			V
		TCAN957V-Q1	0.7 × V_{IO}			V

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

6.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	TCAN957-Q1			0.3 × V_{CC}	V
		TCAN957V-Q1			0.3 × V_{IO}	V
I_{IH}	High-level input leakage current	V_{TXD} = V_{CC} = V_{IO} = 5.25V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	V_{TXD} = 0V, V_{CC} = V_{IO} = 5.25V	–200		–20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	V_{TXD} = 5.25V, V_{CC} = V_{IO} = 0V	–1	0	1	µA
C_I	Input Capacitance			2		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level input voltage	TCAN957-Q;1 I_O = –2mA	0.8 × V_{CC}			V
		TCAN957V-Q1; I_O = –2mA	0.8 × V_{IO}			V
V_{OL}	Low-level input voltage	TCAN957-Q1; I_O = 2mA			0.2 × V_{CC}	V
		TCAN957V-Q1; I_O = 2mA			0.2 × V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.25V, V_{CC} = V_{IO} = 0V	–1	0	1	µA
S Terminal (Silent Mode Input)						
V_{IH}	High-level input voltage	TCAN957-Q1	0.7 × V_{CC}			V
		TCAN957V-Q1	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	TCAN957-Q1			0.3 × V_{CC}	V
		TCAN957V-Q1			0.3 × V_{IO}	V
I_{IH}	High-level input leakage current S	V_{CC} = V_{IO} = S = 5.25V	–2		2	µA
I_{IL}	Low-level input leakage current S	V_{CC}= V_{IO} = 5.25V, S = 0V	–20		–2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	S = 5.25V, V_{CC} = V_{IO} = 0V	–1	0	1	µA

6.9 Switching Characteristics

Over recommended operating conditions with T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	Normal mode, V_{IO} = 3V to 5V, R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF		90	220	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	Normal mode, V_{IO} = 3V to 5V, R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF		100	220	ns
t_{MODE}	Mode change time, from Normal to Silent or from Silent to Normal				45	µs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	R_L = 60Ω, C_L = 100pF, R_{CM} = open		43		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			36		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			4		ns
t_R	Differential output signal rise time			32		ns
t_F	Differential output signal fall time			27		ns
t_{TXD_DTO}	Dominant timeout	R_L = 60Ω, C_L = 100pF	0.8		6.5	ms
Receiver Switching Characteristics						

Copyright © 2026 Texas Instruments Incorporated

6.9 Switching Characteristics (continued)

Over recommended operating conditions with T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	C_{L_RXD} = 15pF		56		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			33		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						
$t_{\Delta Bit(Bus)}$	Transmitted recessive bit width variation: $t_{BIT(TXD)}$ = 500ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(Bus)} = t_{BIT(Bus)} - t_{BIT(TXD)}$	–65		30	ns
$t_{\Delta Bit(Bus)}$	Transmitted recessive bit width variation: $t_{BIT(TXD)}$ = 200ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(Bus)} = t_{BIT(Bus)} - t_{BIT(TXD)}$	–45		10	ns
$t_{\Delta Bit(RXD)}$	Received recessive bit width variation: $t_{BIT(TXD)}$ = 500ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(Bus)} = t_{BIT(RXD)} - t_{BIT(TXD)}$	–100		50	ns
$t_{\Delta Bit(RXD)}$	Received recessive bit width variation: $t_{BIT(TXD)}$ = 200ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $t_{\Delta Bit(Bus)} = t_{BIT(RXD)} - t_{BIT(TXD)}$	–80		20	ns
$t_{\Delta REC}$	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500ns	R_L = 60Ω, C_L = 100pF, C_{L_RXD} = 15pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	–65		40	ns
$t_{\Delta REC}$	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200ns		–45		15	ns

6.10 Typical Characteristics

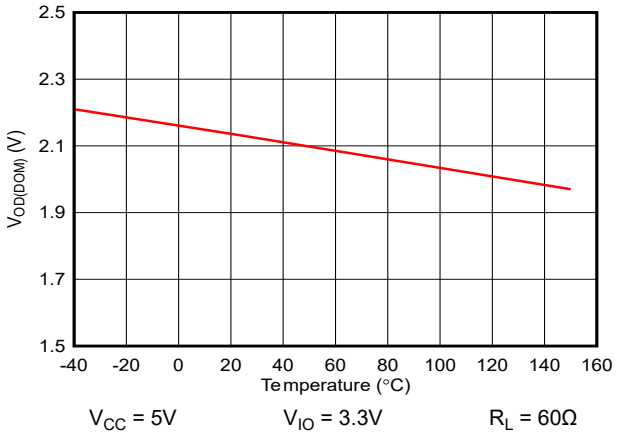


Figure 6-1. $V_{OD(DOM)}$ vs Temperature

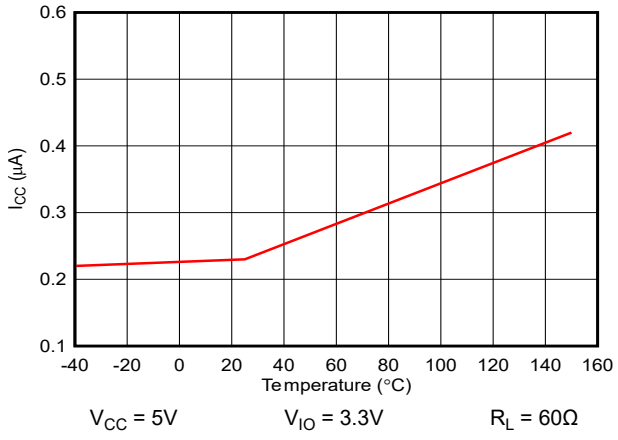


Figure 6-2. I_{CC} Standby (STB) vs Temperature

ADVANCE INFORMATION

6.10 Typical Characteristics (continued)

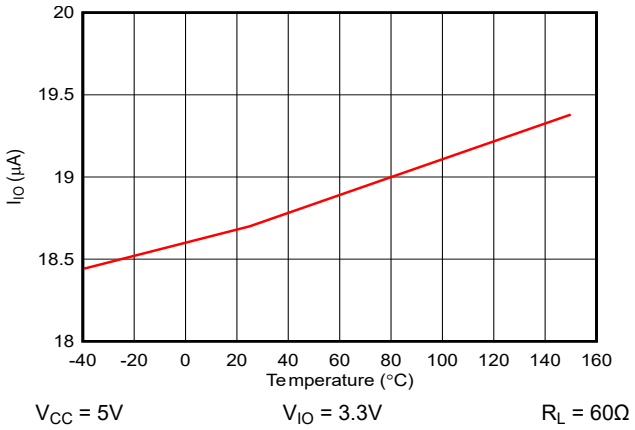


Figure 6-3. I_{IO} Standby (STB) vs Temperature

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

7 Parameter Measurement Information

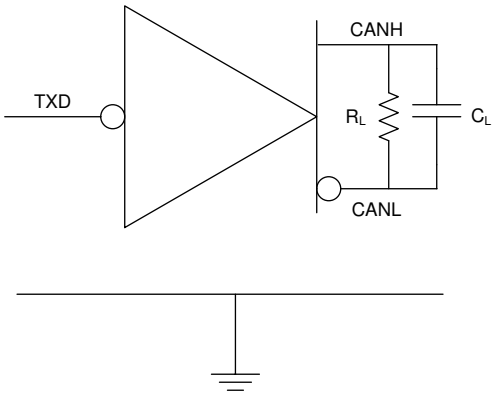


Figure 7-1. I_{CC} Test Circuit

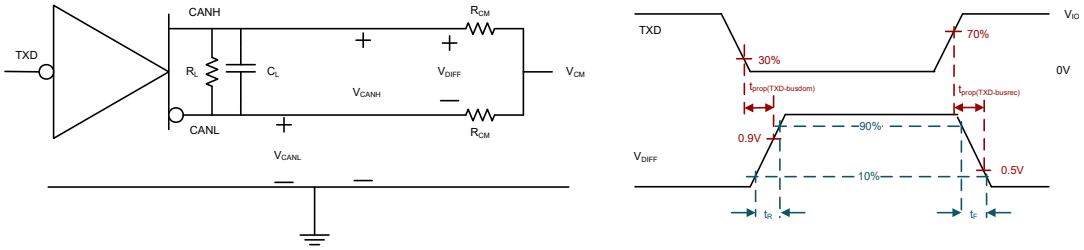


Figure 7-2. Driver Test Circuit and Measurement

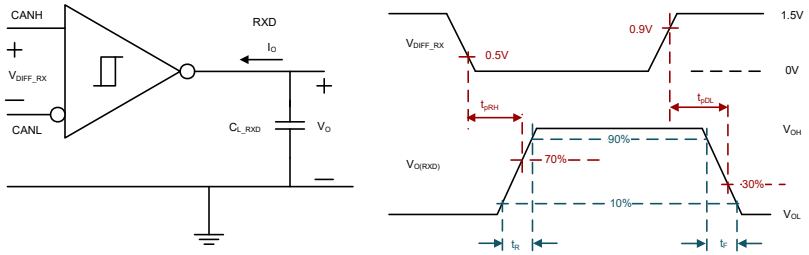


Figure 7-3. Receiver Test Circuit and Measurement

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

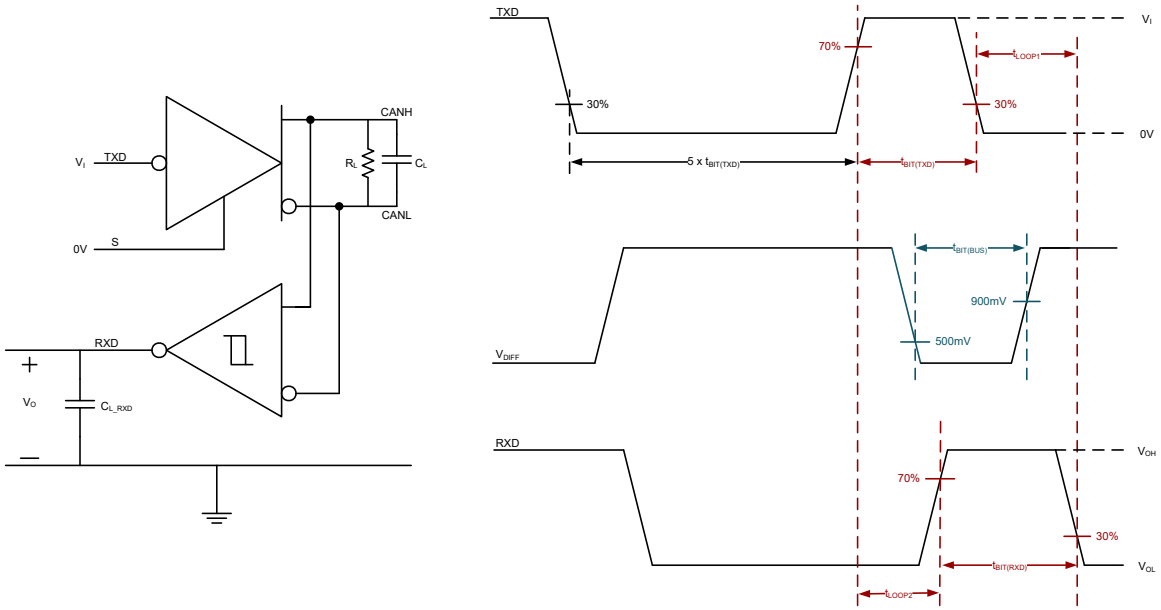


Figure 7-4. Transmitter and Receiver Timing Test Circuit and Measurement

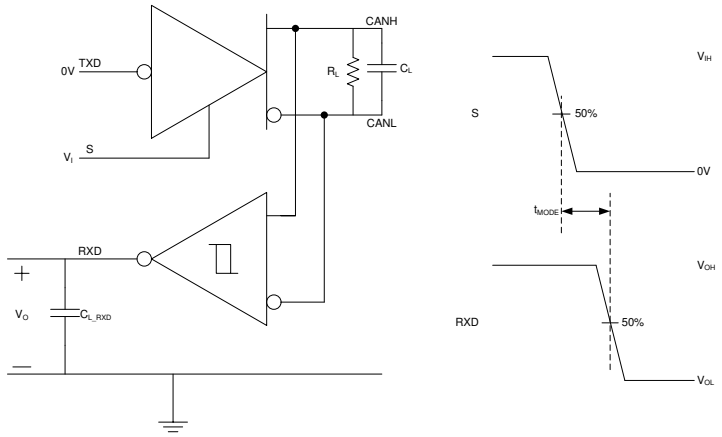


Figure 7-5. t_{MODE} Test Circuit and Measurement

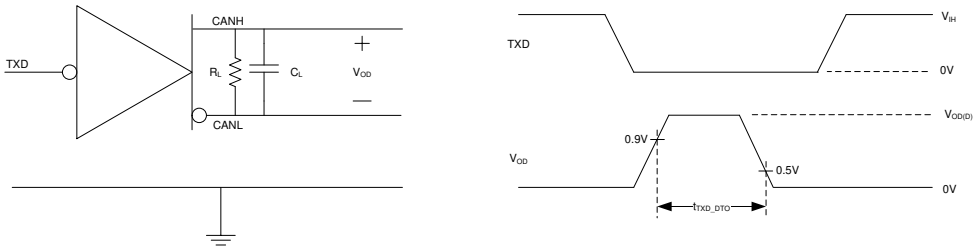


Figure 7-6. TXD Dominant Timeout Test Circuit and Measurement

Copyright © 2026 Texas Instruments Incorporated

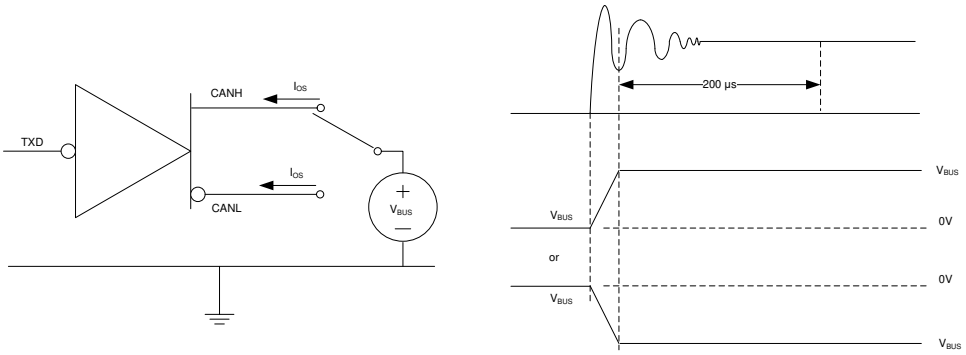


Figure 7-7. Driver Short-Circuit Current Test and Measurement

ADVANCE INFORMATION

ADVANCE INFORMATION

8 Detailed Description

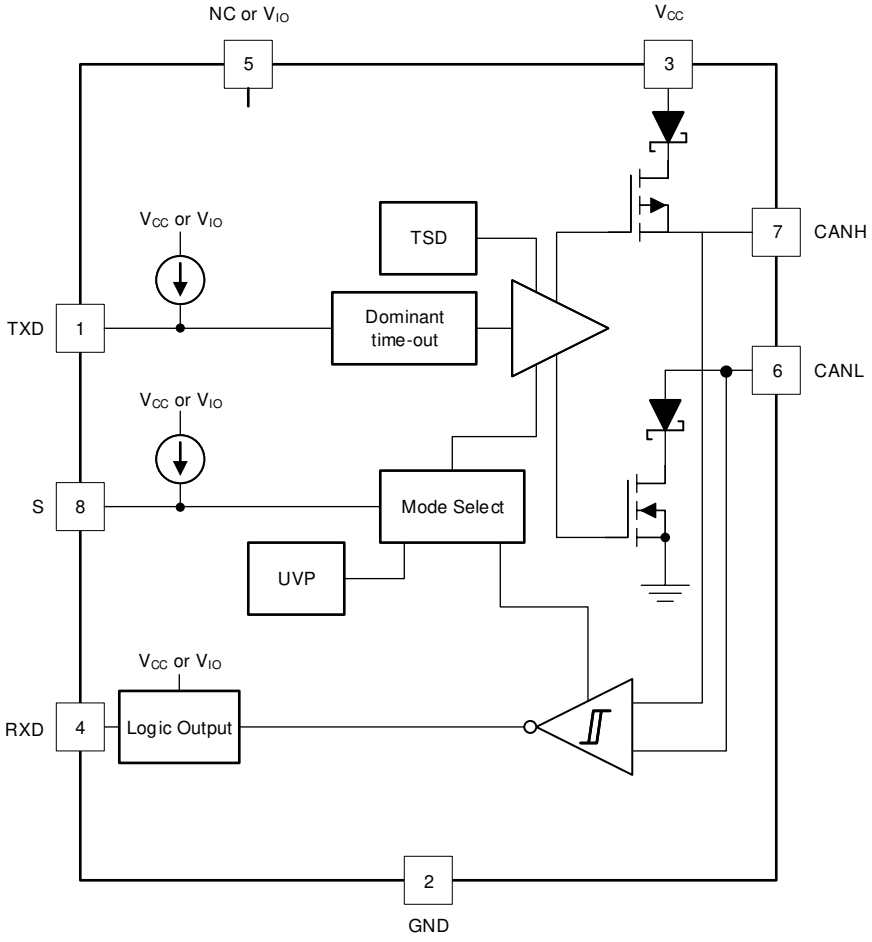
8.1 Overview

The TCAN957(V)-Q1 devices meet or exceed the specifications of the ISO 11898-2:2024 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2024 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features providing for stringent automotive system requirements while also supporting CAN FD data rates up to 5Mbps.

The devices support the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2024 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 2Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500kbps with CAN FD Data at 5Mbps
- Conformance Test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

8.2 Functional Block Diagram



Copyright © 2026 Texas Instruments Incorporated

8.3 Feature Description

8.3.1 Pin Description

8.3.1.1 TXD

The TXD input is a logic-level signal, referenced to either V_{CC} or V_{IO} from a CAN controller to the transceivers.

8.3.1.2 GND

GND is the ground pin of the transceiver, and must be connected to the PCB ground.

8.3.1.3 V_{CC}

V_{CC} provides the 5V power supply to the CAN transceiver.

8.3.1.4 RXD

The RXD output is a logic-level signal, referenced to either V_{CC} or V_{IO}, from the transceivers to the CAN controller. RXD is only driven once V_{IO} is present.

8.3.1.5 V_{IO}

The V_{IO} pin is the input source for the integrated level shifter which provides the transceiver I/O voltage. Connect the V_{IO} pin to the controller I/O voltage source.

8.3.1.6 CANH and CANL

These pins are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transmitter and receiver internally.

8.3.1.7 S (Silent)

The S pin is an input pin used for silent mode control of the transceiver. The S pin can be supplied from either the controller or from a static system voltage source. If normal mode is the only intended mode of operation, then the S pin can be tied directly to system GND using a pulldown resistor. If the silent mode is the only intended mode of operation, then the S pin can be tied directly to a static system voltage source using a pull-up resistor.

8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 8-1.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to V_{CC}/2 though the high-resistance internal input resistors R_{IN}) of the receiver, and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes can be transmitting a dominant bit at the same time during arbitration, and in this case, the differential voltage of the bus is greater than the differential voltage of one driver.

ADVANCE INFORMATION

ADVANCE INFORMATION

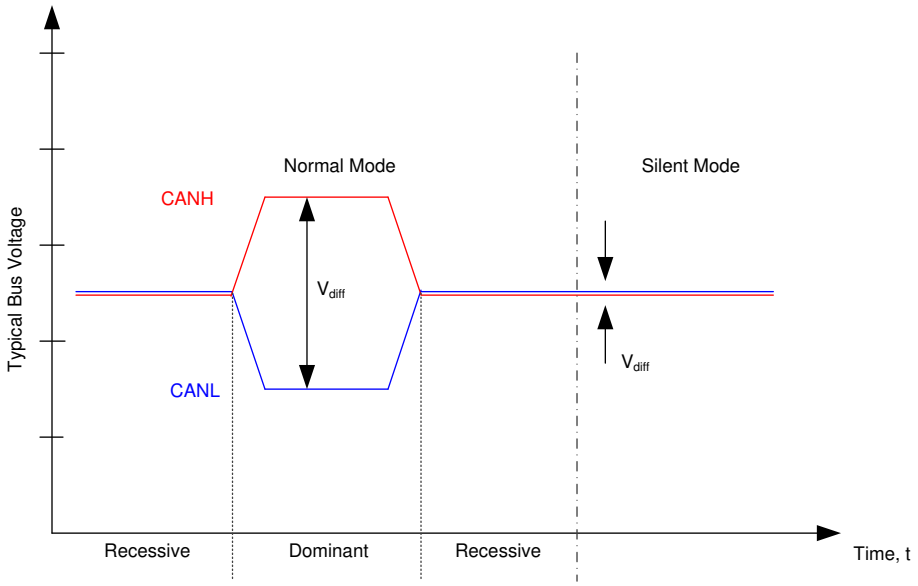


Figure 8-1. Bus States

8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin; thus, clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate can be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD_DTO} = 11 \text{ bits} / 0.8\text{ms} = 13.75\text{Kbps} \quad (1)$$

Copyright © 2026 Texas Instruments Incorporated

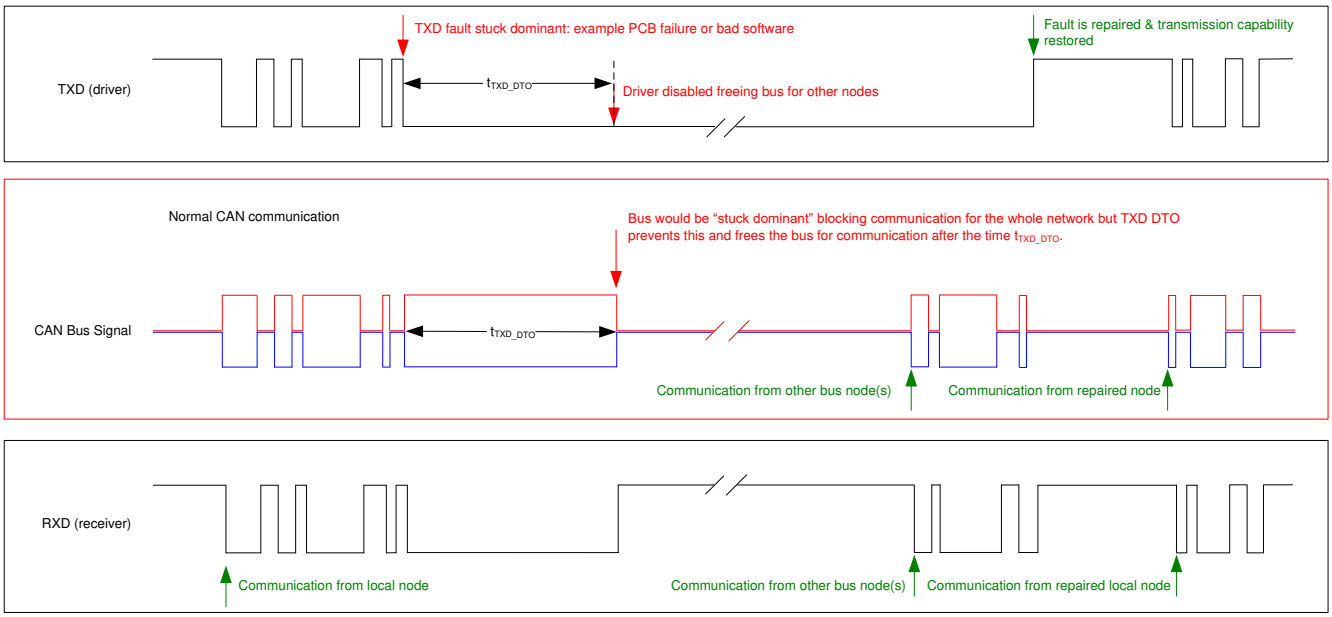


Figure 8-2. Example Timing Diagram for TXD Dominant Timeout

8.3.4 CAN Bus Short-Circuit Current Limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. The features include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state due to a system fault. During CAN communication the bus switches between the dominant and recessive states; thus, the short-circuit current can be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design, the average power rating, $I_{OS(AVG)}$, is used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. Making sure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and the respective short-circuit currents. Use Equation 2 to calculate the average short-circuit current.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC_Bits} \times I_{OS(SS)_REC}) + (\%\ \text{DOM_Bits} \times I_{OS(SS)_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)_DOM}$ is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network is taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The device TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

8.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 8-1. Undervoltage Lockout - TCAN957-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance Weak pulldown to ground(1)	High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$

Table 8-2. Undervoltage Lockout - TCAN957V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	Protected	S = High: Weak pulldown to ground(1)	Recessive
			S = Low: High impedance	
> UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance
< UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$

After the undervoltage condition is cleared and t_{MODE} has expired, the device transitions to normal mode. The host controller can again send and receive CAN traffic.

8.3.7 Unpowered Device

The device is designed to be a no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so the device does not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, and do not load other circuits which can remain powered.

8.3.8 Floating Pins

The device has internal pullups on critical pins which place the device into known states if the pin floats. This internal bias must not be relied upon by design though, especially in noisy environments, but instead is considered a fail-safe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This makes sure the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 8-3 for details on pin bias conditions.

Table 8-3. Pin Bias

PIN	PULLUP OR PULLDOWN	COMMENT
TXD	Pullup	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
S	Pullup	Weakly biases S toward low-power silent mode to prevent excessive system power

Copyright © 2026 Texas Instruments Incorporated

8.4 Device Functional Modes

8.4.1 Operating Modes

The device has two main operating modes; normal mode and silent mode. Operating mode selection is made by applying a high or low level to the S pin.

Table 8-4. Operating Modes

S	DEVICE MODE	DRIVER	RECEIVER	RXD PIN
High	Silent mode	Disabled	Enabled	Mirrors bus state
Low	Normal mode	Enabled	Enabled	

8.4.2 Normal Mode

This mode is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

8.4.3 Silent Mode

In silent mode, the CAN driver is disabled and the high-speed CAN receiver is enabled. CAN communication is unidirectional into the device where the receiver is translating the differential signal from CANH and CANL to a digital output on RXD. The power consumption of the TCAN957(V)-Q1 is reduced in silent mode due to the CAN driver being disabled.

8.4.4 Driver and Receiver Function

The digital input and output levels for the device are CMOS levels with respect to either V_{CC} or V_{IO}.

Table 8-5. Driver Function Table

DEVICE MODE	TXD INPUT(1)	BUS OUTPUTS		DRIVEN BUS STATE(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Silent	X	High impedance	High impedance	Biased recessive

(1) X = irrelevant.
(2) For bus state, see Figure 8-1.

Table 8-6. Receiver Function Table Normal and Silent Mode

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD PIN
Normal or silent	$V_{ID} \geq 0.9V$	Dominant	Low
	$0.5V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \leq 0.5V$	Recessive	High
Any	Open ($V_{ID} \approx 0V$)	Open	High

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Application

Figure 9-1 shows a typical configuration for 5V system using the device. The bus termination is shown for illustrative purposes.

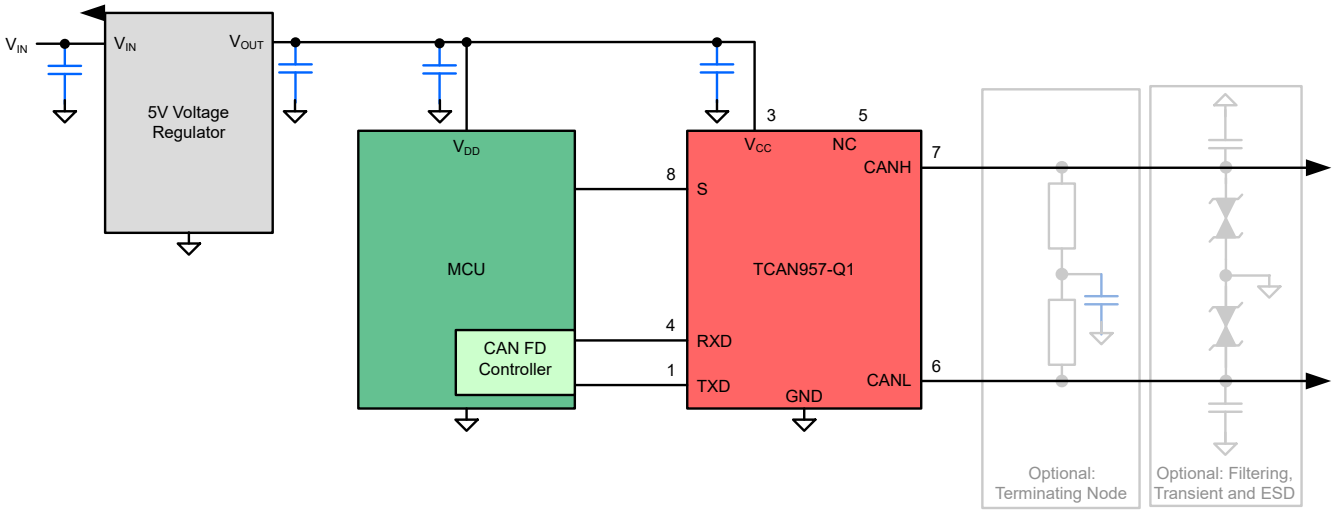


Figure 9-1. Transceiver Application Using 5V I/O Connections

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

9.1.1 Design Requirements

9.1.1.1 CAN Termination

Termination can be one 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination can be used. See Figure 9-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that can be present on the differential signal lines.

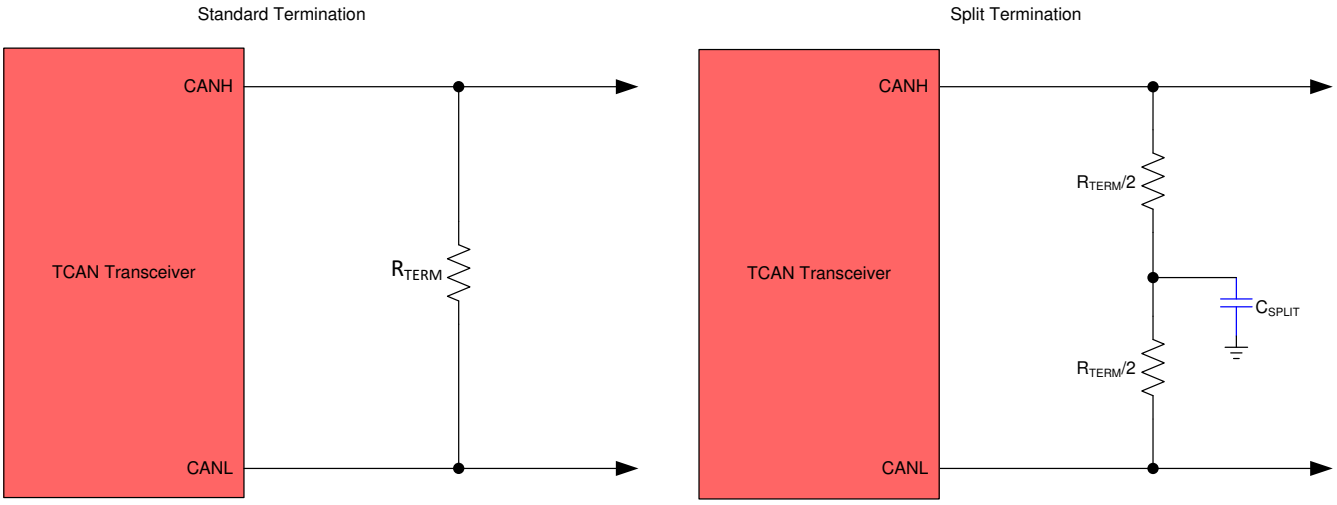


Figure 9-2. CAN Bus Termination Concepts

9.1.2 Detailed Design Procedures

9.1.2.1 Bus Loading, Length, and Number of Nodes

A typical CAN application can have a maximum bus length of 40 meters and maximum stub length of 0.3 meters. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN957(V)-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. There are system level tradeoff decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 specification the driver differential output is specified with a bus load that can range from 50Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN957(V)-Q1 family is specified to meet the 1.5V requirement down to 50Ω and is specified to meet 1.4V differential output at 45Ω bus load. The differential input resistance of the transceiver is a minimum of 40kΩ. If 100 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN957(V)-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity; thus, a practical maximum number of nodes is often lower. Bus length can also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CAN open network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design for a robust network operation.

ADVANCE INFORMATION

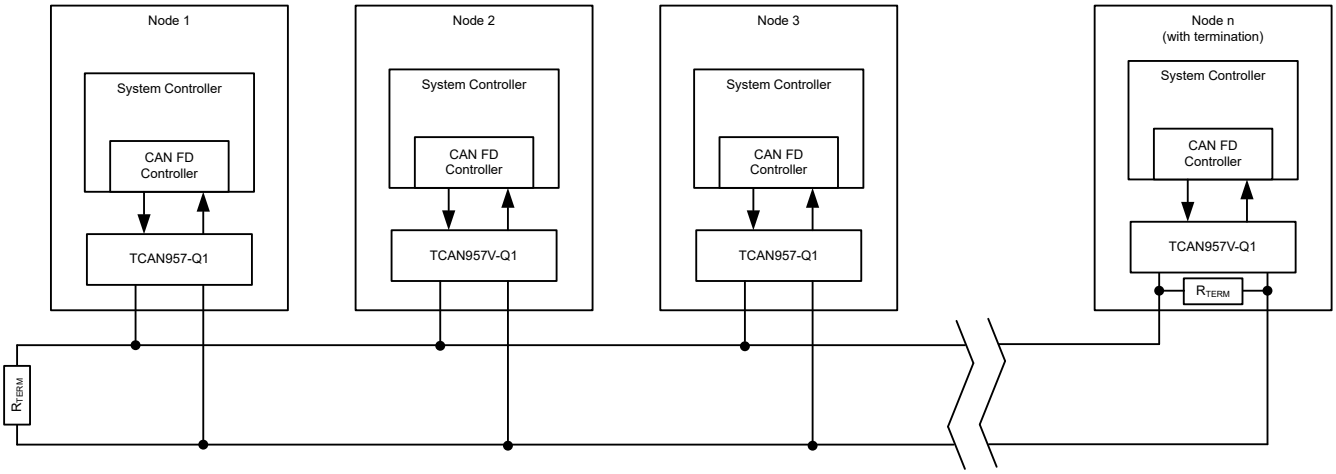
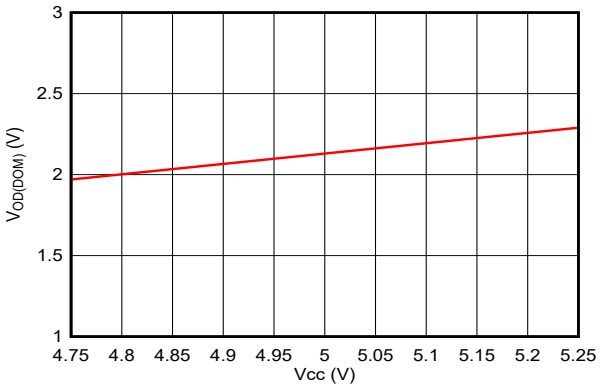


Figure 9-3. Typical CAN Bus

9.1.3 Application Curve



Temp = 25°C R_L = 60Ω

Figure 9-4. $V_{OD(DOM)}$ vs V_{CC}

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

9.2 System Examples

Figure 9-5 shows a typical configuration for 3.3V or 5V systems using the TCAN957(V)-Q1. The bus termination is shown for illustrative purposes.

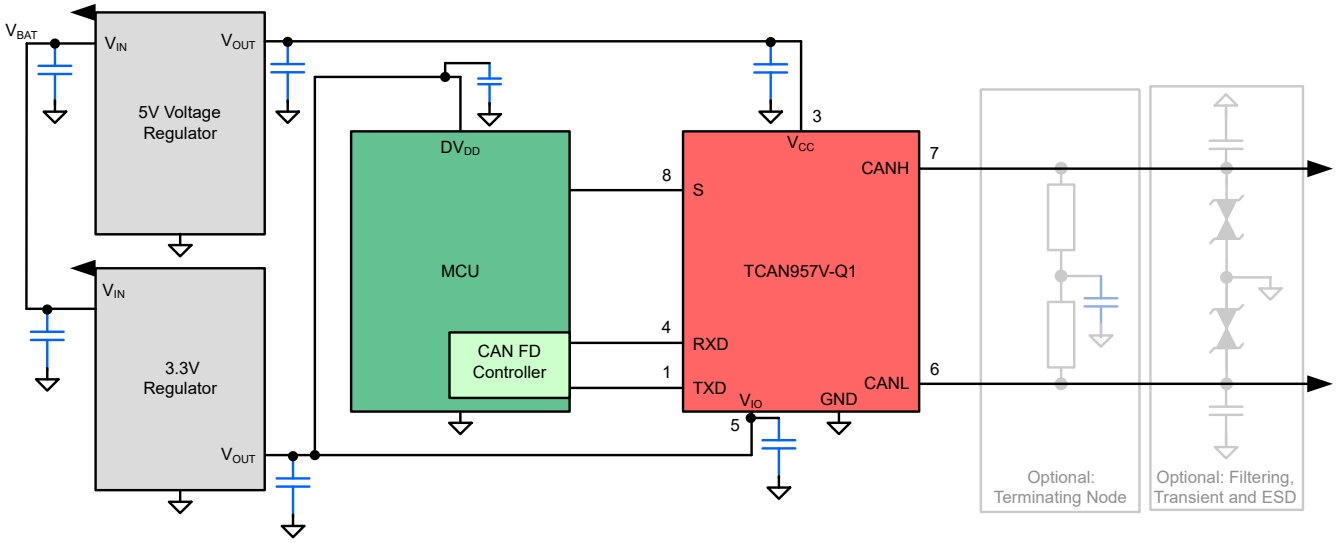


Figure 9-5. Typical Transceiver Application Using 3.3V IO Connections

9.3 Power Supply Recommendations

The TCAN957(V)-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.75V and 5.25V. The TCAN957(V)-Q1 implements an I/O level shifting supply input, V_{IO}, designed for a range between 3V and 5.25V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100nF, is placed near the CAN transceiver main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100nF, is placed near the CAN transceiver V_{IO} supply pin in addition to bypass capacitors.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

ADVANCE INFORMATION

9.4 Layout

Robust and reliable CAN node design can require special layout techniques depending on the application and automotive design requirements. Because transient disturbances have high-frequency content and a wide bandwidth, high-frequency layout techniques can be applied during PCB design.

9.4.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows a optional transient voltage suppression (TVS) diode, D1, which can be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter 0.1µF capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling 0.1µF capacitors is placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination can be implemented on the CAN node. The termination is split into two 60Ω resistors, R4 and R5, with the center or split tap of the termination connected to ground through a 1nF – 100nF capacitor C3. Split termination provides common-mode filtering for the bus. See *CAN Termination*, *CAN Bus Short Circuit Current Limiting*, and Equation 2 for information on termination concepts and power ratings needed for the termination resistors.

9.4.2 Layout Example

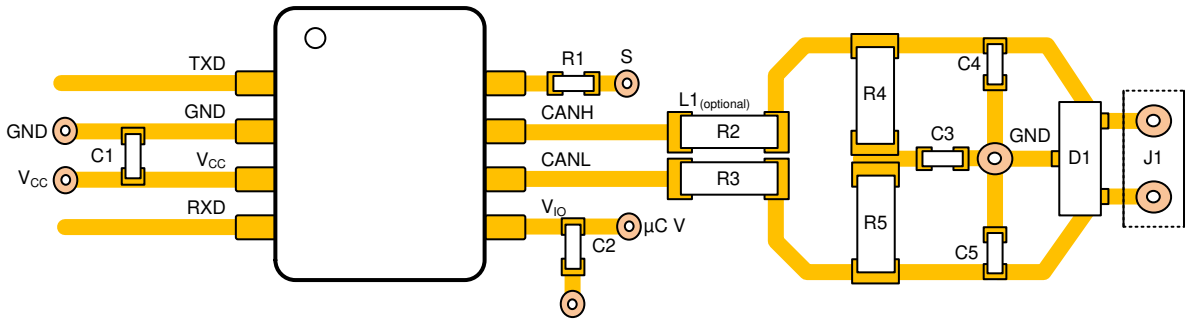


Figure 9-6. Layout Example

Copyright © 2026 Texas Instruments Incorporated

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, see also the left-hand navigation.

ADVANCE INFORMATION

Copyright © 2026 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTCAN957DRBRQ1	Active	Preproduction	SON (DRB) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN957DRQ1	Active	Preproduction	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN957VDRBRQ1	Active	Preproduction	SON (DRB) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
PTCAN957VDRQ1	Active	Preproduction	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

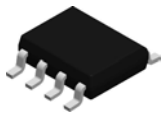
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

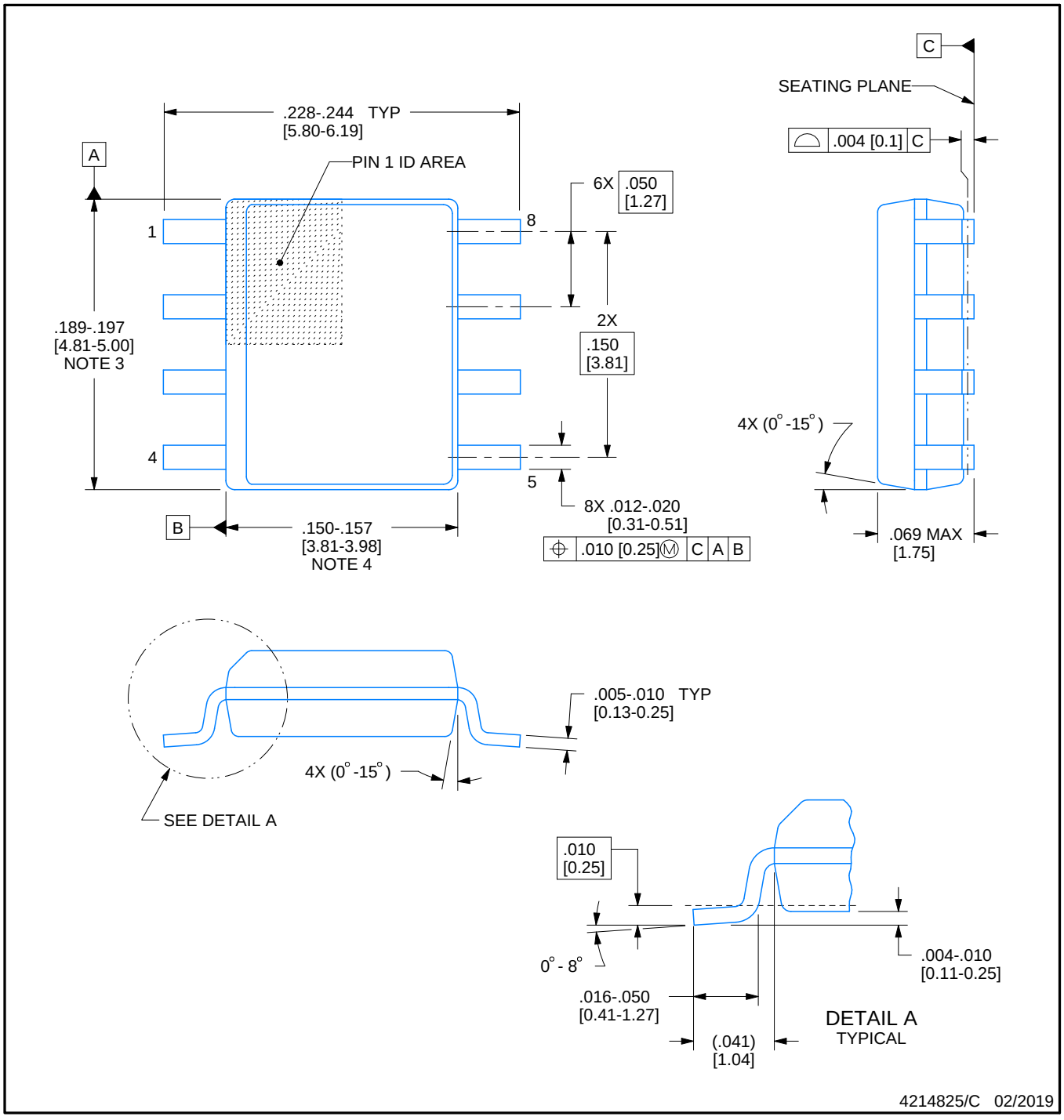


PACKAGE OUTLINE

D0008A

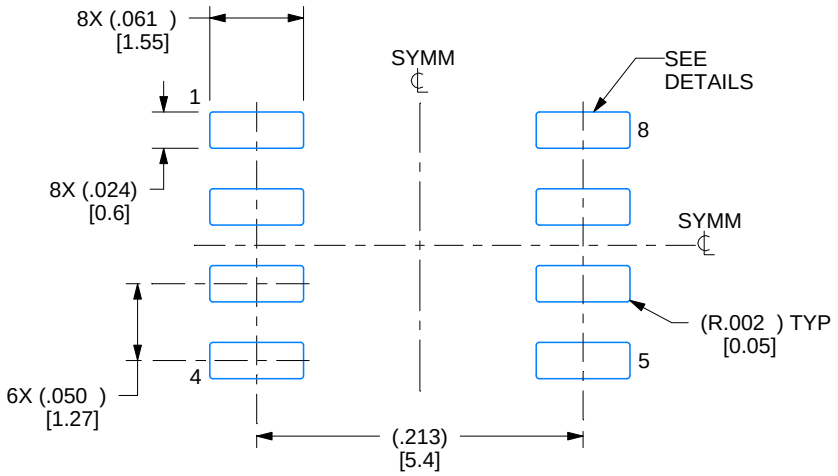
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

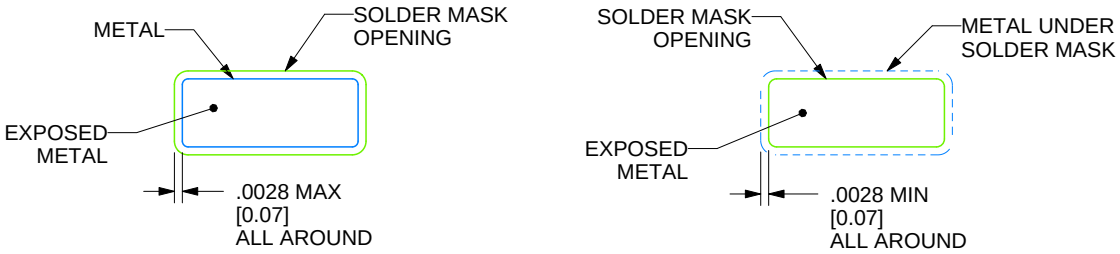


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

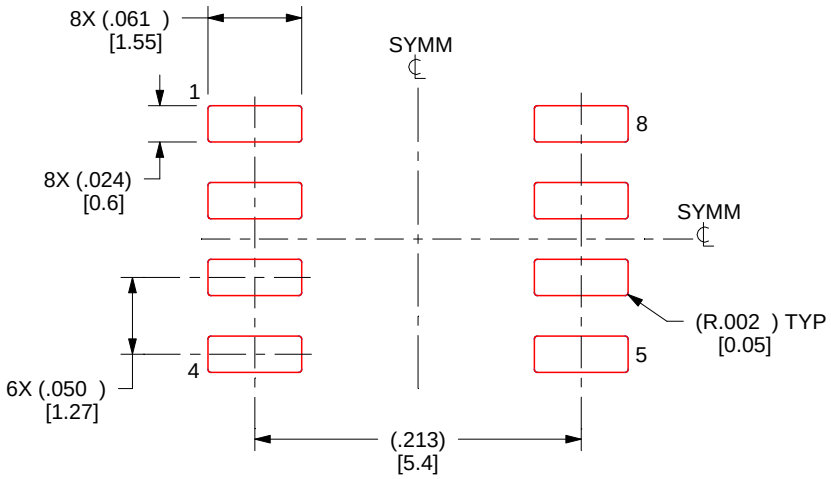
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025