

TDZ8907 Low-Cost, High-Efficiency, 31V_{pp} Boosted Piezo Sounder/Actuator Driver with Volume Control

1 Features

- Supply Voltage Range 2.5V¹ to 5.5V
 - Compatible with alkaline, coin, CR, and lithium batteries
- Integrated programmable boost converter, 11.5V or 15.5V with hardware pin control
- 1uF Load Piezo Capacitance Support
- 98% High-Efficiency Boost
- 20Hz-70kHz DIN Input PWM Frequency Support
- <1nA Ultra-Low Shutdown Current
- <200μs Fast Wake-Up from DIN LO to HI
- DIN Multi-functional Input Pin
 - Input PWM
 - Shutdown and Wake-Up control
 - 100ms shutdown hysteresis from DIN HI to LO
- Additional Boost Load Supported with 33nF Load
 - Up to 80mA from 11.5V boost
 - Up to 50mA from 15.5V boost
- External Boost Mode up to 10.2V
- 2S Lithium Battery Support up to 10V
- Thermal Shutdown Protection
- Over-current Protection
- Over-voltage Protection
- Under-voltage Lockout Protection

1. For 1.8V VBAT support, please contact TI.

2 Applications

- Smoke & heat detector
- Fire safety sounder, speaker, strobe
- Gas detector
- RF smart remote control
- Smart trackers
- Smartwatch
- Insulin pump
- Blood glucose monitor
- Refrigerator & freezer
- Washer & dryer
- Air purifier & humidifier
- Mixer, blender & food processor
- Vacuum robot
- Robotic lawn mower
- Electronic & robotic toys
- Portable field instrumentation
- Test & measurement
- Motor control

3 Description

The TDZ8907 is a low cost, compact, highly efficient, boosted piezoelectric driver optimized for space constrained and power sensitive applications. From a supply voltage down to 2.5V, TDZ8907 integrates a 2-level, programmable boost converter capable of generating 11.5V or 15.5V for volume control with a wide bandwidth differential output stage, making TDZ8907 an excellent choice for compact, battery operated designs such as building automation (fire safety, building security), appliances, smart trackers, and medical backup buzzers. TDZ8907's simple to use design can easily generate audible alerts, beeps, buzzes, or tones in applications using piezo sounders up to 1uF.

The TDZ8907 supports an external input PWM signal for driving complementary output signals across a piezo element. The boost output can be used to supply 80mA current to external peripherals such as LEDs.

The integrated boost converter is designed for low-EMI and small footprint inductance of 1.0uH using a boost switching frequency of 1.8MHz.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TDZ8907	WQFN (10)	2.0mm x 2.0mm

- (1) For all available packages, see [Section 11](#).
 (2) The package size (length × width) is a nominal value and includes pins, where applicable.

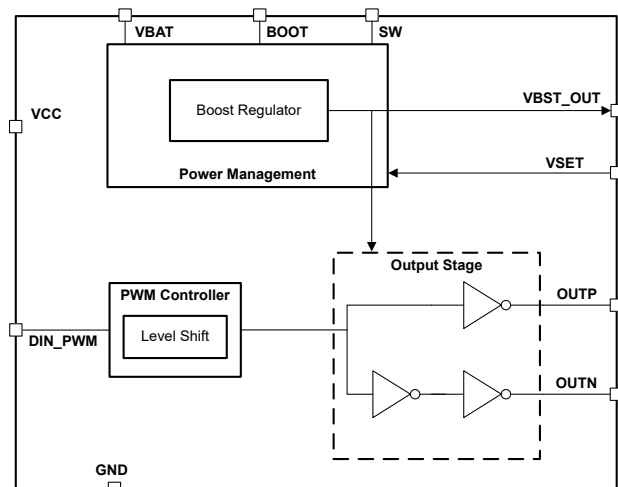


Figure 3-1. Simple Block Diagram



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4 Device Comparison

Table 4-1. Device Comparison

DEVICE NAME	DESCRIPTION
TDZ8907	PWM input piezo sounder driver with VSET pin to enable 11.5V or 15.5V boost output to drive piezo sounders

5 Pin Configuration and Functions

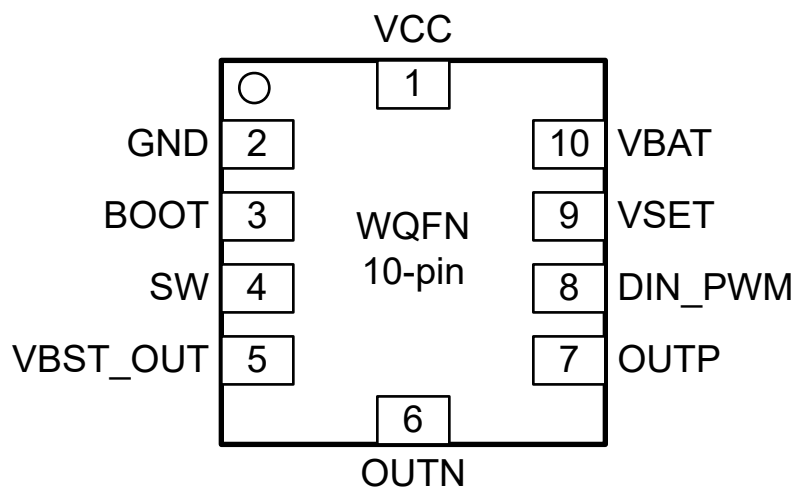


Figure 5-1. WQFN 10-pin Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
VCC	1	O	Can leave as no connect. Optional to connect 1uF capacitor.
GND	2	G	Ground
BOOT	3	P	Bootstrap capacitor connection
SW	4	I/O	Internal boost switch pin
VBST_OUT	5	O	Boost output
OUTN	6	O	N side driver output (connect to piezo terminal)
OUTP	7	O	P side driver output (connect to piezo terminal)
DIN_PWM	8	I	PWM input and Shutdown/Wake-Up control
VSET	9	I	Sets boost output voltage. Drive high for 15.5V. Drive low for 11.5V.
VBAT	10	P	Battery supply voltage

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{BAT}	Supply Voltage	−0.3	6	V
V _{IN}	Digital Input Pins (DIN_PWM, VSET)	−0.3	6	
OUTP, OUTN, V _{BST_OUT} , SW	Output and boost pins	−0.7	21	V
T _A	Ambient temperature	−10	125	°C
T _J	Junction temperature	−10	150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 ⁽¹⁾	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/ JEDEC JS-002 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{BAT}	Supply Voltage	2.5		5.5	V
V _{IH(DigIn)}	Input logic high for digital inputs	0.65*V _{BAT}		V _{BAT}	V
V _{IL(DigIn)}	Input logic low for digital inputs	0		0.3*V _{BAT}	V

6.4 Electrical Characteristics

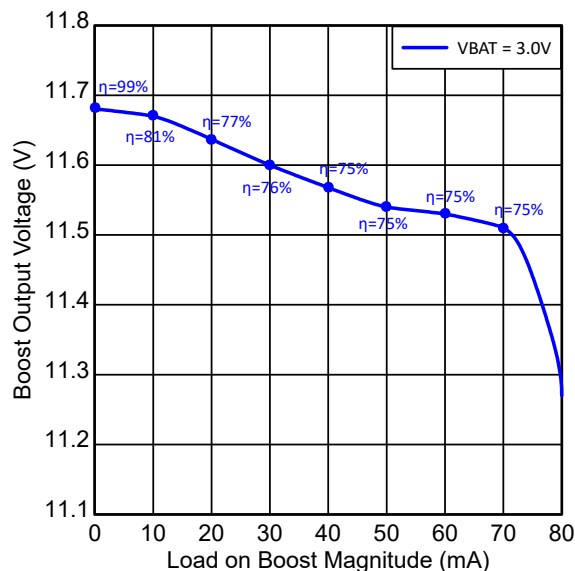
T_A = 25°C, V_{BAT} = 3V, Boost inductor = 1μH, C_{BST} = 1μF, C_{LOAD} = 33nF, f_{DIN_PWM} = 3.2kHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{BST_OUT}	Boost Output Voltage		11.5		V
V _{BST_OUT}	Boost Output Voltage		15.5		V
V _{BAT} UVLO	Battery Voltage Under-Voltage Lock Out	1.3	1.54	1.72	V
V _{BAT} UVLO	Battery Voltage Under-Voltage Lock Out	1.36	1.6	1.78	V
V _{BST_OUT} UVLO	Boost Voltage Under-Voltage Lock Out	4.6	5.4	5.8	V
V _{BST_OUT} UVLO	Boost Voltage Under-Voltage Lock Out	5.35	5.91	6.55	V
V _{BST_OUT} OV	Boost Voltage Over-Voltage Protection	11.4	12.3	13.4	V
V _{BST_OUT} OV	Boost Voltage Over-Voltage Protection	15	16.54	17.8	V

$T_A = 25^{\circ}\text{C}$, $V_{BAT} = 3\text{V}$, Boost inductor = $1\mu\text{H}$, $C_{BST} = 1\mu\text{F}$, $C_{LOAD} = 33\text{nF}$, $f_{DIN_PWM} = 3.2\text{kHz}$ (unless otherwise noted)

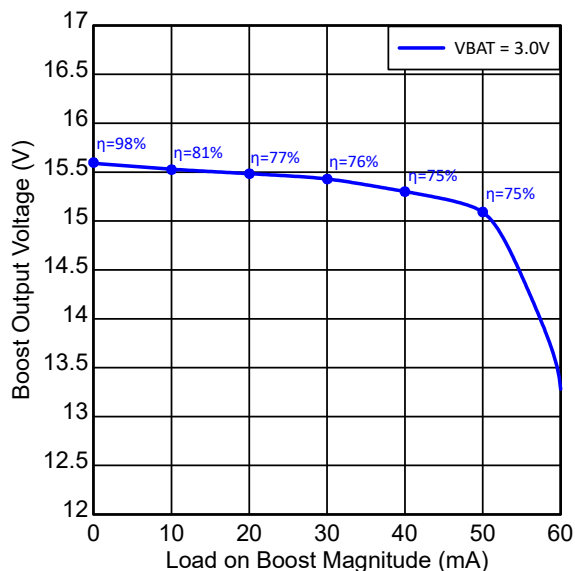
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBAT_NL}	No Load Active Current	$C_{PIEZO} = \text{No Load}$, $f_{DIN_PWM} = 3.2\text{kHz}$, $V_{OUT} = 11.5\text{V}$		2.1		mA
I_{VBAT_NL}	No Load Active Current	$C_{PIEZO} = \text{No Load}$, $f_{DIN_PWM} = 3.2\text{kHz}$, $V_{OUT} = 15.5\text{V}$		2.4		mA
I_{VBAT}	Active Current VBOOST=11.5V	$C_{PIEZO} = 33\text{nF}$, $f_{DIN_PWM} = 3.2\text{kHz}$, $V_{OUT} = 11.5\text{V}$		19		mA
I_{VBAT}	Active Current VBOOST=15.5V	$C_{PIEZO} = 33\text{nF}$, $f_{DIN_PWM} = 3.2\text{kHz}$, $V_{OUT} = 15.5\text{V}$		35		mA
Efficiency	System efficiency VBOOST=11.5V	$C_{PIEZO} = 33\text{nF}$, $f_{DIN_PWM} = 3.2\text{kHz}$, $V_{OUT} = 11.5\text{V}$		99		%
Efficiency	System efficiency VBOOST=15.5V	$C_{PIEZO} = 33\text{nF}$, $f_{DIN_PWM} = 3.2\text{kHz}$, $V_{OUT} = 15.5\text{V}$		98		%
I_{SD}	Shutdown Current	$V_{DIN_PWM} = 0\text{V}$ at 25°C , $V_{BAT}=3\text{V}$	0.000366		0.0064	μA
I_{SD}	Shutdown Current	$V_{DIN_PWM} = 0\text{V}$, across recommended V_{BAT} and temperature range			1.16	μA
C_{Load}	Max Piezo Loading	—			1000	nF
f_{OSC}	Boost Switching Frequency	Measured in Continuous switching operation	1.44	1.8	2.16	MHz
I_{OCP_BST}	Cycle-by-Cycle Over Current Protection for Boost (Peak input current limit from battery)	$V_{BAT}=3\text{V}$		1	1.5	A
I_{OCP_AMP}	Over Current Protection for piezo driver output	—		2	2.5	A
$R_{DS(ON)}$	Piezo Driver On-State Resistance	High Side, $I = 100\text{mA}$		9.3		Ω
$R_{DS(ON)}$	Piezo Driver On-State Resistance	Low Side, $I = 100\text{mA}$		0.6		Ω
t_{ON}	VOUT Start Delay Time	From DIN_PWM Signal High to 90% V_{OUT} Steady State, $V_{BAT}=3\text{V}$, $V_{BOOST}=11.5\text{V}$		162		μs
t_{ON}	VOUT Start Delay Time	From DIN_PWM Signal High to 90% V_{OUT} Steady State, $V_{BAT}=3\text{V}$, $V_{BOOST}=15.5\text{V}$		183		μs
t_{OFF}	Shutdown Delay Time	From $DIN_PWM = \text{High}$ to Low, V_{BST_OUT} off	68	97	126	ms
V_{IH}	Input logic high voltage for digital inputs	DIN_PWM Pin	$0.65 \cdot V_{BAT}$		V_{BAT}	V
V_{IL}	Input logic low voltage for digital inputs	DIN_PWM Pin	0		$0.3 \cdot V_{BAT}$	V
I_{IH}	Input logic high leakage current for digital inputs	$DIN_PWM = V_{DD}$		0.01	5	μA
I_{IL}	Input logic low leakage current for digital inputs	$DIN_PWM = 0$		0.01	1	μA
OT	Over Temperature protection asserted		140	165	190	$^{\circ}\text{C}$
OT_Hyst	Over Temperature protection hysteresis		10	20	30	$^{\circ}\text{C}$

6.5 Typical Characteristics



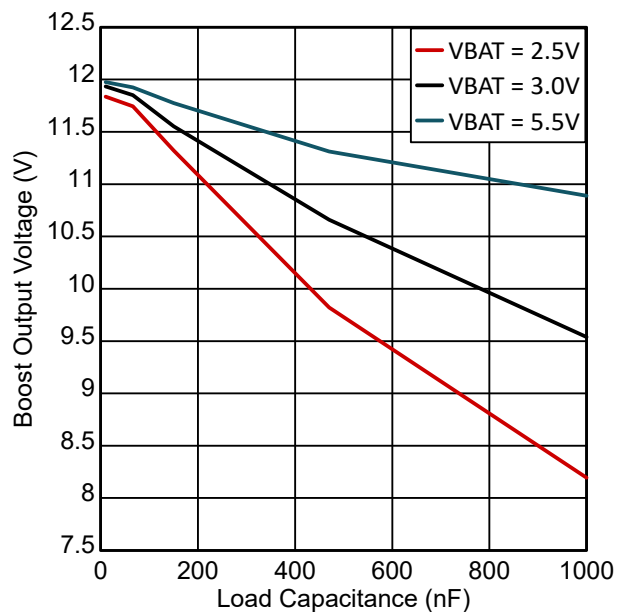
VBOOST = 11.5V C_{Piezo} = 33nF DIN_f = 3.2kHz

Figure 6-1. Boost Output Voltage vs Boost Loading (with Efficiency)



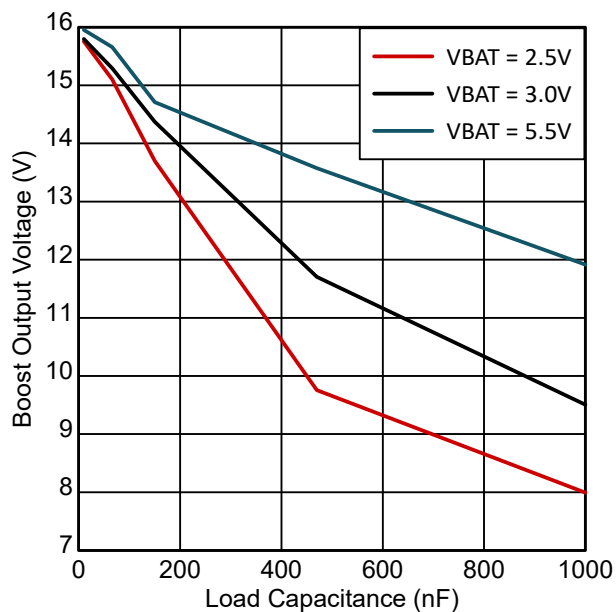
VBOOST = 15.5V C_{Piezo} = 33nF DIN_f = 3.2kHz

Figure 6-2. Boost Output Voltage vs Boost Loading (with Efficiency)



VBOOST = 11.5V DIN_f = 3.2kHz

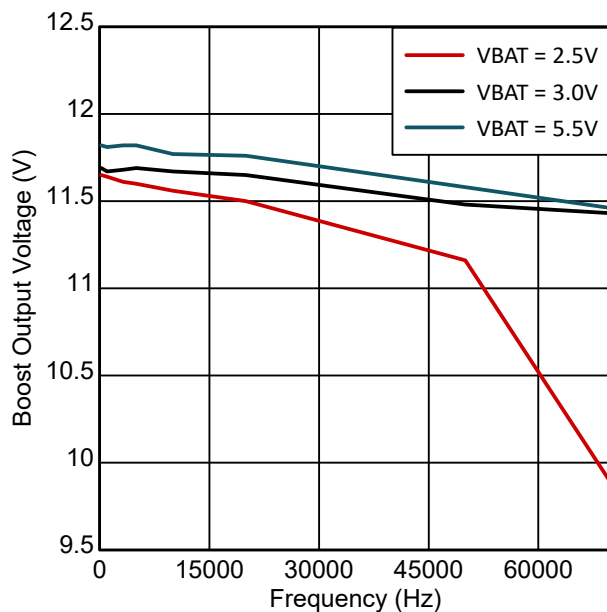
Figure 6-3. Boost Output Voltage vs Load Capacitance



VBOOST = 15.5V DIN_f = 3.2kHz

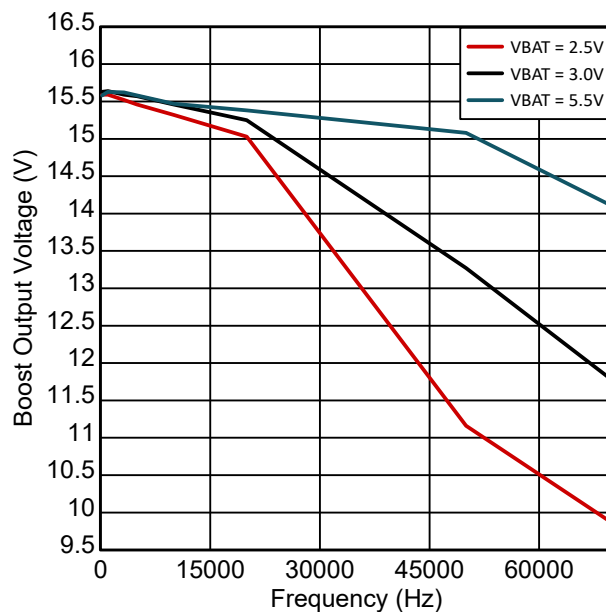
Figure 6-4. Boost Output Voltage vs Load Capacitance

6.5 Typical Characteristics (continued)



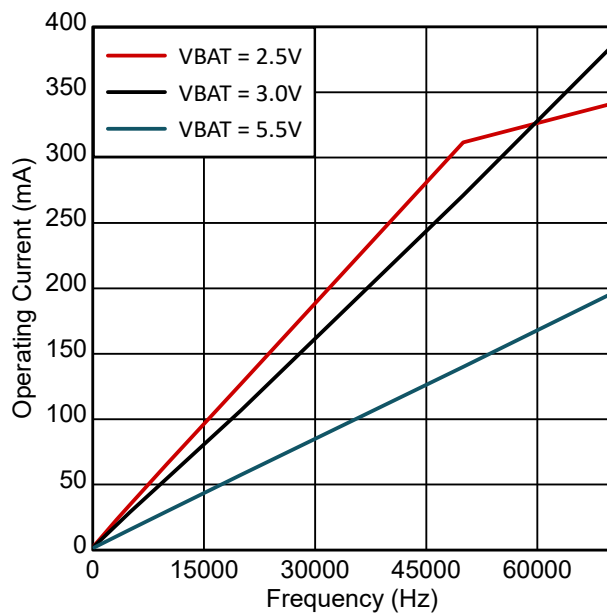
VBOOST = 11.5V $C_{Piezo} = 33nF$

Figure 6-5. Boost Output Voltage vs Frequency



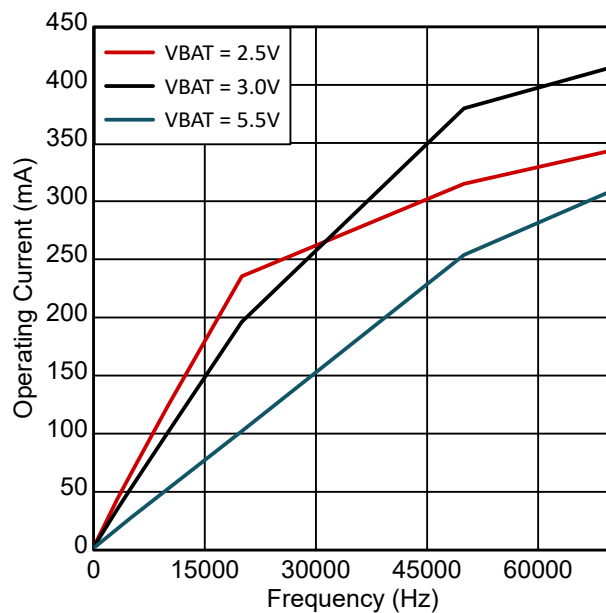
VBOOST = 15.5V $C_{Piezo} = 33nF$

Figure 6-6. Boost Output Voltage vs Frequency



VBOOST = 11.5V $C_{Piezo} = 33nF$

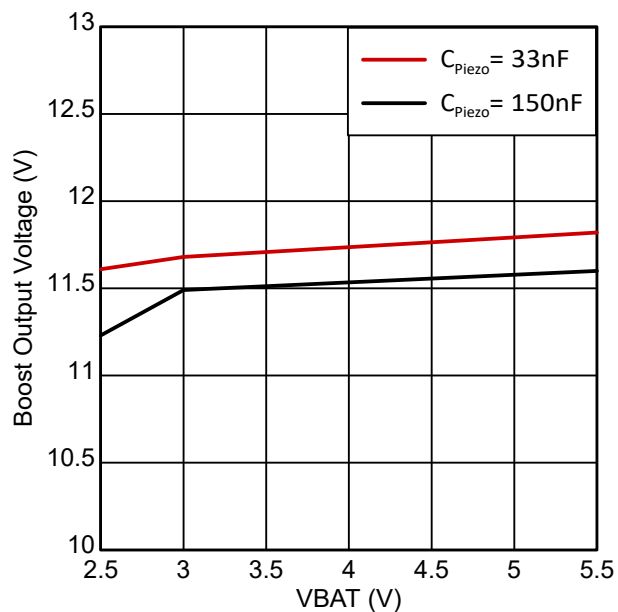
Figure 6-7. Operating Current vs Frequency



VBOOST = 15.5V $C_{Piezo} = 33nF$

Figure 6-8. Operating Current vs Frequency

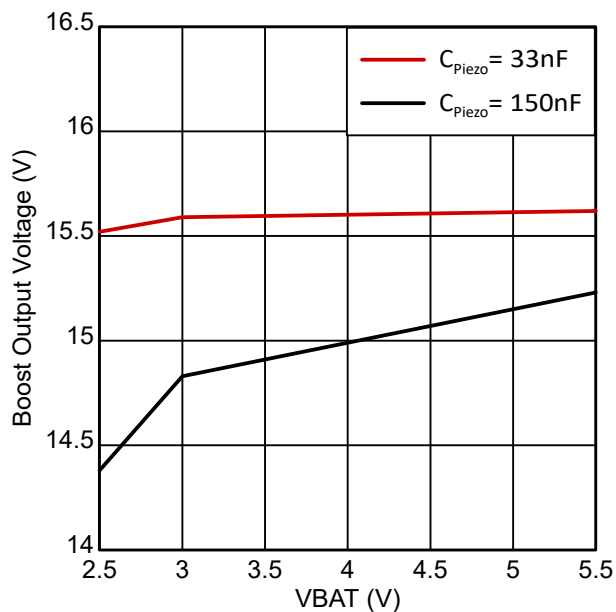
6.5 Typical Characteristics (continued)



VBOOST = 11.5V

DIN_f = 3.2kHz

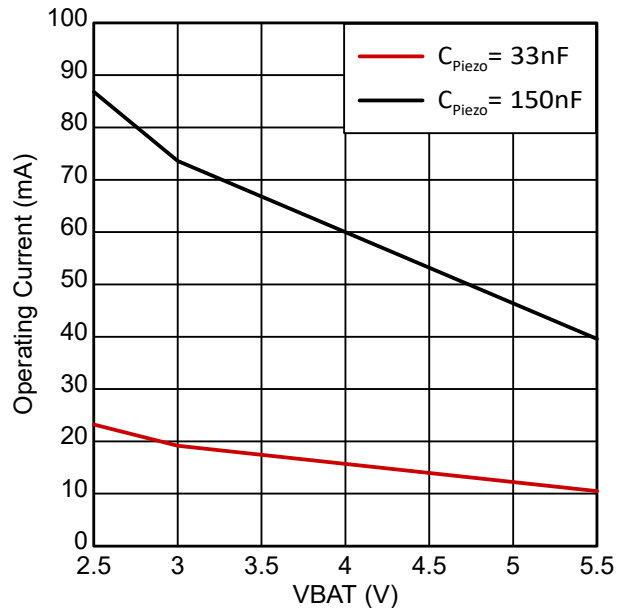
Figure 6-9. Boost Output Voltage vs VBAT



VBOOST = 15.5V

DIN_f = 3.2kHz

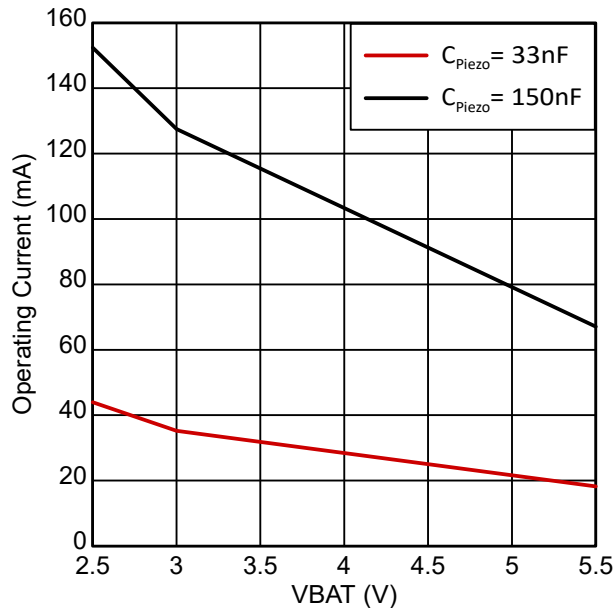
Figure 6-10. Boost Output Voltage vs VBAT



VBOOST = 11.5V

DIN_f = 3.2kHz

Figure 6-11. Operating Current vs VBAT



VBOOST = 15.5V

DIN_f = 3.2kHz

Figure 6-12. Operating Current vs VBAT

6.5 Typical Characteristics (continued)

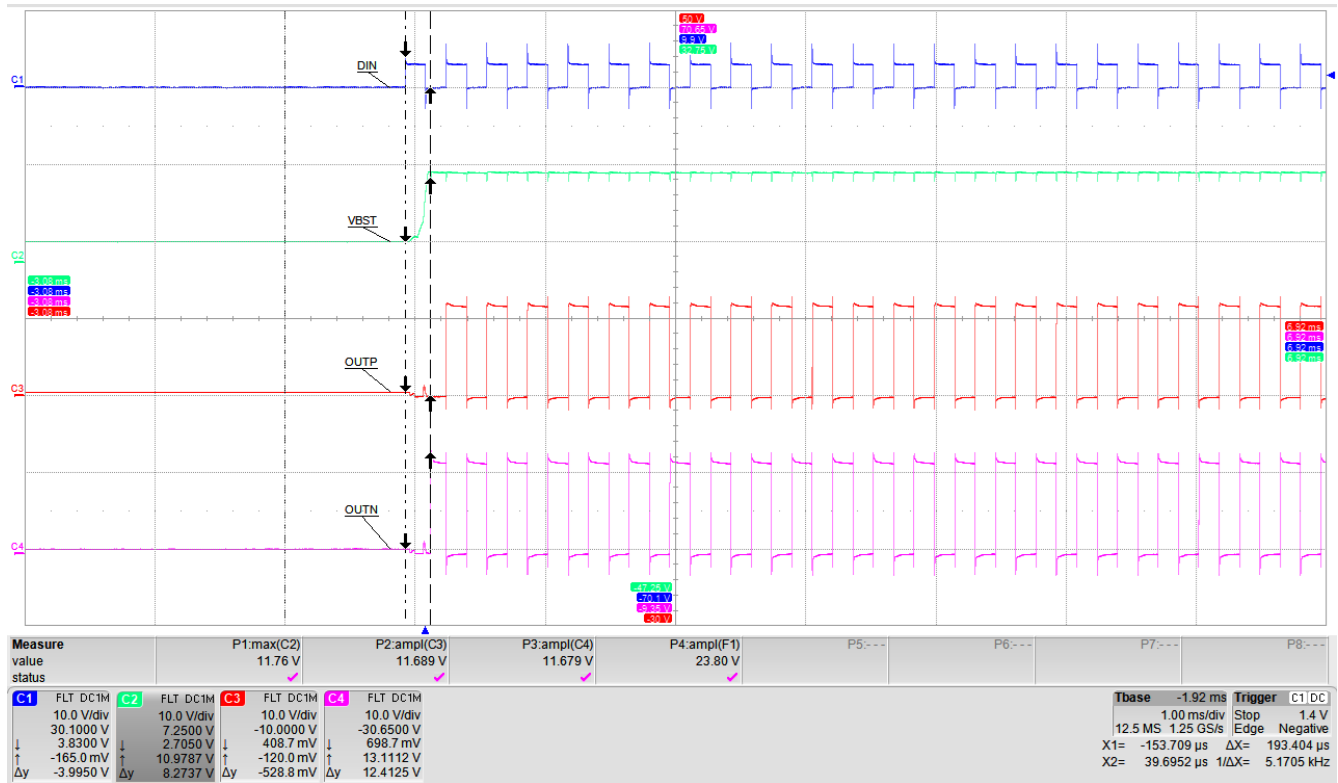


Figure 6-13. Turn-on waveform for 11V boost output voltage

6.5 Typical Characteristics (continued)

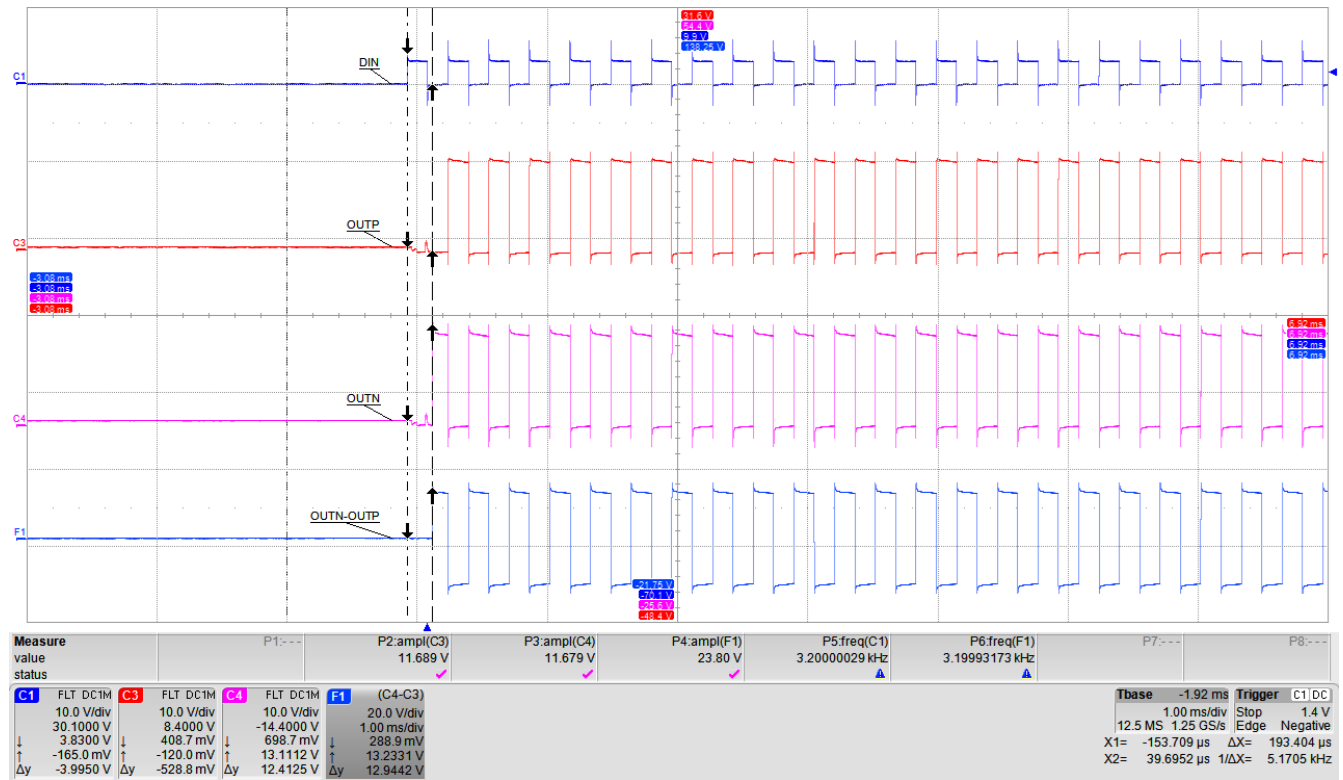


Figure 6-14. Turn-on waveform for 11V boost output voltage

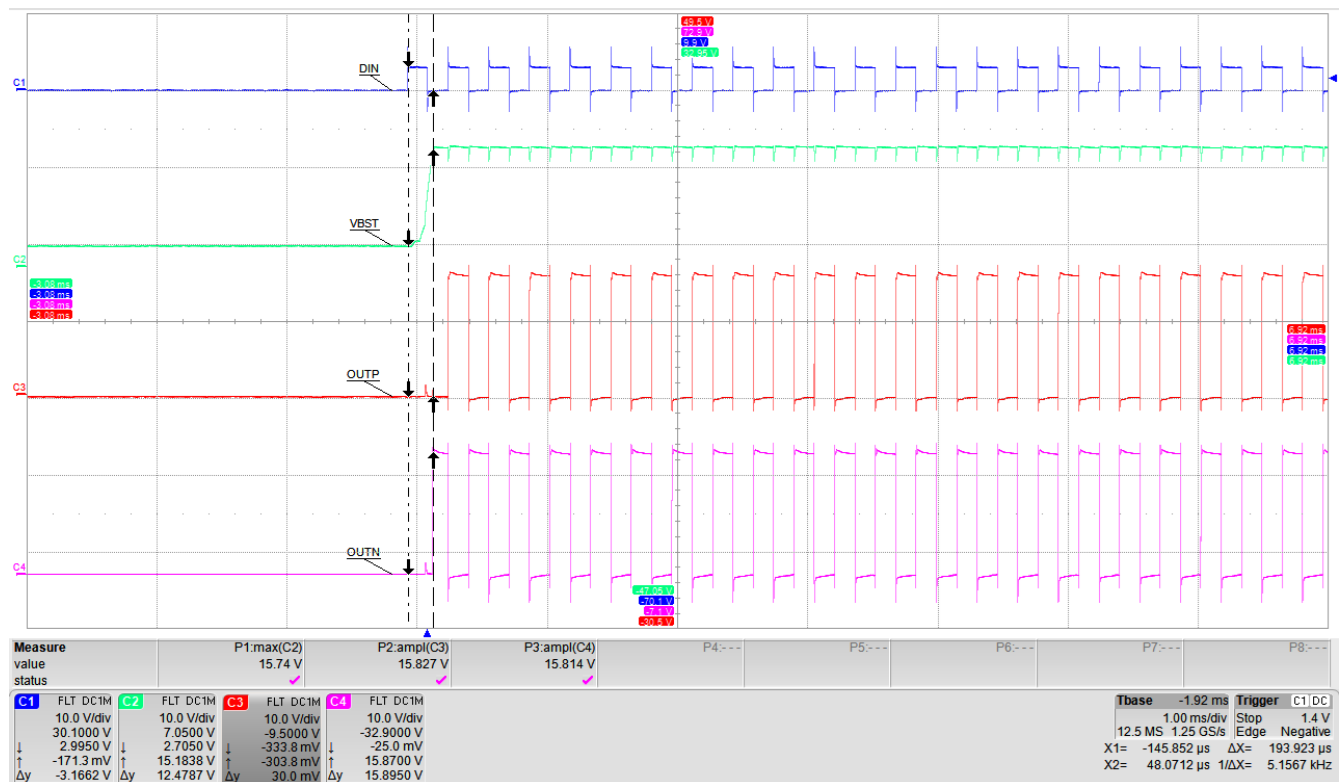


Figure 6-15. Turn-on waveform for 15V boost output voltage

6.5 Typical Characteristics (continued)

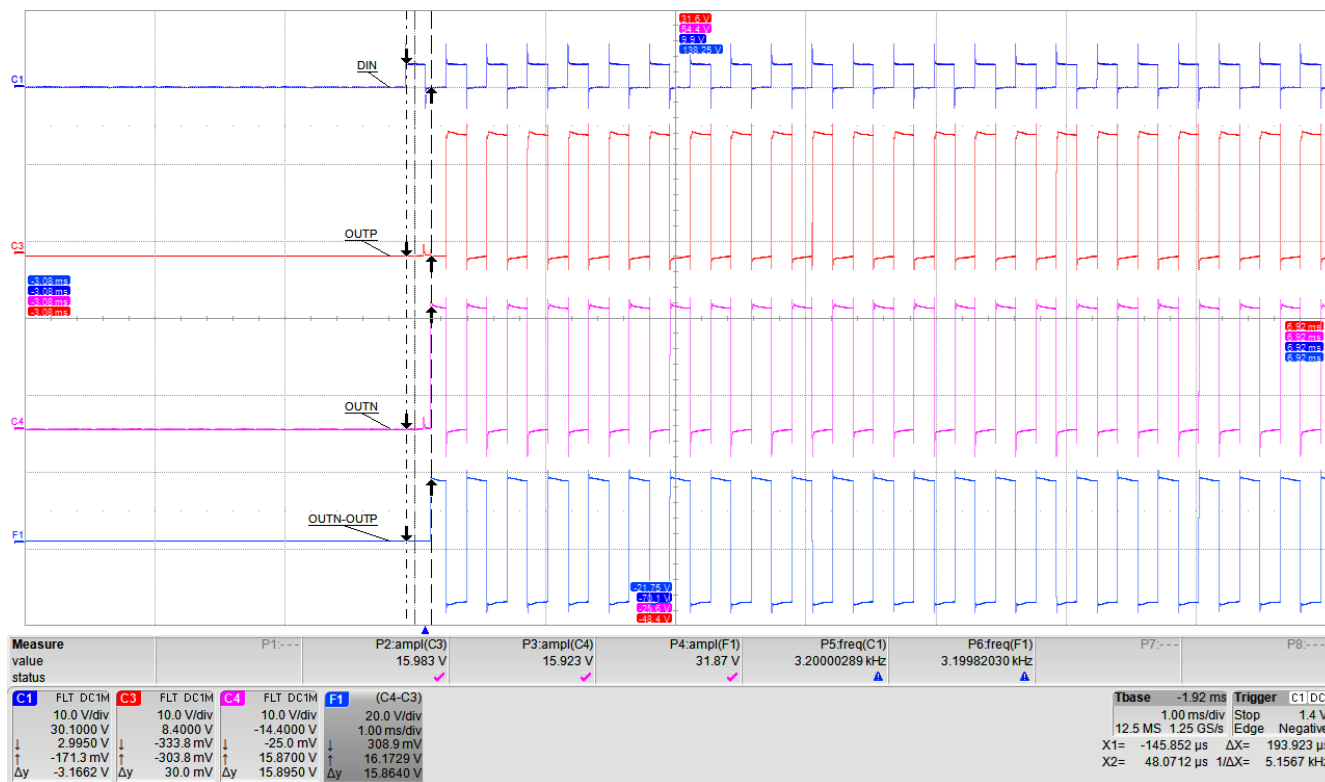


Figure 6-16. Turn-on waveform for 15V boost output voltage

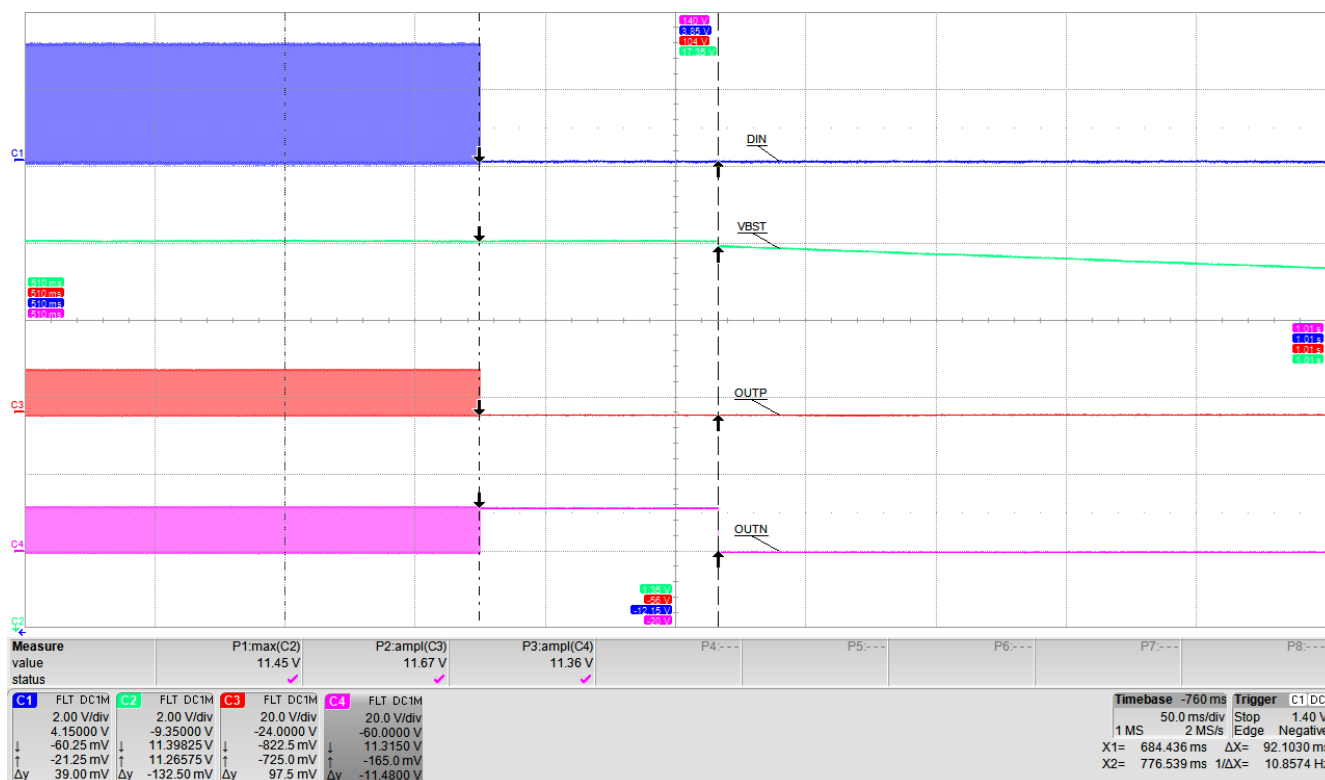


Figure 6-17. Turn-off waveform for 11V boost output voltage

6.5 Typical Characteristics (continued)

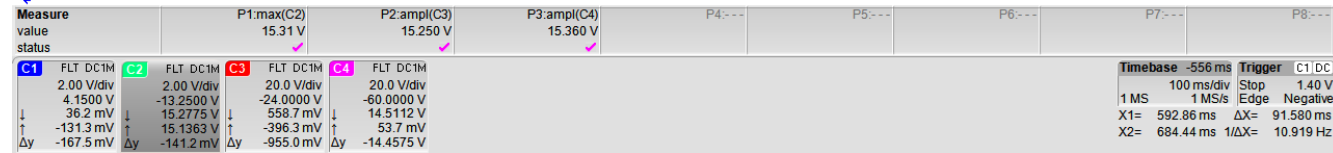


Figure 6-18. Turn-off waveform for 15V boost output voltage

range of 2.5V to 5.5V. The boost output voltage is present on the VBST_OUT pin. When operating under light loads, the boost converter enters the Pulse Frequency Modulation (PFM) mode to conserve power.

The typical components required for the boost converter are an external inductor, L_{BST} , a bootstrap capacitor connected between the SW and BOOT pins, C_{BOOT} , and an external VBST_OUT capacitor, C_{BST} . Optionally, a diode, D_{BST} , can be placed between the SW and VBST_OUT pins to improve efficiency. Recommended values are listed in the [Recommended External Components](#) table.

The boost converter can be bypassed and an external supply up to 10.2V can be provided to the VBST_OUT pin. In this configuration, the BOOT and SW pins are left unconnected with C_{BOOT} and L_{BST} disconnected and the VSET pin is tied to GND. The capacitor C_{BST} is still required. The VBST_OUT pin implements under-voltage lock out, over-current, and over-voltage protection per the [Recommended Operating Conditions](#).

The L_{BST} by C_{BST} derated value ratio must be ≤ 1 for boost stability. If a higher inductor value is used then the boost capacitor must increase accordingly.

The VSET pin on TDZ8907 changes the output voltage of the boost between 11.5V (drive low) and 15.5V (drive high).

7.3.2 PWM Level Shifter and Digital Logic

TDZ8907's input digital logic accepts a pulse-width modulated (PWM) input on the DIN_PWM pin. Once the DIN_PWM signal exceeds the digital high logic threshold specified in [Recommended Operating Conditions](#), TDZ8907 wakes up and starts to power the boost and internal blocks. There is an initial decision determined by the state of the VSET pin. If the VSET pin is set HIGH, then the boost output voltage is set at 15.5V; otherwise if the VSET pin is set LOW, then the boost output voltage is set at 11.5V. After a typical period of 200 μ s, the boost is enabled and output PWM is driven. The VSET pin state is set prior to device powerup and can be changed on the fly during device operation for volume control. If the DIN_PWM pin is pulled low and left low for a period of longer than 100ms, TDZ8907 returns to the shutdown state consuming very little power. When a PWM signal with sufficient voltage magnitude is driven to the DIN_PWM pin, the voltage is level shifted to drive the differential class-D output stage. A minimum 7 μ s high pulse width is required to reliably enable the device. The differential output signal driven reflects the input PWM signal's frequency and duty cycle. When DIN_PWM is high, the OUTP pin is set high and OUTN is set to ground. Conversely, if DIN_PWM is low, then OUTN is set high and OUTP is set to ground.

If the DIN_PWM pin is driven high with a DC signal, then the device continues to power the boost converter and keeps OUTP high until the input changes. If the desired mode of operation is to keep the boost on without driving OUTP high, then the host can pulse the DIN_PWM high at intervals ≤ 80 ms.

7.3.3 Differential Output Class-D Amplifier

TDZ8907 contains a high performance, high impedance full H-bridge, or class-D, output stage. The high $R_{DS(on)}$ impedance allows the class-D to drive piezo loads without causing short circuit events.

7.4 Device Functional Modes

The TDZ8907 operates in the following modes: shutdown, PWM input, digital high input, and pulsed digital high input. The following sections outline the operation of each mode.

7.4.1 Shutdown

When VBAT is powered with DIN_PWM held low, TDZ8907 enters the shutdown state with an ultra-low shutdown current of <1 nA and monitors the DIN_PWM pin. This state shuts down the boost converter, internal LDO, and output amplifier to consume the least amount of power possible. The shutdown state is exited when the DIN_PWM voltage exceeds the V_{IH} threshold. The shutdown state is resumed when the DIN_PWM voltage is below V_{IL} for a typical period of 100ms.

7.4.2 PWM Input and Digital High Input

As described in [Section 7.3.2](#), the TDZ8907 boost is enabled when the DIN_PWM pin voltage increases beyond V_{IH} . The TDZ8907 is constantly monitoring the DIN_PWM pin per the logic and driving the class-D outputs

appropriately. After the start-up period, a high signal on DIN_PWM pulls OUTP high and, by complimentary logic, OUTN is pulled low. Inversely, when DIN_PWM is low, OUTP is pulled low and OUTN is pulled high.

If the DIN_PWM pin is held high, then the boost stays on and the OUTP pin stays high producing a DC voltage.

Lastly, driving a logic high pulse on the DIN_PWM pin in intervals $\leq 80\text{ms}$ keeps the boost powered. This type of operation allows for the powering of external components on VBST_OUT.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

This section details the information required to configure the TDZ8907 for several different applications and provides guidance on integrating the TDZ8907 into larger systems. The TDZ8907 can be used in any application that requires loud alerts/beeps/buzzes/tones using a piezoelectric sounder in a small footprint. The TDZ8907 design allows customers to drive 2-terminal piezo sounders using a single PWM input signal and the integrated boost, or with an external supply for the boost.

8.2 Typical Application - PWM Input Mode

For all inputs, the TDZ8907 can be configured using the internal boost converter or with an external power supplied to the VBST_OUT pin. When using external power for the boost, tie the VSET pin to GND with L_{BST} and C_{BOOT} not installed.

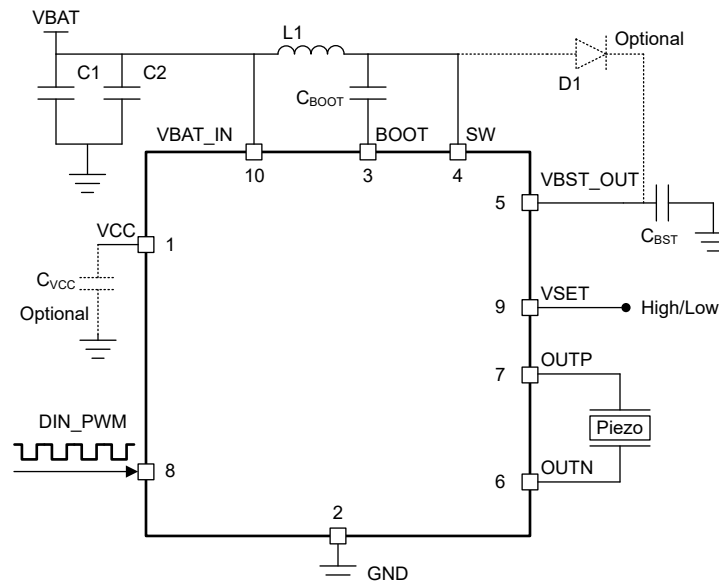


Figure 8-1. PWM Input with Internal Boost Power

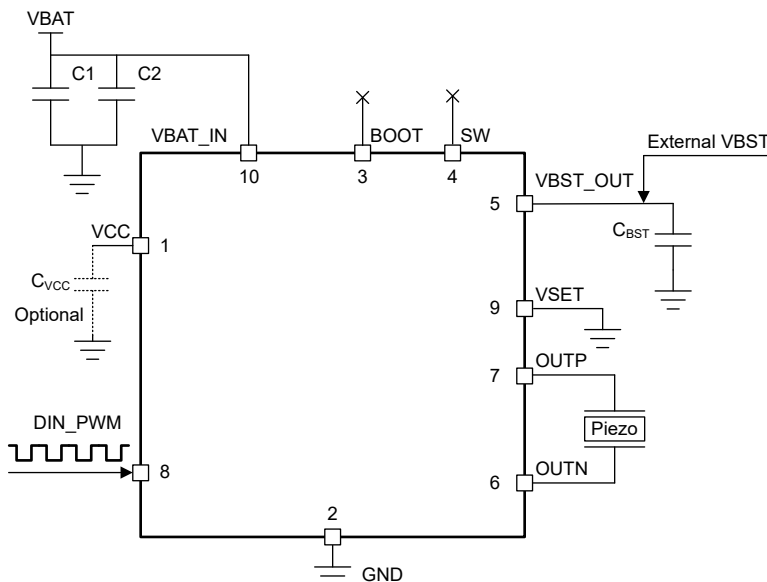


Figure 8-2. PWM Input with External Power

8.2.1 Design Requirements

The design requirements for TDZ8907 are universal for most typical applications. See the recommended external components in [Table 8-1](#). When bypassing the boost converter, the L_1 and C_{BOOT} components are not needed. To improve efficiency, a Schottky diode, D_1 , can be populated. The C_{VCC} capacitor is not required but can be installed if needed. There is no difference in device performance with the C_{VCC} populated or not.

Table 8-1. Recommended External Components

PARAMETER	Description	Specification	Typical Value
C1	VBAT decoupling capacitor	20% tolerance, VBAT*2V rated	10 μ F
C2	VBAT decoupling capacitor	20% tolerance, VBAT*2V rated	1 μ F
C_{BOOT}	Bootstrap capacitor	20% tolerance, 10V rated	0.1 μ F
L_1	Boost converter inductor	20% tolerance, 2A rated	1 μ H
D1	Optional Schottky diode to increase efficiency	2A rated	18V
C_{BST}	Boost decap	20% tolerance, VBOOST*2V rated	1 μ F
C_{VCC}	Optional VCC decap	20% tolerance, VBAT*2V rated	0.1 μ F-1 μ F

8.2.2 Detailed Design Procedure

There are very few design decisions for normal operation using the typical PWM input mode. Once the circuit is powered up with VBAT and, optionally, VBST_OUT external, pull the DIN_PWM high to wake up TDZ8907. After the start-up time, the boost is powered to the voltage level set by the VSET pin and the output follows the DIN_PWM pin per [Section 7.3.2](#).

The VSET pin of TDZ8907 can be changed on the fly to change the boost output voltage between 11.5V and 15.5V for volume control.

When using the TDZ8907 with external power tie VSET to GND.

8.3 What to Do and What Not to Do

- When using external power for the boost, the DIN pin must be held LOW until both VBAT and external supplies are given.
- The VBST_OUT pin must not be loaded through external circuitry when powering up the device (DIN transition from LOW to HIGH) when using the internal boost converter.

- Output short circuit protection is not supported when using external power for the boost.
- For short circuit protection to reliably work in internal boost mode, limit the capacitance on the boost output to 30uF.
- Errata: DIN pin must be LOW before VBAT <2.5V. VBAT must be >2.4V before DIN transitions from LOW to HIGH.

8.4 Power Supply Recommendations

TDZ8907 has only one supply requirement, VBAT, for the default PWM mode using the internal boost.

Best practice is to leave the input signal, DIN, LOW until VBAT is supplied. Once TDZ8907 detects VBAT and DIN are both HIGH, the device is enabled after the typical startup time.

The boost output voltage selection pin, VSET, can be applied in any order with respect to VBAT and DIN and on the fly during device operation. Best practice is to set the VSET pin HIGH or LOW before powering up the device.

When using an external supply for the boost, the external boost power must be supplied first, followed by the VBAT supply. The external boost power and VBAT must both be supplied before DIN is brought HIGH.

8.5 Layout Guidelines

The small footprint of TDZ8907 and minimal required components allow for applications to use a 2 layer board design with most of the signals and power traces laid out on the same layer as the IC. Consider all the critical components to be placed close to the IC on the same layer. The following sections provide further guidance on each of the critical signals and component routings.

8.5.1 GND Connections

- The top and bottom layers are poured with GND at all places that no other signal is required.
- Add via stitching to the GND planes from top to bottom layers for better thermal and electrical performance.
- Add several vias to GND under the IC.
- Add several vias to GND close to the decoupling capacitors, as well as close to GND pin 2.

8.5.2 Power Connections

- Place the 1uF decoupling capacitors as close to each of VBAT and VBST_OUT pins as possible.
- Place the larger 10uF VBAT capacitor close to the boost inductor.
- Place the 0.1uF bootstrap capacitor as close to device pins BOOT and SW and possible.
- Place the SW inductor as close to the bootstrap capacitor and IC as possible.
- Keep the SW routing as short and wide as possible. Avoid using vias in the high current SW node.
- If the optional 1uF on VCC is installed, the capacitor can be placed further away from the device pins to allow closer placement of other components.
- If the optional Schottky diode is installed, keep the routing as short as possible.

8.5.3 Layout Example

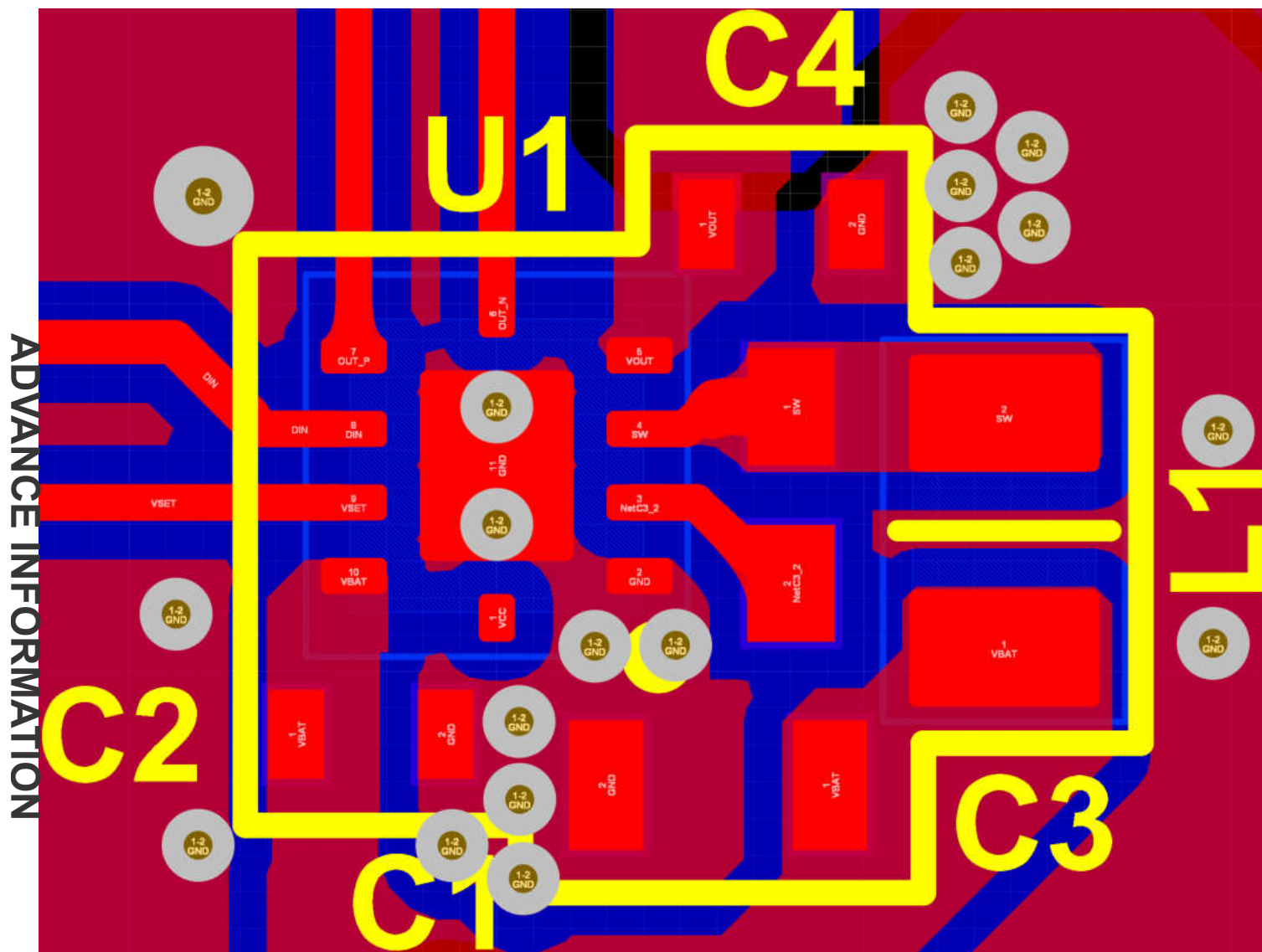


Figure 8-3. Layout Example 2D View

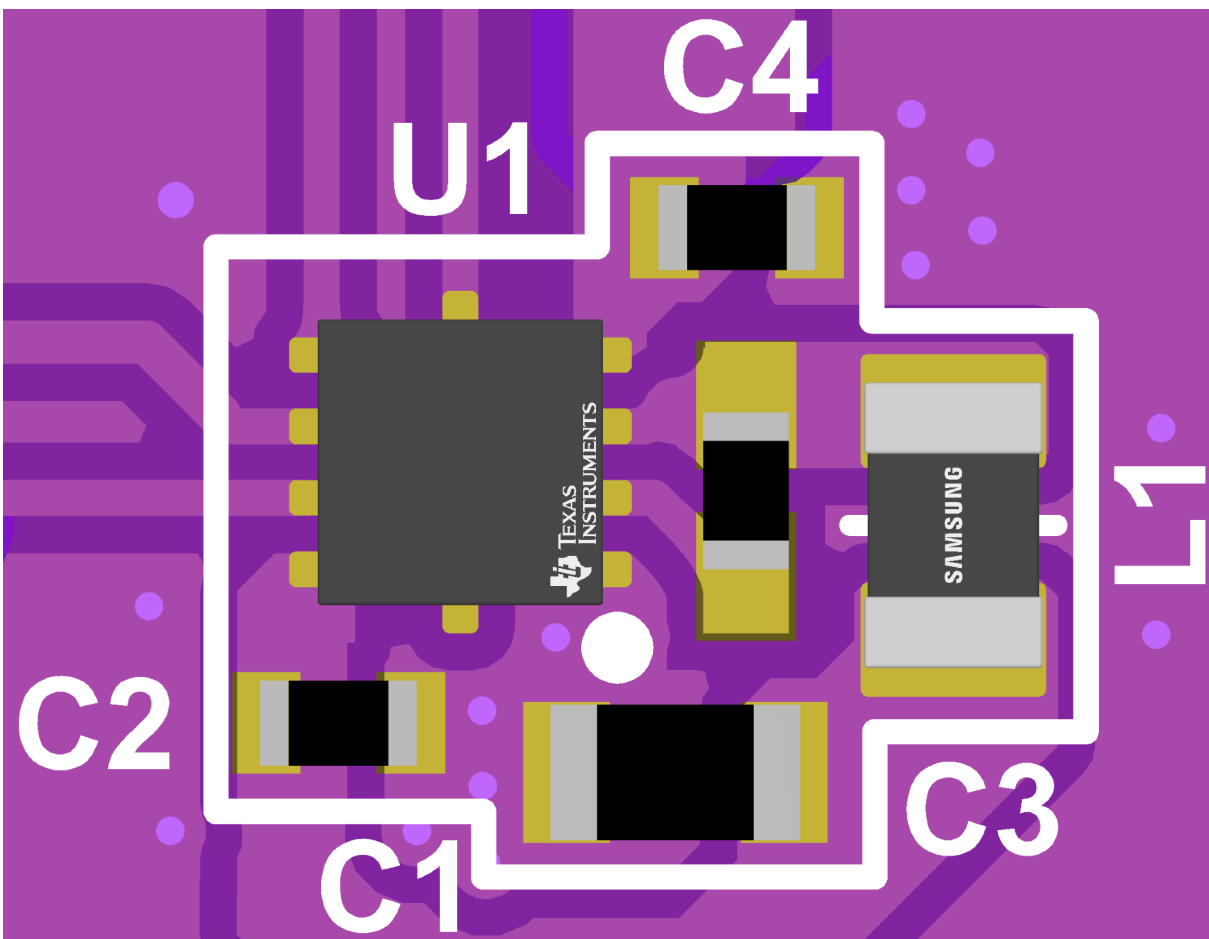


Figure 8-4. Layout Example 3D View

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.3 Trademarks

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

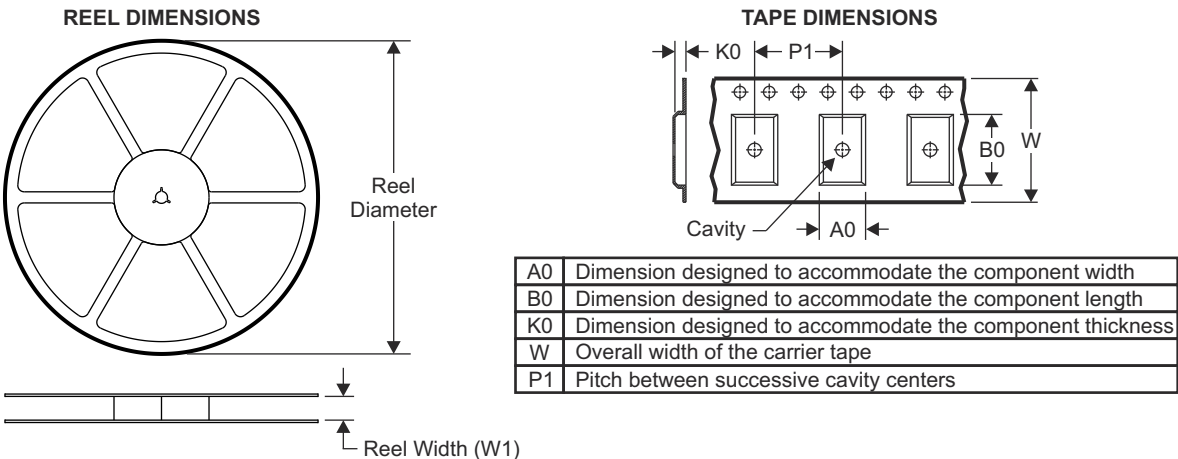
PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/Ball material	MSL rating/Peak reflow	Op temp (°C)	Part marking
TDZ8907RFG	Preview	Preproduction	WQFN (RFG) 10	3000 LARGE T&R	Yes	MATTE SN	Level-1-260C-UNLIM	-20 to 125	P897

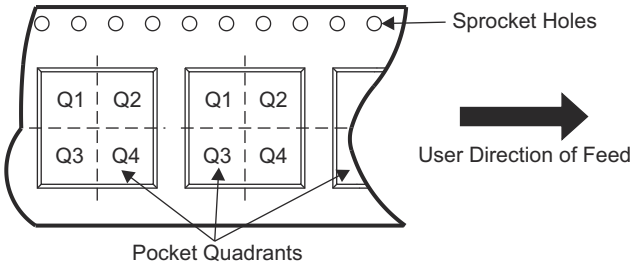
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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11.1 Tape and Reel Information

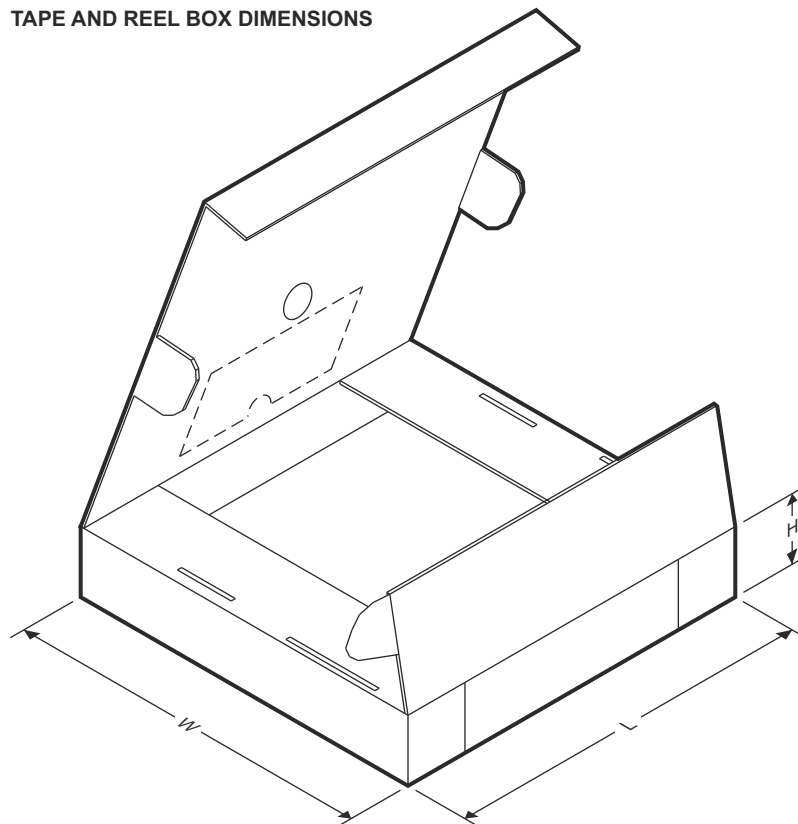


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



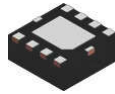
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDZ8907RFGR	WQFN	RFGR	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDZ8907RFGR	WQFN	RFG	10	3000	210.0	185.0	35.0

ADVANCE INFORMATION

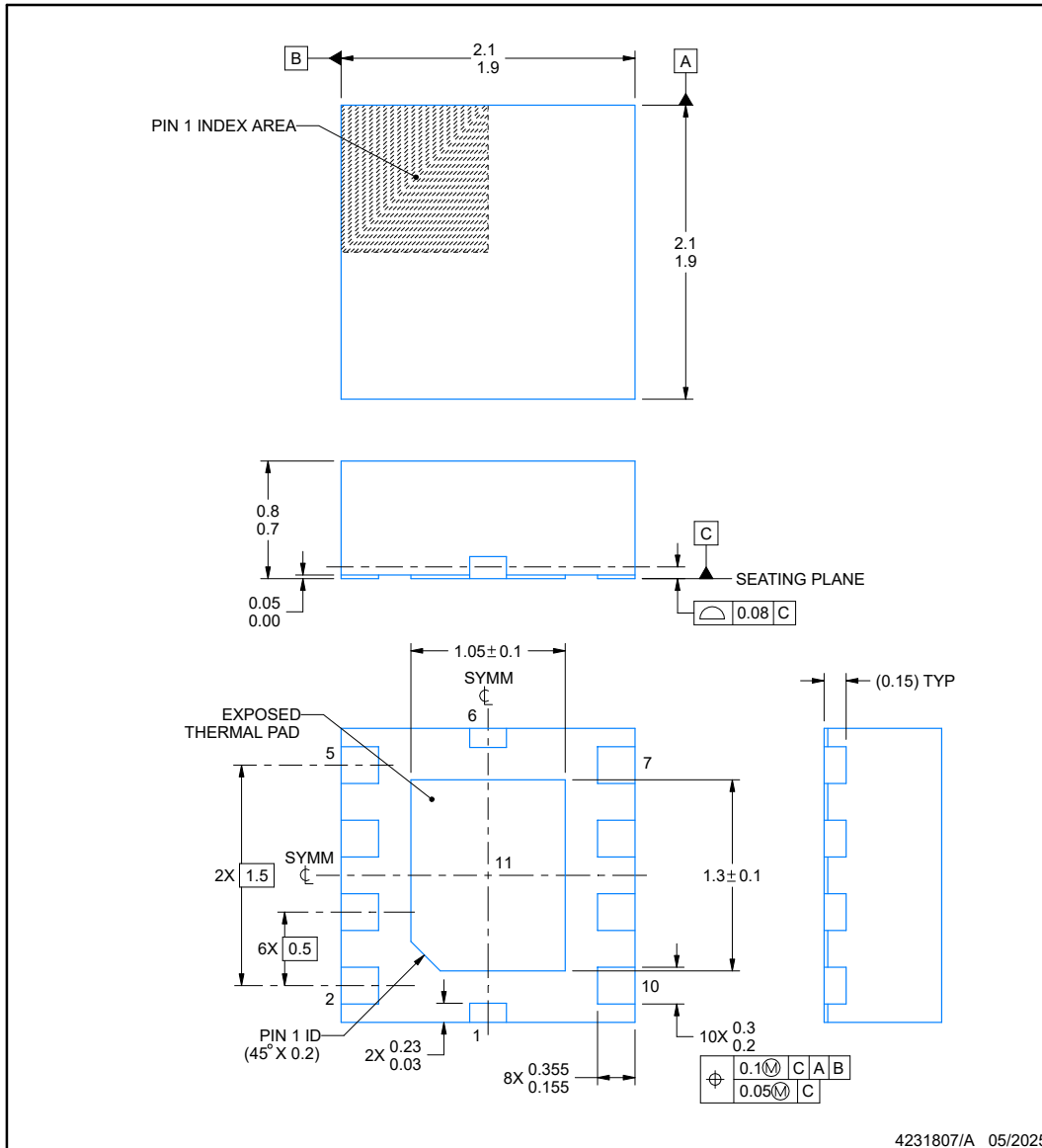


RFG0010A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4231807/A 05/2025

NOTES:

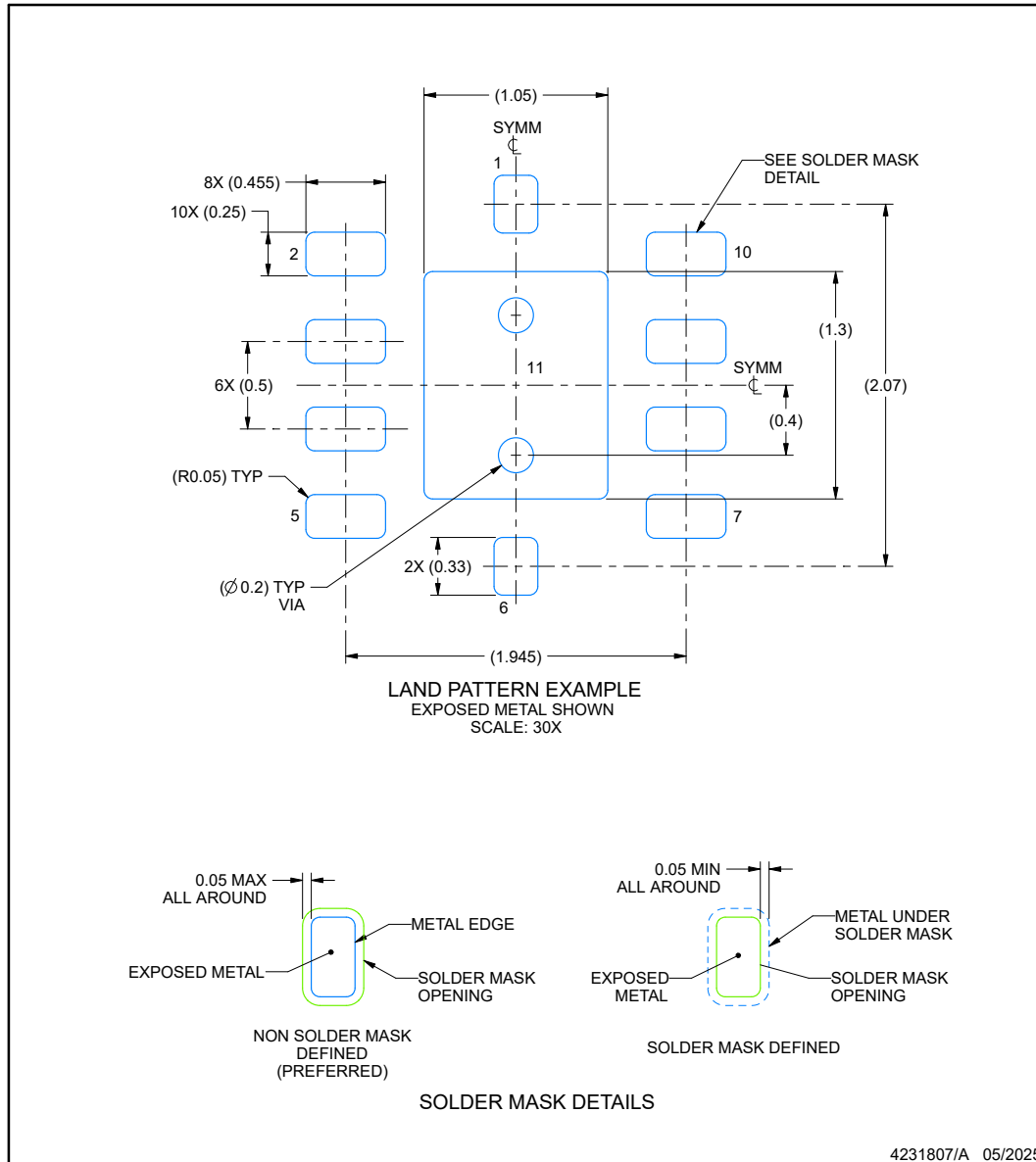
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RFG0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

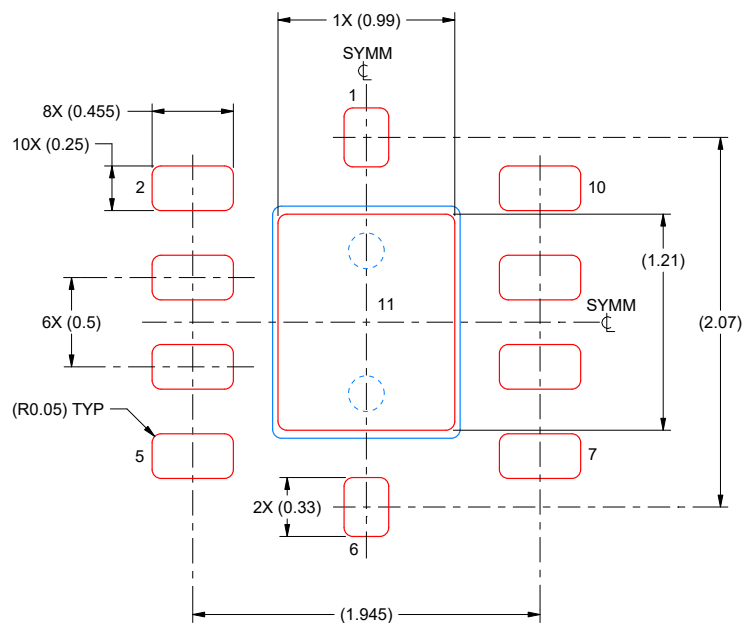
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RFG0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 11
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231807/A 05/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTDZ8907RFG	Active	Preproduction	WQFN (RFG) 10	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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